EGRATED CIRCUITS

Display Drivers and I^2C-bus Peripherals

Data Handbook IC12
2000

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I²C Peripherals

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Short-form specification	The data in this specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

PREFACE

Since Philips first invented it almost 20 years ago, the two-wire I²C-bus has grown far beyond our initial expectations. I²C it is now firmly established worldwide as the 'King of Serial Buses' for embedded applications.

Since its birth as a serial bus for consumer electronics, the I²C-bus is now used extensively in PCs and workstations as a diagnostics and power management bus, in mobile phones it's used to control Synthesizers, LCD and Realtime clocks, in wired phones for access to DTMF and EEPROM ICs. It's also used as a de-facto standard in Plug-in Video cards for PCs due to Philips' extensive range of video processing ICs with I²C. And when you see an LCD display in a car dashboard or car radio, odds are it's got I²C running behind the glass.

For simple tasks such as monitoring a keypad, driving an LED or LCD, storing crucial non-volatile data, measuring a temperature, driving a reed-relay, tracking the time-of-day, to all sorts of complex functions for video, audio, and closed-loop control applications, I²C is the serial bus of choice.

In this 1999 edition of our I²C Peripherals Handbook, we have compiled an ever-growing list of Philips' I²C Peripheral ICs for general purpose. Specialized I²C peripherals for specific applications (i.e. video/audio processors, synthesizers) can be found in Philips application-specific data handbooks.

Philips also provides a large palette of microcontrollers with dedicated I²C interface. Contact your local Philips Semiconductors representative for further details about I²C-bus microcontrollers, specialized peripherals, demoboards, emulators, evaluation tools, and application notes. They will be happy to assist you with your I²C bus designs!

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ASSIGNED I²C-BUS ADDRESSES (IN ALPHANUMERIC ORDER OF TYPE NUMBER)

TYPE NUMBER	DESCRIPTION	I²C SLAVE ADDRESSES[1]						
		A6	A5	A4	A3	A2	A1	A0
-	General call address	0	0	0	0	0	0	0
-	Reserved addresses	0	0	0	0	X	X	X
-	Reserved addresses	1	1	1	1	X	X	X
CCR921	RDS/RBDS decoder	0	0	1	0	0	A	A
NE5751	Audio processor for RF communication	1	0	0	0	0	0	A
OM4085	Universal LCD driver for low multiplex rates	0	1	1	1	1	1	A
PCA1070	Programmable speech transmission IC	0	1	0	0	0	0	A
PCA8516	Stand-alone OSD IC	1	0	1	1	1	0	1
PCA8581/C	128 × 8-bit EEPROM	1	0	1	0	A	A	A
PCB2421	1K dual mode serial EEPROM	1	0	1	0	0	0	0
PCD3311C	DTMF/modem/musical tone generator	0	1	0	0	1	0	A
PCD3312C	DTMF/modem/musical tone generator	0	1	0	0	1	0	A
PCD3316	Caller-ID on Call Waiting (CIDCW) receiver	1	1	1	0	0	0	0
PCD4440	Voice scrambler/descrambler for mobile telephones	1	1	0	1	1	1	A
PCD5002	Pager decoder	0	1	0	0	1	1	1
PCD5096	Universal codec	0	0	1	1	0	A	A
PCE84C467/8	8-bit CMOS auto-sync monitor controller	0	1	1	0	0	1	1
PCE84C882	8-bit microcontroller for monitor applications	0	1	1	0	0	1	1
PCE84C886	8-bit microcontroller for monitor applications	0	1	1	0	0	1	1
PCF2103	LCD controller/driver	0	1	1	1	0	1	A
PCF2104	LCD controller/driver	0	1	1	1	0	1	A
PCF2105	LCD controller/driver	0	1	1	1	0	1	A
PCF2113	LCD controller/driver	0	1	1	1	0	1	A
PCF2116	LCD controller/driver	0	1	1	1	0	1	A
PCF2119	LCD controller/driver	0	1	1	1	0	1	A
PCF8522/4	512 × 8-bit CMOS EEPROM	1	0	1	0	A	A	A
PCF8531	34 × 128 pixel matrix driver	0	1	1	1	1	0	A
PCF8533	Universal LCD driver for low multiplex rates	0	1	1	1	0	0	A
PCF8535	65 × 133 pixel matrix LCD driver	0	1	1	1	1	A	A
PCF8548	65 × 102 pixels matrix LCD driver	0	1	1	1	1	0	A
PCF8549	65 × 102 pixels matrix LCD driver	0	1	1	1	1	0	A
PCF8563	Real-time clock/calendar	1	0	1	0	0	0	1
PCF8566	96-segment LCD driver 1:1 - 1:4 Mux rates	0	1	1	1	1	1	A
PCF8568	LCD row driver for dot matrix displays	0	1	1	1	1	0	A
PCF8569	LCD column driver for dot matrix displays	0	1	1	1	1	0	A
PCF8570	256 × 8-bit static RAM	1	0	1	0	A	A	A
PCF8573	Clock/calendar	1	1	0	1	0	A	A
PCF8574	8-bit remote I/O port (I²C-bus to parallel converter)	0	1	0	0	A	A	A

Assigned I²C-bus addresses

TYPE NUMBER	DESCRIPTION	I²C SLAVE ADDRESSES(1)						
		A6	A5	A4	A3	A2	A1	A0
PCF8574A	8-bit remote I/O port (I²C-bus to parallel converter)	0	1	1	1	A	A	A
PCF8575	Remote 16-bit I/O expander	0	1	0	0	A	A	A
PCF8575C	Remote 16-bit I/O expander	0	1	0	0	A	A	A
PCF8576	16-segment LCD driver 1:1 - 1:4 Mux rates	0	1	1	1	0	0	A
PCF8576C	16-segment LCD driver 1:1 - 1:4 Mux rates	0	1	1	1	0	0	A
PCF8577C	32/64-segment LCD display driver	0	1	1	1	0	1	0
PCF8578/9	Row/column LCD dot matrix driver/display	0	1	1	1	1	0	A
PCF8582/A	256 × 8-bit EEPROM	1	0	1	0	A	A	A
PCF8583	256 × 8-bit RAM/clock/calendar	1	0	1	0	0	0	A
PCF8584	I²C-bus controller	X	X	X	X	X	X	X
PCF8591	4-channel, 8-bit Mux ADC and one DAC	1	0	0	1	A	A	A
PCF8593	Low-power clock calender	1	0	1	0	0	0	1
PCX8594	512 × 8-bit CMOS EEPROM	1	0	1	0	A	A	P
PCX8598	1024 × 8-bit CMOS EEPROM	1	0	1	0	A	P	P
PDIUSB11	Universal serial bus	0	0	1	1	0	1	1
SAA1064	4-digit LED driver	0	1	1	1	0	A	A
SAA1300	Tuner switch circuit	0	1	0	0	0	A	A
SAA1770	D2MAC decoder for satellite and cable TV	0	0	1	1	1	1	A
SAA2502	MPEG audio source decoder	0	0	1	1	1	0	1
SAA2510	Video-CD MPEG-audio/video decoder	0	0	1	1	0	1	A
SAA2530	ADR/DMX digital receiver	0	0	0	1	1	A	A
SAA4700/T	VPS dataline processor	0	0	1	0	0	0	A
SAA5233	Dual standard PDC decoder	0	0	1	0	0	0	A
SAA5243	Computer controlled teletext circuit	0	0	1	0	0	0	1
SAA5244	Integrated VIP and teletext	0	0	1	0	0	0	1
SAA5245	525-line teletext decoder/controller	0	0	1	0	0	0	1
SAA5246A	Integrated VIP and teletext	0	0	1	0	0	0	1
SAA5249	VIP and teletext controller	0	0	1	0	0	0	1
SAA5252	Line 21 decoder	0	0	1	0	1	0	0
SAA5301	MOJI processor for Japan/China	0	1	1	0	0	0	0
SAA6750	MPEG2 encoder for Desk Top Video (=SAA7137)	0	1	0	0	0	0	0
SAA7110A	Digital multistandard decoder	1	0	0	1	1	1	A
SAA7140B	High performance video scaler	0	1	1	1	0	0	A
SAA7151B	8-bit digital multistandard TV decoder	1	0	0	0	1	A	1
SAA7165	Video enhancement D/A processor	1	0	1	1	1	1	1
SAA7186	Digital video scaler	1	0	1	1	1	A	0
SAA7191B	Digital multistandard TV decoder	1	0	0	0	1	A	1
SAA7192	Digital colour space-converter	1	1	1	0	0	0	A
SAA7199B	Digital multistandard encoder	1	0	1	1	0	0	A

Assigned I²C-bus addresses

TYPE NUMBER	DESCRIPTION	I²C SLAVE ADDRESSES[1]						
		A6	A5	A4	A3	A2	A1	A0
SAA7370	CD-decoder plus digital servo processor	0	0	1	1	0	0	A
SAA9056	Digital SCAM colour decoder	1	0	0	0	1	A	1
SAA9065	Video enhancement and D/A processor	1	0	1	1	1	1	1
SAB9075H	PIP controller for NTSC	0	0	1	0	1	1	A
SAF1135	Dataline 16 decoder for VPS (call array)	0	0	1	0	0	A	A
TDA1551Q	2 × 22 W BTL audio power amplifier	1	1	0	1	1	0	0
TDA4670/1/2	Picture signal improvement (PSI) circuit	1	0	0	0	1	0	0
TDA4680/5/7/8	Video processor	1	0	0	0	1	0	0
TDA4780	Video control with gamma control	1	0	0	0	1	0	0
TDA4845	Vector processor for TV-pictures tubes	1	1	0	1	1	A	A
TDA4885	150 MHz video controller	1	0	0	0	1	0	0
TDA8043	QPSK demodulator and decoder	1	1	0	1	0	0	A
TDA8045	QAM-64 demodulator	0	0	0	1	1	A	A
TDA4853/4	Autosync deflection processor	1	0	0	0	1	1	0
TDA8366	Multistandard one-chip video processor	1	0	0	0	1	0	1
TDA8373	NTSC one-chip video processor	1	0	0	0	1	0	1
TDA8374	Multistandard one-chip video processor	1	0	0	0	1	0	1
TDA8375/A	Multistandard one-chip video processor	1	0	0	0	1	0	1
TDA8376/A	Multistandard one-chip video processor	1	0	0	0	1	0	1
TDA8415	TV/VCR stereo/dual sound processor	1	0	0	0	0	1	0
TDA8416	TV/VCR stereo/dual sound processor	1	0	1	1	0	1	0
TDA8417	TV/VCR stereo/dual sound processor	1	0	0	0	0	1	0
TDA8421	Audio processor	1	0	0	0	0	0	A
TDA8424/5/6	Audio processor	1	0	0	0	0	0	1
TDA8433	TV deflection processor	1	0	0	0	1	1	A
TDA8440	Video/audio switch	1	0	0	1	A	A	A
TDA8442	Interface for colour decoder	1	0	0	0	1	0	0
TDA8443A	YUV/RGB matrix switch	1	1	0	1	A	A	A
TDA8444	Octuple 6-bit DAC	0	1	0	0	A	A	A
TDA8480T	RGB gamma-correction processor	1	0	0	0	0	1	A
TDA8540	4 × 4 video switch matrix	1	0	0	1	A	A	A
TDA8722	Negative video modulator with FM sound	1	1	0	0	1	0	0
TDA8735	150 MHz PLL frequency synthesiser	1	1	0	0	0	1	A
TDA8745	Satellite sound decoder	1	1	0	1	0	1	A
TDA8752	Triple fast ADC for LCD	1	0	0	1	1	A	A
TDA9141/3/4	Alignment-free multistandard decoder	1	0	0	0	1	A	1
TDA9150B	Deflection processor	1	0	0	0	1	1	0
TDA9151B	Programmable deflection processor	1	0	0	0	1	1	0
TDA9160	Multistandard decoder/sync. processor	1	0	0	0	1	A	1

Assigned I²C-bus addresses — Selection guide

TYPE NUMBER	DESCRIPTION	I²C SLAVE ADDRESSES(1)						
		A6	A5	A4	A3	A2	A1	A0
TDA9161A	Bus-controlled decoder/sync. processor	1	0	0	0	1	0	1
TDA9162	Multistandard decoder/sync. processor	1	0	0	0	1	A	1
TDA9170	YUV processor with picture improvement	1	1	0	1	0	0	A
TDA9177	2nd address for LTI (1st is '40')	1	1	1	0	0	0	0
TDA9177	YUV transient improvement processor	0	1	0	0	0	0	0
TDA9178	2nd address for LTI (1st is '40')	1	1	1	0	0	0	0
TDA9178	YUV transient improvement processor	0	1	0	0	0	0	0
TDA9610	Audio FM processor for VHS	1	0	1	1	1	0	0
TDA9614H	Audio processor for VHS	1	0	1	1	1	0	0
TDA9840	TV stereo/dual sound processor	1	0	0	0	0	1	0
TDA9850	BTSC stereo/SAP decoder	1	0	1	1	0	1	A
TDA9852	BTSC stereo/SAP decoder	1	0	1	1	0	1	1
TDA9855	BTSC stereo/SAP decoder	1	0	1	1	0	1	A
TDA9860	Hi-fi audio processor	1	0	0	0	0	0	A
TEA6100	FM/IF for computer-controlled radio	1	1	0	0	0	0	1
TEA6300	Sound fader control and preamplifier/source selector	1	0	0	0	0	0	0
TEA6320/1/2/3	Sound fader control circuit	1	0	0	0	0	0	0
TEA6330	Tone/volume controller	1	0	0	0	0	0	0
TEA6360	5-band equalizer	1	0	0	0	1	1	A
TEA6821/2	Car radio AM	1	1	0	0	0	1	0
TEA6824T	Car radio IF IC	1	1	0	0	0	1	0
TSA5511/2/4	1.3 GHz PLL frequency synthesizer for TV	1	1	0	0	0	A	A
TSA5522/3M	1.4 GHz PLL frequency synthesizer for TV	1	1	0	0	0	A	A
TSA6057	Radio tuning PLL frequency synthesizer	1	1	0	0	0	1	A
TSA6060	Radio tuning PLL frequency synthesizer	1	1	0	0	0	1	A
UMA1000T	Data processor for mobile telephones	1	1	0	1	1	A	A
UMA1014	Frequency synthesizer for mobile telephones	1	1	0	0	0	1	A

Note

1. X = Don't care, A = Programmable address bit, P = Page selection bit.

I²C-BUS ALLOCATION TABLE (IN GROUP ORDER)

The group number represents the hexadecimal equivalent of the four most significant bits of the slave address (A6-A3).

GROUP[1]			TYPE NUMBER	DESCRIPTION
Group 0 (0000)				
0	0	0	-	General call address
X	X	X	-	Reserved addresses
Group 1 (0001)				
1	A1	A0	SAA2530	ADR/DMX digital receiver
1	A1	A0	TDA8045	QAM-64 demodulator
Group 2 (0010)				
0	0	A0	SAA4700/T	VPS dataline processor
0	0	A0	SAA5233	Dual standard PDC decoder
0	0	1	SAA5243	Computer controlled teletext circuit
0	0	1	SAA5244	Integrated VIP and teletext
0	0	1	SAA5245	525-line teletext decoder/controller
0	0	1	SAA5246A	Integrated VIP and teletext
0	0	1	SAA5249	VIP and teletext controller
0	A1	A0	CCR921	RDS/RBDS decoder
0	A1	A0	SAF1135	Dataline 16 decoder for VPS (call array)
1	0	0	SAA5252	Line 21 decoder
1	1	A0	SAB9075H	PIP controller for NTSC
Group 3 (0011)				
0	0	A0	SAA7370	CD-decoder plus digital servo processor
0	A1	A0	PCD5096	Universal codec
0	1	A0	SAA2510	Video-CD MPEG-audio/video decoder
0	1	1	PDIUSB11	Universal serial bus
1	0	1	SAA2502	MPEG audio source decoder
1	1	A0	SAA1770	D2MAC decoder for satellite and cable TV
Group 4 (0100)				
0	0	0	SAA6750	MPEG2 encoder for Desk Top Video (=SAA7137)
0	0	0	TDA9177	YUV transient improvement processor
0	0	0	TDA9178	YUV transient improvement processor
0	0	A0	PCA1070	Programmable speech transmission IC
0	A1	A0	PCF8575	Remote 16-bit I/O expander
0	A1	A0	PCF8575C	Remote 16-bit I/O expander
0	A1	A0	SAA1300	Tuner switch circuit
A2	A1	A0	TDA8444	Octuple 6-bit DAC
A2	A1	A0	PCF8574	8-bit remote I/O port (I²C-bus to parallel converter)
1	0	A0	PCD3311C	DTMF/modem/musical tone generator
1	0	A0	PCD3312C	DTMF/modem/musical tone generator
1	1	1	PCD5002	Pager decoder

GROUP[1]			TYPE NUMBER	DESCRIPTION
Group 6 (0110)				
0	0	0	SAA5301	MOJI processor for Japan/China
0	1	1	PCE84C467/8	8-bit CMOS auto-sync monitor controller
0	1	1	PCE84C882	8-bit microcontroller for monitor applications
0	1	1	PCE84C886	8-bit microcontroller for monitor applications
Group 7 (0111)				
0	0	A0	SAA7140B	High performance video scaler
0	0	A0	PCF8533	Universal LCD driver for low multiplex rates
0	0	A0	PCF8576	16-segment LCD driver 1:1 - 1:4 Mux rates
0	0	A0	PCF8576C	16-segment LCD driver 1:1 - 1:4 Mux rates
0	A1	A0	SAA1064	4-digit LED driver
A2	A1	A0	PCF8574A	8-bit remote I/O port (I²C-bus to parallel converter)
0	1	0	PCF8577C	32/64-segment LCD display driver
0	1	A0	PCF2103	LCD controller/driver
0	1	A0	PCF2104	LCD controller/driver
0	1	A0	PCF2105	LCD controller/driver
0	1	A0	PCF2113	LCD controller/driver
0	1	A0	PCF2119	LCD controller/driver
0	1	A0	SAA2116	LCD controller/driver
1	0	A0	PCF8531	34 × 128 pixel matrix driver
1	0	A0	PCF8548	65 × 102 pixels matrix LCD driver
1	0	A0	PCF8549	65 × 102 pixels matrix LCD driver
1	0	A0	PCF8578/9	Row/column LCD dot matrix driver/display
1	0	A0	PCF8568	LCD row driver for dot matrix displays
1	0	A0	PCF8569	LCD column driver for dot matrix displays
1	A1	A0	PCF8535	65 × 133 pixel matrix LCD driver
1	1	A0	OM4085	Universal LCD driver for low multiplex rates
1	1	A0	PCF8566	96-segment LCD driver 1:1 - 1:4 Mux rates
Group 8 (1000)				
0	0	0	TEA6300	Sound fader control and preamplifier/source selector
0	0	0	TEA6320/1/2/3	Sound fader control circuit
0	0	0	TEA6330	Tone/volume controller
0	0	A0	NE5751	Audio processor for RF communication
0	0	A0	TDA8421	Audio processor
0	0	A0	TDA9860	Hi-fi audio processor
0	0	1	TDA8424/5/6	Audio processor
0	1	0	TDA8415	TV/VCR stereo/dual sound processor
0	1	0	TDA8417	TV/VCR stereo/dual sound processor
0	1	0	TDA9840	TV stereo/dual sound processor
0	1	A0	TDA8480T	RGB gamma-correction processor

I²C address allocation table

GROUP[1]			TYPE NUMBER	DESCRIPTION
1	0	0	TDA4670/1/2	Picture signal improvement (PSI) circuit
1	0	0	TDA4680/5/7/8	Video processor
1	0	0	TDA4780	Video control with gamma control
1	0	0	TDA4885	150 MHz video controller
1	0	0	TDA8442	Interface for colour decoder
1	0	1	TDA8366	Multistandard one-chip video processor
1	0	1	TDA8373	NTSC one-chip video processor
1	0	1	TDA8374	Multistandard one-chip video processor
1	0	1	TDA8375/A	Multistandard one-chip video processor
1	0	1	TDA8376/A	Multistandard one-chip video processor
1	0	1	TDA9161A	Bus-controlled decoder/sync. processor
1	A1	1	SAA7151B	8-bit digital multistandard TV decoder
1	A1	1	SAA7191B	Digital multistandard TV decoder
1	A1	1	SAA9056	Digital SCAM colour decoder
1	A1	1	TDA9141/3/4	Alignment-free multistandard decoder
1	A1	1	TDA9160	Multistandard decoder/sync. processor
1	A1	1	TDA9162	Multistandard decoder/sync. processor
1	1	0	TDA4853/4	Autosync deflection processor
1	1	0	TDA9150B	Deflection processor
1	1	0	TDA9151B	Programmable deflection processor
1	1	A0	TEA6360	5-band equalizer
1	1	A0	TDA8433	TV deflection processor
Group 9 (1001)				
A2	A1	A0	PCF8591	4-channel, 8-bit Mux ADC and one DAC
A2	A1	A0	TDA8440	Video/audio switch
A2	A1	A0	TDA8540	4 × 4 video switch matrix
1	A1	A0	TDA8752	Triple fast ADC for LCD
1	1	A0	SAA7110A	Digital multistandard decoder
Group A (1010)				
0	0	0	PCB2421	1K dual mode serial EEPROM
0	0	A0	PCF8583	Real-time clock/calendar
0	0	1	PCF8563	Low-power clock calender
0	0	1	PCF8593	Low-power clock calender
A2	A1	A0	PCF8570	256 × 8-bit static RAM
A2	A1	A0	PCF8522/4	512 × 8-bit CMOS EEPROM
A2	A1	A0	PCA8581/C	128 × 8-bit EEPROM
A2	A1	A0	PCF8582/A	256 × 8-bit EEPROM
A2	A1	P0	PCX8594	512 × 8-bit CMOS EEPROM
A2	P1	P0	PCX8598	1024 × 8-bit CMOS EEPROM

I²C address allocation table — Selection guide

GROUP[1]			TYPE NUMBER	DESCRIPTION
Group B (1011)				
0	0	A0	SAA7199B	Digital multistandard encoder
0	1	0	TDA8416	TV/VCR stereo/dual sound processor
0	1	A0	TDA9850	BTSC stereo/SAP decoder
0	1	A0	TDA9855	BTSC stereo/SAP decoder
0	1	1	TDA9852	BTSC stereo/SAP decoder
1	0	0	TDA9610	Audio FM processor for VHS
1	0	0	TDA9614H	Audio processor for VHS
1	A1	0	SAA7186	Digital video scaler
1	0	1	PCA8516	Stand-alone OSD IC
1	1	1	SAA7165	Video enhancement D/A processor
1	1	1	SAA9065	Video enhancement and D/A processor
Group C (1100)				
0	0	1	TEA6100	FM/IF for computer-controlled radio
0	1	0	TEA6821/2	Car radio AM
0	1	0	TEA6824T	Car radio IF IC
0	A1	A0	TSA5511/2/4	1.3 GHz PLL frequency synthesizer for TV
0	A1	A0	TSA5522/3M	1.4 GHz PLL frequency synthesizer for TV
0	1	A0	TDA8735	150 MHz PLL frequency synthesizer
0	1	A0	TSA6057	Radio tuning PLL frequency synthesizer
0	1	A0	TSA6060	Radio tuning PLL frequency synthesizer
0	1	A0	UMA1014	Frequency synthesizer for mobile telephones
1	0	0	TDA8722	Negative video modulator with FM sound
Group D (1101)				
0	0	A0	TDA8043	QPSK demodulator and decoder
0	0	A0	TDA9170	YUV processor with picture improvement
0	A1	A0	PCF8573	Clock/calendar
A2	A1	A0	TDA8443A	YUV/RGB matrix switch
0	1	A0	TDA8745	Satellite sound decoder
1	0	0	TDA1551Q	2 × 22 W BTL audio power amplifier
1	A1	A0	TDA4845	Vector processor for TV-pictures tubes
1	A1	A0	UMA1000T	Data processor for mobile telephones
1	1	A0	PCD4440	Voice scrambler/descrambler for mobile telephones
Group E (1110)				
0	0	0	PCD3316	Caller-ID on Call Waiting (CIDCW) receiver
0	0	0	TDA9177	2nd address for LTI (1st is '40')
0	0	0	TDA9178	2nd address for LTI (1st is '40')
0	0	A0	SAA7192	Digital colour space-converter

I²C address allocation table

GROUP[1]			TYPE NUMBER	DESCRIPTION
Group F (1111)				
X	X	X	-	Reserved addresses
Group 0 to F (0000 to 1111)				
X	X	X	PCF8584	I²C-bus controller

Note

1. X = Don't care, A = Programmable address bit, P = Page selection bit

Microcontroller internet and bulletin board access

INTERNET ACCESS

Philips Semiconductors World Wide Web:

http://www.semiconductors.philips.com

Microcontroller Support Files:

Using a web browser: www.philipsmcu.com

Using FTP: ftp.philipsmcu.com

Philips Microcontroller Discussion Forum:

Send forum messages to: forum@philipsmcu.com

Forum messages on the web: webforum.philipsmcu.com

Email forum Subscriptions*: forum–request@philipsmcu.com

Philips Microcontroller Newsletter:

Newsletter Subscriptions*: news–request@philipsmcu.com

80C51 Applications Support Email Address:

80C51_help@sv.sc.philips.com

XA Applications Support Email Address:

XA_help@sv.sc.philips.com

* These are email-oriented internet services. To subscribe, send an email to the internet address listed above and include 'subscribe' in the subject category.

BULLETIN BOARD

To better serve our customers, Philips maintains a microcontroller bulletin board. This computer bulletin board system features microcontroller newsletters, application and demonstration programs for download, and the ability to send messages to microcontroller application engineers.

The telephone number is:

+31 40 2721102
MAX 14.400 baud
Standards V32/V42/V42.bis/HST
(The Netherlands)

Files from the former North American Bulletin Board are available on the world wide web (see previous page).

Sunnyvale ROMcode Bulletin Board

We also have a ROM code bulletin board through which you can submit ROM codes. This is a closed bulletin board for security reasons. To get an ID, contact your local sales office. The system can be accessed with a 2400, 1200, or 300 baud modem, and is available 24 hours a day.

The telephone number is:

(408) 991-3459

All code for application notes in this databook are available on the Philips web site.

80C51 microcontroller family features guide

Memory from 1K to 8K

Prefix	Part Number ROM/ROMless/ OTP/Flash	Memory			New and Improved (Note 6)	Counter				I/O Pins	Serial Interfaces	Comments/ Special Features
		ROM	EPROM	RAM		#	PWM	PCA	WD			
P	83C750	1K		64		1	N	N	N	19	–	Lowest cost, 1 (16-bit) Timer, SSOP
P	87C750		1K	64		1	N	N	N	19	–	Lowest cost, 1 (16-bit) Timer, SSOP
P	83C748	2K		64		2	N	N	N	19	–	'751 w/o I^2C, 1 (16-bit) Timer, SSOP
P	87C748		2K	64		2	N	N	N	19	–	'751 w/o I^2C, 1 (16-bit) Timer, SSOP
S	83C751	2K		64		1	N	N	N	19	I^2C (bit)	1 (16-bit) Timer, SSOP
S	87C751		2K	64		1	N	N	N	19	I^2C (bit)	1 (16-bit) Timer, SSOP
P	83C749	2K		64		2	Y	N	N	21	–	'752 w/o I^2C, 1 (16-bit) Timer, SSOP
P	87C749		2K	64		2	Y	N	N	21	–	'752 w/o I^2C, 1 (16-bit) Timer, SSOP
S	83C752	2K		64		1	Y	N	N	21	I^2C (bit)	1 (16-bit) Timer, SSOP
S	87C752		2K	64		1	Y	N	N	21	I^2C (bit)	1 (16-bit) Timer, SSOP
P	***80C51/80C31***	***4K***		***128***	***Y***	***2***	***N***	***N***	***N***	***32***	***UART***	***CMOS***
P	***87C51***		***4K***	***128***	***Y***	***2***	***N***	***N***	***N***	***32***	***UART***	***CMOS***
P	80CL51/80CL31	4K		128		2	N	N	N	32	UART	Low voltage (1.8V–6V), Low power
P	83C434	4K		128								LCD driver
P	83CL410/80CL410	4K		128		2	N	N	N	32	I^2C	Low voltage (1.8V–6V), Low power
SC	83C451/80C451	4K		128		2	N	N	N	56	UART	Extended I/O, Processor bus interface
SC	87C451		4K	128		2	N	N	N	56	UART	Extended I/O, Processor bus interface
P	83C550/80C550	4K		128		2	N	N	Y	32	UART	8 channel 8-bit A/D w/Hdw WD
P	87C550		4K	128		2	N	N	Y	32	UART	8 channel 8-bit A/D w/Hdw WD
P	83C851/80C851	4K		128		2	N	N	N	32	UART	256B EEPROM, 80C51 pin-compatible
P	83C754	4K		256		3	Y	Y	N	11	UART	8-bit DAC, 3-input mux comparator, Ref V Out
P	87C754		4K	256		3	Y	Y	N	11	UART	(see above)
P	83C852	6K		256		2	N	N	N	16	–	Smartcard controller with 2K EEPROM (Data, Code) Cryptographic Calc Unit
P	***80C52/80C32***	***8K***		***256***	***Y***	***3***	***N***	***N***	***N***	***32***	***UART***	***80C51 pin-compatible***
P	***87C52***		***8K***	***256***	***Y***	***3***	***N***	***N***	***N***	***32***	***UART***	***80C51 pin-compatible***
P	***83C51RA+/80C51RA+***	***8K***		***512***	***Y***	***4***	***Y***	***Y***	***Y***	***32***	***UART***	***w/Hdw WD, 2.7–5.5V versions***
P	***89C51RA+/87C51RA+***		***8K***	***512***	***Y***	***4***	***Y***	***Y***	***Y***	***32***		***(see above) (FLASH–5V only)***
P	83C652/80C652	8K		256		2	N	N	N	32	UART, I^2C	80C51 pin-compatible
S	87C652		8K	256		2	N	N	N	32	UART, I^2C	80C51 pin-compatible
P	83C453/80C453	8K		256		2	N	N	N	56	UART	Extended I/O, processor bus interface
P	87C453		8K	256		2	N	N	N	56	UART	Extended I/O, processor bus interface
P	***83C51FA/80C51FA***	***8K***		***256***	***Y***	***4***	***Y***	***Y***	***Y***	***32***	***UART***	***Enhanced UART, 3 timers + PCA***
P	***87C51FA***		***8K***	***256***	***Y***	***4***	***Y***	***Y***	***Y***	***32***	***UART***	***Enhanced UART, 3 timers + PCA***
P	83C575/80C575	8K		256		4	Y	Y	Y	32	UART	w/Hdw WD, low voltage detect, osc fail detect, analog comparators, PCA
P	87C575		8K	256		4	Y	Y	Y	32	UART	(see above)
P	83C576	8K		256		4	Y	Y	Y	32	UART	Same as 8xC575 plus UPI and 10-bit A/D
P	87C576	8K		256		4	Y	Y	Y	32	UART	(see above)
P	83C845	8K		256		2	Y	N	N	28	–	On-screen display, 9 PWM outputs, 3 software A/D inputs
P	83C880	8K		512								DDC interface for monitors, auto sync detection and sync processor
PCx	83C562/80C562	8K		256		3	Y	N	Y	48	UART	8 channel 8-bit A/D, 2 PWM outputs, Capture/Compare timer, w/Hdw WD
PCx	83C552/80C552	8K		256		3	Y	N	Y	48	UART, I^2C	8 channel 10-bit A/D, 2 PWM outputs, Capture/Compare timer, w/Hdw WD
S	87C552		8K	256		3	Y	N	Y	48	UART, I^2C	(see above)
P	83C834	8K		256								LCD driver
P	83CL883	8K	8K	256		3	N	N	Y	19	UART	1.8–3.6V operation, low voltage detection
P	83CL884	8K	8K	256		3	N	N	Y	18	UART	1.8–3.6V operation, low voltage detection

NOTES:
Part number prefixes are noted in the first column.
All combinations of part type, speed, temperature and package may not be available.
Parts in Italics bold are 51plus microcontrollers.

Memory from 1K to 8K (continued)

Part Number ROM/ROMless/ OTP/Flash		A/D		External Interrupt	Program Security ?	Clock Freq. (MHz)	Temperature Range (°C)			Package		
		Bits	Channels				0 to +70	–40 to +85	–55 to +125	PDIP	PLCC	PQFP/SSOP
83C750	S			2	N	3.5 to 40	X	X		N24	A28	DB24 (0–70F)
87C750	S			2	Y	3.5 to 40	X	X		N24	A28	DB24 (0–70F)
83C748	S			2	N	3.5 to 16	X	X		N24	A28	DB24 (0–70F)
87C748	S			2	Y	3.5 to 16	X	X		N24	A28	DB24 (0–70F)
83C751	S			2	N	3.5 to 16	X	X		N24	A28	DB24 (0–70F)
87C751	S			2	Y	3.5 to 16	X	X		N24	A28	DB24 (0–70F)
83C749	S	8	5	2	N	3.5 to 16	X	X		N28	A28	DB28 (0–70F)
87C749	S	8	5	2	Y	3.5 to 16	X	X		N28	A28	DB28 (0–70F)
83C752	S	8	5	2	N	3.5 to 16	X	X	X	N28	A28	DB28 (0–70F)
87C752	S	8	5	2	Y	3.5 to 16	X	X	X	N28	A28	DB28 (0–70F)
80C51/80C31	***S***			***2***	***Y***	***0 to 33***	***X***	***X***		***N40***	***A44***	***B44 (5)***
87C51	***S***			***2***	***Y***	***0 to 33***	***X***	***X***		***N40***	***A44***	***B44 (5)***
80CL51/80CL31	Z			10	N	0 to 16 (1)		X		N40 (2)		B44
83C434	T					12MHz		X		NB42		B44
83CL410/80CL410	Z			10	N	0 to 12 (1)		X		N40 (2)		B44
83C451/80C451	S			2	N	3.5 to 16	X	X		N64 (4)	A68	
87C451	S			2	Y	3.5 to 16	X	X		N64 (4)	A68	
83C550/80C550	S	8	8	2	Y	3.5 to 16	X	X		N40	A44	
87C550	S	8	8	2	Y	3.5 to 16	X	X		N40	A44	
83C851/80C851	H			2	Y	1.2 to 16	X	X		N40	A44	B44
83C754	S			2	Y	3.5 to 16	X					
87C754	S			2	Y	3.5 to 16	X					DB28
83C852	H			1	Y	1 to 12	X			SO28 or die		
80C52/80C32	***S***			***2***	***Y***	***0 to 33***	***X***	***X***		***N40***	***A44***	***B44 (5)***
87C52	***S***			***2***	***Y***	***0 to 33***	***X***	***X***	***X***	***N40***	***A44***	***B44 (5)***
83C51RA+/80C51RA+	***S***			***2***	***Y***	***0 to 33***	***X***	***X***		***N40***	***A44***	***B44***
89C51RA+/87C51RA+	***S***			***2***	***Y***	***0 to 33***	***X***	***X***		***N40***	***A44***	***B44***
83C652/80C652	H			2	Y	3.5 to 24	X	X	–40 to +125	N40	A44	B44
87C652	S			2	Y	3.5 to 16	X	X	X	N40	A44	
83C453/80C453	S			2	N	3.5 to 16	X	X			A68	
87C453	S			2	Y	3.5 to 16	X	X			A68	
83C51FA/80C51FA	***S***			***2***	***Y***	***0 to 33***	***X***	***X***		***N40***	***A44***	***B44***
87C51FA	***S***			***2***	***Y***	***0 to 33***	***X***	***X***		***N40***	***A44***	***B44***
83C575/80C575	S			2	Y	4 to 16	X	X	X	N40	A44	B44
87C575	S			2	Y	4 to 16	X	X	X	N40	A44	B44
83C576	S	10	6	2	Y	6 to 16	X	X	X	N40	A44	B44
87C576	S	10	6	2	Y	6 to 16	X	X	X	N40	A44	B44
83C845	T			2	N	3.5 to 20	X			NB42		
83C880												
83C562/80C562	H	8	8	2	N	3.5 to 16	X	X	–40 to +125		A68	B80
83C552/80C552	H	10	8	2	N	3.5 to 30	X	X	–40 to +125		A68	B80
87C552	S	10	8	2	Y	3.5 to 16	X				A68	
83C834	T					16		X		NB42		B44
83CL883	Z			8		3.58	–25 to +70					SO28
83CL884	Z			8		3.58	–25 to +70					SO28

NOTES:
Production Centers are indicated in the second column:
H = Hamburg; S = Sunnyvale, T = Taiwan, Z = Zurich
All combinatiuons of part type, speed, temperature and package may not be available.
Parts in Italics bold are 51plus microcontrollers.

1. Oscillator options start from 32kHz.
2. Also available in VSO40 package.
3. Also available in VSO56 package.
4. Not recommended for new design.
5. Package available up to 16MHz only.
6. New and Improved devices operate from 2.7V–5.5V @ 16MHz. Static Core, 33MHz operation, Dual Data Pointers, and more.

Memory from 12K to 64K

Prefix	Part Number ROM/ROMless/ OTP/Flash	Memory			New and Improved (Note 6)	Counter				I/O Pins	Serial Interfaces	Comments/ Special Features
		ROM	EPROM/ FLASH	RAM		#	PWM	PCA	WD			
P	83C145	12K		256		2	Y	N	N	28	–	On-Screen Display, 9 PWM outputs, 3 software A/D inputs
P	83CL887/87CL887	12K	12K	256		3	N	N	Y	18	UART	1.8V–3.6V operation, low voltage detection
P	83C055	16K		256		2	Y	N	N	28	–	On-Screen Display, 9 PWM outputs 3 software A/D inputs
P	87C055		16K	256		2	Y	N	N	28	–	(see above)
P	83C180	16K	16K	512								DDC interface for monitors, auto sync detection and sync processor
P	***80C54***	***16K***		***256***	***Y***	***3***	***N***	***N***	***N***	***32***	***UART***	***Standard; 80C51 compatible***
P	***87C54***		***16K***	***256***	***Y***	***3***	***N***	***N***	***N***	***32***	***UART***	***Standard; 87C51 compatible***
P	89C138		16K	256		3	N	N	N	32	UART	Reduced EMI, Hdw. Watchdog timer
P	83C654/80C654	16K		256		2	N	N	N	32	UART, I²C	80C51 pin-compatible
S	87C654		16K	256		2	N	N	N	32	UART, I²C	80C51 pin-compatible
P	***83C51FB***	***16K***		***256***	***Y***	***4***	***Y***	***Y***	***Y***	***32***	***UART***	***Enhanced UART, 3 timers + PCA***
P	***87C51FB***		***16K***	***256***	***Y***	***4***	***Y***	***Y***	***Y***	***32***	***UART***	***Enhanced UART, 3 timers + PCA***
P	83C524	16K		512		3	N	N	Y	32	UART, I²C-bit	512 RAM
P	87C524		16K	512		3	N	N	Y	32	UART, I²C-bit	512 RAM
P	***83C51RB+***	***16K***		***512***	***Y***	***4***	***Y***	***Y***	***Y***	***32***	***UART***	***Extended RAM (512 bytes), 2.7V–5.5V versions***
P	***89C51RB+/87C51RB+***		***16K***	***512***	***Y***	***4***	***Y***	***Y***	***Y***	***32***	***UART***	***(see above) (FLASH–5V only)***
P	83CL886/87CL886	16K	16K	512		3		N	Y	18	UART	1.8V–3.6V operation, low voltage detection
P	83C592/80C592/ 87C592	16K	16K	512		3	N	N	Y	48	UART, CAN	CAN bus controller, 8×10-bit A/D, 2 PWM outputs, Capture/Compare timer
P	83C280	24K		512								DDC interface for monitors, auto sync detection and sync processor
P	83C380	32K		512			Y					DDC interface for monitors, auto sync detection and sync processor
P	***80C58***	***32K***		***256***	***Y***	***3***	***N***	***N***	***N***	***32***	***UART***	***Standard; 80C51 compatible***
P	***87C58***		***32K***	***256***	***Y***	***3***	***N***	***N***	***N***	***32***	***UART***	***Standard; 87C51 compatible***
P	***83C51FC***	***32K***		***256***	***Y***	***4***	***Y***	***Y***	***Y***	***32***	***UART***	***Enhanced UART, 3 timers + PCA***
P	***87C51FC***		***32K***	***256***	***Y***	***4***	***Y***	***Y***	***Y***	***32***	***UART***	***Enhanced UART, 3 timers + PCA***
P	83C528/80C528	32K		512		3	N	N	Y	32	UART, I²C-bit	Large memory for high level languages
P	87C528		32K	512		3	N	N	Y	32	UART, I²C-bit	Large memory for high level languages
P	83CE528	32K		512		3	N	N	Y	32	UART, I²C-bit	8XC528 with Reduced EMI
P	***83C51RC+***	***32K***		***512***	***Y***	***4***	***Y***	***Y***	***Y***	***32***	***UART***	***Extended RAM (512 bytes), 2.7V–5.5V versions***
P	***89C51RC+/87C51RC+***		***32K***	***512***	***Y***	***4***	***Y***	***Y***	***Y***	***32***	***UART***	***(see above) (FLASH–5V only)***
P	89C238		32K	256		3	N	N	Y	32	UART	Reduced EMI, Hdw. Watchdog timer
P	83CE598/80CE598/ 89CE598	32K	32K	512		3	Y	N	Y	48	UART, CAN	CAN bus controller, 8×10-bit A/D, 2 PWM outputs, WD, T2, Reduced EMI
P	83C557E4/80C557E4/ 89C557E4	32K	32K	1024		3	Y	N	Y	48	UART, I²C	Low EMI, 8 Channel 10-bit A/D, 2 PWM outputs, Capture/Compare Timer
P	83C557E6/80C557E6	48K	48K	1536		3	Y	N	Y	48	UART, I²C	(Same as above)
P	83C557E8/80C557E8/ 87C557E8	64K	64K	2048		3	Y	N	Y	48	UART, I²C	(Same as above)
P	89C738	64K		512		3	N	N	N	32	UART	Open Collector outputs
P	***83C51RD+***	***64K***		***1024***	***Y***	***4***	***Y***	***Y***	***Y***	***32***	***UART***	***Extended RAM (1K), 2.7V–5.5V versions***
P	***89C51RD+/87C51RD+***		***64K***	***1024***	***Y***	***4***	***Y***	***Y***	***Y***	***32***	***UART***	***(see above) (FLASH–5V only)***
P	87CL881		64K	2048		3	Y	N	Y	32	UART	1.8V–3.6V operation, low voltage detection
XA Family												
P	51XAG30/G37/G33	32K	32K	512		3	N	N	Y	32	2 UARTs	2.7V–5.5V operation, 16-bit XA core, compatible with 80C51
P	51XAS3		32K	1024		4	Y	Y	Y	50	2 UARTs, I²C	16M byte address range, 2.7V–5.5V operation, 8-bit DAC

NOTES:
Part number prefixes are noted in the first column.
All combinations of part type, speed, temperature and package may not be available.
Parts in Italics bold are 51plus microcontrollers.

Memory from 12K to 64K (continued)

Part Number ROM/ROMless/ OTP/Flash		A/D		External Interrupt	Program Security?	Clock Freq. (MHz)	Temperature Range (°C)			Package		
		Bits	Channels				0 to +70	–40 to +85	–55 to +125	PDIP	PLCC	PQFP/ Other
83C145	T			2	N	3.5 to 20	X			NB42		
83CL887/ 87CL887	T			8	N	3.58	–25 to +70					SO28
83C055	T			2	N	3.5 to 20	X			NB42		
87C055	T			2	N	3.5 to 20	X			NB42		
83C180	T					16		–25 to +85		NB42		
80C54	***S***			***2***	***Y***	***0 to 33***	***X***	***X***		***N40***	***A44***	***B44***
87C54	***S***			***2***	***Y***	***0 to 33***	***X***	***X***		***N40***	***A44***	***B44***
89C138	T			3	Y	3.5 to 40	X			NB42	A44	B44
83C654/80C654	H			2	Y	3.5 to 24	X	X	–40 to +125	R42, N40	A44	B44
87C654	S			2	Y	3.5 to 20	X	X		N40	A44	B44
83C51FB	***S***			***2***	***Y***	***0 to 33***	***X***	***X***		***N40***	***A44***	***B44***
87C51FB	***S***			***2***	***Y***	***0 to 33***	***X***	***X***		***N40***	***A44***	***B44***
83C524	H			2	Y	3.5 to 24	X	X		N40	A44	B44
87C524	S			2	Y	3.5 to 16	X	X		N40	A44	B44
83C51RB+	***S***			***2***	***Y***	***0 to 33***	***X***	***X***		***N40***	***A44***	***B44***
89C51RB+/87C51RB+	***S***			***2***	***Y***	***0 to 33***	***X***	***X***		***N40***	***A44***	***B44***
83CL886/87CL886	Z			8								
83C592/80C592/ 87C592	H	10	8	6	Y	1.2 to 16		X	–40 to +125		A68	
83C280	T					16		–25 to +85		NB42		
83C380	T					16		–25 to +85		NB42		
80C58	***S***			***2***	***Y***	***0 to 33***	***X***	***X***		***N40***	***A44***	***B44***
87C58	***S***			***2***	***Y***	***0 to 33***	***X***	***X***		***N40***	***A44***	***B44***
83C51FC	***S***			***2***	***Y***	***0 to 33***	***X***	***X***		***N40***	***A44***	***B44***
87C51FC	***S***			***2***	***Y***	***0 to 33***	***X***	***X***		***N40***	***A44***	***B44***
83C528/80C528	H			2	Y	3.5 to 16	X	X	–40 to +125	N40, R42	A44	B44
87C528	S			2	Y	3.5 to 16	X	X		N40	A44	B44
83CE528	H			2	Y	3.5 to 16		X			A44	B44
83C51RC+	***S***			***2***	***Y***	***0 to 33***	***X***	***X***		***N40***	***A44***	***B44***
89C51RC+/87C51RC+	***S***			***2***	***Y***	***0 to 33***	***X***	***X***		***N40***	***A44***	***B44***
89C238	T			3	Y	3.5 to 40	X			NB42	A44	B44
83CE598/80CE598 89CE598	H	10	8	6	Y	1.2 to 16		X	–40 to +125			B80
83C557E4/80C557E4 89C557E4	T	10	8	2	Y	1.2 to 16	X	X	–40 to +125			B80
83C557E6/80C557E6	T	10	8	2	Y	1.2 to 16	X	X	–40 to +125			B80
83C557E8/80C557E8 87C557E8	T	10	8	2	Y	1.2 to 16	X	X	–40 to +125			B80
89C738	T			3	N	3.5 to 16	X			N40	A44	B44
83C51RD+	***S***			***2***	***Y***	***0 to 33***	***X***	***X***		***N40***	***A44***	***B44***
89C51RD+/87C51RD+	***S***			***2***	***Y***	***0 to 33***	***X***	***X***		***N40***	***A44***	***B44***
87CL881	T			8		1 to 10	–25 to +70					BD44
XA Family												
51XAG30/G37/G33	S			2	Y	30	X	X			A44	BD44
51XAS3	S	8	8	2	Y	30	X	X			A68	B80

NOTES:
Production Centers are indicated in the second column:
H = Hamburg; S = Sunnyvale, T = Taiwan, Z = Zurich
All combinatiuons of part type, speed, temperature and package may not be available.
Parts in Italics bold are 51plus microcontrollers.

1. Oscillator options start from 32kHz.
2. Also available in VSO40 package.
3. Also available in VSO56 package.
4. Not recommended for new design.
5. Package available up to 16MHz only.
6. New and Improved devices operate from 2.7V–5.5V @ 16MHz. Static Core, 33MHz operation, Dual Data Pointers, and more.

CMOS and NMOS 8-bit microcontroller family

8400 FAMILY CMOS

TYPE	ROM	RAM	SPEED (MHz)	PACKAGE	FUNCTIONS	REMARKS	PROBE SDS	EMULATOR
84C81A	8 k	256	10	DIL28/SO28	20 I/O lines 8-bit timer Byte I^2C		OM1083	OM1025 (LSDS)
84C12A	1 k	64	16	DIL20/SO20	13 I/O lines 8-bit timer		OM1083+ Adapter_1	OM1025 (LSDS)
84C122A 84C122B 84C422A 84C422B 84C822A 84C822B 84C822C	1 k 4 k 8 k	32 32 32	10	A: SO20 B: SO24 C: SO28	Controller for remote control A: 12 I/O B: 16 I/O C: 20 I/O		OM4830	
84C440 84C441 84C443 84C444 84C640 84C641 84C643 84C644 84C840 84C841 84C843 84C844	4 k 4 k 4 k 4 k 6 k 6 k 6 k 6 k 8 k 8 k 8 k 8 k	128 128 128 128 128 128 128 128 192 192 192 192	10 10 10 10 10 10 10 10 10 10 10 10	DIP42 shrunk	RC: 29 I/O lines LC: 28 I/O lines 8-bit timer 1 14-bit PWM 5 6-bit PWM 3-bit ADC OSD 2L-16	I^2C, RC I^2C, LC RC LC I^2C, RC I^2C, LC RC LC I^2C, RC I^2C, LC RC LC	OM1074	For emulation of LC versions, use OM1074 + adapter_3 + 2 adapter_5 Baud for LCDS OM4831
84C646 84C846	6 k 8 k	192 192	10 10	DIP42 shrunk	30 I/O lines DOS clock = PLL 8 bit timer 1-14 bit PWM 4-6 bit PWM 4-7 bit PWM 3-4 bit ADC DOS: 64 disp. RAM 62 char. fonts Char. blinking Shadow modes 8 foreground colors/char. 8 background colors/word DOS: clock: 8 . . 20 MHz	I^2C, RC I^2C, RC	OM4829 + OM4832	OM4833 for LCD584

CMOS and NMOS 8-bit microcontroller family

8400 FAMILY NMOS

TYPE	ROM	RAM	SPEED (MHz)	PACKAGE	FUNCTIONS	REMARKS	EMULATOR TOOLS	REMARKS
8411 8421 8441 8461	1 k 2 k 4 k 6 k	64 64 128 128	6 6 6 6	DIL28/SO28 DIL28/SO28 DIL28/SO28 DIL28/SO28	20 I/O lines 8-bit timer Byte I^2C			OM1025 (LCDS) + OM1026
8422 8442	2 k 4 k	64 128	6 6	DIL20 DIL20	13 I/O lines 8-bit timer Bit I^2C			
8401B	0	128	6	28-pin		Piggyback for 84X1		

3300 FAMILY CMOS

TYPE	ROM	RAM	SPEED (MHz)	PACKAGE	FUNCTIONS	EMULATOR TOOLS
3349A	4 k	224	1–16	DIL28/SO28	20 I/O lines 8-bit timer DTMF generator	OM5501/2
3350A	8 k	128	1–16	QFP44 LQFP32	34 I/O lines 8-bit timer DTMF generator 256 bytes EEPROM	OM5501/2
3351A/C	2 k	64	1–16	DIL28/SO28 LQFP32	20 I/O lines 8-bit timer DTMF generator 128 bytes EEPROM	OM5501/2
3352A/C	4 k	128	1–16	DIL28/SO28 LQFP32	20 I/O lines 8-bit timer DTMF generator 128 byte EEPROM	OM5501/2
3353A/C	6 k	128	1–16	DIL28/SO28 LQFP32	20 I/O lines 8-bit timer DTMF generator Ringer out 128 bytes EEPROM	OM5501/2
3354A	8 k	256	1–16	QFP44	36 I/O lines 2x 8-bit timer DTMF generator Ringer out 256 bytes EEPROM	OM5501/2
3359A	2	64	1–16	DIL28 SO28 LQFP32	20 I/O lines 128 bytes EEPROM DTMF, 2x 8-bit counters	OM5501/2
3755A/3756A	8 k(OTP)	128	1–16	DIL28/SO28	20 I/O lines 2x 8-bit timer DTMF generator Melody output 128 bytes EEPROM	OM5501/2
3354B					Piggyback for 3354A	
All 33xx +37xx						OM1025 + OM5024

NOTE:
Further information on these products can be found in Databook IC03 or on our internet page http://www.semiconductors.philips.com

CMOS 16-bit microcontroller family

16-BIT CONTROLLERS (XA ARCHITECTURE)

TYPE	(EP)ROM	RAM	SPEED (MHz)	FUNCTIONS	REMARKS	DEVELOPMENT TOOLS
XA-G1	8k	512	30	3 timers, watchdog, 2 UARTs	–40 to +125°C	Nohau Ashling Future Designs
XA-G2	16k	512	30	3 timers, watchdog, 2 UARTs	–40 to +125°C	Nohau Ashling Future Designs
XA-G3	32k	512	30	3 timers, watchdog, 2 UARTs	–40 to +125°C	Nohau Ashling Future Designs
XA–S3	32K	1K	30	A/D converter, 3 Timers, PCA, watchdog, 2 UARTS, I^2C		Nohau Future Designs
XA-SCC	0K	256	30	DRAM controller, glueless support for most memory types, dynamic bus sizing, 4 high speed serial communication channels with hardware autobaud, v.54, and 2047, SCp, IDL, 2 timers, watchdog, 100-pin LQFP		Nohau Future Designs Tasking

CMOS 16-bit microcontroller family

16-BIT CONTROLLERS (68000 ARCHITECTURE)

TYPE	(EP)ROM	RAM	SPEED (MHz)	FUNCTIONS	REMARKS	PHILIPS TOOLS	THIRD-PARTY TOOLS
68070	–	–	17.5	2 DMA channels, MMU, UART, 16-bit timer, I^2C, 68000 bus interface, 16Mb address range		OM4160 Microcore 1 OM4160/2 Microcore 2 OM4161 (SBE68070) OM4767/2 XRAY68070SBE high level symbolic debugger OM4222 68070DS development system OM4226 XRAY68070DS high level symbolic debugger	TRACE32-ICE68070 (Lauterbach)
93C101	34k	512	15	Derivative with low power modes	Not for new design		
90CE201	16MB external ROM	16MB external RAM	24	UART, fast I^2C, 3 timers (16 bit), Watchdog timer. 68000 software compatible, EMC, QFP64	–25 to +85°C	OM4162 Microcore 4	TRACE32 – (Lauterbach)
P90CL301	16MB external ROM 256 internal	512	27	2xUART, 12C, 2xtimer (16–bit), watchdog timer (21–bit), low power modes, 2xPWM (8–bit), 4xinput ADC (8–bit), LQPF80		OM5040 Microcore 5	TRACE32 (Lauterbach)

GENERAL

TOTAL QUALITY MANAGEMENT

Philips Semiconductors is a Quality Company, renowned for the high quality of our products and service. We keep alive this tradition by constantly aiming towards one ultimate standard, that of zero defects. This aim is guided by our Total Quality Management (TQM) system, the basis of which is described in the following paragraphs.

Quality assurance

Based on ISO 9000 standards, customer standards such as Ford TQE and IBM MDQ. Our factories are certified to ISO 9000 by external inspectorates.

Partnerships with customers

PPM co-operations, design-in agreements, ship-to-stock, just-in-time and self-qualification programmes, and application support.

Partnerships with suppliers

Ship-to-stock, statistical process control and ISO 9000 audits.

Quality improvement programme

Continuous process and system improvement, design improvement, complete use of statistical process control, realization of our final objective of zero defects, and logistics improvement by ship-to-stock and just-in-time agreements.

ADVANCED QUALITY PLANNING

During the design and development of new products and processes, quality is built-in by advanced quality planning. Through failure-mode-and-effect analysis the critical parameters are detected and measures taken to ensure good performance on these parameters. The capability of process steps is also planned in this phase.

PRODUCT CONFORMANCE

The assurance of product conformance is an integral part of our quality assurance (QA) practice. This is achieved by:

- Incoming material management through partnerships with suppliers.
- In-line quality assurance to monitor process reproducibility during manufacture and initiate any necessary corrective action. Critical process steps are 100% under statistical process control.
- Acceptance tests on finished products to verify conformance with the device specification. The test results are used for quality feedback and corrective actions. The inspection and test requirements are detailed in the general quality specifications.
- Periodic inspections to monitor and measure the conformance of products.

PRODUCT RELIABILITY

With the increasing complexity of Original Equipment Manufacturer (OEM) equipment, component reliability must be extremely high. Our research laboratories and development departments study the failure mechanisms of semiconductors. Their studies result in design rules and process optimization for the highest built-in product reliability. Highly accelerated tests are applied to the products reliability evaluation. Rejects from reliability tests and from customer complaints are submitted to failure analysis, to result in corrective action.

CUSTOMER RESPONSES

Our quality improvement depends on joint action with our customer. We need our customer's inputs and we invite constructive comments on all aspects of our performance. Please contact our local sales representative.

RECOGNITION

The high quality of our products and services is demonstrated by many Quality Awards granted by major customers and international organizations.

BASIC TYPE NUMBER

This type designation code applies to semiconductor monolithic, semiconductor multi-chip, thin film, thick film and hybrid integrated circuits. The basic type number comprises three letters followed by a serial number.

First and second letters

DIGITAL FAMILY CIRCUITS

The first two letters identify the family.(1)

SOLITARY CIRCUITS

The first letter divides solitary circuits into:

S Solitary digital circuits

T Analog circuits

U Mixed analog/digital circuits.

The second letter is a serial letter without any further significance except 'H' which stands for hybrid circuits.(2)

MICROPROCESSORS

The first two letters identify microprocessors and related circuits:

MA Microcomputer or central processing unit

MB Slice processor (functional slice of microprocessor)

MD Related memories

ME Other related circuits such as interfaces, clocks, peripheral controllers, etc.

CHARGE-TRANSFER DEVICES AND SWITCHED CAPACITORS

The first two letters identify:

NH Hybrid circuits

NL Logic circuits

NM Memories

NS Analog signal processing using switched capacitors

NT Analog signal processing using charge-transfer devices

NX Imaging devices

NY Other related circuits.

(1) A logic family is an assembly of digital circuits designed to be interconnected and defined by its base electrical characteristics, such as supply voltage, power consumption, propagation delay, noise immunity.

(2) The first letter 'S' should be used for all solitary memories, to which, in the event of hybrids, the second letter 'H' should be added, for example, SH for bubble memories.

Third letter

The third letter indicates the operating ambient temperature range:

A temperature range not specified below

B 0 to +70 °C

C −55 to +125 °C

D −25 to +70 °C

E −25 to +85 °C

F −40 to +85 °C

G −55 to +85 °C.

If a device has another temperature range, the letter 'A' or a letter indicating a narrower temperature may be used, for example, the range of 0 to +75 °C can be indicated by 'A' or 'B'. Should two devices with the same basic type number both have temperature ranges other than those specified, one would use the letter 'A' and the other the letter 'X'.

SERIAL NUMBER

This may be a four-digit number assigned by Pro Electron, or the serial number (which may be a combination of figures and letters) of an existing company type designation of the manufacturer.

VERSION LETTER

A single version letter may be added to the basic type number. This indicates a minor variant of the basic type or the package. The version letter has no fixed meaning except for 'Z' which means customized wiring. The following letters are recommended for package variants:

C Cylindrical

D Ceramic dual in-line (CERDIL, CERDIP)

F Flat pack (two leads)

G Flat pack (four leads)

H Quad flat pack (QFP)

L Chip on tape (foil)

P Plastic dual in-line (DIL)

Q Quad in-line (QUIL)

T Mini pack (SOL, SO, VSO)

U Uncased chip.

TWO-LETTER SUFFIX

A two-letter suffix may be used instead of a single package version letter to give more information. To avoid confusion with serial numbers that end with a letter, a hyphen should precede the suffix.

First letter (general shape)

C Cylindrical

D Dual in-line (DIL)

E Power DIL (with external heatsink)

F Flat pack (leads on two sides)

G Flat pack (leads on four sides)

H Quad flat pack (QFP)

K Diamond (TO-3 family)

M Multiple in-line (except dual, triple and quad)

Q Quad in-line (QUIL)

R Power QUIL (with external heatsink)

S Single in-line (SIL)

T Triple in-line

W Leaded chip carrier (LCC)

X Leadless chip carrier (LLCC)

Y Pin grid array (PGA).

Second letter (material)

C Metal-ceramic

G Glass-ceramic

M Metal

P Plastic.

EXAMPLES

PCF1105WP: digital IC; PC family; operating temperature range −40 to +85 °C; serial number 1105; plastic leaded chip carrier.

GMB74LS00A-DC: digital IC; GM family; operating temperature range 0 to +70 °C; company number 74LS00A; ceramic DIL package.

TDA1000P: analog IC; operating temperature range non-standard; serial number 1000; plastic DIL package.

SAC2000: solitary digital circuit; operating temperature range −55 to +125 °C; serial number 2000.

RATING SYSTEMS

The rating systems described are those recommended by the IEC in its publication number 134.

Definitions of terms used

ELECTRONIC DEVICE

An electronic tube or valve, transistor or other semiconductor device. This definition excludes inductors, capacitors, resistors and similar components.

CHARACTERISTIC

A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

BOGEY ELECTRONIC DEVICE

An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics that are directly related to the application.

RATING

A value that establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms. Limiting conditions may be either maxima or minima.

RATING SYSTEM

The set of principles upon which ratings are established and which determine their interpretation. The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

Absolute maximum rating system

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type, as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout the life of the device, no absolute maximum value for the intended service is exceeded with any device, under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

Design maximum rating system

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout the life of the device, no design maximum value for the intended service is exceeded with a bogey electronic device, under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

Design centre rating system

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

ELECTROSTATIC CHARGES

Electrostatic charges can exist in many things; for example, man-made-fibre clothing, moving machinery, objects with air blowing across them, plastic storage bins, sheets of paper stored in plastic envelopes, paper from electrostatic copying machines, and people. The charges are caused by friction between two surfaces, at least one of which is non-conductive. The magnitude and polarity of the charges depend on the different affinities for electrons of the two materials rubbing together, the friction force and the humidity of the surrounding air.

Electrostatic discharge is the transfer of an electrostatic charge between bodies at different potentials and occurs with direct contact or when induced by an electrostatic field. All of our MOS devices are internally protected against electrostatic discharge but they **can** be damaged if the following precautions are not taken.

WORK STATION

Figure 1 shows a working area suitable for safely handling electrostatic sensitive devices. It has a work bench, the surface of which is conductive or covered by an antistatic sheet. Typical resistivity for the bench surface is between 1 and 500 kΩ per cm^2. The floor should also be covered with antistatic material. The following precautions should be observed:

- Persons at a work bench should be earthed via a wrist strap and a resistor.
- All mains-powered electrical equipment should be connected via an earth leakage switch.
- Equipment cases should be earthed.
- Relative humidity should be maintained between 50 and 65%.
- An ionizer should be used to neutralize objects with immobile static charges.

RECEIPT AND STORAGE

MOS devices are packed for dispatch in antistatic/conductive containers, usually boxes, tubes or blister tape. The fact that the contents are sensitive to electrostatic discharge is shown by warning labels on both primary and secondary packing.

The devices should be kept in their original packing whilst in storage. If a bulk container is partially unpacked, the unpacking should be performed at a protected work station. Any MOS devices that are stored temporarily should be packed in conductive or antistatic packing or carriers.

ASSEMBLY

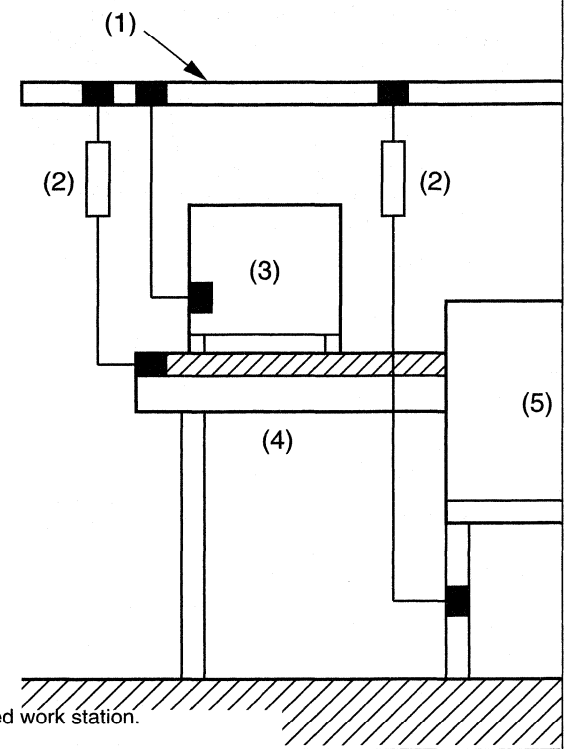
MOS devices must be removed from their protective packing with earthed component pincers or short-circuit clips. Short-circuit clips must remain in place during mounting, soldering and cleansing/drying processes. Do not remove more devices from the storage packing than are needed at any one time. Production/assembly documents should state that the product contains electrostatic sensitive devices and that special precautions need to be taken.

During assembly, ensure that the MOS devices are the last of the components to be mounted and that this is done at a protected work station.

All tools used during assembly, including soldering tools and solder baths, must be earthed. All hand tools should be of conductive or antistatic material and, where possible, should not be insulated.

Measuring and testing of completed circuit boards must be done at a protected work station. Place the soldered side of the circuit board on conductive or antistatic foam and remove the short-circuit clips. Remove the circuit board from the foam, holding the board only at the edges. Make sure the circuit board does not touch the conductive surface of the work bench. After testing, replace the circuit board on the conductive foam to await packing.

Assembled circuit boards containing MOS devices should be handled in the same way as unmounted MOS devices. They should also carry warning labels and be packed in conductive or antistatic packing.



(1) Earthing rail.
(2) Resistor (500 kΩ ± 10%, 0.5 W).
(3) Ionizer.
(4) Work bench.
(5) Chair.
(6) Wrist strap.
(7) Electrical equipment.
(8) Conductive surface/antistatic sheet.
(9) Antistatic floor.

Fig.1 Protected work station.

I²C SPECIFIC INFORMATION

APPLICATION NOTES

The following abstracts are of the application notes that can be found printed in-full in Philips Semiconductor's Data Handbook IC20 *80C51-based 8-bit microcontrollers*, ordering code 9397 750 00963.

AN422 - Using the 8XC751 microcontroller as an I²C-bus master

The 83C751/87C751 combines the benefits of a high-performance microcontroller with on-board hardware supporting the I²C-bus interface, and thus allows systems to be completely software defined. This article shows how best to connect the microcontroller to an I²C-bus configuration, describes the 8XC751 I²C hardware and gives a programming example demonstrating a bus-master code.

AN425 - Interfacing the PCF8584 I²C-bus controller to 80C51 family microcontrollers

This application note describes how to use the PCF8584 I²C-bus controller with the 80C51 family of microcontrollers. A typical way of connecting the PCF8584 to an 80C31 is given, and some basic software routines are described showing how to transmit and receive bytes in a single master system. There is also an example of how to use these routines in an application that uses the I²C circuits on an I²C demonstration board.

AN95068 - C routines for the PCF8584

This application note demonstrates how to write a driver in C for the Philips PCF8584 I²C-bus controller IC and includes a set of application interface routines to quickly implement a complete PC multimaster system application.

The driver supports polled or interrupt driver message handling, slave message transfers and multimaster system applications. Furthermore, it is suitable for use in conjunction with real-time operating systems like OS-9 or pSOS+.

AN430 - Using the 8XC751/752 in multimaster I²C applications

This article discusses the most important technical features of the I²C-bus and describes the special I²C hardware interface of the 8XC751/752. The author gives an example of how the microcontroller can be programmed for a multimaster environment along with details of the software interface for the communications routes.

AN433 - I²C slave routines for the 83C751

The 8XC751 microcontroller can be programmed as an I²C-bus master, slave, or both. This article focuses on its use as a slave and gives a programming example demonstrating the communications routes of the 8XC751 as a slave on the I²C-bus. This example complements the program given in article AN422.

AN434 - Connecting a PC keyboard to the I²C-bus

This application note illustrates the use of the 8XC751 microcontroller to interface a standard PC/AT keyboard to the I²C bus. The application software example easily fits within the 2K-bytes code and 64-bytes data memory provided on the 8XC751.

AN438 - I²C routines for 8XC528

This article presents a set of software routines to drive the I²C interface in 8XC528-type microcontrollers.
A description of the I²C interface is given along with examples of how to use these routines in PL/M-51, C and assembly source code.

AN444 - Using the P82B715 I²C extender on long cables

The P82B715 I²C buffer was designed to extend the range of the logical I²C-bus out to 50 m. This application note describes the results of testing the buffer on several different types of cables to determine the maximum operating distance possible. The results are summarized in a table for easy reference.

ETV/AN89004 - PLM51 I²C software interface IIC51 (version 0.5)

This document is a user manual for the I²C software module IIC51, and is intended for Intel PLM51 users who need to control an I²C-bus. There is a general description on the IIC51 software module, although some basic knowledge about I²C and Intel PLM51 is assumed.

EIE/AN91007 - I²C driver routines for 8XC751/1 microcontrollers

This report described the I²C drivers that are written for the 8XC751/2 and explains the structure of the software and

how to use the routines. The software is written around a set of basic routines and a message handler. The message handles contain no specific 8XC751 code so, by rewriting a set of basic routines, the software example can easily be modified for any other bit level I²C interface.

Programming the I²C interface

This article is taken from Dr. Dobb's Journal and gives a good overview of I²C-bus basics. It describes hardware requirements, building a framework and how to connect to the I²C-bus.

The following application note is printed separately. The full version can be ordered from Philips Semiconductors.

AN94078 - P90CL301 I²C driver routines

This application note demonstrates how to write an I²C-bus driver for the Philips P90CL301 microcontroller and includes a set of application interface software routines to quickly implement a complete I²C multimaster system application.

The driver allows you to link modules to your application software and includes a head-file into the application source programs. A programming example on how to use the driver is also listed in the article.

The driver supports polled or interrupt driven message handling, slave message transfer and multimaster system applications. Furthermore, it is suitable for use in conjunction with real-time operating systems such as pSOS+.

AN97055 - Bi-directional level shifter for I²C-bus and other systems

Present technologies for integrated circuits with clearances of 0.5 µm and less limit the maximum supply voltage and consequently the logic levels for the digital I/O signals. To interface these lower voltage circuits with existing 5 V devices, a level shifter is needed. For bi-directional bus systems like the I²C-bus, such a level shifter must also be bi-directional, without the need of a direction control signal. The simplest way to solve this problem is by connecting a discrete MOS-FET to each bus line.

This application note gives a description of such a level shifter and explains how, by using this method, it is possible to connect two section of an I²C-bus system, with each section having a different supply voltage and different logic level.

The I²C-bus from theory to practice

This 300-page book covers the I²C-bus history, protocol, applications and development tools, and is intended both for engineering students and professional electronics engineers. The book, and its accompanying software disk, may be ordered directly from the publisher, John Wiley & Son Ltd UK, telephone number +44 (0) 1243 770216, ISDN: 0471962686.

The I²C-bus specification

CONTENTS

The I²C-bus specification

1 PREFACE

1.1 Version 1.0 - 1992

This version of the 1992 I²C-bus specification includes the following modifications:

- Programming of a slave address by software has been omitted. The realization of this feature is rather complicated and has not been used.
- The "low-speed mode" has been omitted. This mode is, in fact, a subset of the total I²C-bus specification and need not be specified explicitly.
- The Fast-mode is added. This allows a fourfold increase of the bit rate up to 400 kbit/s. Fast-mode devices are downwards compatible i.e. they can be used in a 0 to 100 kbit/s I²C-bus system.
- 10-bit addressing is added. This allows 1024 additional slave addresses.
- Slope control and input filtering for Fast-mode devices is specified to improve the EMC behaviour.

NOTE: Neither the 100 kbit/s I²C-bus system nor the 100 kbit/s devices have been changed.

1.2 Version 2.0 - 1998

The I²C-bus has become a de facto world standard that is now implemented in over 1000 different ICs and licensed to more than 50 companies. Many of today's applications, however, require higher bus speeds and lower supply voltages. This updated version of the I²C-bus specification meets those requirements and includes the following modifications:

- The High-speed mode (Hs-mode) is added. This allows an increase in the bit rate up to 3.4 Mbit/s. Hs-mode devices can be mixed with Fast- and Standard-mode devices on the one I²C-bus system with bit rates from 0 to 3.4 Mbit/s.
- The low output level and hysteresis of devices with a supply voltage of 2 V and below has been adapted to meet the required noise margins and to remain compatible with higher supply voltage devices.
- The 0.6 V at 6 mA requirement for the output stages of Fast-mode devices has been omitted.
- The fixed input levels for new devices are replaced by bus voltage-related levels.
- Application information for bi-directional level shifter is added.

1.3 Purchase of Philips I²C-bus components

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips.

2 THE I²C-BUS BENEFITS DESIGNERS AND MANUFACTURERS

In consumer electronics, telecommunications and industrial electronics, there are often many similarities between seemingly unrelated designs. For example, nearly every system includes:

- Some intelligent control, usually a single-chip microcontroller
- General-purpose circuits like LCD drivers, remote I/O ports, RAM, EEPROM, or data converters
- Application-oriented circuits such as digital tuning and signal processing circuits for radio and video systems, or DTMF generators for telephones with tone dialling.

To exploit these similarities to the benefit of both systems designers and equipment manufacturers, as well as to maximize hardware efficiency and circuit simplicity, Philips developed a simple bi-directional 2-wire bus for efficient inter-IC control. This bus is called the Inter IC or I²C-bus. At present, Philips' IC range includes more than 150 CMOS and bipolar I²C-bus compatible types for performing functions in all three of the previously mentioned categories. All I²C-bus compatible devices incorporate an on-chip interface which allows them to communicate directly with each other via the I²C-bus. This design concept solves the many interfacing problems encountered when designing digital control circuits.

Here are some of the features of the I²C-bus:

- Only two bus lines are required; a serial data line (SDA) and a serial clock line (SCL)
- Each device connected to the bus is software addressable by a unique address and simple master/slave relationships exist at all times; masters can operate as master-transmitters or as master-receivers
- It's a true multi-master bus including collision detection and arbitration to prevent data corruption if two or more masters simultaneously initiate data transfer
- Serial, 8-bit oriented, bi-directional data transfers can be made at up to 100 kbit/s in the Standard-mode, up to 400 kbit/s in the Fast-mode, or up to 3.4 Mbit/s in the High-speed mode
- On-chip filtering rejects spikes on the bus data line to preserve data integrity
- The number of ICs that can be connected to the same bus is limited only by a maximum bus capacitance of 400 pF.

Figure 1 shows two examples of I²C-bus applications.

2.1 Designer benefits

I²C-bus compatible ICs allow a system design to rapidly progress directly from a functional block diagram to a prototype. Moreover, since they 'clip' directly onto the I²C-bus without any additional external interfacing, they allow a prototype system to be modified or upgraded simply by 'clipping' or 'unclipping' ICs to or from the bus.

Here are some of the features of I²C-bus compatible ICs which are particularly attractive to designers:

- Functional blocks on the block diagram correspond with the actual ICs; designs proceed rapidly from block diagram to final schematic.
- No need to design bus interfaces because the I²C-bus interface is already integrated on-chip.
- Integrated addressing and data-transfer protocol allow systems to be completely software-defined
- The same IC types can often be used in many different applications
- Design-time reduces as designers quickly become familiar with the frequently used functional blocks represented by I²C-bus compatible ICs
- ICs can be added to or removed from a system without affecting any other circuits on the bus
- Fault diagnosis and debugging are simple; malfunctions can be immediately traced
- Software development time can be reduced by assembling a library of reusable software modules.

In addition to these advantages, the CMOS ICs in the I²C-bus compatible range offer designers special features which are particularly attractive for portable equipment and battery-backed systems.

They all have:

- Extremely low current consumption
- High noise immunity
- Wide supply voltage range
- Wide operating temperature range.

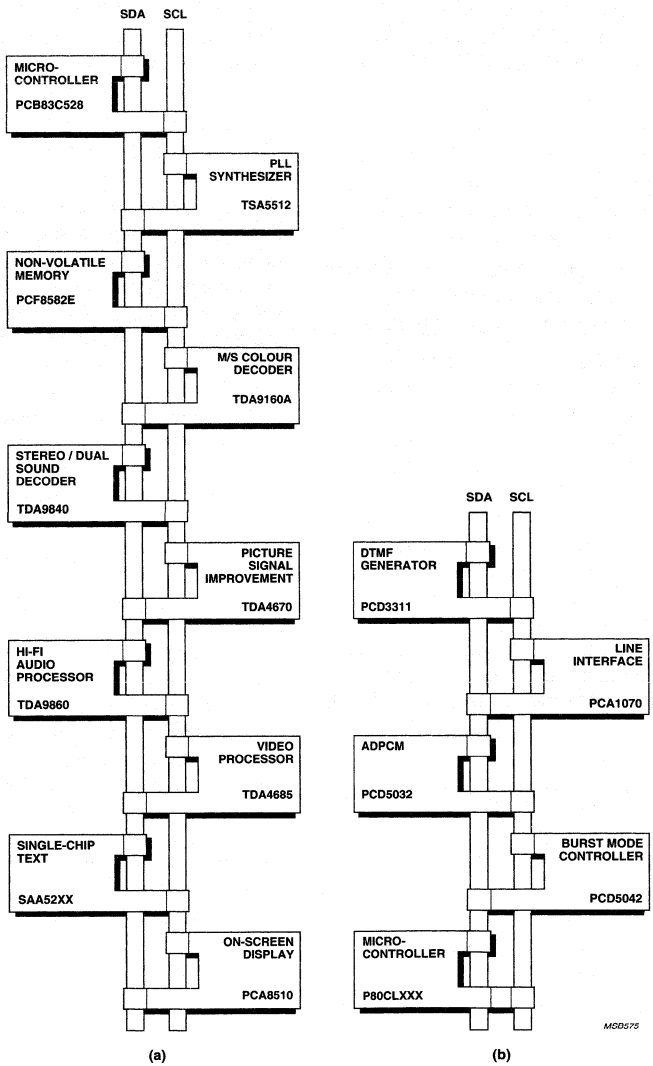


Fig.1 Two examples of I²C-bus applications: (a) a high performance highly-integrated TV set (b) DECT cordless phone base-station.

2.2 Manufacturer benefits

I²C-bus compatible ICs don't only assist designers, they also give a wide range of benefits to equipment manufacturers because:

- The simple 2-wire serial I²C-bus minimizes interconnections so ICs have fewer pins and there are not so many PCB tracks; result - smaller and less expensive PCBs
- The completely integrated I²C-bus protocol eliminates the need for address decoders and other 'glue logic'
- The multi-master capability of the I²C-bus allows rapid testing and alignment of end-user equipment via external connections to an assembly-line
- The availability of I²C-bus compatible ICs in SO (small outline), VSO (very small outline) as well as DIL packages reduces space requirements even more.

These are just some of the benefits. In addition, I²C-bus compatible ICs increase system design flexibility by allowing simple construction of equipment variants and easy upgrading to keep designs up-to-date. In this way, an entire family of equipment can be developed around a basic model. Upgrades for new equipment, or enhanced-feature models (i.e. extended memory, remote control, etc.) can then be produced simply by clipping the appropriate ICs onto the bus. If a larger ROM is needed, it's simply a matter of selecting a micro-controller with a larger ROM from our comprehensive range. As new ICs supersede older ones, it's easy to add new features to equipment or to increase its performance by simply unclipping the outdated IC from the bus and clipping on its successor.

3 INTRODUCTION TO THE I²C-BUS SPECIFICATION

For 8-bit oriented digital control applications, such as those requiring microcontrollers, certain design criteria can be established:

- A complete system usually consists of at least one microcontroller and other peripheral devices such as memories and I/O expanders
- The cost of connecting the various devices within the system must be minimized
- A system that performs a control function doesn't require high-speed data transfer
- Overall efficiency depends on the devices chosen and the nature of the interconnecting bus structure.

To produce a system to satisfy these criteria, a serial bus structure is needed. Although serial buses don't have the throughput capability of parallel buses, they do require less wiring and fewer IC connecting pins. However, a bus is not merely an interconnecting wire, it embodies all the formats and procedures for communication within the system.

Devices communicating with each other on a serial bus must have some form of protocol which avoids all possibilities of confusion, data loss and blockage of information. Fast devices must be able to communicate with slow devices. The system must not be dependent on the devices connected to it, otherwise modifications or improvements would be impossible. A procedure has also to be devised to decide which device will be in control of the bus and when. And, if different devices with different clock speeds are connected to the bus, the bus clock source must be defined. All these criteria are involved in the specification of the I²C-bus.

4 THE I²C-BUS CONCEPT

The I²C-bus supports any IC fabrication process (NMOS, CMOS, bipolar). Two wires, serial data (SDA) and serial clock (SCL), carry information between the devices connected to the bus. Each device is recognized by a unique address (whether it's a microcontroller, LCD driver, memory or keyboard interface) and can operate as either a transmitter or receiver, depending on the function of the device. Obviously an LCD driver is only a receiver, whereas a memory can both receive and transmit data. In addition to transmitters and receivers, devices can also be considered as masters or slaves when performing data transfers (see Table 1). A master is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a slave.

The I²C-bus specification

Table 1 Definition of I²C-bus terminology

TERM	DESCRIPTION
Transmitter	The device which sends data to the bus
Receiver	The device which receives data from the bus
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Slave	The device addressed by a master
Multi-master	More than one master can attempt to control the bus at the same time without corrupting the message
Arbitration	Procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the winning message is not corrupted
Synchronization	Procedure to synchronize the clock signals of two or more devices

The I²C-bus is a multi-master bus. This means that more than one device capable of controlling the bus can be connected to it. As masters are usually micro-controllers, let's consider the case of a data transfer between two microcontrollers connected to the I²C-bus (see Fig.2).

This highlights the master-slave and receiver-transmitter relationships to be found on the I²C-bus. It should be noted that these relationships are not permanent, but only depend on the direction of data transfer at that time. The transfer of data would proceed as follows:

1) Suppose microcontroller A wants to send information to microcontroller B:

- microcontroller A (master), addresses microcontroller B (slave)
- microcontroller A (master-transmitter), sends data to microcontroller B (slave- receiver)
- microcontroller A terminates the transfer

2) If microcontroller A wants to receive information from microcontroller B:

- microcontroller A (master) addresses microcontroller B (slave)
- microcontroller A (master- receiver) receives data from microcontroller B (slave- transmitter)
- microcontroller A terminates the transfer.

Even in this case, the master (microcontroller A) generates the timing and terminates the transfer.

The possibility of connecting more than one microcontroller to the I²C-bus means that more than one master could try to initiate a data transfer at the same time. To avoid the chaos that might ensue from such an event - an arbitration procedure has been developed. This procedure relies on the wired-AND connection of all I²C interfaces to the I²C-bus.

If two or more masters try to put information onto the bus, the first to produce a 'one' when the other produces a 'zero' will lose the arbitration. The clock signals during arbitration are a synchronized combination of the clocks generated by the masters using the wired-AND connection to the SCL line (for more detailed information concerning arbitration see Section 8).

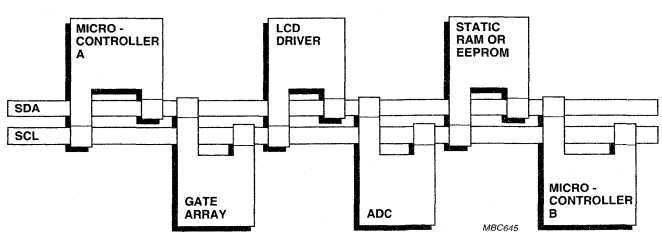


Fig.2 Example of an I²C-bus configuration using two microcontrollers.

Generation of clock signals on the I²C-bus is always the responsibility of master devices; each master generates its own clock signals when transferring data on the bus. Bus clock signals from a master can only be altered when they are stretched by a slow-slave device holding-down the clock line, or by another master when arbitration occurs.

5 GENERAL CHARACTERISTICS

Both SDA and SCL are bi-directional lines, connected to a positive supply voltage via a current-source or pull-up resistor (see Fig.3). When the bus is free, both lines are HIGH. The output stages of devices connected to the bus must have an open-drain or open-collector to perform the wired-AND function. Data on the I²C-bus can be transferred at rates of up to 100 kbit/s in the Standard-mode, up to 400 kbit/s in the Fast-mode, or up to 3.4 Mbit/s in the High-speed mode. The number of interfaces connected to the bus is solely dependent on the bus capacitance limit of 400 pF. For information on High-speed mode master devices, see Section 13.

6 BIT TRANSFER

Due to the variety of different technology devices (CMOS, NMOS, bipolar) which can be connected to the I²C-bus, the levels of the logical '0' (LOW) and '1' (HIGH) are not fixed and depend on the associated level of V_{DD} (see Section 15 for electrical specifications). One clock pulse is generated for each data bit transferred.

6.1 Data validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW (see Fig.4).

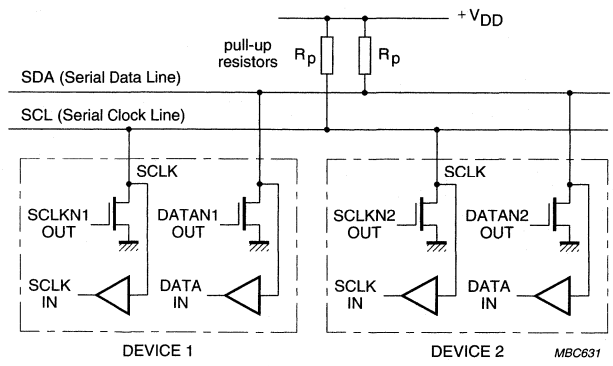


Fig.3 Connection of Standard- and Fast-mode devices to the I²C-bus.

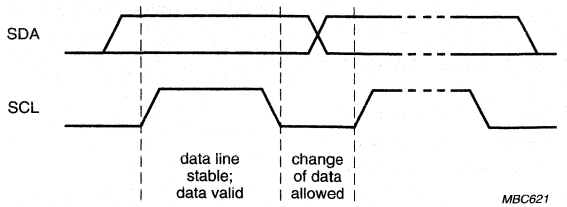


Fig.4 Bit transfer on the I²C-bus.

6.2 START and STOP conditions

Within the procedure of the I²C-bus, unique situations arise which are defined as START (S) and STOP (P) conditions (see Fig.5).

A HIGH to LOW transition on the SDA line while SCL is HIGH is one such unique case. This situation indicates a START condition.

A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition.

START and STOP conditions are always generated by the master. The bus is considered to be busy after the START condition. The bus is considered to be free again a certain time after the STOP condition. This bus free situation is specified in Section 15.

The bus stays busy if a repeated START (Sr) is generated instead of a STOP condition. In this respect, the START (S) and repeated START (Sr) conditions are functionally identical (see Fig. 10). For the remainder of this document, therefore, the S symbol will be used as a generic term to represent both the START and repeated START conditions, unless Sr is particularly relevant.

Detection of START and STOP conditions by devices connected to the bus is easy if they incorporate the necessary interfacing hardware. However, microcontrollers with no such interface have to sample the SDA line at least twice per clock period to sense the transition.

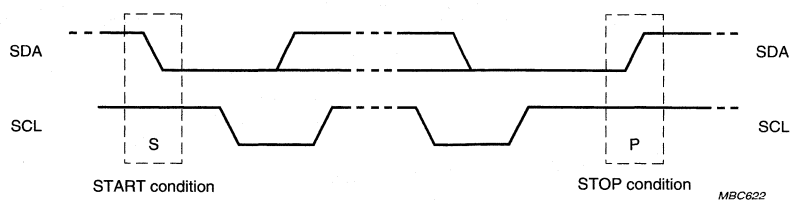


Fig.5 START and STOP conditions.

7 TRANSFERRING DATA

7.1 Byte format

Every byte put on the SDA line must be 8-bits long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first (see Fig.6) . If a slave can't receive or transmit another complete byte of data until it has performed some other function, for example servicing an interna! interrupt, it can hold the clock line SCL LOW to force the master into a wait state. Data transfer then continues when the slave is ready for another byte of data and releases clock line SCL.

In some cases, it's permitted to use a different format from the I²C-bus format (for CBUS compatible devices for example). A message which starts with such an address can be terminated by generation of a STOP condition, even during the transmission of a byte. In this case, no acknowledge is generated (see Section 10.1.3).

7.2 Acknowledge

Data transfer with acknowledge is obligatory. The acknowledge-related clock pulse is generated by the master. The transmitter releases the SDA line (HIGH) during the acknowledge clock pulse.

The receiver must pull down the SDA line during the acknowledge clock pulse so that it remains stable LOW during the HIGH period of this clock pulse (see Fig.7) . Of course, set-up and hold times (specified in Section 15) must also be taken into account.

Usually, a receiver which has been addressed is obliged to generate an acknowledge after each byte has been received, except when the message starts with a CBUS address (see Section 10.1.3).

When a slave doesn't acknowledge the slave address (for example, it's unable to receive or transmit because it's performing some real-time function), the data line must be left HIGH by the slave. The master can then generate either a STOP condition to abort the transfer, or a repeated START condition to start a new transfer.

If a slave-receiver does acknowledge the slave address but, some time later in the transfer cannot receive any more data bytes, the master must again abort the transfer. This is indicated by the slave generating the not-acknowledge on the first byte to follow. The slave leaves the data line HIGH and the master generates a STOP or a repeated START condition.

If a master-receiver is involved in a transfer, it must signal the end of data to the slave- transmitter by not generating an acknowledge on the last byte that was clocked out of the slave. The slave-transmitter must release the data line to allow the master to generate a STOP or repeated START condition.

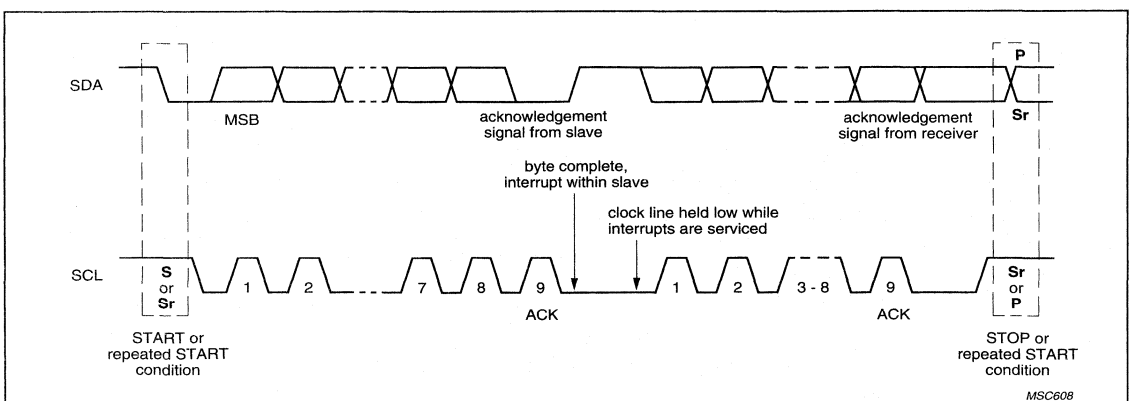


Fig.6 Data transfer on the I²C-bus.

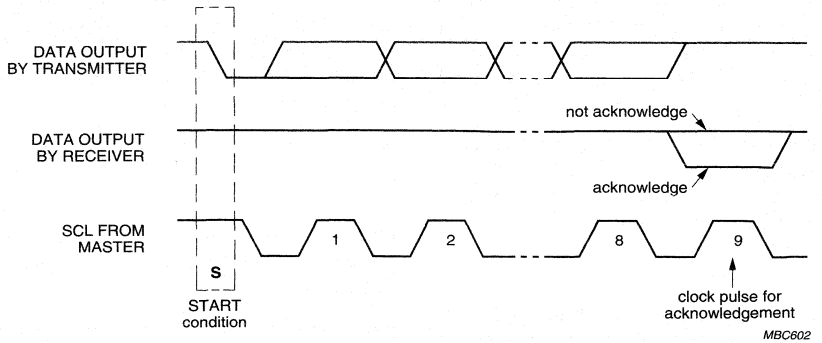


Fig.7 Acknowledge on the I²C-bus.

8 ARBITRATION AND CLOCK GENERATION

8.1 Synchronization

All masters generate their own clock on the SCL line to transfer messages on the I²C-bus. Data is only valid during the HIGH period of the clock. A defined clock is therefore needed for the bit-by-bit arbitration procedure to take place.

Clock synchronization is performed using the wired-AND connection of I²C interfaces to the SCL line. This means that a HIGH to LOW transition on the SCL line will cause the devices concerned to start counting off their LOW period and, once a device clock has gone LOW, it will hold the SCL line in that state until the clock HIGH state is reached (see Fig.8). However, the LOW to HIGH transition of this clock may not change the state of the SCL line if another clock is still within its LOW period. The SCL line will therefore be held LOW by the device with the longest LOW period. Devices with shorter LOW periods enter a HIGH wait-state during this time.

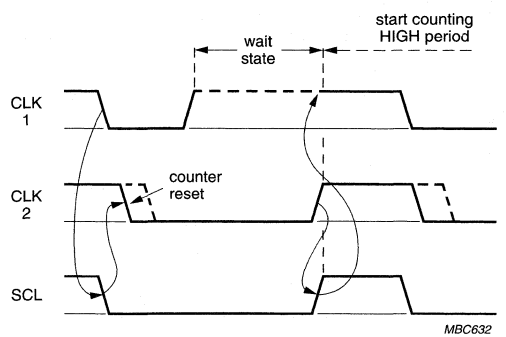


Fig.8 Clock synchronization during the arbitration procedure.

When all devices concerned have counted off their LOW period, the clock line will be released and go HIGH. There will then be no difference between the device clocks and the state of the SCL line, and all the devices will start counting their HIGH periods. The first device to complete its HIGH period will again pull the SCL line LOW.

In this way, a synchronized SCL clock is generated with its LOW period determined by the device with the longest clock LOW period, and its HIGH period determined by the one with the shortest clock HIGH period.

8.2 Arbitration

A master may start a transfer only if the bus is free. Two or more masters may generate a START condition within the minimum hold time ($t_{HD;STA}$) of the START condition which results in a defined START condition to the bus.

Arbitration takes place on the SDA line, while the SCL line is at the HIGH level, in such a way that the master which transmits a HIGH level, while another master is transmitting a LOW level will switch off its DATA output stage because the level on the bus doesn't correspond to its own level.

Arbitration can continue for many bits. Its first stage is comparison of the address bits (addressing information is given in Sections 10 and 14). If the masters are each trying to address the same device, arbitration continues with comparison of the data-bits if they are master-transmitter, or acknowledge-bits if they are master-receiver. Because address and data information on the I²C-bus is determined by the winning master, no information is lost during the arbitration process.

A master that loses the arbitration can generate clock pulses until the end of the byte in which it loses the arbitration.

As an Hs-mode master has a unique 8-bit master code, it will always finish the arbitration during the first byte (see Section 13).

If a master also incorporates a slave function and it loses arbitration during the addressing stage, it's possible that the winning master is trying to address it. The losing master must therefore switch over immediately to its slave mode.

Figure 9 shows the arbitration procedure for two masters. Of course, more may be involved (depending on how many masters are connected to the bus). The moment there is a difference between the internal data level of the master generating DATA 1 and the actual level on the SDA line, its data output is switched off, which means that a HIGH output level is then connected to the bus. This will not affect the data transfer initiated by the winning master.

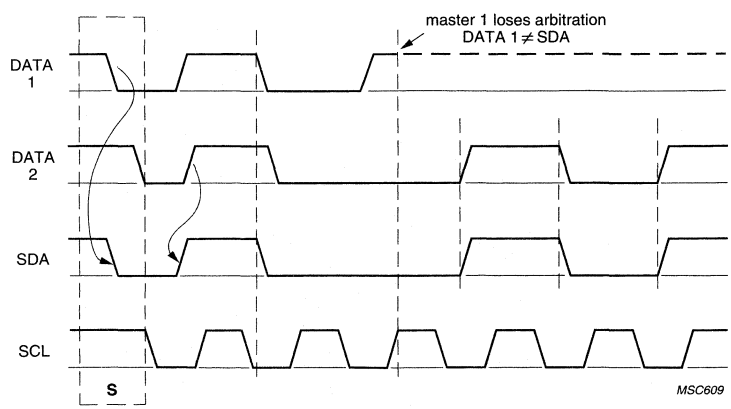


Fig.9 Arbitration procedure of two masters.

Since control of the I²C-bus is decided solely on the address or master code and data sent by competing masters, there is no central master, nor any order of priority on the bus.

Special attention must be paid if, during a serial transfer, the arbitration procedure is still in progress at the moment when a repeated START condition or a STOP condition is transmitted to the I²C-bus. If it's possible for such a situation to occur, the masters involved must send this repeated START condition or STOP condition at the same position in the format frame. In other words, arbitration isn't allowed between:

- A repeated START condition and a data bit
- A STOP condition and a data bit
- A repeated START condition and a STOP condition.

Slaves are not involved in the arbitration procedure.

8.3 Use of the clock synchronizing mechanism as a handshake

In addition to being used during the arbitration procedure, the clock synchronization mechanism can be used to enable receivers to cope with fast data transfers, on either a byte level or a bit level.

On the byte level, a device may be able to receive bytes of data at a fast rate, but needs more time to store a received byte or prepare another byte to be transmitted. Slaves can then hold the SCL line LOW after reception and acknowledgment of a byte to force the master into a wait state until the slave is ready for the next byte transfer in a type of handshake procedure (see Fig.6).

On the bit level, a device such as a microcontroller with or without limited hardware for the I²C-bus, can slow down the bus clock by extending each clock LOW period. The speed of any master is thereby adapted to the internal operating rate of this device.

In Hs-mode, this handshake feature can only be used on byte level (see Section 13).

9 FORMATS WITH 7-BIT ADDRESSES

Data transfers follow the format shown in Fig.10. After the START condition (S), a slave address is sent. This address is 7 bits long followed by an eighth bit which is a data direction bit (R/$\overline{W}$) - a 'zero' indicates a transmission (WRITE), a 'one' indicates a request for data (READ). A data transfer is always terminated by a STOP condition (P) generated by the master. However, if a master still wishes to communicate on the bus, it can generate a repeated START condition (Sr) and address another slave without first generating a STOP condition. Various combinations of read/write formats are then possible within such a transfer.

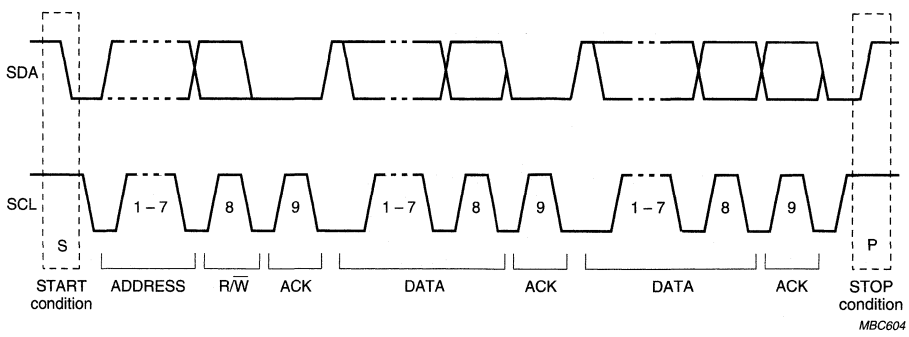


Fig.10 A complete data transfer.

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Possible data transfer formats are:

- Master-transmitter transmits to slave-receiver. The transfer direction is not changed (see Fig.11).
- Master reads slave immediately after first byte (see Fig.12). At the moment of the first acknowledge, the master- transmitter becomes a master- receiver and the slave-receiver becomes a slave-transmitter. This first acknowledge is still generated by the slave. The STOP condition is generated by the master, which has previously sent a not-acknowledge ($\overline{A}$).
- Combined format (see Fig.13). During a change of direction within a transfer, the START condition and the slave address are both repeated, but with the R/$\overline{W}$ bit reversed. If a master receiver sends a repeated START condition, it has previously sent a not-acknowledge ($\overline{A}$).

NOTES:

1. Combined formats can be used, for example, to control a serial memory. During the first data byte, the internal memory location has to be written. After the START condition and slave address is repeated, data can be transferred.
2. All decisions on auto-increment or decrement of previously accessed memory locations etc. are taken by the designer of the device.
3. Each byte is followed by an acknowledgment bit as indicated by the A or $\overline{A}$ blocks in the sequence.
4. I²C-bus compatible devices must reset their bus logic on receipt of a START or repeated START condition such that they all anticipate the sending of a slave address, even if these START conditions are not positioned according to the proper format.
5. A START condition immediately followed by a STOP condition (void message) is an illegal format.

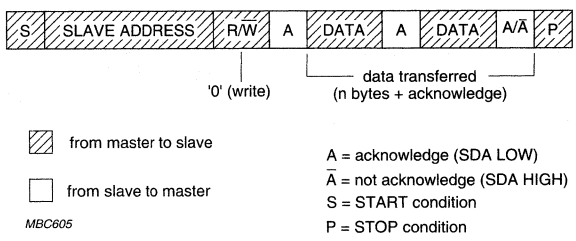


Fig.11 A master-transmitter addressing a slave receiver with a 7-bit address. The transfer direction is not changed.

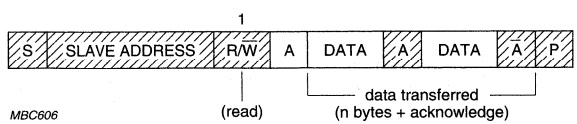


Fig.12 A master reads a slave immediately after the first byte.

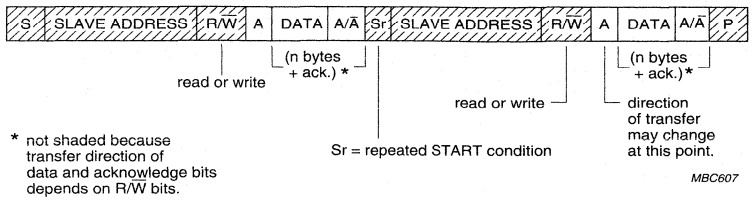


Fig.13 Combined format.

10 7-BIT ADDRESSING

The addressing procedure for the I²C-bus is such that the first byte after the START condition usually determines which slave will be selected by the master. The exception is the 'general call' address which can address all devices. When this address is used, all devices should, in theory, respond with an acknowledge. However, devices can be made to ignore this address. The second byte of the general call address then defines the action to be taken. This procedure is explained in more detail in Section 10.1.1. For information on 10-bit addressing, see Section 14

10.1 Definition of bits in the first byte

The first seven bits of the first byte make up the slave address (see Fig.14). The eighth bit is the LSB (least significant bit). It determines the direction of the message. A 'zero' in the least significant position of the first byte means that the master will write information to a selected slave. A 'one' in this position means that the master will read information from the slave.

When an address is sent, each device in a system compares the first seven bits after the START condition with its address. If they match, the device considers itself addressed by the master as a slave-receiver or slave-transmitter, depending on the R/W bit.

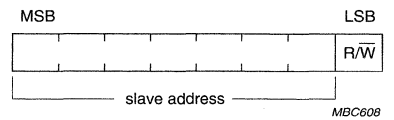


Fig.14 The first byte after the START procedure.

A slave address can be made-up of a fixed and a programmable part. Since it's likely that there will be several identical devices in a system, the programmable part of the slave address enables the maximum possible number of such devices to be connected to the I²C-bus. The number of programmable address bits of a device depends on the number of pins available. For example, if a device has 4 fixed and 3 programmable address bits, a total of 8 identical devices can be connected to the same bus.

The I²C-bus committee coordinates allocation of I²C addresses. Further information can be obtained from the Philips representatives listed on the back cover. Two groups of eight addresses (0000XXX and 1111XXX) are reserved for the purposes shown in Table 2. The bit combination 11110XX of the slave address is reserved for 10-bit addressing (see Section 14).

Table 2 Definition of bits in the first byte

SLAVE ADDRESS	R/$\overline{W}$ BIT	DESCRIPTION
0000 000	0	General call address
0000 000	1	START byte(1)
0000 001	X	CBUS address(2)
0000 010	X	Reserved for different bus format(3)
0000 011	X	Reserved for future purposes
0000 1XX	X	Hs-mode master code
1111 1XX	X	Reserved for future purposes
1111 0XX	X	10-bit slave addressing

Notes

1. No device is allowed to acknowledge at the reception of the START byte.
2. The CBUS address has been reserved to enable the inter-mixing of CBUS compatible and I²C-bus compatible devices in the same system. I²C-bus compatible devices are not allowed to respond on reception of this address.
3. The address reserved for a different bus format is included to enable I²C and other protocols to be mixed. Only I²C-bus compatible devices that can work with such formats and protocols are allowed to respond to this address.

10.1.1 General call address

The general call address is for addressing every device connected to the I²C-bus. However, if a device doesn't need any of the data supplied within the general call structure, it can ignore this address by not issuing an acknowledgment. If a device does require data from a general call address, it will acknowledge this address and behave as a slave- receiver. The second and following bytes will be acknowledged by every slave- receiver capable of handling this data. A slave which cannot process one of these bytes must ignore it by not-acknowledging. The meaning of the general call address is always specified in the second byte (see Fig.15).

There are two cases to consider:

- When the least significant bit B is a 'zero'.
- When the least significant bit B is a 'one'.

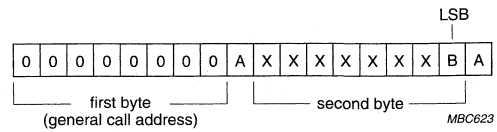


Fig.15 General call address format.

When bit B is a 'zero'; the second byte has the following definition:

- 00000110 (H'06'). Reset and write programmable part of slave address by hardware. On receiving this 2-byte sequence, all devices designed to respond to the general call address will reset and take in the programmable part of their address. Pre-cautions have to be taken to ensure that a device is not pulling down the SDA or SCL line after applying the supply voltage, since these low levels would block the bus.
- 00000100 (H'04'). Write programmable part of slave address by hardware. All devices which define the programmable part of their address by hardware (and which respond to the general call address) will latch this programmable part at the reception of this two byte sequence. The device will not reset.
- 00000000 (H'00'). This code is not allowed to be used as the second byte.

Sequences of programming procedure are published in the appropriate device data sheets.

The remaining codes have not been fixed and devices must ignore them.

When bit B is a 'one'; the 2-byte sequence is a 'hardware general call'. This means that the sequence is transmitted by a hardware master device, such as a keyboard scanner, which cannot be programmed to transmit a desired slave address. Since a hardware master doesn't know in advance to which device the message has to be transferred, it can only generate this hardware general call and its own address - identifying itself to the system (see Fig.16).

The seven bits remaining in the second byte contain the address of the hardware master. This address is recognized by an intelligent device (e.g. a microcontroller) connected to the bus which will then direct the information from the hardware master. If the hardware master can also act as a slave, the slave address is identical to the master address.

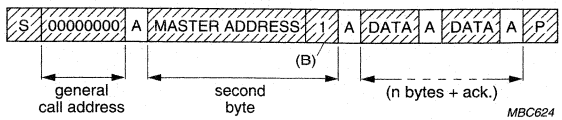


Fig.16 Data transfer from a hardware master-transmitter.

In some systems, an alternative could be that the hardware master transmitter is set in the slave-receiver mode after the system reset. In this way, a system configuring master can tell the hardware master-transmitter (which is now in slave-receiver mode) to which address data must be sent (see Fig.17). After this programming procedure, the hardware master remains in the master-transmitter mode.

10.1.2 START BYTE

Microcontrollers can be connected to the I²C-bus in two ways. A microcontroller with an on-chip hardware I²C-bus interface can be programmed to be only interrupted by requests from the bus. When the device doesn't have such an interface, it must constantly monitor the bus via software. Obviously, the more times the microcontroller monitors, or polls the bus, the less time it can spend carrying out its intended function.

There is therefore a speed difference between fast hardware devices and a relatively slow microcontroller which relies on software polling.

In this case, data transfer can be preceded by a start procedure which is much longer than normal (see Fig.18). The start procedure consists of:

- A START condition (S)
- A START byte (00000001)
- An acknowledge clock pulse (ACK)
- A repeated START condition (Sr).

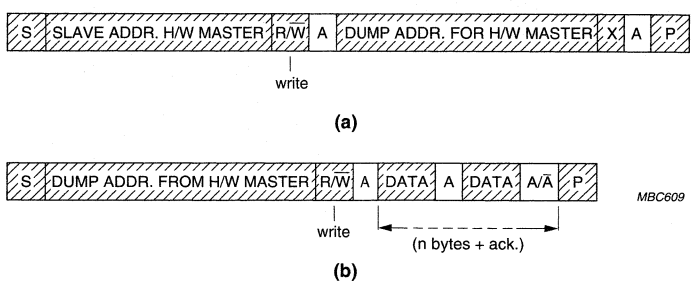


Fig.17 Data transfer by a hardware-transmitter capable of dumping data directly to slave devices.
(a) Configuring master sends dump address to hardware master
(b) Hardware master dumps data to selected slave.

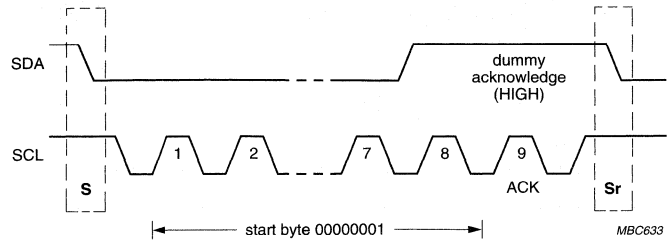


Fig.18 START byte procedure.

After the START condition S has been transmitted by a master which requires bus access, the START byte (00000001) is transmitted. Another microcontroller can therefore sample the SDA line at a low sampling rate until one of the seven zeros in the START byte is detected. After detection of this LOW level on the SDA line, the microcontroller can switch to a higher sampling rate to find the repeated START condition Sr which is then used for synchronization.

A hardware receiver will reset on receipt of the repeated START condition Sr and will therefore ignore the START byte.

An acknowledge-related clock pulse is generated after the START byte. This is present only to conform with the byte handling format used on the bus. No device is allowed to acknowledge the START byte.

10.1.3 CBUS COMPATIBILITY

CBUS receivers can be connected to the Standard-mode I²C-bus. However, a third bus line called DLEN must then be connected and the acknowledge bit omitted. Normally, I²C transmissions are sequences of 8-bit bytes; CBUS compatible devices have different formats.

In a mixed bus structure, I²C-bus devices must not respond to the CBUS message. For this reason, a special CBUS address (0000001X) to which no I²C-bus compatible device will respond, has been reserved. After transmission of the CBUS address, the DLEN line can be made active and a CBUS-format transmission sent (see Fig.19). After the STOP condition, all devices are again ready to accept data.

Master-transmitters can send CBUS formats after sending the CBUS address. The transmission is ended by a STOP condition, recognized by all devices.

NOTE: If the CBUS configuration is known, and expansion with CBUS compatible devices isn't foreseen, the designer is allowed to adapt the hold time to the specific requirements of the device(s) used.

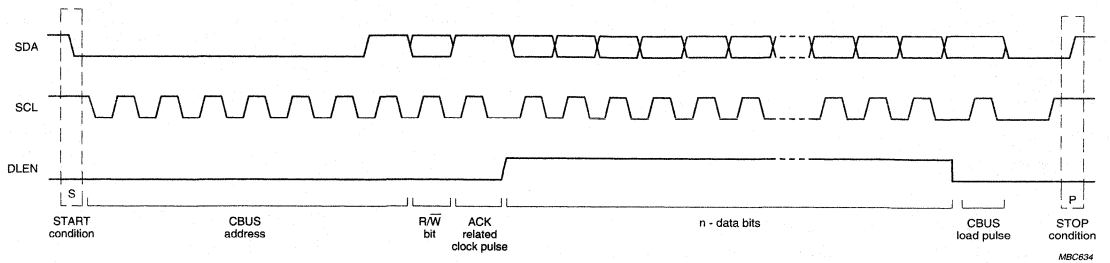


Fig.19 Data format of transmissions with CBUS transmitter/receiver.

11 EXTENSIONS TO THE STANDARD-MODE I²C-BUS SPECIFICATION

The Standard-mode I²C-bus specification, with its data transfer rate of up to 100 kbit/s and 7-bit addressing, has been in existence since the beginning of the 1980's. This concept rapidly grew in popularity and is today accepted worldwide as a de facto standard with several hundred different compatible ICs on offer from Philips Semiconductors and other suppliers. To meet the demands for higher speeds, as well as make available more slave address for the growing number of new devices, the Standard-mode I²C-bus specification was upgraded over the years and today is available with the following extensions:

- **Fast-mode**, with a bit rate up to 400 kbit/s.
- **High-speed mode (Hs-mode)**, with a bit rate up to 3.4 Mbit/s.
- **10-bit addressing**, which allows the use of up to 1024 additional slave addresses.

There are two main reasons for extending the regular I²C-bus specification:

- Many of today's applications need to transfer large amounts of serial data and require bit rates far in excess of 100 kbit/s (Standard-mode), or even 400 kbit/s (Fast-mode). As a result of continuing improvements in semiconductor technologies, I²C-bus devices are now available with bit rates of up to 3.4 Mbit/s (Hs-mode) without any noticeable increases in the manufacturing cost of the interface circuitry.
- As most of the 112 addresses available with the 7-bit addressing scheme were soon allocated, it became apparent that more address combinations were required to prevent problems with the allocation of slave addresses for new devices. This problem was resolved with the new 10-bit addressing scheme, which allowed about a tenfold increase in available addresses.

New slave devices with a Fast- or Hs-mode I²C-bus interface can have a 7- or a 10-bit slave address. If possible, a 7-bit address is preferred as it is the cheapest hardware solution and results in the shortest message length. Devices with 7- and 10-bit addresses can be mixed in the same I²C-bus system regardless of whether it is an F/S- or Hs-mode system. Both existing and future masters can generate either 7- or 10-bit addresses.

12 FAST-MODE

With the Fast-mode I²C-bus specification, the protocol, format, logic levels and maximum capacitive load for the SDA and SCL lines quoted in the Standard-mode I²C-bus specification are unchanged. New devices with an I²C-bus interface must meet at least the minimum requirements of the Fast- or Hs-mode specification (see Section 13).

Fast-mode devices can receive and transmit at up to 400 kbit/s. The minimum requirement is that they can synchronize with a 400 kbit/s transfer; they can then prolong the LOW period of the SCL signal to slow down the transfer. Fast-mode devices are downward-compatible and can communicate with Standard-mode devices in a 0 to 100 kbit/s I²C-bus system. As Standard-mode devices, however, are not upward compatible, they should not be incorporated in a Fast-mode I²C-bus system as they cannot follow the higher transfer rate and unpredictable states would occur.

The I²C-bus specification

The Fast-mode I²C-bus specification has the following additional features compared with the Standard-mode:

- The maximum bit rate is increased to 400 kbit/s.
- Timing of the serial data (SDA) and serial clock (SCL) signals has been adapted. There is no need for compatibility with other bus systems such as CBUS because they cannot operate at the increased bit rate.
- The inputs of Fast-mode devices incorporate spike suppression and a Schmitt trigger at the SDA and SCL inputs.
- The output buffers of Fast-mode devices incorporate slope control of the falling edges of the SDA and SCL signals.
- If the power supply to a Fast-mode device is switched off, the SDA and SCL I/O pins must be floating so that they don't obstruct the bus lines.
- The external pull-up devices connected to the bus lines must be adapted to accommodate the shorter maximum permissible rise time for the Fast-mode I²C-bus. For bus loads up to 200 pF, the pull-up device for each bus line can be a resistor; for bus loads between 200 pF and 400 pF, the pull-up device can be a current source (3 mA max.) or a switched resistor circuit (see Fig.43).

13 Hs-MODE

High-speed mode (Hs-mode) devices offer a quantum leap in I²C-bus transfer speeds. Hs-mode devices can transfer information at bit rates of up to 3.4 Mbit/s, yet they remain fully downward compatible with Fast- or Standard-mode (F/S-mode) devices for bi-directional communication in a mixed-speed bus system. With the exception that arbitration and clock synchronization is not performed during the Hs-mode transfer, the same serial bus protocol and data format is maintained as with the F/S-mode system. Depending on the application, new devices may have a Fast or Hs-mode I²C-bus interface, although Hs-mode devices are preferred as they can be designed-in to a greater number of applications.

13.1 High speed transfer

To achieve a bit transfer of up to 3.4 Mbit/s the following improvements have been made to the regular I²C-bus specification:

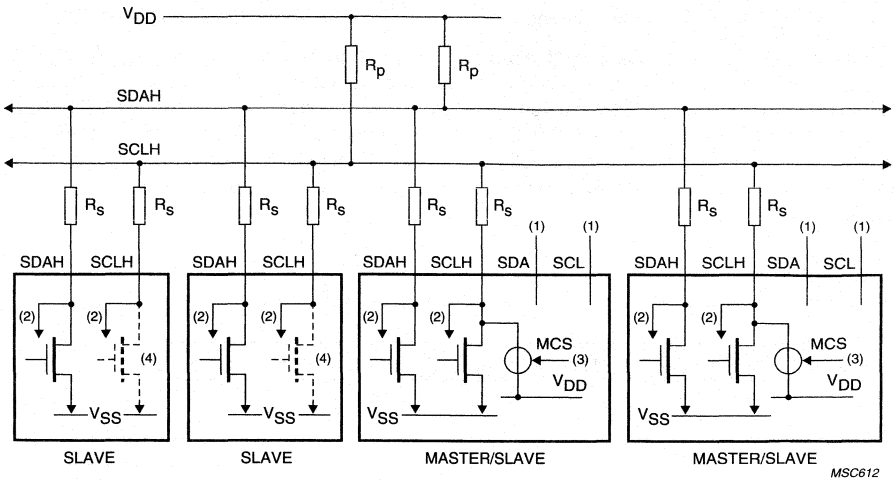
- Hs-mode master devices have an open-drain output buffer for the SDAH signal and a combination of an open-drain pull-down and current-source pull-up circuit on the SCLH output(1). This current-source circuit shortens the rise time of the SCLH signal. Only the current-source of one master is enabled at any one time, and only during Hs-mode.
- No arbitration or clock synchronization is performed during Hs-mode transfer in multi-master systems, which speeds-up bit handling capabilities. The arbitration procedure always finishes after a preceding master code transmission in F/S-mode.
- Hs-mode master devices generate a serial clock signal with a HIGH to LOW ratio of 1 to 2. This relieves the timing requirements for set-up and hold times.
- As an option, Hs-mode master devices can have a built-in bridge(1). During Hs-mode transfer, the high speed data (SDAH) and high-speed serial clock (SCLH) lines of Hs-mode devices are separated by this bridge from the SDA and SCL lines of F/S-mode devices. This reduces the capacitive load of the SDAH and SCLH lines resulting in faster rise and fall times.
- The only difference between Hs-mode slave devices and F/S-mode slave devices is the speed at which they operate. Hs-mode slaves have open-drain output buffers on the SCLH and SDAH outputs. Optional pull-down transistors on the SCLH pin can be used to stretch the LOW level of the SCLH signal, although this is only allowed after the acknowledge bit in Hs-mode transfers.
- The inputs of Hs-mode devices incorporate spike suppression and a Schmitt trigger at the SDAH and SCLH inputs.
- The output buffers of Hs-mode devices incorporate slope control of the falling edges of the SDAH and SCLH signals.

Figure 20 shows the physical I²C-bus configuration in a system with only Hs-mode devices. Pins SDA and SCL on the master devices are only used in mixed-speed bus systems and are not connected in an Hs-mode only system. In such cases, these pins can be used for other functions.

Optional series resistors R_s protect the I/O stages of the I²C-bus devices from high-voltage spikes on the bus lines and minimize ringing and interference.

Pull-up resistors R_p maintain the SDAH and SCLH lines at a HIGH level when the bus is free and ensure the signals are pulled up from a LOW to a HIGH level within the required rise time. For higher capacitive bus-line loads (>100 pF), the resistor R_p can be replaced by external current source pull-ups to meet the rise time requirements. Unless proceeded by an acknowledge bit, the rise time of the SCLH clock pulses in Hs-mode transfers is shortened by the internal current-source pull-up circuit MCS of the active master.

(1) Patent application pending.



(1) SDA and SCL are not used here but may be used for other functions.
(2) To input filter.
(3) Only the active master can enable its current-source pull-up circuit
(4) Dotted transistors are optional open-drain outputs which can stretch the serial clock signal SCLH.

Fig.20 I²C-bus configuration with Hs-mode devices only.

13.2 Serial data transfer format in Hs-mode

Serial data transfer format in Hs-mode meets the Standard-mode I²C-bus specification. Hs-mode can only commence after the following conditions (all of which are in F/S-mode):

1. START condition (S)
2. 8-bit master code (00001XXX)
3. not-acknowledge bit ($\overline{A}$)

Figures 21 and 22 show this in more detail. This master code has two main functions:

- It allows arbitration and synchronization between competing masters at F/S-mode speeds, resulting in one winning master.
- It indicates the beginning of an Hs-mode transfer.

Hs-mode master codes are reserved 8-bit codes, which are not used for slave addressing or other purposes. Furthermore, as each master has its own unique master code, up to eight Hs-mode masters can be present on the one I²C-bus system (although master code 0000 1000 should be reserved for test and diagnostic purposes). The master code for an Hs-mode master device is software programmable and is chosen by the System Designer.

Arbitration and clock synchronization only take place during the transmission of the master code and not-acknowledge bit ($\overline{A}$), after which one winning master remains active. The master code indicates to other devices that an Hs-mode transfer is to begin and the connected devices must meet the Hs-mode specification. As no device is allowed to acknowledge the master code, the master code is followed by a not-acknowledge ($\overline{A}$).

After the not-acknowledge bit ($\overline{A}$), and the SCLH line has been pulled-up to a HIGH level, the active master switches to Hs-mode and enables (at time t_H, see Fig.22) the current-source pull-up circuit for the SCLH signal. As other devices can delay the serial transfer before t_H by stretching the LOW period of the SCLH signal, the active master will enable its current-source pull-up circuit when all devices have released the SCLH line and the SCLH signal has reached a HIGH level, thus speeding up the last part of the rise time of the SCLH signal.

The active master then sends a repeated START condition (Sr) followed by a 7-bit slave address (or 10-bit slave

address, see Section 14) with a R/$\overline{W}$ bit address, and receives an acknowledge bit (A) from the selected slave.

After each acknowledge bit (A) or not-acknowledge bit ($\overline{A}$) the active master disables its current-source pull-up circuit. This enables other devices to delay the serial transfer by stretching the LOW period of the SCLH signal. The active master re-enables its current-source pull-up circuit again when all devices have released and the SCLH signal reaches a HIGH level, and so speeds up the last part of the SCLH signal's rise time.

Data transfer continues in Hs-mode after the next repeated START (Sr), and only switches back to F/S-mode after a STOP condition (P). To reduce the overhead of the master code, it's possible that a master links a number of Hs-mode transfers, separated by repeated START conditions (Sr).

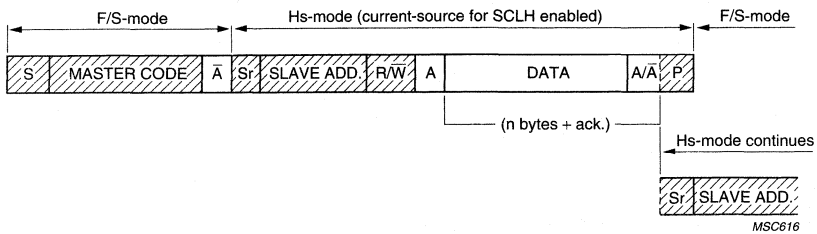


Fig.21 Data transfer format in Hs-mode.

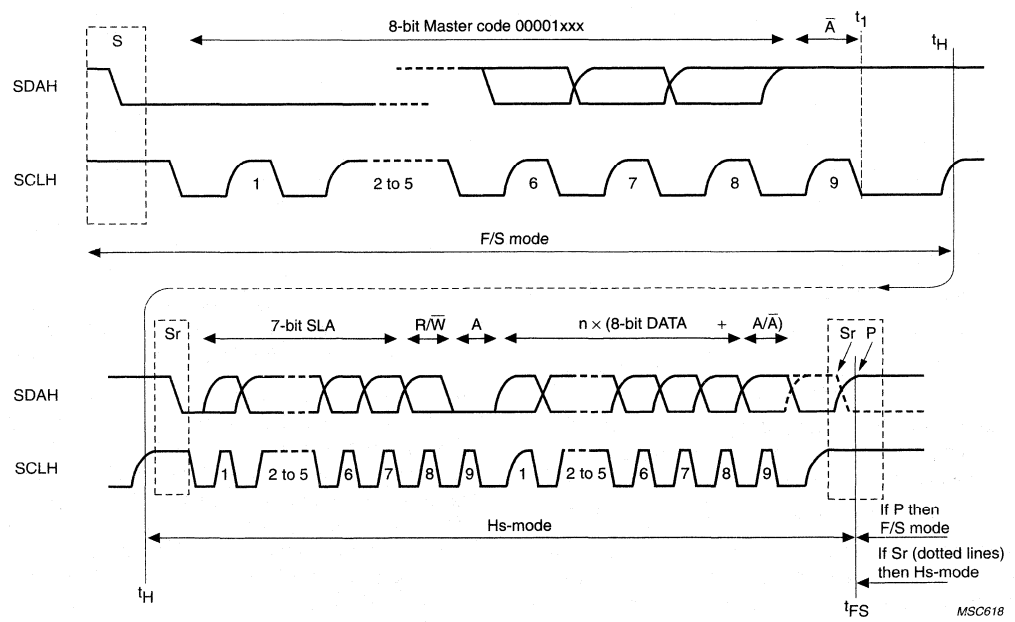


Fig.22 A complete Hs-mode transfer.

13.3 Switching from F/S- to Hs-mode and back

After reset and initialization, Hs-mode devices must be in Fast-mode (which is in effect F/S-mode as Fast-mode is downward compatible with Standard-mode). Each Hs-mode device can switch from Fast- to Hs-mode and back and is controlled by the serial transfer on the I²C-bus.

Before time t_1 in Fig.22, each connected device operates in Fast-mode. Between times t_1 and t_H (this time interval can be stretched by any device) each connected device must recognized the "S 00001XXX $\overline{A}$" sequence and has to switch its internal circuit from the Fast-mode setting to the Hs-mode setting. Between times t_1 and t_H the connected master and slave devices perform this switching by the following actions.

The active (winning) master:

1. Adapts its SDAH and SCLH input filters according to the spike suppression requirement in Hs-mode.
2. Adapts the set-up and hold times according to the Hs-mode requirements.
3. Adapts the slope control of its SDAH and SCLH output stages according to the Hs-mode requirement.
4. Switches to the Hs-mode bit-rate, which is required after time t_H.
5. Enables the current source pull-up circuit of its SCLH output stage at time t_H.

The non-active, or loosing masters:

1. Adapt their SDAH and SCLH input filters according to the spike suppression requirement in Hs-mode.
2. Wait for a STOP condition to detect when the bus is free again.

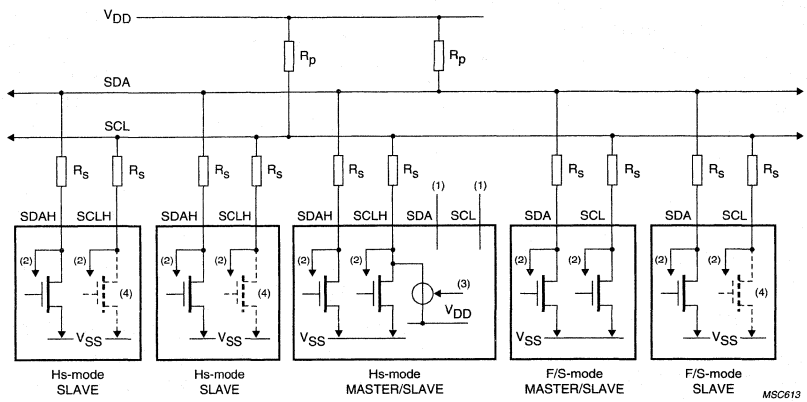
All slaves:

1. Adapt their SDAH and SCLH input filters according to the spike suppression requirement in Hs-mode.
2. Adapt the set-up and hold times according to the Hs-mode requirements. This requirement may already be fulfilled by the adaptation of the input filters.
3. Adapt the slope control of their SDAH output stages, if necessary. For slave devices, slope control is applicable for the SDAH output stage only and, depending on circuit tolerances, both the Fast- and Hs-mode requirements may be fulfilled without switching its internal circuit.

At time t_{FS} in Fig.22, each connected device must recognize the STOP condition (P) and switch its internal circuit from the Hs-mode setting back to the Fast-mode setting as present before time t_1. This must be completed within the minimum bus free time as specified in Table 5 according to the Fast-mode specification.

13.4 Hs-mode devices at lower speed modes

Hs-mode devices are fully downwards compatible, and can be connected to an F/S-mode I²C-bus system (see Fig.23). As no master code will be transmitted in such a configuration, all Hs-mode master devices stay in F/S-mode and communicate at F/S-mode speeds with their current-source disabled. The SDAH and SCLH pins are used to connect to the F/S-mode bus system, allowing the SDA and SCL pins (if present) on the Hs-mode master device to be used for other functions.



(1) Bridge not used. SDA and SCL may have an alternative function.

(2) To input filter.

(3) The current-source pull-up circuit stays disabled.

(4) Dotted transistors are optional open-drain outputs which can stretch the serial clock signal SCL.

Fig.23 Hs-mode devices at F/S-mode speed.

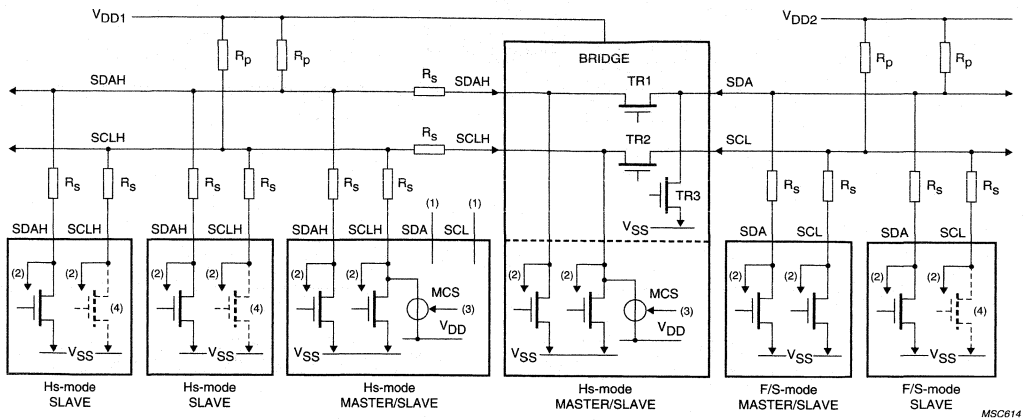
13.5 Mixed speed modes on one serial bus system

If a system has a combination of Hs-, Fast- and/or Standard-mode devices, it's possible, by using an interconnection bridge, to have different bit rates between different devices (see Figs 24 and 25).

One bridge is required to connect/disconnect an Hs-mode section to/from an F/S-mode section at the appropriate time. This bridge includes a level shift function that allows devices with different supply voltages to be connected. For example F/S-mode devices with a V_{DD2} of 5 V can be connected to Hs-mode devices with a V_{DD1} of 3 V or less (i.e. where $V_{DD2} \geq V_{DD1}$), provided SDA and SCL pins are 5 V tolerant. This bridge is incorporated in Hs-mode master devices and is completely controlled by the serial signals SDAH, SCLH, SDA and SCL. Such a bridge can be implemented in any IC as an autonomous circuit.

TR1, TR2 and TR3 are N-channel transistors. TR1 and TR2 have a transfer gate function, and TR3 is an open-drain pull-down stage. If TR1 or TR2 are switched on they transfer a LOW level in both directions, otherwise when both the drain and source rise to a HIGH level there will be a high impedance between the drain and source of each switched on transistor. In the latter case, the transistors will act as a level shifter as SDAH and SCLH will be pulled-up to V_{DD1} and SDA and SCL will be pulled-up to V_{DD2}

During F/S-mode speed, a bridge on one of the Hs-mode masters connects the SDAH and SCLH lines to the corresponding SDA and SCL lines thus permitting Hs-mode devices to communicate with F/S-mode devices at slower speeds. Arbitration and synchronization is possible during the total F/S-mode transfer between all connected devices as described in Section 8. During Hs-mode transfer, however, the bridge opens to separate the two bus sections and allows Hs-mode devices to communicate with each other at 3.4 Mbit/s. Arbitration between Hs-mode devices and F/S-mode devices is only performed during the master code (00001XXX), and normally won by one Hs-mode master as no slave address has four leading zeros. Other masters can win the arbitration only if they send a reserved 8-bit code (00000XXX). In such cases, the bridge remains closed and the transfer proceeds in F/S-mode. Table 3 gives the possible communication speeds in such a system.



(1) Bridge not used. SDA and SCL may have an alternative function.

(2) To input filter.

(3) Only the active master can enable its current-source pull-up circuit.

(4) Dotted transistors are optional open-drain outputs which can stretch the serial clock signal SCL or SCLH.

Fig.24 Bus system with transfer at Hs- and F/S-mode speeds.

Table 3 Communication bit-rates in a mixed speed bus system

TRANSFER BETWEEN	SERIAL BUS SYSTEM CONFIGURATION			
	Hs + FAST + STANDARD	Hs + FAST	Hs + STANDARD	FAST + STANDARD
Hs <–> Hs	0 to 3.4 Mbit/s	0 to 3.4 Mbit/s	0 to 3.4 Mbit/s	–
Hs <–> Fast	0 to 100 kbit/s	0 to 400 kbit/s	–	–
Hs <–> Standard	0 to 100 kbit/s	–	0 to 100 kbit/s	–
Fast <–> Standard	0 to 100 kbit/s	–	–	0 to 100 kbit/s
Fast <–> Fast	0 to 100 kbit/s	0 to 400 kbit/s	–	0 to 100 kbit/s
Standard <–> Standard	0 to 100 kbit/s	–	0 to 100 kbit/s	0 to 100 kbit/s

13.5.1 F/S-MODE TRANSFER IN A MIXED-SPEED BUS SYSTEM

The bridge shown in Fig.24 interconnects corresponding serial bus lines, forming one serial bus system. As no master code (00001XXX) is transmitted, the current-source pull-up circuits stay disabled and all output stages are open-drain. All devices, including Hs-mode devices, communicate with each other according the protocol, format and speed of the F/S-mode I²C-bus specification.

13.5.2 HS-MODE TRANSFER IN A MIXED-SPEED BUS SYSTEM

Figure 25 shows the timing diagram of a complete Hs-mode transfer, which is invoked by a START condition, a master code, and a not-acknowledge $\overline{A}$ (at F/S-mode speed). Although this timing diagram is split in two parts, it should be viewed as one timing diagram were time point t_H is a common point for both parts.

The I²C-bus specification

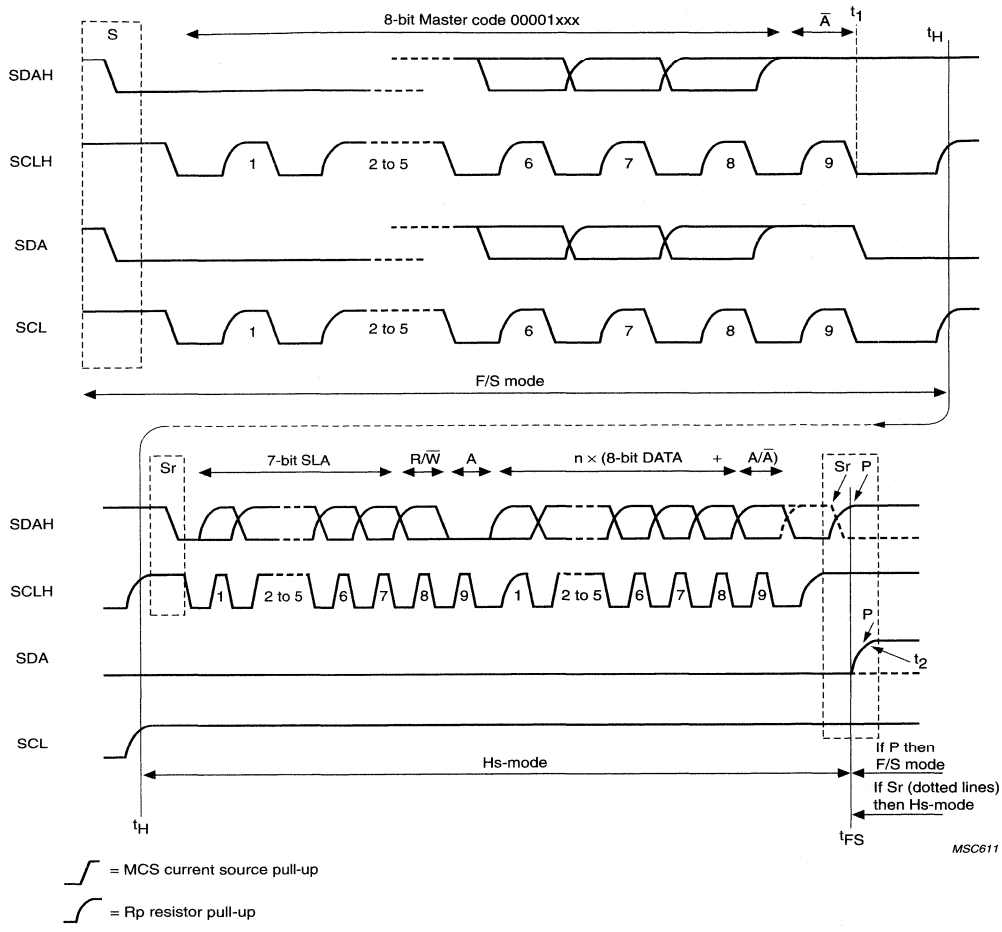


Fig.25 A complete Hs-mode transfer in a mixed-speed bus system.

The master code is recognized by the bridge in the active or non-active master (see Fig.24). The bridge performs the following actions:

1. Between t_1 and t_H (see Fig.25), transistor TR1 opens to separate the SDAH and SDA lines, after which transistor TR3 closes to pull-down the SDA line to V_{SS}.
2. When both SCLH and SCL become HIGH (t_H in Fig.25), transistor TR2 opens to separate the SCLH and SCL lines. TR2 must be opened before SCLH goes LOW after Sr.

Hs-mode transfer starts after t_H with a repeated START condition (Sr). During Hs-mode transfer, the SCL line stays at a HIGH and the SDA line at a LOW steady-state level, and so is prepared for the transfer of a STOP condition (P).

After each acknowledge (A) or not-acknowledge bit ($\overline{A}$) the active master disables its current-source pull-up circuit. This enables other devices to delay the serial transfer by stretching the LOW period of the SCLH signal. The active master re-enables its current-source pull-up circuit again when all devices are released and the SCLH signal reaches a HIGH level, and so speeds up the last part of the SCLH signal's rise time. In irregular situations, F/S-mode devices can close the bridge (TR1 and TR2 closed, TR3 open) at any time by pulling down the SCL line for at least 1 μs, e.g. to recover from a bus hang-up.

Hs-mode finishes with a STOP condition and brings the bus system back into the F/S-mode. The active master disables its current-source MCS when the STOP condition (P) at SDAH is detected (t_{FS} in Fig.25). The bridge also recognizes this STOP condition and takes the following actions:

1. Transistor TR2 closes after t_{FS} to connect SCLH with SCL; both of which are HIGH at this time. Transistor TR3 opens after t_{FS}, which releases the SDA line and allows it to be pulled HIGH by the pull-up resister R_p. This is the STOP condition for the F/S-mode devices. TR3 must open fast enough to ensure the bus free time between the STOP condition and the earliest next START condition is according to the Fast-mode specification (see t_{BUF} in Table 5).
2. When SDA reaches a HIGH (t_2 in Fig.25) transistor TR1 closes to connect SDAH with SDA. (Note: interconnections are made when all lines are HIGH, thus preventing spikes on the bus lines). TR1 and TR2 must be closed within the minimum bus free time according to the Fast-mode specification (see t_{BUF} in Table 5).

13.5.3 Timing requirements for the bridge in a mixed-speed bus system

It can be seen from Fig.25 that the actions of the bridge at t_1, t_H and t_{FS} must be so fast that it does not affect the SDAH and SCLH lines. Furthermore the bridge must meet the related timing requirements of the Fast-mode specification for the SDA and SCL lines.

14 10-BIT ADDRESSING

This section describes 10-bit addressing and can be disregarded if only 7-bit addressing is used.

10-bit addressing is compatible with, and can be combined with, 7-bit addressing. Using 10 bits for addressing exploits the reserved combination 1111XXX for the first seven bits of the first byte following a START (S) or repeated START (Sr) condition as explained in Section 10.1. The 10-bit addressing does not affect the existing 7-bit addressing. Devices with 7-bit and 10-bit addresses can be connected to the same I²C-bus, and both 7-bit and 10-bit addressing can be used in F/S-mode and Hs-mode systems.

Although there are eight possible combinations of the reserved address bits 1111XXX, only the four combinations 11110XX are used for 10-bit addressing. The remaining four combinations 11111XX are reserved for future I²C-bus enhancements.

14.1 Definition of bits in the first two bytes

The 10-bit slave address is formed from the first two bytes following a START condition (S) or a repeated START condition (Sr).

The first seven bits of the first byte are the combination 11110XX of which the last two bits (XX) are the two most-significant bits (MSBs) of the 10-bit address; the eighth bit of the first byte is the R/$\overline{W}$ bit that determines the direction of the message. A 'zero' in the least significant position of the first byte means that the master will write information to a selected slave. A 'one' in this position means that the master will read information from the slave.

If the R/$\overline{W}$ bit is 'zero', then the second byte contains the remaining 8 bits (XXXXXXXX) of the 10-bit address. If the R/$\overline{W}$ bit is 'one', then the next byte contains data transmitted from a slave to a master.

14.2 Formats with 10-bit addresses

Various combinations of read/write formats are possible within a transfer that includes 10-bit addressing. Possible data transfer formats are:

- Master-transmitter transmits to slave-receiver with a 10-bit slave address.
  The transfer direction is not changed (see Fig.26). When a 10-bit address follows a START condition, each slave compares the first seven bits of the first byte of the slave address (11110XX) with its own address and tests if the eighth bit (R/$\overline{W}$ direction bit) is 0. It is possible that more than one device will find a match and generate an acknowledge (A1). All slaves that found a match will compare the eight bits of the second byte of the slave address (XXXXXXXX) with their own addresses, but only one slave will find a match and generate an acknowledge (A2). The matching slave will remain addressed by the master until it receives a STOP

condition (P) or a repeated START condition (Sr) followed by a different slave address.

- Master-receiver reads slave- transmitter with a 10-bit slave address.
  The transfer direction is changed after the second R/$\overline{W}$ bit (Fig.27). Up to and including acknowledge bit A2, the procedure is the same as that described for a master-transmitter addressing a slave-receiver. After the repeated START condition (Sr), a matching slave remembers that it was addressed before. This slave then checks if the first seven bits of the first byte of the slave address following Sr are the same as they were after the START condition (S), and tests if the eighth (R/$\overline{W}$) bit is 1. If there is a match, the slave considers that it has been addressed as a transmitter and generates acknowledge A3. The slave-transmitter remains addressed until it receives a STOP condition (P) or until it receives another repeated START condition (Sr) followed by a different slave address. After a repeated START condition (Sr), all the other slave devices will also compare the first seven bits of the first byte of the slave address (11110XX) with their own addresses and test the eighth (R/$\overline{W}$) bit. However, none of them will be addressed because R/$\overline{W}$ = 1 (for 10-bit devices), or the 11110XX slave address (for 7-bit devices) does not match.
- Combined format. A master transmits data to a slave and then reads data from the same slave (Fig.28). The same master occupies the bus all the time. The transfer direction is changed after the second R/$\overline{W}$ bit.
- Combined format. A master transmits data to one slave and then transmits data to another slave (Fig.29). The same master occupies the bus all the time.
- Combined format. 10-bit and 7-bit addressing combined in one serial transfer (Fig.30). After each START condition (S), or each repeated START condition (Sr), a 10-bit or 7-bit slave address can be transmitted.
  Figure 27 shows how a master-transmits data to a slave with a 7-bit address and then transmits data to a second slave with a 10-bit address. The same master occupies the bus all the time.

NOTES:

1. Combined formats can be used, for example, to control a serial memory. During the first data byte, the internal memory location has to be written. After the START condition and slave address is repeated, data can be transferred.
2. All decisions on auto-increment or decrement of previously accessed memory locations etc. are taken by the designer of the device.
3. Each byte is followed by an acknowledgment bit as indicated by the A or blocks in the sequence.
4. I²C-bus compatible devices must reset their bus logic on receipt of a START or repeated START condition such that they all anticipate the sending of a slave address.

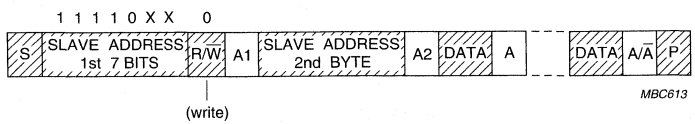


Fig.26 A master-transmitter addresses a slave-receiver with a 10-bit address.

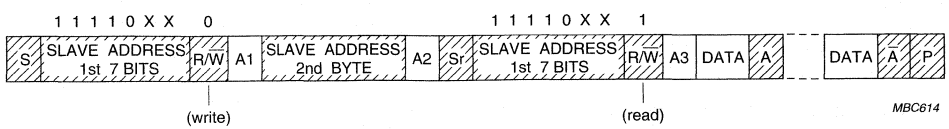


Fig.27 A master-receiver addresses a slave-transmitter with a 10-bit address.

The I²C-bus specification

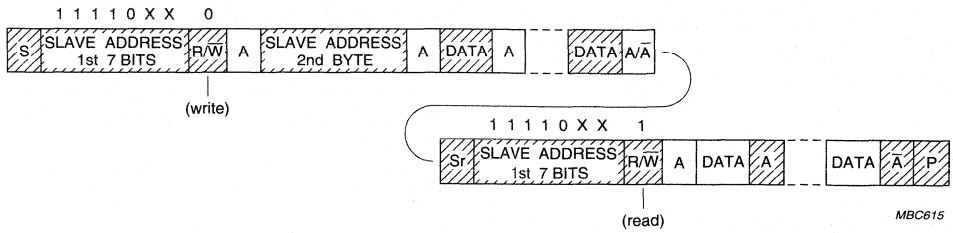


Fig.28 Combined format. A master addresses a slave with a 10-bit address, then transmits data to this slave and reads data from this slave.

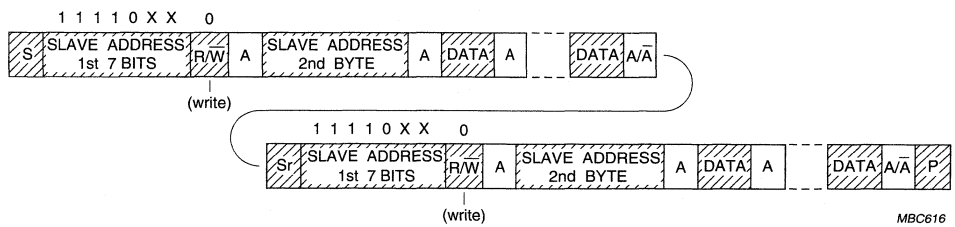


Fig.29 Combined format. A master transmits data to two slaves, both with 10-bit addresses.

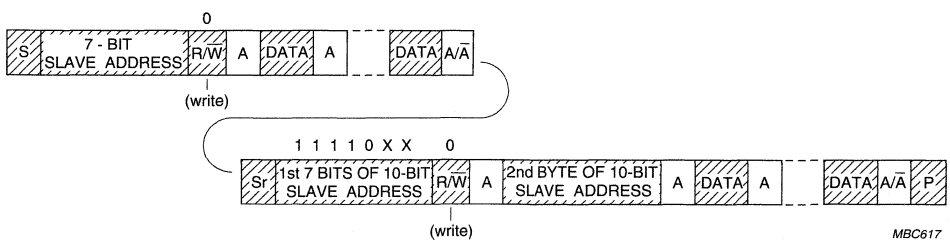


Fig.30 Combined format. A master transmits data to two slaves, one with a 7-bit address, and one with a 10-bit address.

14.3 General call address and start byte with 10-bit addressing

The 10-bit addressing procedure for the I²C-bus is such that the first two bytes after the START condition (S) usually determine which slave will be selected by the master. The exception is the "general call" address 00000000 (H'00'). Slave devices with 10-bit addressing will react to a "general call" in the same way as slave devices with 7-bit addressing (see Section 10.1.1).

Hardware masters can transmit their 10-bit address after a 'general call'. In this case, the 'general call' address byte is followed by two successive bytes containing the 10-bit address of the master-transmitter. The format is as shown in Fig.10 where the first DATA byte contains the eight least-significant bits of the master address.

The START byte 00000001 (H'01') can precede the 10-bit addressing in the same way as for 7-bit addressing (see Section 10.1.2).

15 ELECTRICAL SPECIFICATIONS AND TIMING FOR I/O STAGES AND BUS LINES

15.1 Standard- and Fast-mode devices

The I/O levels, I/O current, spike suppression, output slope control and pin capacitance for F/S-mode I²C-bus devices are given in Table 4. The I²C-bus timing characteristics, bus-line capacitance and noise margin are given in Table 5. Figure 31 shows the timing definitions for the I²C-bus.

The minimum HIGH and LOW periods of the SCL clock specified in Table 5 determine the maximum bit transfer rates of 100 kbit/s for Standard-mode devices and 400 kbit/s for Fast-mode devices. Standard-mode and Fast-mode I²C-bus devices must be able to follow transfers at their own maximum bit rates, either by being able to transmit or receive at that speed or by applying the clock synchronization procedure described in Section 8 which will force the master into a wait state and stretch the LOW period of the SCL signal. Of course, in the latter case the bit transfer rate is reduced.

Table 4 Characteristics of the SDA and SCL I/O stages for F/S-mode I²C-bus devices

PARAMETER	SYMBOL	STANDARD-MODE		FAST-MODE		UNIT
		MIN.	MAX.	MIN.	MAX.	
LOW level input voltage: fixed input levels V_{DD}-related input levels	V_{IL}	 −0.5 −0.5	 1.5 $0.3V_{DD}$	 n/a −0.5	 n/a $0.3V_{DD}$ (1)	 V V
HIGH level input voltage: fixed input levels V_{DD}-related input levels	V_{IH}	 3.0 $0.7V_{DD}$	 (2) (2)	 n/a $0.7V_{DD}$(1)	 n/a (2)	 V V
Hysteresis of Schmitt trigger inputs: V_{DD} > 2 V V_{DD} < 2 V	V_{hys}	 n/a n/a	 n/a n/a	 $0.05V_{DD}$ $0.1V_{DD}$	 – –	 V V
LOW level output voltage (open drain or open collector) at 3 mA sink current: V_{DD} > 2 V V_{DD} < 2 V	 V_{OL1} V_{OL3}	 0 n/a	 0.4 n/a	 0 0	 0.4 $0.2V_{DD}$	 V V
Output fall time from V_{IHmin} to V_{ILmax} with a bus capacitance from 10 pF to 400 pF	t_{of}	–	250(4)	$20 + 0.1C_b$(3)	250(4)	ns
Pulse width of spikes which must be suppressed by the input filter	t_{SP}	n/a	n/a	0	50	ns
Input current each I/O pin with an input voltage between $0.1V_{DD}$ and $0.9V_{DDmax}$	I_i	−10	10	−10(5)	10(5)	μA
Capacitance for each I/O pin	C_i	–	10	–	10	pF

Notes

1. Devices that use non-standard supply voltages which do not conform to the intended I²C-bus system levels must relate their input levels to the V_{DD} voltage to which the pull-up resistors R_p are connected.
2. Maximum $V_{IH} = V_{DDmax} + 0.5$ V.
3. C_b = capacitance of one bus line in pF.
4. The maximum t_f for the SDA and SCL bus lines quoted in Table 5 (300 ns) is longer than the specified maximum t_{of} for the output stages (250 ns). This allows series protection resistors (R_s) to be connected between the SDA/SCL pins and the SDA/SCL bus lines as shown in Fig.36 without exceeding the maximum specified t_f.
5. I/O pins of Fast-mode devices must not obstruct the SDA and SCL lines if V_{DD} is switched off.

n/a = not applicable

Table 5 Characteristics of the SDA and SCL bus lines for F/S-mode I²C-bus devices[1]

PARAMETER	SYMBOL	STANDARD-MODE		FAST-MODE		UNIT
		MIN.	MAX.	MIN.	MAX.	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	4.0	–	0.6	–	µs
LOW period of the SCL clock	t_{LOW}	4.7	–	1.3	–	µs
HIGH period of the SCL clock	t_{HIGH}	4.0	–	0.6	–	µs
Set-up time for a repeated START condition	$t_{SU;STA}$	4.7	–	0.6	–	µs
Data hold time: for CBUS compatible masters (see NOTE, Section 10.1.3) for I²C-bus devices	$t_{HD;DAT}$	 5.0 0[2]	 – 3.45[3]	 – 0[2]	 – 0.9[3]	 µs µs
Data set-up time	$t_{SU;DAT}$	250	–	100[4]	–	ns
Rise time of both SDA and SCL signals	t_r	–	1000	$20 + 0.1C_b$[5]	300	ns
Fall time of both SDA and SCL signals	t_f	–	300	$20 + 0.1C_b$[5]	300	ns
Set-up time for STOP condition	$t_{SU;STO}$	4.0	–	0.6	–	µs
Bus free time between a STOP and START condition	t_{BUF}	4.7	–	1.3	–	µs
Capacitive load for each bus line	C_b	–	400	–	400	pF
Noise margin at the LOW level for each connected device (including hysteresis)	V_{nL}	$0.1V_{DD}$	–	$0.1V_{DD}$	–	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{nH}	$0.2V_{DD}$	–	$0.2V_{DD}$	–	V

Notes

1. All values referred to V_{IHmin} and V_{ILmax} levels (see Table 4).
2. A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
3. The maximum $t_{HD;DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
4. A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r\,max} + t_{SU;DAT} = 1000 + 250 = 1250$ ns (according to the Standard-mode I²C-bus specification) before the SCL line is released.
5. C_b = total capacitance of one bus line in pF. If mixed with Hs-mode devices, faster fall-times according to Table 6 are allowed.

n/a = not applicable

The I²C-bus specification

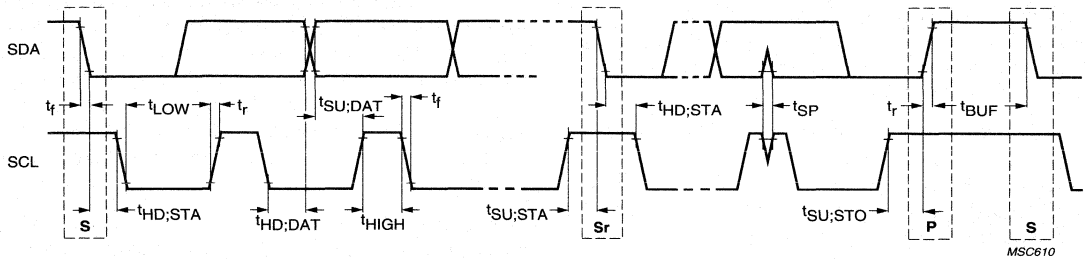


Fig.31 Definition of timing for F/S-mode devices on the I²C-bus.

15.2 Hs-mode devices

The I/O levels, I/O current, spike suppression, output slope control and pin capacitance for I²C-bus Hs-mode devices are given in Table 6. The noise margin for HIGH and LOW levels on the bus lines are the same as specified for F/S-mode I²C-bus devices.

Figure 32 shows all timing parameters for the Hs-mode timing.The "normal" START condition S does not exist in Hs-mode. Timing parameters for Address bits, R/$\overline{W}$ bit, Acknowledge bit and DATA bits are all the same. Only the rising edge of the first SCLH clock signal after an acknowledge bit has an larger value because the external R_p has to pull-up SCLH without the help of the internal current-source.

The Hs-mode timing parameters for the bus lines are specified in Table 7. The minimum HIGH and LOW periods and the maximum rise and fall times of the SCLH clock signal determine the highest bit rate.

With an internally generated SCLH signal with LOW and HIGH level periods of 200 ns and 100 ns respectively, an Hs-mode master can fulfil the timing requirements for the external SCLH clock pulses (taking the rise and fall times into account) for the maximum bit rate of 3.4 Mbit/s. So a basic frequency of 10 MHz, or a multiple of 10 MHz, can be used by an Hs-mode master to generate the SCLH signal. There are no limits for maximum HIGH and LOW periods of the SCLH clock, and there is no limit for a lowest bit rate.

Timing parameters are independent for capacitive load up to 100 pF for each bus line allowing the maximum possible bit rate of 3.4 Mbit/s. At a higher capacitive load on the bus lines, the bit rate decreases gradually. The timing parameters for a capacitive bus load of 400 pF are specified in Table 7, allowing a maximum bit rate of 1.7 Mbit/s. For capacitive bus loads between 100 pF and 400 pF, the timing parameters must be interpolated linearly. Rise and fall times are in accordance with the maximum propagation time of the transmission lines SDAH and SCLH to prevent reflections of the open ends.

Table 6 Characteristics of the SDAH, SCLH, SDA and SCL I/O stages for Hs-mode I²C-bus devices

PARAMETER	SYMBOL	Hs-MODE		UNIT
		MIN.	MAX.	
LOW level input voltage	V_{IL}	−0.5	$0.3V_{DD}$(1)	V
HIGH level input voltage	V_{IH}	$0.7V_{DD}$(1)	$V_{DD} + 0.5$(2)	V
Hysteresis of Schmitt trigger inputs	V_{hys}	$0.1V_{DD}$(1)	–	V
LOW level output voltage (open drain) at 3 mA sink current at SDAH, SDA and SCLH for: $V_{DD} > 2$ V $V_{DD} < 2$ V	V_{OL}	 0 0	 0.4 $0.2V_{DD}$	 V V
On resistance of the transfer gate, for both current directions at V_{OL} level between SDA and SDAH or SCL and SCLH at 3 mA	R_{onL}	–	50	Ω
On resistance of the transfer gate between SDA and SDAH or SCL and SCLH if both are at V_{DD} level	R_{onH}(2)	50	–	kΩ
Pull-up current of the SCLH current-source. Applies for SCLH output levels between $0.3V_{DD}$ and $0.7V_{DD}$	I_{CS}	3	12	mA
Output rise time (current-source enabled) and fall time at SCLH with a capacitive load from 10 to 100 pF	t_{rCL}, t_{fCL}	10	40	ns
Output rise time (current-source enabled) and fall time at SCLH with an external pull-up current source of 3 mA and a capacitive load of 400 pF	t_{rCL}(3), t_{fCL}(3)	20	80	ns
Output fall time at SDAH with a capacitive load from 10 to 100 pF	t_{fDA}	20	80	ns
Output fall time at SDAH with a capacitive load of 400 pF	t_{fDA}(3)	40	160	ns
Pulse width of spikes at SDAH and SCLH that must be suppressed by the input filters	t_{SP}	0	10	ns
Input current each I/O pin with an input voltage between $0.1V_{DD}$ and $0.9V_{DD}$	I_i(4)	–	10	μA
Capacitance for each I/O pin	C_i	–	10	pF

Notes

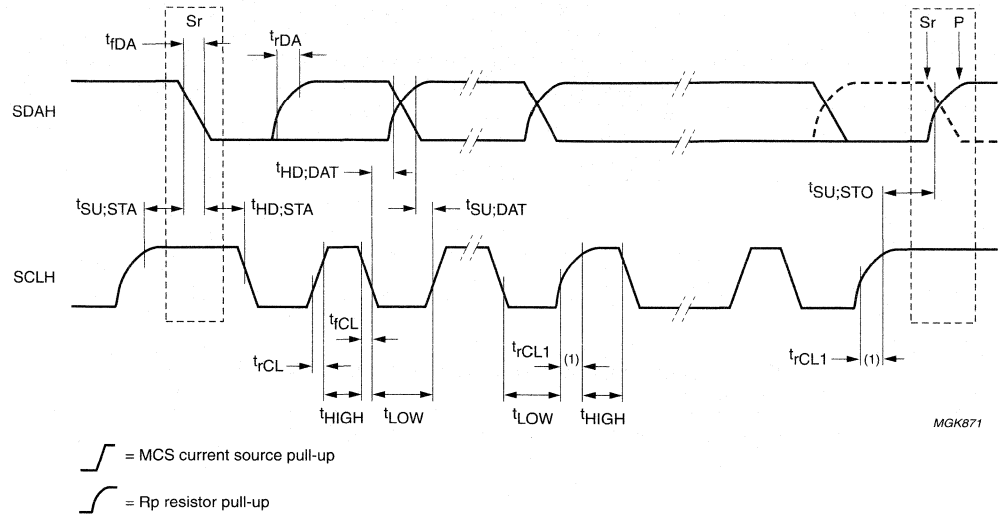
1. Devices that use non-standard supply voltages which do not conform to the intended I²C-bus system levels must relate their input levels to the V_{DD} voltage to which the pull-up resistors R_p are connected.
2. Devices that offer the level shift function must tolerate a maximum input voltage of 5.5 V at SDA and SCL.
3. For capacitive bus loads between 100 and 400 pF, the rise and fall time values must be linearly interpolated.
4. SDAH and SCLH I/O stages of Hs-mode slave devices must have floating outputs if their supply voltage has been switched off. Due to the current-source output circuit, which normally has a clipping diode to V_{DD}, this requirement is not mandatory for the SCLH or the SDAH I/O stage of Hs-mode master devices. This means that the supply voltage of Hs-mode master devices cannot be switched off without affecting the SDAH and SCLH lines.

Table 7 Characteristics of the SDAH, SCLH, SDA and SCL bus lines for Hs-mode I²C-bus devices[1]

PARAMETER	SYMBOL	C_b = 100 pF MAX.		C_b = 400 pF[2]		UNIT
		MIN.	MAX.	MIN.	MAX.	
SCLH clock frequency	f_{SCLH}	0	3.4	0	1.7	MHz
Set-up time (repeated) START condition	$t_{SU;STA}$	160	–	320	–	ns
Hold time (repeated) START condition	$t_{HD;STA}$	160	–	320	–	ns
LOW period of the SCLH clock	t_{LOW}	160	–	320	–	ns
HIGH period of the SCLH clock	t_{HIGH}	60	–	120	–	ns
Data set-up time	$t_{SU;DAT}$	10	–	10	–	ns
Data hold time	$t_{HD;DAT}$	0[3]	70	0[3]	150	ns
Rise time of SCLH signal	t_{rCL}	10	40	20	80	ns
Rise time of SCLH signal after acknowledge bit	t_{rCL1}	20	80	40	160	ns
Fall time of SCLH signal	t_{fCL}	10	40	20	80	ns
Rise time of SDAH signal	t_{rDA}	20	80	40	160	ns
Fall time of SDAH signal	t_{fDA}	20	80	40	160	ns
Set-up time for STOP condition	$t_{SU;STO}$	160	–	320	–	ns
Capacitive load for SDAH and SCLH lines	C_b[2]	–	100	–	400	pF
Capacitive load for SDAH + SDA line and SCLH + SCL line	C_b	–	400	–	400	pF
Noise margin at the LOW level for each connected device (including hysteresis)	V_{nL}	$0.1V_{DD}$	–	$0.1V_{DD}$	–	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{nH}	$0.2V_{DD}$	–	$0.2V_{DD}$	–	V

Notes

1. All values referred to V_{IHmin} and V_{ILmax} levels (see Table 6).
2. For bus line loads C_b between 100 and 400 pF the timing parameters must be linearly interpolated.
3. A device must internally provide a Data hold time to bridge the undefined part between V_{IH} and V_{IL} of the falling edge of the SCLH signal. An input circuit with a threshold as low as possible for the falling edge of the SCLH signal minimizes this hold time.



(1) Rising edge of the first SCLH clock pulse after an acknowledge bit.

Fig.32 Definition of timing for Hs-mode devices on the I²C-bus.

16 ELECTRICAL CONNECTIONS OF I²C-BUS DEVICES TO THE BUS LINES

The electrical specifications for the I/Os of I²C-bus devices and the characteristics of the bus lines connected to them are given in Section 15.

I²C-bus devices with fixed input levels of 1.5 V and 3 V can each have their own appropriate supply voltage. Pull-up resistors must be connected to a 5 V ± 10% supply (Fig.33). I²C-bus devices with input levels related to V_{DD} must have one common supply line to which the pull-up resistor is also connected (Fig.34).

When devices with fixed input levels are mixed with devices with input levels related to V_{DD}, the latter devices must be connected to one common supply line of 5 V ± 10% and must have pull-up resistors connected to their SDA and SCL pins as shown in Fig.35.

New Fast- and Hs-mode devices must have supply voltage related input levels as specified in Tables 4 and 6.

Input levels are defined in such a way that:

- The noise margin on the LOW level is $0.1V_{DD}$
- The noise margin on the HIGH level is $0.2V_{DD}$
- As shown in Fig.36, series resistors (R_S) of e.g. 300 Ω can be used for protection against high-voltage spikes on the SDA and SCL lines (resulting from the flash-over of a TV picture tube, for example).

The I²C-bus specification

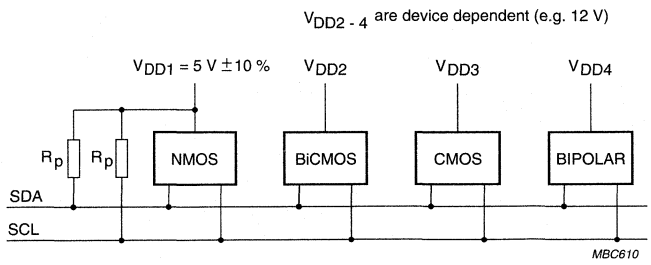


Fig.33 Fixed input level devices connected to the I²C-bus.

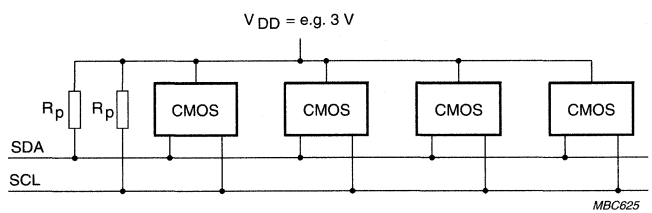


Fig.34 Devices with wide supply voltage range connected to the I²C-bus.

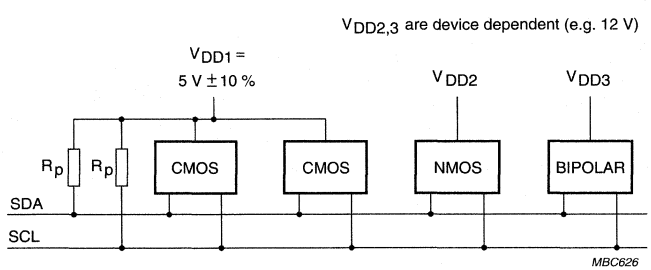


Fig.35 Devices with input levels related to V_{DD} (supply V_{DD1}) mixed with fixed input level devices (supply $V_{DD2,3}$) on the I²C-bus.

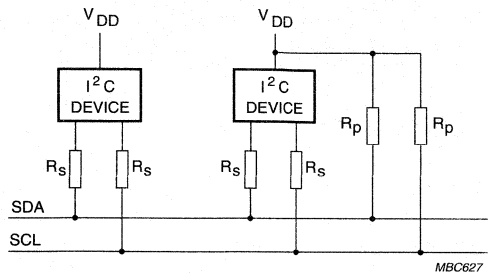


Fig.36 Series resistors (R_s) for protection against high-voltage spikes.

16.1 Maximum and minimum values of resistors R_p and R_s for Standard-mode I²C-bus devices

For Standard-mode I²C-bus systems, the values of resistors R_p and R_s in Fig.33 depend on the following parameters:

- Supply voltage
- Bus capacitance
- Number of connected devices (input current + leakage current).

The supply voltage limits the minimum value of resistor R_p due to the specified minimum sink current of 3 mA at V_{OLmax} = 0.4 V for the output stages. V_{DD} as a function of $R_{p\,min}$ is shown in Fig.37. The required noise margin of $0.1V_{DD}$ for the LOW level, limits the maximum value of R_s. $R_{s\,max}$ as a function of R_p is shown in Fig.38.

The bus capacitance is the total capacitance of wire, connections and pins. This capacitance limits the maximum value of R_p due to the specified rise time. Fig.39 shows $R_{p\,max}$ as a function of bus capacitance.

The maximum HIGH level input current of each input/output connection has a specified maximum value of 10 μA. Due to the required noise margin of 0.2 V_{DD} for the HIGH level, this input current limits the maximum value of R_p. This limit depends on V_{DD}. The total HIGH level input current is shown as a function of $R_{p\,max}$ in Fig.40.

The I²C-bus specification

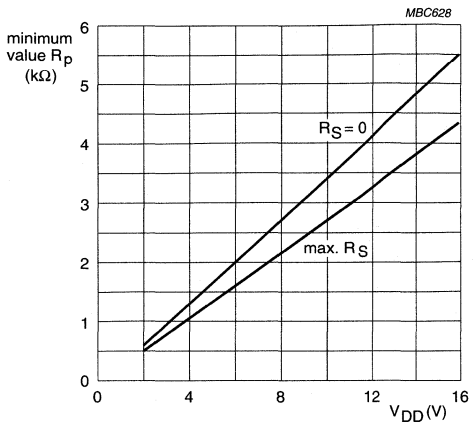


Fig.37 Minimum value of R_p as a function of supply voltage with the value os R_s as a parameter.

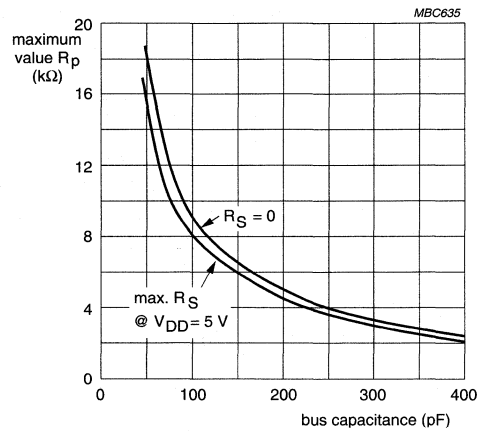


Fig.39 Maximum value of R_p as a function of bus capacitance for a Standard-mode I²C-bus.

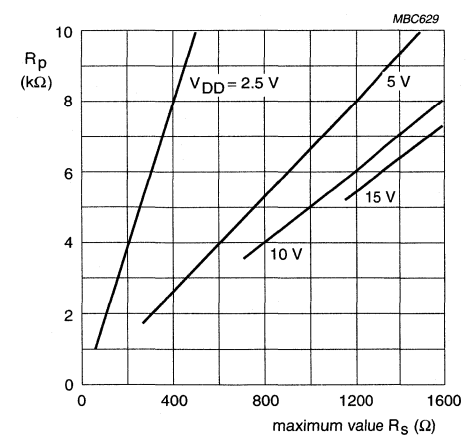


Fig.38 Maximum value of R_s as a function of the value of R_p with supply voltage as a parameter.

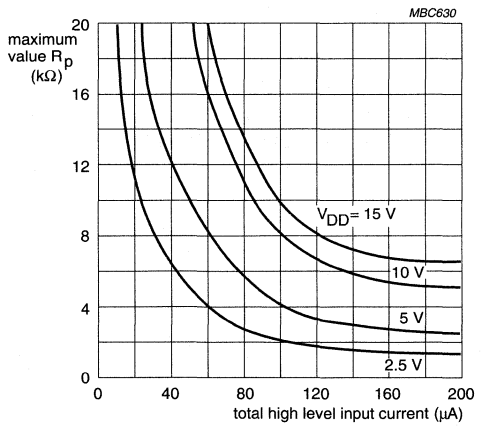


Fig.40 Total HIGH level input current as a function of the maximum value of R_p with supply voltage as a parameter.

17 APPLICATION INFORMATION

17.1 Slope-controlled output stages of Fast-mode I²C-bus devices

The electrical specifications for the I/Os of I²C-bus devices and the characteristics of the bus lines connected to them are given in Section 15.

Figures 41 and 42 show examples of output stages with slope control in CMOS and bipolar technology. The slope of the falling edge is defined by a Miller capacitor (C1) and a resistor (R1). The typical values for C1 and R1 are indicated on the diagrams. The wide tolerance for output fall time t_{of} given in Table 4 means that the design is not critical. The fall time is only slightly influenced by the external bus load (C_b) and external pull-up resistor (R_p). However, the rise time (t_r) specified in Table 5 is mainly determined by the bus load capacitance and the value of the pull-up resistor.

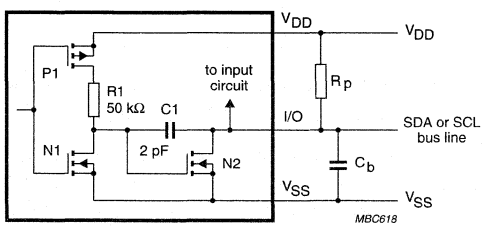


Fig.41 Slope-controlled output stage in CMOS technology.

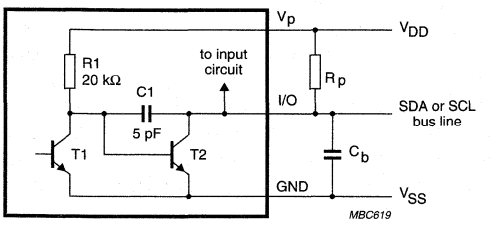


Fig.42 Slope-controlled output stage in bipolar technology.

17.2 Switched pull-up circuit for Fast-mode I²C-bus devices

The supply voltage (V_{DD}) and the maximum output LOW level determine the minimum value of pull-up resistor R_p (see Section 16.1). For example, with a supply voltage of V_{DD} = 5 V ± 10% and V_{OLmax} = 0.4 V at 3 mA, $R_{p\,min}$ = (5.5 − 0.4)/0.003 = 1.7 kΩ. As shown in Fig.33, this value of R_p limits the maximum bus capacitance to about 200 pF to meet the maximum t_r requirement of 300 ns. If the bus has a higher capacitance than this, a switched pull-up circuit as shown in Fig.43 can be used.

The switched pull-up circuit in Fig.43 is for a supply voltage of V_{DD} = 5 V ± 10% and a maximum capacitive load of 400 pF. Since it is controlled by the bus levels, it needs no additional switching control signals. During the rising/falling edges, the bilateral switch in the HCT4066 switches pull-up resistor R_{p2} on/off at bus levels between 0.8 V and 2.0 V. Combined resistors R_{p1} and R_{p2} can pull-up the bus line within the maximum specified rise time (t_r) of 300 ns.

Series resistors R_s are optional. They protect the I/O stages of the I²C-bus devices from high-voltage spikes on the bus lines, and minimize crosstalk and undershoot of the bus line signals. The maximum value of R_s is determined by the maximum permitted voltage drop across this resistor when the bus line is switched to the LOW level in order to switch off R_{p2}.

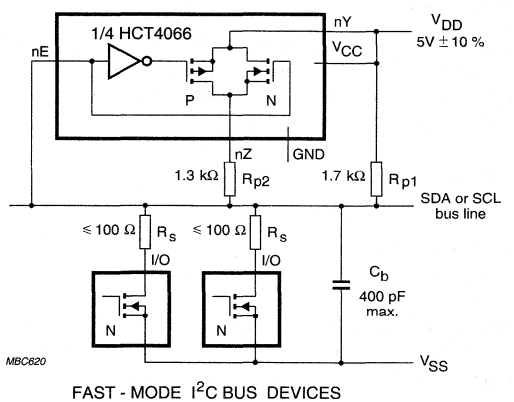


Fig.43 Switched pull-up circuit.

17.3 Wiring pattern of the bus lines

In general, the wiring must be so chosen that crosstalk and interference to/from the bus lines is minimized. The bus lines are most susceptible to crosstalk and interference at the HIGH level because of the relatively high impedance of the pull-up devices.

If the length of the bus lines on a PCB or ribbon cable exceeds 10 cm and includes the V_{DD} and V_{SS} lines, the wiring pattern must be:

SDA ——————————

V_{DD} ——————————

V_{SS} ——————————

SCL ——————————

If only the V_{SS} line is included, the wiring pattern must be:

SDA ——————————

V_{SS} ——————————

SCL ——————————

These wiring patterns also result in identical capacitive loads for the SDA and SCL lines. The V_{SS} and V_{DD} lines can be omitted if a PCB with a V_{SS} and/or V_{DD} layer is used.

If the bus lines are twisted-pairs, each bus line must be twisted with a V_{SS} return. Alternatively, the SCL line can be twisted with a V_{SS} return, and the SDA line twisted with a V_{DD} return. In the latter case, capacitors must be used to decouple the V_{DD} line to the V_{SS} line at both ends of the twisted pairs.

If the bus lines are shielded (shield connected to V_{SS}), interference will be minimized. However, the shielded cable must have low capacitive coupling between the SDA and SCL lines to minimize crosstalk.

17.4 Maximum and minimum values of resistors R_p and R_s for Fast-mode I²C-bus devices

The maximum and minimum values for resistors R_p and R_s connected to a Fast-mode I²C-bus can be determined from Figs 37, 38 and 40 in Section 16.1. Because a Fast-mode I²C-bus has faster rise times (t_r) the maximum value of R_p as a function of bus capacitance is less than that shown in Fig.39 The replacement graph for Fig.39 showing the maximum value of R_p as a function of bus capacitance (C_b) for a Fast-mode I²C-bus is given in Fig.44.

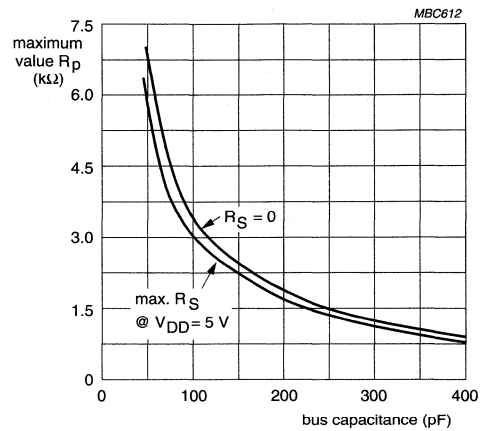


Fig.44 Maximum value of R_p as a function of bus capacitance for meeting the $t_{r\,max}$ requirement for a Fast-mode I²C-bus.

17.5 Maximum and minimum values of resistors R_p and R_s for Hs-mode I²C-bus devices

The maximum and minimum values for resistors R_p and R_s connected to an Hs-mode I²C-bus can be calculated from the data in Tables 6 and 7. Many combinations of these values are possible, owing to different rise and fall times, bus line loads, supply voltages, mixed speed systems and level shifting. Because of this, no further graphs are included in this specification.

18 BI-DIRECTIONAL LEVEL SHIFTER FOR F/S-MODE I²C-BUS SYSTEMS

Present technology processes for integrated circuits with clearances of 0.5 μm and less limit the maximum supply voltage and consequently the logic levels for the digital I/O signals. To interface these lower voltage circuits with existing 5 V, devices a level shifter is needed. For bi-directional bus systems like the I²C-bus, such a level shifter must also be bi-directional, without the need of a direction control signal[1]. The simplest way to solve this problem is by connecting a discrete MOS-FET to each bus line.

(1) US 5,689,196 granted; corresponding patent applications pending.

In spite of its surprising simplicity, such a solution not only fulfils the requirement of bi-directional level shifting without a direction control signal, it also:

- isolates a powered-down bus section from the rest of the bus system
- protects the "lower voltage" side against high voltage spikes from the "higher-voltage" side.

The bi-directional level shifter can be used for both Standard-mode (up to100 kbit/s) or in Fast-mode (up to 400 kbit/s) I²C-bus systems. It is not intended for Hs-mode systems, which may have a bridge with a level shifting possibility (see Section 13.5)

18.1 Connecting devices with different logic levels

Section 16 described how different voltage devices could be connected to the same bus by using pull-up resistors to the supply voltage line. Although this is the simplest solution, the lower voltage devices must be 5 V tolerant, which can make them more expensive to manufacture. By using a bi-directional level shifter, however, it's possible to interconnect two sections of an I²C-bus system, with each section having a different supply voltage and different logic levels. Such a configuration is shown in Fig.45. The left "low-voltage" section has pull-up resistors and devices connected to a 3.3 V supply voltage, the right "high-voltage" section has pull-up resistors and devices connected to a 5 V supply voltage. The devices of each section have I/Os with supply voltage related logic input levels and an open drain output configuration.

The level shifter for each bus line is identical and consists of one discrete N-channel enhancement MOS-FET; TR1 for the serial data line SDA and TR2 for the serial clock line SCL. The gates (g) have to be connected to the lowest supply voltage V_{DD1}, the sources (s) to the bus lines of the "lower-voltage" section, and the drains (d) to the bus lines of the "higher-voltage" section. Many MOS-FETs have the substrate internally connected with its source, if this is not the case, an external connection should be made. Each MOS-FET has an integral diode (n-p junction) between the drain and substrate.

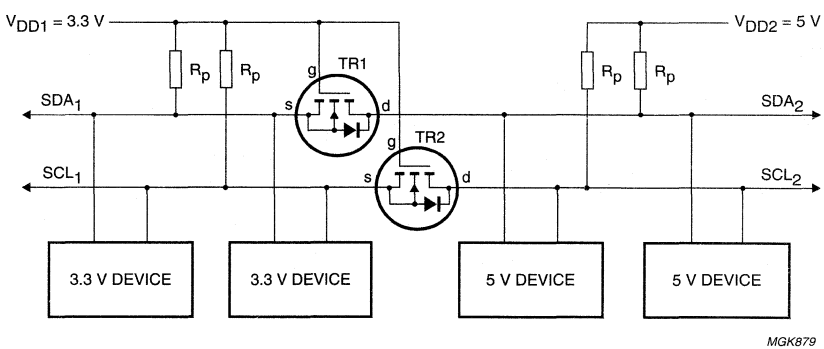


Fig.45 Bi-directional level shifter circuit connecting two different voltage sections in an I²C-bus system.

18.1.1 Operation of the level shifter

The following three states should be considered during the operation of the level shifter:

1. No device is pulling down the bus line.
   The bus line of the "lower-voltage" section is pulled up by its pull-up resistors R_p to 3.3 V. The gate and the source of the MOS-FET are both at 3.3 V, so its V_{GS} is below the threshold voltage and the MOS-FET is not conducting. This allows the bus line at the "higher-voltage" section to be pulled up by its pull-up resistor R_p to 5 V. So the bus lines of both sections are HIGH, but at a different voltage level.
2. A 3.3 V device pulls down the bus line to a LOW level. The source of the MOS-FET also becomes LOW, while the gate stay at 3.3 V. V_{GS} rises above the threshold and the MOS-FET starts to conduct. The bus line of the "higher-voltage" section is then also pulled down to a LOW level by the 3.3 V device via the conducting MOS-FET. So the bus lines of both sections go LOW to the same voltage level.
3. A 5 V device pulls down the bus line to a LOW level. The drain-substrate diode of the MOS-FET the "lower-voltage" section is pulled down until V_{GS} passes the threshold and the MOS-FET starts to conduct. The bus line of the "lower-voltage" section is then further pulled down to a LOW level by the 5 V device via the conducting MOS-FET. So the bus lines of both sections go LOW to the same voltage level.

The three states show that the logic levels are transferred in both directions of the bus system, independent of the driving section. State 1 performs the level shift function. States 2 and 3 perform a "wired AND" function between the bus lines of both sections as required by the I²C-bus specification.

Supply voltages other than 3.3 V for V_{DD1} and 5 V for V_{DD2} can also be applied, e.g. 2 V for V_{DD1} and 10 V for V_{DD2} is feasible. In normal operation V_{DD2} must be equal to or higher than V_{DD1} (V_{DD2} is allowed to fall below V_{DD1} during switching power on/off).

19 DEVELOPMENT TOOLS AVAILABLE FROM PHILIPS

Table 8 I²C evaluation boards

PRODUCT	DESCRIPTION
OM4151/ S87C00KSD	I²C-bus evaluation board with microcontroller, LCD, LED, Par. I/O, SRAM, EEPROM, Clock, DTMF generator, AD/DA conversion.
OM5500	Demo kit for the PCF2166 LCD driver and PCD3756A telecom microcontroller

Table 9 Development tools for 80C51-based systems

PRODUCT	DESCRIPTION
PDS51	A board-level, full featured, in-circuit emulator: RS232 interface to PC, universal motherboard, controlled via terminal emulation

Table 10 Development tools for 68000-based systems

PRODUCT	DESCRIPTION
OM4160/2	Microcore-2 demonstration/evaluation board with SCC68070
OM4160/4	Microcore-4 demonstration/evaluation board with 90CE201
OM4160/5	Microcore-5 demonstration/evaluation board with 90CE301

Table 11 I²C analyzers

PRODUCT	DESCRIPTION
OM1022	PC I²C-bus analyzer with multi-master capability. Hardware and software (runs on IBM or compatible PC) to experiment with and analyze the behaviour of the I²C-bus (includes documentation)
OM4777	Similar to OM1022 but for single-master systems only
PF8681	I²C-bus analyzer support package for the PM3580 logic analyzer family

20 SUPPORT LITERATURE

Table 12 Data handbooks

TITLE	ORDERING CODE
IC01: Semiconductors for Radio, Audio and CD/DVD Systems	9397 750 02453
IC02: Semiconductors for Television and Video Systems	9397 750 01989
IC03: Semiconductors for Wired Telecom Systems (parts a & b)	9397 750 00839, 9397 750 00811
IC12: I²C Peripherals	9397 750 01647
IC14: 8048-based 8-bit microcontrollers	9398 652 40011
IC17: Semiconductors for wireless communications	9397 750 01002
IC18: Semiconductors for in-car electronics	9397 750 00418
IC19: ICs for data communications	9397 750 00138
IC20: 80C51-based 8-bit microcontrollers + Application notes and Development tools	9397 750 00963
IC22: Multimedia ICs	9397 750 02183

Table 13 Brochures/leaflets/lab. reports/books etc.

TITLE	ORDERING CODE
Can you make the distance... with I²C-bus (information about the P82B715 I²C-bus extender IC)	9397 750 00008
I²C-bus multi-master & single-master controller kits	9397 750 00953
Desktop video (CD-ROM)	9397 750 00644
80C51 core instructions quick reference	9398 510 76011
80C51 microcontroller selection guide	9397 750 01587
OM5027 I²C-bus evaluation board for low-voltage, low-power ICs & software	9398 706 98011
P90CL301 I²C driver routines	AN94078
User manual of Microsoft Pascal I²C-bus driver (MICDRV4.OBJ)	ETV/IR8833
C routines for the PCF8584	AN95068
Using the PCF8584 with non-specified timings and other frequently asked questions	AN96040
User's guide to I²C-bus control programs	ETV8835
The I²C-bus from theory to practice (book and disk)	Author: D. Paret Publisher: Wiley ISBN: 0-471-96268-6
Bi-directional level shifter for I²C-bus and other systems	AN97055
OM5500 demo kit for the PCF2166 LCD driver and PCD3756A telecom microcontroller	9397 750 00954

For more information about Philips Semiconductors and how we can help in your I²C-bus design, contact your nearest Philips Semiconductors national organization from the address list of the back of this book, or visit our worldwide web site at http://www.semiconductors.philips.com

EMBEDDED SYSTEMS

Programming the I²C Interface

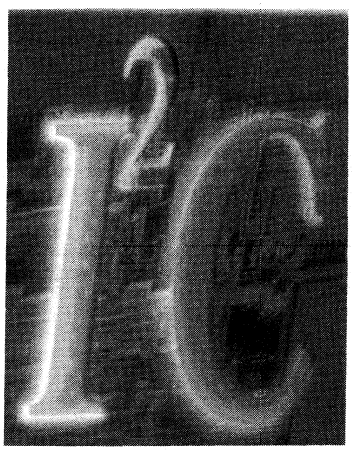
When intelligent devices need to communicate

Mitchell Kahn

The Inter-Integrated Circuit Bus ("I²C Bus" for short) is a two-wire, synchronous, serial interface designed primarily for communication between intelligent IC devices. The I²C bus offers several advantages over "traditional" serial interfaces such as Microwire and RS-232. Among the advanced features of I²C are multimaster operation, automatic baud-rate adjustment, and "plug-and-play" network extensions.

Mention the I²C bus to a group of American engineers and you'll likely get hit with an abundance of blank stares. I say American engineers because until recently the I²C bus was primarily a European phenomenon. Within the last year, however, interest in I²C in the United States has risen dramatically. Embedded systems designers are realizing the cost, space, and power savings afforded by robust serial interchip protocols.

The idea of serial interconnect between integrated circuits is not new. Many semiconductor vendors offer devices designed to "talk" via serial links with other processors. Current examples include Microwire (National Semiconductor), SPI (Motorola), and most recently Echelon's Neuron chips. In all cases, the goal is the same: to reduce the wiring and pincount necessary for a parallel data bus. It simply does not make economic sense to route a full-speed parallel bus to a slow peripheral.



Unfortunately for most serial-bus-capable devices, the choice of a bus protocol will dictate the CPU architecture. For example, only two CPU architectures implement an on-chip I²C port. If your choice of architecture precludes use of these architectures, then your only option is to implement the protocol in software.

The software implementation of the I²C protocol discussed in this article came about as a result of an implicit challenge during a staff meeting. One of our managers proposed that we hire a consultant to write a software I²C driver for the Intel 80C186EB embedded processor. Being somewhat new to the group, I took exception (although not verbally!) to his suggestion. A weekend of intense hacking later, I presented the first prototype of the driver. My reward? I got to write a generic version of the driver for general distribution.

Design Trade-offs

Three distinct tasks are involved in implementing the I²C protocol: watching the bus, waiting for a specific amount of time, and driving the bus. This became apparent when I flowcharted 1 byte of a typical bus transaction; see Figure 1. The time delays associated with creating the bus waveforms would normally have been relegated to the 80C186EB's on-chip timers. I could not, however, assume that the end users of my code would be able to spare a timer for the software I²C port. I had to forego the elegance (and to some extent accuracy) of the on-chip timers for the sledgehammer approach of software timing loops. Luckily, the I²C protocol is extremely forgiving with regard to timing accuracy. The decision to use assembly instead of a high-level language stemmed directly from the need to control program-execution time. I had neither the time nor the inclination to hand-tune high-level code.

Having made the decision to use assembly language, I faced my next problem: Could I make the code portable? Intel offers a plethora of CPU and embedded-controller architectures. Would it be possible to make the code somewhat portable between disparate assembly languages? I found my answer in the use of macros.

Mitch is a senior strategic development engineer for Intel and can be contacted at 5000 W. Chandler Blvd., Chandler, AZ 85226 or at mkahn@sedona.intel.com.

All the basic building blocks of the I²C protocol (watching, waiting, and doing) can be compartmentalized into distinct macros. The algorithms that make up the I²C driver are written with these macros as the framework. You don't need to understand the intricacies of the I²C protocol to port these routines—you just need to know how to make your CPU watch, wait, and do.

For example, a 4.7_uS delay is a common event during a transfer. The macro *%Wait_4_7_uS* implements just such a delay by using the 8086 LOOP instruction with a couple of NOPs for tuning; see Example 1(a). Total execution time is readily calculated from instruction timing tables. The same macro is ported to the i960 architecture in Example 1(b). Although I am a neophyte when it comes to i960 programming, I had no problems porting the core macros.

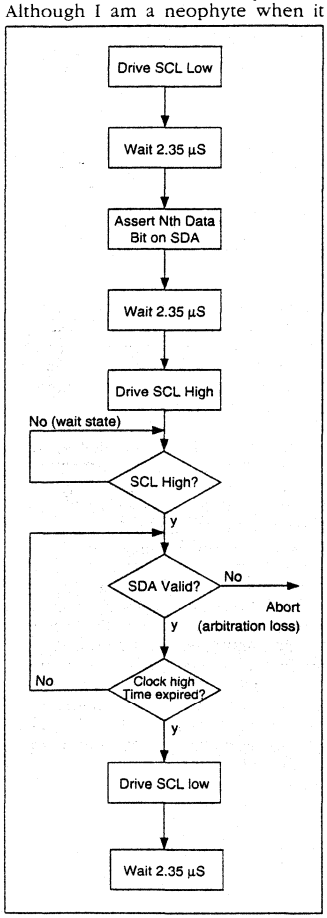


Figure 1: *Flowchart of process for transmission of a single bit.*

Hardware Dependencies

A few words about the target hardware are in order before I discuss the code. Any implementation of the I²C protocol requires two open-drain (or open-collector), bidirectional port pins for the Serial Clock (SCL) and Serial Data (SDA) lines. The code in this article was designed for the 80C186EB embedded processor, which has two open-drain ports on-chip. The two pins, P2.6 (SCL) and P2.7 (SDA), are part of a larger 8-bit port. Processors without open-drain I/O ports can easily implement I²C with the addition of an external open-collector latch.

Two special-function registers, P2PIN and P2LTCH, are used to read and write the state of the port pins. The 80C186EB allows the special-function registers to be located anywhere in either memory or I/O space. For this implementation, I chose to leave the registers in I/O space, even though this limited my choice of instructions. The 80186 architecture does not provide for read-modify-write instructions in I/O space (an AND to I/O, for example); it can only load and store (IN and OUT). So why did I limit myself? Again, I had to assume the lowest common denominator for our customers when designing my code.

Building the Framework

Early on in development, I decided to partition my code macros according to physical processes involved in the I²C protocol. Code not directly involved in mimicking the actions of a hardware I²C port was not written as macros. For example, the code necessary to access the stack frame is not written as a macro, whereas the code needed to toggle the clock line is. This was done to isolate architecture-dependent code sequences from the more generic I²C functions. Macros were also not used for "gray areas" such as the shifting of serial data, which is both architecture dependent and physical in nature. The I²C functions that passed the litmus test fell into the three aforementioned categories of watching, waiting, and doing.

The "waiting" macros provide a fixed-minimum time delay. They are implemented using a simple LOOP $ delay. The LOOP instruction decrements the CX register, then branches to the target (in this case itself) if the result is nonzero. The delay is (n–1)*15+5 clocks, where n is the starting value in the CX register. All the delays were calculated assuming a 16-MHz clock rate (62.5 nanoseconds per clock). The code still works at lower CPU speeds because the I²C protocol only specifies minimum timings. In fact, the delay macros are only "accurate enough," providing timings as close as I could get to the specified minimum without undue tuning.

The "watching" macros are "spin-on-bit" polling loops. These pieces of code wait for a transition on the appropriate I²C line to occur before allowing execution to continue. There are two polling macros for each of the two I²C signal lines; one for high-to-low transitions and one for low-to-high transitions. The

(a)

```
%*DEFINE(Wait_4_7_uS)(
        mov     cx, 5           ; 4 clocks
        loop    $               ; 4*15+5 = 65 clocks
        nop                     ; 3 clocks
        nop                     ; 3 clocks
                                ; total = 75 clocks
                                ; 75 * 62.5ns = 4.69uS (close enough)
        )
```

(b)

```
define(Wait_4_7_uS,'
        lda     0x17, r4        # instruction may be issued in parallel
                                # so assume no clocks.
0b:     cmpdeco 0, r4           # compare and decrement counter in r4
        bne.t   0b              # if !=0 branch back (predict taken
                                # branch)
                                #
                                # The cmpdeco and bne.t together take 3
                                # clocks in parallel minimum.
                                #
                                # 0x17 (25 decimal) * 3 = 75 clocks
                                # at 16MHz this is 4.69uS
')
```

Example 1: *(a) 80C186 implementation of 4.7_uS wait macro; (b) 80960CA implementation of 4.7_uS wait macro.*

polling of the SCL line that gives rise to an important feature of I²C: automatic, bit-by-bit baud-rate adjustment. Any device on the I²C bus may hold the clock line low in order to stall the bus for more time (a serial wait state). The other devices on the bus are then forced to poll the SCL line until the slow device releases control of the clock.

The *%Get_SDA_Bit* macro also falls under the category of "watching." Its function is simply to return the state of the SDA line without waiting for a transition. *%Get_SDA_Bit* is used primarily to pull the serial data off the bus when the clock is valid.

The "doing" macros control the state of the clock and data lines. As with the polling macros, there are four types—one for each transition of the SCL or SDA lines. The "doing" macros are named to reflect the physical operations they perform. For example, *%Drive_SCL_Low* always drives the SCL line to a low state. *%Release_SCL_High*, on the other hand, relinquishes control of the SCL line, which may then be pulled high or driven low by another device on the bus. A read-modify-write operation is used for the bit manipulation so that the other 6 bits of Port 2 are not affected by the I²C operations.

Getting on the Bus

Three procedures were created using the macro framework. I'll describe only the master transmit (Listing One, page 106) and master receive functions (Listing Two, page 108), as they represent the needs of most I²C users. The slave procedure is long and intricate and will not be described here.

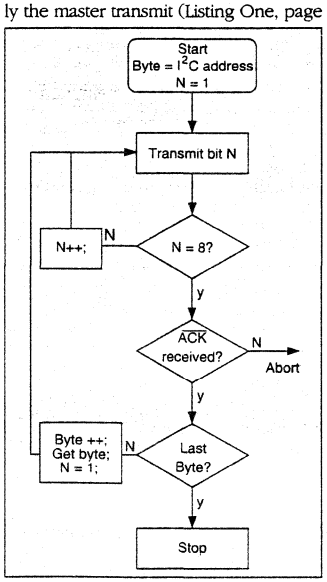


Figure 2: *Flowchart for I²C transmit procedure.*

An I²C master transmission proceeds as follows:

1. The master polls the bus to see if it is in use.
2. The master generates a start condition on the bus.
3. The master broadcasts the slave address and expects an acknowledge (ACK) from the addressed slave.
4. The master transmits 0 or more bytes of data, expecting an ACK following each byte.
5. The master generates a stop condition and releases the bus.

The stack frame for the master transmit procedure, I2CXA.A86, includes a far pointer to the message for transmission, the byte count for the message, and the slave address. Far pointers and far procedure calls are used in all the procedures. No attempt was made to conform to a specific high-level language calling convention, although such a conversion would be trivial. The procedures save only the state of the modified segment registers.

The master transmit procedure performs error checking on the passed parameters before attempting to send the message. The maximum message length is set at 64 Kbytes by the segmentation of the 80186 memory space. This restriction could be removed by including code to handle segment boundaries. The transmit procedure also checks the direction bit in the slave address to ensure that a reception was not erroneously indicated. Errors are reported back to the calling procedure through the AX register. (The exact code is in Listing One.)

The first step in sending a message is getting on the I²C bus. The macro *%Check_For_Bus_Free* simply polls the bus to determine if any transactions are in progress. If so, the transmit procedure aborts with the appropriate error code. If the bus is free, a start condition is generated. The start condition is defined as a high-to-low transition of SDA with SCL high followed by a 4.7_uS pause. These waveforms are easily generated with the *%Drive_SDA_Low* and *%Wait_4_7_uS* macros.

All communication on the I²C bus between the stop and start conditions, including addressing and data, takes place as an 8-bit data value followed by an acknowledge bit. This lead to the natural nested loop structure for the body of the procedure; see Figure 2.

The inner loop is responsible for transmitting the 8 bits of each data byte. Each transmitted bit generates the appropriate data (SDA) and clock (SCL) waveforms while checking for both serial wait states and potential bus collisions. A bus collision occurs when two masters attempt to gain control of the bus simultaneously. The I²C protocol handles collisions with the simple rule: "He who transmits the first 0 on the SDA line wins the bus." To ensure that we (the master transmit procedure) own the bus, the SDA line is checked whenever transmitting a 1. If a 0 is present, then a collision has occurred (because another master is pulling the line low), and the transfer must be aborted.

Three distinct tasks are involved in implementing the I²C protocol: watching the bus, waiting for a specific amount of time, and driving the bus

Control is turned over to the outer loop after the 8 bits of data (or address) have been transmitted. The outer loop immediately checks for an acknowledge from the addressed slave. The transfer is aborted if an acknowledge is not received. At the end of the ACK bit the message length counter is decremented. Control is returned to the inner loop if more data remains, otherwise a stop condition is generated and the master transmit procedure terminates.

Registers are used for intermediate result storage throughout the body of the procedure. For example, the AH register is used to hold the current value (either address or data) being shifted onto the SDA line. This eliminates the need for local data storage within the procedure.

On the Receiving End

The steps involved in an I²C master receive transaction are almost identical to those in transmission:

1. The master polls the bus to see if it is in use.
2. The master generates a start condi-

tion on the bus.

3. The master broadcasts the slave address and expects an ACK from the addressed slave.
4. The master receives 0 or more bytes of data and sends an ACK to the slave after each byte. The master signals the last byte by not sending an ACK.
5. The master generates a stop condition and releases the bus.

A far pointer to the receive buffer is passed on the stack to the master receive procedure. The remainder of the parameters—slave address and message count—are identical between the two procedures. The received message length is fixed at 64 Kbytes, again because of segmentation. The error-checking, bus-availability sensing, and start-condition generation sections of the receive procedure are lifted verbatim from the transmit code.

The structure of the receive procedure differs slightly once the start condition has been generated; see Figure 3. The slave address is transmitted using one iteration of the transmit procedure's outer loop. Control is passed to the receive loop once the slave acknowledges its address.

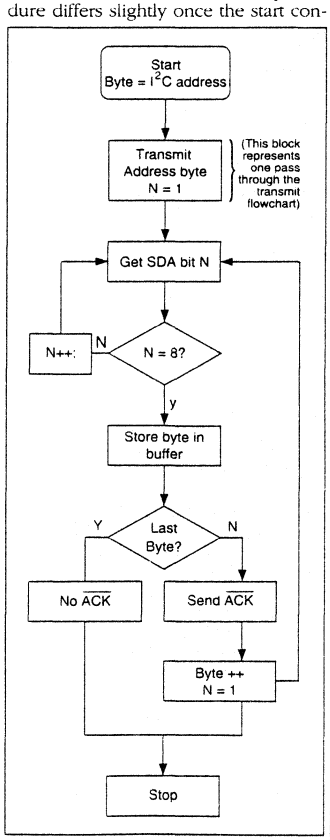


Figure 3: *Flowchart for I2C receive procedure.*

The receive loop structure is patterned after that of the transmit procedure. The inner loop controls the clocking of the SCL line and the shifting of the serial data off the SDA line into the CPU. Eight iterations of the inner loop are performed to receive each byte. The outer loop stores the received byte in the buffer, decrements the byte count, then sends an ACK to the slave. The last data byte is signalled by not sending an ACK.

Using the Procedures

Listing Three (page 110) shows a short program that uses both the master transmit and master receive procedures. The call to procedure I2C_XMIT displays the word "bUS-" on a four-character, seven-segment display controlled by the SAA1064 I²C compatible display driver. The time of day is read from the PCF8583 real-time clock by the call to procedure I2C_RECV.

Please note that interrupts must be disabled during the execution of both procedures. An interruption at an inopportune time (when the master is not in control of the clock) could cause the bus to hang. If you need to service interrupts periodically, then enable them only when the clock is driven low.

These procedures have been tested on a wide array of I²C devices ranging from serial EEPROMs to voice synthesizers. No compatibility problems have been seen to date.

Enhancing the Code

I've kicked around many ideas for enhancing the I²C procedures. You could, for example, replace the timing loops with timed interrupts. That way, the CPU could perform useful work during the pauses. Along the same lines, the pauses could be scheduled using a real-time kernel, again improving CPU throughput. Finally, you could add a high-level language calling structure.

The use of timed interrupts adds an order of magnitude to the complexity of the code, but would be worth it for high-performance, real-time systems.

All the basic building blocks of the I²C protocol (watching, waiting, and doing) can be compartmentalized into distinct macros

Conclusion

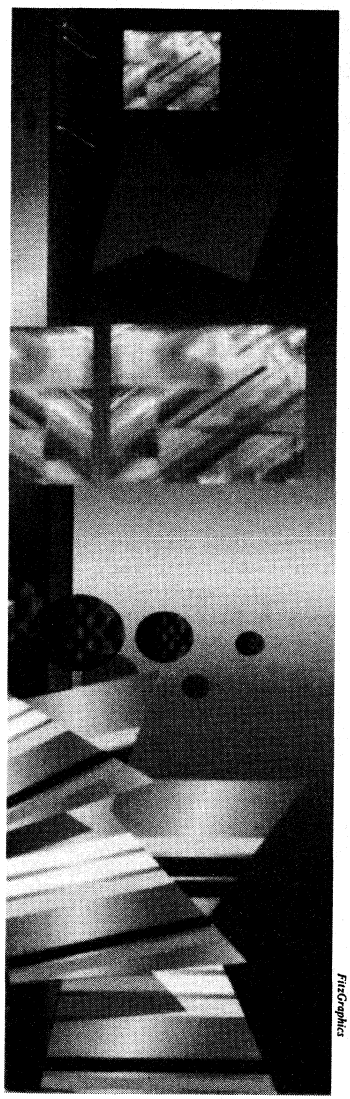
I²C is not the only game in town when in comes to serial protocols. Hopefully, some of the techniques presented here will carry over into the development of other "simulated" serial protocols, such as those targeted at the home-automation market. Who knows, maybe someday a snippet of my code may find its way into a truly intelligent dishwasher. I'll be waiting....

References

I²C Bus Specification, Philips Corporation (undated).

DDJ

Exploring I²C



FitzGraphics

Serial data buses are a well-proven tool in embedded systems. When you are communicating with slow peripheral devices, serial buses are often often more convenient and less expensive than parallel buses. Additionally, a serial interface featuring a UART or similar intermediary chip can also serve to isolate the CPU from noise and line glitches that might bring down the house if they were to occur on the processor bus. Peripherals can usually be controlled over a much greater distance by a serial bus. The serial approach offers greater resilience and noise immunity.

The price you pay for the convenience is a slower transmission rate and, possibly, the need for added interface circuitry at higher voltages. Many peripheral devices, however, are not in constant communication with the CPU and are not greatly affected by a slower bus. On the hardware side, any added interface circuitry required for serial-bus support is frequently compensated for by the resulting simplicity and tighter pinout of the serial peripherals.

The choice of bus and protocol depends at least as much on the system's software as it does on the manufacturer's data sheets.

CHOOSING THE PROPER ROUTE

Having decided that a serial bus makes sense for your application, your next task is to select the most appropriate bus and protocol. Here, as with rapid transit, your choice should be determined by your destination. Contrary to what some people may tell you, the choice of bus and protocol depends at least as much on the nature of the system's software as it does on the manufacturer's data sheets.

Consider, for example, the serial-peripheral interface (SPI) and multidrop serial buses. Both buses are popular, but each exhibits severly constrained performance in large networks. SPI, as embodied in the Motorola 6800 family, was designed primarily for one-on-one exchanges between two devices. Similarly, the multidrop approach used in various 8051 family members as well as in the 68HC11 and various UART chips finds its broadest expression in RS485/422 half-duplex transmissions. Multidrop has no deterministic arbitration scheme between multiple masters, leaving it mainly suitable for single-master multiple-slave situations. *(For more on multidrop, see Jack Woehr's article, "Multidrop Processing," Embedded Systems Programming, March 1990, pp 58-67—ed.)* A different approach is to use a three-wire protocol called MicroWire, available from National Semiconductor in Santa Clara, Calif., which is fine for use with addressable peripherals, but requires an individual chip select for each device ad-

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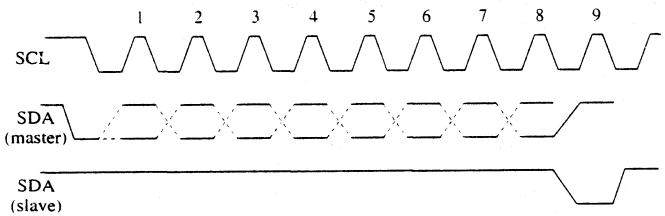
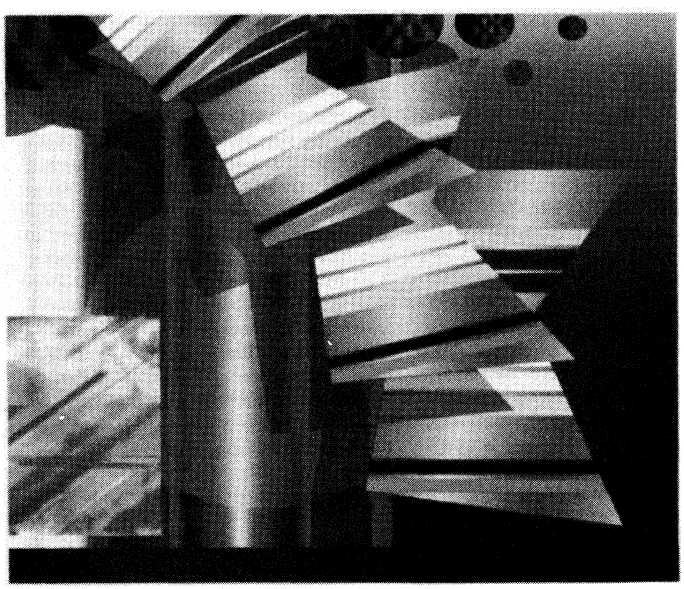
dressed. The added wiring offers no advantage to developers, and the bus offers nothing towards achieving multiple-mastering capabilities.

One of the more versatile options available to developers is the I²C bus promulgated by Philips/Signetics in Sunnyvale, Calif. I²C allows you to set up a multiple-master, multiple-slave communications bus with conflict arbitration, using only twisted-pair wiring to connect the processors and peripherals. Philips/Signetics has moved to support this protocol (which is quite popular in Europe) with a large assortment of interesting doodads, and is actively encouraging other manufacturers to join in the fun. If your next design features a microprocessor that supports I²C or you are prepared to implement I²C in software using a PIA as this article illustrates, your reward could be a decreased chip count and lower power consumption—along with a comfortable distributed-programming model for peripheral devices.

Open-collector configuration means that the output stage can only pull the node to ground.

Figure 1
Generation of acknowledge.





I²C is more flexible than the protocols noted above, since only two wires are required to service a large network of addressable masters and addressable slaves. A third wire may be added if interrupt service is required, though Philips/Signetics microprocessors featuring I²C support feature on-chip circuitry and are capable of interrupting the processor upon receipt of a valid address.

HOW I²C WORKS

The I²C bus consists of two lines: serial clock (SCL) and serial data (SDA). The beauty of the I²C bus is that each of these lines is bidirectional. Bidirectional means that everything on the bus is equal, unlike most other serial-peripheral busses such as SPI or MicroWire, which have dedicated inputs and outputs. Each I²C transaction line (SCL and SDA) is an open collector of output and input. The

pullup resistor is external.

Open-collector (actually, they are CMOS, so "open drain" is more appropriate) configuration means that the output stage can only pull the node to ground. A passive resistor pulls the node high, which means that any number of open collector outputs can be connected together with no deliterious results, because it is impossible to pull more current through the resistor than any one output will produce. Tying outputs together will produce disastrous results if the same procedure is tried with standard TTL outputs. If some of the outputs go high and some are low, the current is unlimited and the logic level of the output will be in an indeterminate state. Tying open-collector outputs together is also known as "wire ORing" because if either A or B goes low, so does the single-output line.

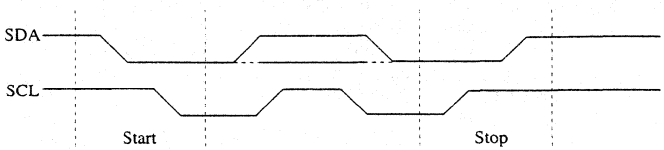
The I²C bus speed is specified at a maximum SCL rate of 100kHz SCL, which, admittedly, is not blazingly fast. The speed limit stems from the meager ability of a pullup resistor to source current to a long distributed line of peripherals. The 10-microsecond period allows plenty of time to charge the parasitic capacitance of the wires. (The maximum specified wire capacitance is 400 pF.)

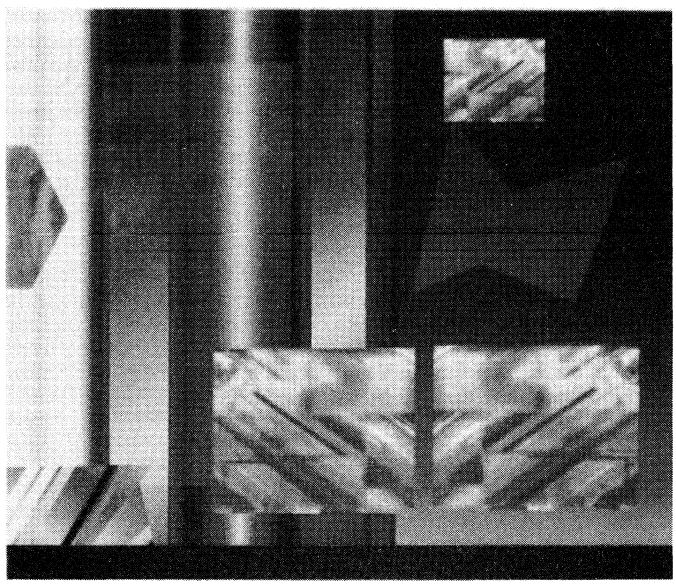
PUTTING IT TOGETHER

Although I²C supports multiple-master operation, here we use single-master, single-slave transactions to keep the example code simple. The master, as you might imagine, is defined as the unit that initiates the data transfer and generates the SCL signal. (In a multimaster system, each master would be responsible for generating its own SCL signal.) In our example, based strongly on the design of one of our company's single-board computers, the processor doesn't directly support I²C. Instead, we've implemented the I²C bus using a couple of the pins on an 8255 peripheral I/O chip. Consequently, the bulk of the example application code is simple setup and housekeeping routines. *(Steven R. Wheeler's example application listing was a bit too long to run in this issue. Interested readers may download it from the library 12 of CLMFORUM on CompuServe or from the* Embedded Systems Programming *bulletin board service at (415) 905-2689—ed.)*

By definition, a slave can be any processor or peripheral that responds to the master. Slaves all have unique, 7-bit addresses that are based on the device type and the wiring of address pins on the chip. All I²C peripherals have the top nibble of an address built in. For the PCF8574 I/O-port expanders we're us-

Figure 2
Start and stop conditions.





Exploring I²C

ing as examples, the address is 0100*xxx*. The *xxx* indicates the address selected by the state of the three address pins on the peripheral.

I²C serial transactions are always eight bits of data from the transmitter followed by a ninth ACK bit from the receiver. The first step in any I²C data transfer is to send the address of the slave on the SDA line. This act might seem confusing, since we seem to be mixing 7-bit addresses with 8-bit data. In practice, it's quite easy to work with: addresses are always seven bits long, and the eighth bit is used to determine whether the operation is a read or a write. For example, upon transmitting 01000001 to the PCF8574, the slave, assuming it exists on the bus and is strapped to address 000, will respond with a low on the SDA line after the master has finished with its last (eighth) data bit. The master leaves the line high. If it doesn't find a slave with address 10000, the data line will remain high and a failed communication attempt can be detected.

If a slave is connected, it begins putting data on the SDA line as soon as it has detected that the eighth bit is set (which is a read request). The SDA line is driven to the data level when the SCL line is low. Data is read when SCL is high, so SDA must not change when SCL is high. This protocol leads to a simple definition of the start of an I²C transaction—SDA goes from high to low when the clock is high.

The end of a transaction is equally simple to detect: SDA goes from low to high when SCL is high. This cycle leaves SDA and SCL in the high state, which is necessary if any other open-collector I²C peripheral wants access to the bus. Figure 2 illustrates the start and stop conditions of an I²C bus transaction.

ADDITIONAL DESIGN ROUTES

As you've seen, the I²C protocol is easy to work with and relatively simple to implement, even if you're not using a processor that directly implements it. If you're not planning to use Philips/Signetics microprocessors with onboard I²C support (such as the 68070 or various members of the 8051 family), you can still use the wide variety of available peripheral chips.

The number of integrated circuits using the I²C serial bus is increasing all the time. Application-oriented integrated circuits that support I²C include a voice sythesizer, a transcoder for IR remote control, several digital tuning circuits for computer-controlled television, several audio processors, PLL frequency synthesizers, tone generators, and frequency synthesizers. General-purpose integrated circuits using I²C include LCD drivers, digital-to-analog converters, SRAMs, EEPROMs, and a RAM clock/calender.

I²C is very popular in Europe, where Philips has been aggressively marketing this flexible method of extending peripheral support to control projects, and it is currently catching fire on this side of the Atlantic. It seems reasonable to expect that, given the burden of printed-wire requirements for embedded systems based on increasingly wider chip buses, more and more designers seeking economy of means will be attracted to the economy of I²C.

Steven Sarns is the president of Vesta Technology in Wheat Ridge, Colo. He is a member of Mensa, Intertel, and the Michigan Society of Professional Engineers. Sarns is also a founding member of the Denver chapter of the Forth Interest Group.

Jack Woehr is a senior project manager at Vesta Technology Inc. in Wheat Ridge, Colo. He is a Chapter Coordinator for the Forth Interest Group and is currently a member of the X3J14 Technical committee for ANS Forth. He can be reached by E-mail as jax@well.sf.ca.us or as VESTA on GEnie.

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BY MARK GARDNER

Bit-Banging Serial Ports

They say that necessity is the mother of invention, and it certainly seems to be the case in embedded systems work. No sooner do you accomplish the impossible in one project than your boss or customer asks you to do it again, only faster and cheaper this time. Even when you're working with low-cost microcontrollers, there's still that incentive to make things cheaper through magic software.

Performing miracles through software trickery is a skill that all embedded developers must cultivate. An opportunity for me to practice such tricks came in the form of a project using the Signetics 8x751 microcontroller. The 8x751 is an 8051 derivative that has no internal serial port—no attachment of SBUF shift registers to RxD and TxD, no diversion of timers to baud rate pacing, no serial interrupts. But the chip is low-priced and offers a small-footprint, and hence is desirable in many applications. Where the price or size outweighs the need for a simple serial port, one must be built out of firmware by appropriately controlling a single bit in a port. The practice is affectionately known as "bit-banging."

The approach I'll describe here has the advantages of being simple and fast. There is no transmit state-machine, no special provision for start and stop bits, and it takes less than two dozen machine cycles for each bit. It has a further advantage that the data doesn't need to be specially organized for transmitting. That is, the bits that are adjacent in the transmit data stream don't need to be adjacent when they are stored in memory. This solution is for a transmitter only, but I have used a similar procedure for receiving.

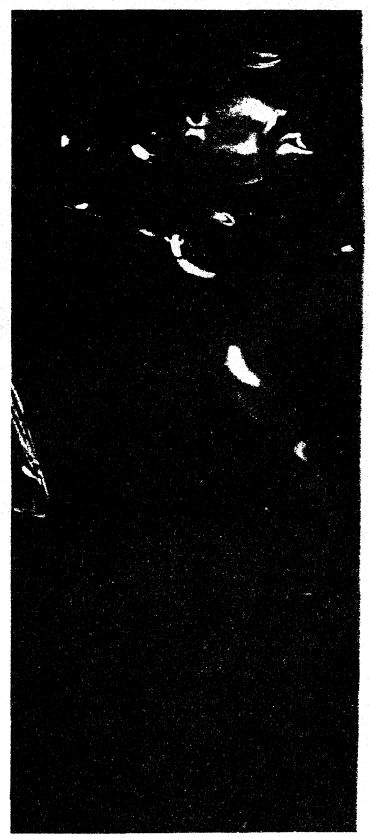
The shift (or rotate) operation is the first thing that comes to mind when you're designing code to provide a serial data output.

My project was required to operate at 9600 baud. This rate gives a per-bit time of 104 microseconds, or 104 cycles if you're using a 12-MHz part. The application in question had plenty of other activities as well as a serial port (such as reading a serial analog-to-digital converter, performing averages, and so on), so it was imperative that the serial port handling take an absolute minimum of time. Since I chose to execute in a fixed-time loop (to avoid interrupt overhead), it was also a goal that the code take a fixed amount of time regardless of the current transmit state.

THE STRUCTURE POINTER SOLUTION

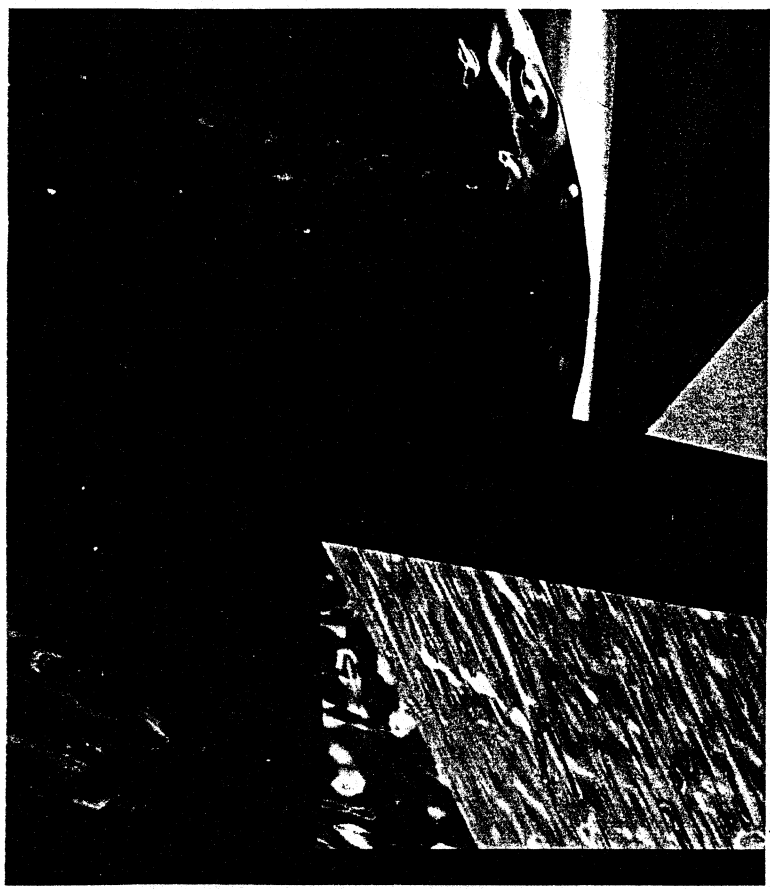
Generally, the shift (or rotate) operation is the first thing that comes to mind when you're designing code to provide a serial data output—the format of the data suggests such a scheme. With this approach, however, special states and a counter are needed to provide the start and stop bits and to sequence through the set of bytes to be transmitted.

The method presented here provides an array of structures (in the code or PROM space) that defines the transmit sequence bit by bit and uses a pointer to this array as the only controlling element. This means that only two bytes of scarce internal RAM is used.



The structures are referenced consecutively. Each gives the source of a bit to be transmitted and a flag to indicate whether the pointer should be increased to point to a new bit. The transmission is terminated by having a structure that refers to an "idle" bit and does not increase the pointer. Transmission is initiated by changing the pointer to point to the first structure. Start and stop bits are not distinguished from data bits. The bit update portion of the code is constant-time, and the pointer update can be easily padded if necessary to achieve this part of the goal.

Franklin's C51 compiler was used for the work described here. The 8x751 does not support external RAM, so the small model is used. (If the transmit data resided in external RAM, the algorithm could be applied, but would be expected to take a little longer to execute.)



pixelworks

THE DECLARATIONS

The structure that provides individual bit definitions is:

```
// transmit bit-reference structure
struct BR {
        unsigned char index ;
        unsigned char mask ;
        unsigned char bump ;
} ;
```

No memory is allocated by this definition—it is essentially a `typedef`. The actual allocation and initialization are provided by the definition (in a header file, send_seq.h, in this case) of the `BitRef` array:

```
code struct BR BitRef[41] = { ... } ;
```

where the details will be given in a moment. The pointer is defined as:

```
// pointer to BitRef structure array
data struct BR code *BR_ptr ;
```

In Franklin's C51, the declaration tokens are interpreted as follows. In the struct `BR` declaration, the token `code` assigns the `BitRef` array to program memory (which is then accessed with the `movc` instruction). In the `*BR_ptr` declaration, the token `code` implies that `BR_ptr` is exclusively a pointer to the program space, so it requires only two bytes to be completely defined. The token `data` causes the compiler to store the pointer value in

internal RAM. (Since I was using the small model, this would have been the default storage anyway.)

The index entry in each structure allows the serial bit to be selected from an array of bytes called transmit[4] in my case. The transmit array can, if desired, be set up to literally overlay all of the internal memory, so that the maximum "random access" can be achieved. This was not necessary in my case.

The physical port pin to be exercised is defined:

```
/*     transmit is on P3.3 */
sbit TransBit = 0xB3 ;
```

THE STRUCTURE INITIALIZATION

Each bit to be transmitted is defined by an index and mask. These are initialized in the BitRef structure so that characters can be formed as desired in the output bit stream. The index is the offset within the transmit array. The initialization in my case, for a sequence of 40 bits making up four characters, was:

```
code struct BR BitRef[41] = {
//  index    mask      bump    comment

    3 , b01000000 , 1,    //  0 start bit

    1 , b00000001 , 1,    // D6
    1 , b00000010 , 1,    // D7
    1 , b00000100 , 1,    // D8
    1 , b00001000 , 1,    // D9
    1 , b00010000 , 1,    // D10
    1 , b00100000 , 1,    // D11

    3 , b10000000 , 1,    //  1 fixed
    3 , b10000000 , 1,    //  1 fixed
    3 , b10000000 , 1,    //  1 stop bit

    3 , b01000000 , 1,    //  0 start bit
    ...
    ...
    ...
    3 , b01000000 , 1,    //  0 fixed
    3 , b10000000 , 1,    //  1 stop bit
    3 , b10000000 , 0     //  1 idle bit
} ;
```

(The "masks" are given in binary notation. [*See "A Binary Upgrade for C," pp. 60-62.—Ed.*] Because of my assembler and hardware background, this notation is natural for me in bit mask references.)

The "bump" is a flag that continues the transmission. When it finally reaches 0, the serial output sequence will stop.

The "index" refers, as mentioned, to the element of "transmit" in which the bit resides. Some initialization code has guaranteed that the upper two bits of transmit[3] will be 10, so that they can be referred to for start and stop bits and for any fixed-value bits that happen to be in the data stream (in my case, the fixed bits are used to indicate data byte order).

The "bump" is a flag that continues the transmission. When it is finally 0, the serial output sequence will stop.

THE CODE

The code fragment that accomplishes the transmission is:

```
(a) TransBit =
  (bit)( transmit[ BR_ptr->index ]
    & BR_ptr->mask ) ;
(b) if ( BR_ptr->bump )
  BR_ptr++ ;
```

The program sequence for section (a) looks like this:

```
BR_ptr->index
  -- looks up current index, then used in
transmit[index]
  -- to get byte with desired bit,
     then ANDed with mask
BR_ptr->mask
  -- to get zero/nonzero value, which
(bit)(value & value)
  -- is then cast to a bit for output
TransBit = bit
  -- to port pin, the ultimate goal.
```

The pointer is increased in (b), depending on the value of BR_ptr->bump. As indicated earlier, this is *always* one except in the last structure, so the serial transmission always proceeds to the defined end. The statement:

```
BR_ptr = &BitRef[40] ;
```

in initialization will keep the transmitter off during startup, and:

```
BR_ptr = BitRef ;
```

is used to initiate a transmission sequence.

Bit-Banging Serial Ports

The previous transmitting code compiles, with only a little manual assistance, to:

```
; TransBit = (bit)( transmit[
  BR_ptr->index ] & BR_ptr->mask ) ;
    MOV     DPL,BR_ptr+01H
    MOV     DPH,BR_ptr
    CLR     A
    MOVC    A,@A+DPTR
    ADD     A,#transmit
    MOV     R0,A
    MOV     A,@R0
    MOV     R7,A
    INC     DPTR
    CLR     A
    MOVC    A,@A+DPTR
    ANL     A,R7
    ADD     A,#0FFH
    MOV     TransBit,C
; if ( BR_ptr->bump )
    INC     DPTR
    CLR     A
    MOVC    A,@A+DPTR
    JZ      ?C0011
;     BR_ptr++ ;
    MOV     A,#03H
    ADD     A,BR_ptr+01H
    MOV     BR_ptr+01H,A
    CLR     A
    ADDC    A,BR_ptr
    MOV     BR_ptr,A
?C0011:
```

The assembly language code reveals that the mechanism is pretty efficient. This method is in use in one of my clients' products and has proved effective.

BIT-BANGING WORKS

This bit-banging solution serves to provide serial transmission in an embedded system that has no hardware specifically dedicated to the function. Although alternate and more traditional solutions would have worked, the need for speed encouraged development of a code-pointer-based solution that works fast enough in this case and takes up only two internal RAM bytes for operation. I hope that this presentation will prove to be useful for you.

Mark Gardner is a consultant based in Acton, CA. He has been designing hardware and writing firmware for embedded systems for over 15 years. He has an MS in electronic engineering from the University of Illinois.

For more information, contact:

Philips Semiconductors
811 E. Arques Avenue
P.O. Box 3409
Sunnyvale, CA 94088-3409
(408) 991-3552

I²C-BUS DEVELOPMENT TOOLS FOR ALL SYSTEMS

OM1022

This Philips Semiconductors support tool, called the I²C-analyzer (or in the US, Port MSC) is a PC board that can be connected with a cable to the Centronics printer port via a 25-pin sub-D connector. The I²C has a 4-stake connector for convenient use in the laboratory. There are several flavours to this board, with the latest version supporting multimaster operation. A Philips 8400-series microcontroller executes the low-level I²C tasks on this board, and the Centronics port is used for two-way communications between the PC software and the microcontroller. Control programs for the Philips interface will run on any IBM-compatible PC. The software is mainly intended for interactive control of devices on the I²C-bus. The user can interactively construct, send and receive I²C messages. A database, which comes with the software, contains information about many specific devices, thus making operation is even easier for many Philips devices. The user is prompted to enter control data for the specific registers that are relevant to the device, and the software takes care of the routines by checking the validity of the input data and constructing the correct I²C message. An illustrated description of the internals of the controlled device and its status is available for some devices.

Currently, four programs are supplied with the OM1022 that provide various control options for specific and general purpose I²C devices.

I²C TV	version 3.5
I²C radio	version 2.6
I²C PLL	version 2.3
I²C CELL	version 1.5

The *Users Guide to I²C-bus Control Programs* and *The I²C-bus and how to use it* brochures are also included with each OM1022. The ordering code for the OM1022 is 9339 931 10112.

I²C/ACCESS.bus Monitor MIIC-101

The MIIC-101 is a stand-alone trouble shooting tool for the I²C and ACCESS.bus. When connected to an I²C-bus or ACCESS.bus network, the 101 bus monitor can collect, display or upload information on all bus activity. Its key features are:

- I²C and ACCESS.bus compatible
- operating modes: line status, forward/backward trace, view and remote
- monitoring of all or selected bus addresses
- trace buffer stores up to 2700 messages
- easy to read alphanumeric display (byte, message and buffer scrolling)
- hand-held portable unit (battery, external supply or bus-powered)
- RS-232 port supports remote data capture and uploading.

The MIIC-101 is manufactured by:

Micro Computer Control Corporation
PO Box 275
17 Model Avenue, Hopewell
New Jersey 08525
USA

Tel.+1 609 466 1751
Fax+1 609 466 4116

PF8681 I²C-bus and ACCESS.bus Analysis Support Package

The PF8681 has been designed for use with the PM3580 family of logic analyzers. It provides facilities for analyzing and troubleshooting data streams on the I²C-bus and ACCESS.bus.

Captured data from either bus can be displayed on a logical analyzer screen in various number systems. The PF8681 includes a disassembler for both the I²C-bus and ACCESS.bus. The adapter allows simultaneous measurements in the timing and state domain without any reconnection or multiple probing of the I²C signal lines. This single probing approach avoids additional DC and AC loading of the I²C and ACCESS.bus signal lines.

The I²C-bus disassembler supports all present day features of the I²C-bus system including 10-bit and fast-mode. The ACCESS.bus disassembler supports the BASE-protocol specifications as mentioned in the ACCESS.bus specifications version 2.0.

The PF8681 I²C/ACCESS.bus package includes an adaptor, disassembler and special ACCESS.bus interface cable. Pricing and delivery is available from Fluke.

Calibre ICA-90 plug-in, half length IBM-PC compatible I²C adapter card

This PC card interfaces to the I²C-bus via a 9-pin D-connector. It is based on Philip's PCF8584 I²C-bus controller IC, which can interface the bus at high speeds. Calibre supplies the board with a library of I²C-control routines in both C and Turbo BASIC, which can be retrieved by the user's application software. These routines support both master and slave operation. The software is not interactive (i.e. users must write and compile their own programs) but the interface to the library routines is straightforward, and examples are supplied. They also supply a stand-alone monitor program with the ICA-90. This allows non-intrusive, real-time tracing of I²C-bus activity. Captured data is stored in PC memory and until the buffer is full, when the trace stops and the data is formatted and moved onto a disk file. Data presentation includes occurrences of Start, Stop and Acknowledge conditions. Users can display and analyze the data with any word processor or browsing program. The monitor program requires at least a 6 MHz 286-based PC or faster. This board is recommended for speed-critical or complex I²C-systems (i.e. Multimaster) due to its real-time monitor capability.

You can purchase the ICA-90 from:

Calibre Electronics Ltd.
Cornwall House
Cornwall Terrace
Bradford West Yorkshire
England BD8 7JS

Tel. +44 1274 394125
Fax +44 1274 730960

or

Saelig Co.
1193 Moseley Rd.
Victor
New York 14564
USA

Tel. +1 716 425 3753
Fax +1 716 425 3835

I²C control and analysis tools

AET in Germany supply a variety of I²C-bus and analysis tools, such as:

- PC-RIC RS232 to I²C-bus convertor
- IDB I²C demonstration board for the PC (eight I²C peripherals plus software driver source-code in Pascal, Borland C++ and Microsoft-C)
- MAB I²C 100: an I²C magnetic card reader
- ITM I²C PC monitor and I²C controller (PC plug-in card)
- SIMON I²C PC monitor software for the ITM I²C controller card.

For more information on these products, contact:

ART Automatisierung & Rechnertechnik GmbH
Johann-Kraus Strasse 8a
88662 Uberlingen
Germany

Tel. +49 7551 4056
Fax +49 7551 4058

I²C-BUS EVALUATION BOARDS

OM4151/S87C00KSD

I²C-bus evaluation board with microcontroller, LCD, LED, Par. I/O, SRAM, EEPROM, clock, DTMF generator, AD/DA conversion. This board is available from Philips Semiconductors.

I²C-BUS DEVELOPMENT TOOLS FOR 80C51-BASED SYSTEMS

PDS51

A board-level, full featured, 12 MHz in-circuit emulator, providing complete access to the internal registers and full execution control without consuming chip resources. This means that the microcontroller in the target system can be replaced with the PDS51, enabling the target system to be easily run, monitored and debugged without any changes to code or hardware.

I²C-BUS DEVELOPMENT TOOLS FOR 68000-BASED SYSTEMS

OM4160

Microcore-1 demonstration/evaluation board: SCC68070, 128K EPROM, 512K DRAM, I²C, RS-232C, VSC SCC66470, resident monitor.

OM4160/3

Microcore-3 demonstration/evaluation board: 128K EPROM, 64K SRAM, I²C, RS-232C, 40 I/O (inc. 8051-compatible bus), resident monitor.

OM4160/3QFP

Microcore-3 demonstration/evaluation board for 9XC101 (QFP80 package).

ADDRESSES OF I²C-BUS HARDWARE MANUFACTURES

In Germany:

ART Automatisierung & Rechnertechnik GmbH
Johann-Kraus Strasse 8a
88662 Ueberlingen
Germany

Tel. +49 75514056
Fax +49 75514058

In United Kingdom:

Calibre Electronics Ltd.
Cornwall House
Cornwall Terrace
Bradford West Yorkshire
England BD8 7JS

Tel. +44 1274 394125
Fax +44 1274 730960

In France:

COGEMA
B.P. 1515 - 87020 Limoges CEDEX
France

Tel. +33 55 383184
Fax +33 55 371639

In USA:

Saelig Co.
1193 Moseley Rd.
Victor
New York 14564
USA

Tel. +1 716 425 3753
Fax +1 716 425 3835

Micro Computer Control Corporation
PO Box 275
17 Model Avenue, Hopewell
New Jersey 08525
USA

Tel.+1 609 466 1751
Fax+1 609 466 4116

DEVICE DATA

(in alphanumeric sequence)

I²C bus extender 82B715

DESCRIPTION

The 82B715 is a bipolar integrated circuit intended for application in I²C bus systems.

While retaining all the operating modes and features of the I²C system it permits extension of the practical separation distance between components on the I²C bus by buffering both the data (SDA) and the clock (SCL) lines.

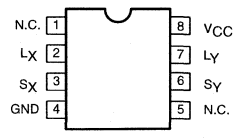
The I²C bus capacitance limit of 400pF restricts practical communication distances to a few meters. Using one 82B715 at each end of longer cables reduces the cable loading capacitance on the I²C bus by a factor of 10 times and may allow the use of low cost general purpose wiring to extend bus lengths.

FEATURES

- Dual, bi-directional, unity voltage gain buffer
- I²C bus compatible
- Logic signal levels may include both supply and ground
- X10 impedance transformation
- Wide supply voltage range

PIN CONFIGURATIONS

8-Pin Dual In-Line or SO
82B715



SU00290

PINNING

PIN	SYMBOL	FUNCTION
1	N.C.	
2	L_X	Buffered Bus, LDA or LCL
3	S_X	I²C Bus, SDA or SCL
4	GND	Negative Supply
5	N.C.	
6	S_Y	I²C Bus, SCL or SDA
7	L_Y	Buffered Bus, LCL or LDA
8	V_{CC}	Positive Supply

QUICK REFERENCE DATA

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN.	TYP.	MAX.	
V_{CC}	Supply voltage	4.5		12	V
I_{CC}	Quiescent current		16		mA
I_{line}	Output sink capability	30			mA
V_{in}	Input voltage range	0		V_{CC}	V
V_{out}	Output voltage range	0		V_{CC}	V
Z_{in}/Z_{out}	Impedance transformation	8	10	13	
T_{amb}	Temperature range	−40		+85	°C

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	DRAWING NUMBER
8-pin plastic dual In-line package	P82B715P N	SOT97-1
8-pin plastic small outline package	P82B715T D	SOT96-1

NOTE:
1. For applications requiring, 3V operation and additional buffer performance, see P82B96 Data Sheet.

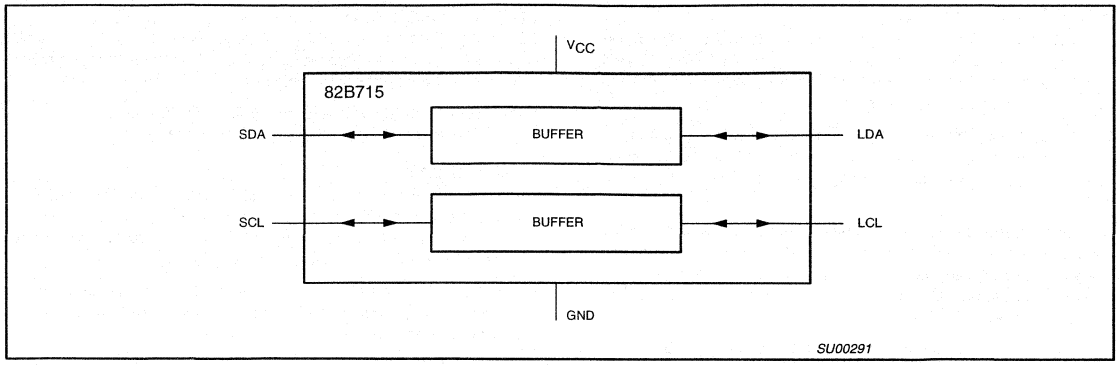


Figure 1. Block Diagram: 82B715

FUNCTIONAL DESCRIPTION

The 82B715 bipolar integrated circuit contains two identical buffer circuits which enable I²C and similar bus systems to be extended over long distances without degradation of system performance or requiring the use of special cables.

The buffer has an effective current gain of ten from I²C bus to Buffered bus. Whatever current is flowing out of the I²C bus side, ten times that current will be flowing into the Buffered bus side (see Figure 2).

As a consequence of this amplification the system is able to drive capacitive loads up to ten times the standard limit on the Buffered bus side. This current based buffering approach preserves the bi-directional, open-collector/open-drain characteristic of the I²C SDA/SCL lines.

To minimize interference and ensure stability, current rise and fall rates are internally controlled.

APPLICATION NOTES

By using two (or more) 82B715 ICs, a sub-system can be built which retains the interface characteristics of an I²C device so that it may be included in, or optionally added to, any I²C or related system.

The sub-system features a low impedance or "Buffered" bus, capable of driving large wiring capacities (see Figure 3).

I²C Systems

As with the standard I²C system, pull-up resistors are required to aprovide the logic HIGH levels on the Buffered bus. (Standard open-collector configuration of the I²C bus). The size and number of these pull-up resistors depends on the system.

If the buffer is to be permanently connected into the system, the circuit should be configured with only one pull-up resistor on the Buffered bus and none on the I²C bus.

Alternatively a buffer may be connected to an existing I²C system. In this case the Buffered bus pull-up will act in parallel with the I²C bus pull-up.

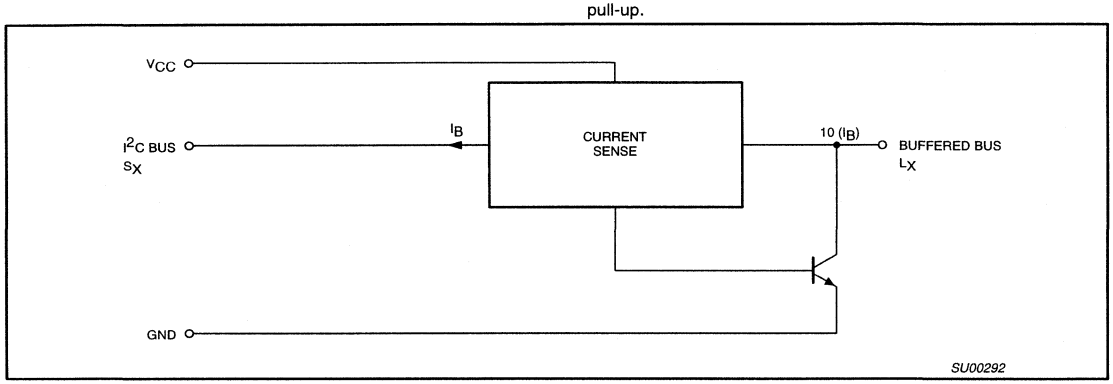


Figure 2. Equivalent Circuit: One Half 82B715

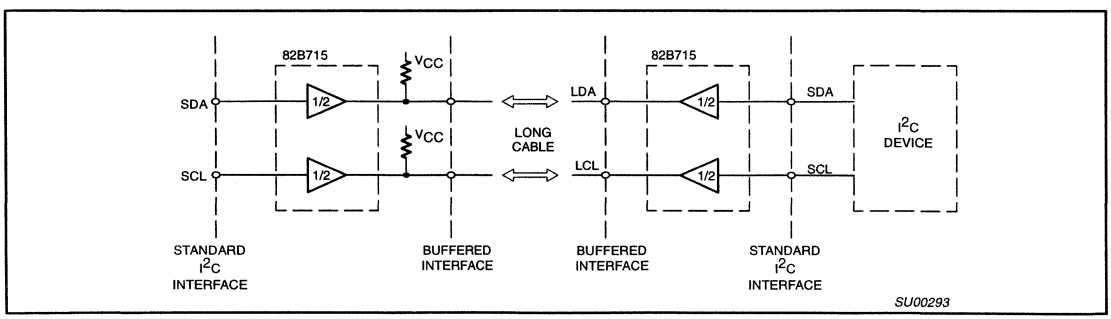


Figure 3. Minimum Sub-System with 82B715

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134).
Voltages with respect to pin GND (DIL-8 pin 4).

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN.	MAX.	
V_{CC} to GND	Supply voltage range V_{CC}	−0.3	+12	V
V_{bus}	Voltage range I²C Bus, SCL or SDA	0	V_{CC}	V
V_{buff}	Voltage range Buffered Bus	0	V_{CC}	V
I	DC current (any pin)		60	mA
P_{tot}	Power dissipation		300	mW
T_{stg}	Storage temperature range	−55	+125	°C
T_{amb}	Operating ambient temperature range	−40	+85	°C

CHARACTERISTICS

At T_{amb} = +25°C and V_{CC} = 5 Volts, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN.	TYP.	MAX.	
Power Supply					
V_{CC}	Supply voltage (operating)	4.5	—	12	V
I_{CC}	Supply current	—	16	—	mA
I_{CC}	Supply current at V_{CC} = 12V	—	22	—	mA
I_{CC}	Supply current, both I²C inputs LOW, both buffered outputs sinking 30mA.	—	28	—	mA
Drive Currents					
I_{Sx}, I_{Sy}	Output sink on I²C bus V_{Sx}, V_{Sy} LOW = 0.4V V_{Lx}, V_{Ly} LOW on Buffered bus = 0.3V	3	—	—	mA
I_{Lx}, I_{Ly}	Output sink on Buffered bus V_{Lx}, V_{Ly} LOW = 0.4V V_{Sx}, V_{Sy} LOW on I²C bus = 0.3V	30	—	—	mA
Input Currents					
I_{Sx}, I_{Sy}	Input current from I²C bus when I_{Lx}, I_{Ly} sink on Buffered bus = 30mA	—	—	3	mA
I_{Lx}, I_{Ly}	Input current from Buffered bus when I_{Sx}, I_{Sy} sink on I²C bus = 3mA	—	—	3	mA
I_{Lx}, I_{Ly}	Leakage current on Buffered bus V_{Lx}, V_{Ly} = V_{CC}, and V_{Sx}, V_{Sy} = V_{CC}	—	—	200	µA
Impedance Transformation					
Z_{in}/Z_{out}	Input/Output impedance	8	10	13	

Pull-Up Resistance Calculation

In calculating the pull-up resistance values, the gain of the buffer introduces scaling factors which must be applied to the system components. Viewing the system from the Buffered bus, all I²C bus capacitances have effectively 10 times their I²C bus value.

In practical systems the pull-up resistance is determined by the rise time limit for I²C systems. As an approximation this limit will be satisfied if the time constant (product of the net resistance and net capacitance) of the total system is set to 1 microsecond.

The total time constant may either be set by considering each bus node individually (i.e., the I²C nodes, and the Buffered bus node) and choosing pull-up resistors to give time constants of 1 microsecond for each node; or by combining the capacitances into an equivalent capacitive loading on the Buffered bus, and calculating the Buffered bus pull-up resistor required by this equivalent capacitance.

For each separate bus the pull-up resistor may be calculated as follows:

$$R = \frac{1\mu sec}{C_{device} + C_{wiring}}$$

Where: C_{device} = sum of device capacitances connected to each bus,

and C_{wiring} = total wiring and stray capacitance on each bus.

If these capacitances are not known then a good approximation is to assume that each device presents 10pF of load capacitance and 10pF of wiring capacitance.

The capacitance figures for one or more individual I²C bus nodes should be multiplied by a factor of 10 times, and then added to the Buffered bus capacitance. Calculation of a new Buffered bus pull-up resistor will alllow this single pull-up resistor to act for both the included I²C bus nodes and the Buffered bus. Thus it is possible to combine some or all of these separate pull-up resistors into a single resistor on the Buffered bus (the value of which is calculated from the sum of the scaled capacitances on the Buffered bus). If the buffer is to be permanently connected into the system then all the separate pull-up resistors should be combined. But if it is to be connected by adding it onto an existing system, then only those on the additional I²C bus system can be combined onto the Buffered bus if the original system is required to be able to still operate on a stand-alone basis.

A further restriction is that the maximum pull-up current, with the bus LOW, should not exceed the I²C bus specification maximum of 3mA, or 30mA on the Buffered bus. The following formula applies:

$$30mA > \frac{V_{CC} - 0.4}{R_P}$$

Where: R_P = scaled parallel combination of all pull-up resistors.

If this condition is met, the fall time specifications will also be met.

Figure 4 shows typical loading calculations for the expanded I²C bus.

Sx, Sy, I²C Bus, SDA or SCL

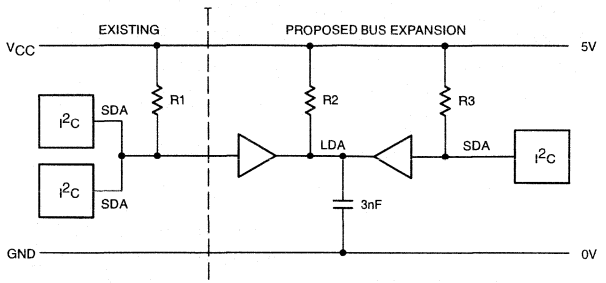
Because the two buffer circuits in the 82B715 are identical either input pin can be used as the I²C Bus SDA data line, or the SCL clock line.

Lx, Ly, Buffered Bus, LDA or LCL

On the buffered low impedance line side, the corresponding output becomes LDA and LCL.

V_{CC}, GND — Positive and Negative Supply Pins

In normal use the power supply voltages at each end of the low impedance line should be comparable. If these differ by a significant amount, noise margin is sacrificed.



EFFECTIVE CAPACITANCE NEAR I²C DEVICES

2 × I²C Devices	20pF
Strays	20pF
82B715 Buffer	10pF
TOTAL CAP.	50pF

I²C pull-up

$$R1 = \frac{1\mu sec}{50pF} = 20K\Omega$$

EFFECTIVE CAPACITANCE BUFFERED LINE

Wiring Cap.	3000pF
TOTAL CAP.	3000pF

Buffered Bus pull-up

$$R2 = \frac{1\mu sec}{3000pF} = 333\Omega$$

EFFECTIVE CAPACITANCE REMOTE I²C DEVICES

1 × I²C Devices	10pF
Strays	10pF
82B715 Buffer	10pF
TOTAL CAP.	30pF

I²C pull-up

$$R3 = \frac{1\mu sec}{30pF} = 33K\Omega$$

AS AN ADDITION TO AN EXISTING SYSTEM * :

R1 = 20KΩ

$$R2' = \frac{R2 \times 0.1R3}{R2 + 0.1R3} = 300\Omega$$

R3 not required since buffer always connected

FOR A PERMANENT SYSTEM * :

R1 not required since buffer always connected

$$R2' = \frac{1}{\frac{1}{0.1R1} + \frac{1}{0.1R2} + \frac{1}{0.1R3}} = 262\Omega$$

R3 not required since buffer always connected

*** NOTE:**
R1, R2 and R3 are calculated from the capacitive loading and a 1μsec time constant on each bus node. For an addition to an existing system, R2' (the new value for R2) is shown as being calculated from the parallel combination of R2 and the scaled value of R3; while for a permanent system R2, and scaled values of R1 and R3 have been used. Note that this example has used scaled resistor values and combined the node and cable capacitances.

CHECK FOR MAXIMUM PULL-UP CURRENT:

$$\frac{(5 - 0.4)V}{260\Omega} = 17.6mA < 30mA$$

SU00294

Figure 4. Typical Loading Calculation: I²C Bus with 82B715

LCD driver for low multiplex rates OM4068

FEATURES

- Single-chip LCD controller/driver
- Static/duplex/triplex drive modes with up to 32/64/96 LCD segments drive capability per device
- Selectable backplane drive configuration: static or 2 or 3 backplane multiplexing
- Selectable display bias configuration drive: static, $\frac{1}{2}$ or $\frac{1}{3}$
- 32 segment drivers
- Serial data input (word length 32 to 96 bits)
- On-chip generation of intermediate LCD bias voltages
- 2 MHz fast serial bus interface
- CMOS compatible
- Compatible with any 4-bit, 8-bit or 16-bit microprocessors/microcontrollers
- May be cascaded for large LCD applications
- Logic supply voltage range ($V_{DD} - V_{SS}$) of 2.5 to 5.5 V
- Display supply voltage range ($V_{LCD} - V_{SS}$) of 3.5 to 6.5 V
- Low power consumption, suitable for battery operated systems
- No external components needed by the oscillator
- Manufactured in silicon gate CMOS process.

APPLICATIONS

- Telecom equipment
- Portable instruments
- Alarm systems
- Automotive equipment.

GENERAL DESCRIPTION

The OM4068 is a low-power CMOS LCD driver, designed to drive Liquid Crystal Displays (LCDs) with low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to three backplanes and up to 32 segment lines and can be easily cascaded for larger LCD applications. All necessary functions for the display are provided in a single chip, including on-chip generation of LCD bias voltages, resulting in a minimum of external components and lower power consumption. A 3-line bus structure enables serial data transfer with most microprocessors/microcontrollers. All inputs are CMOS compatible.

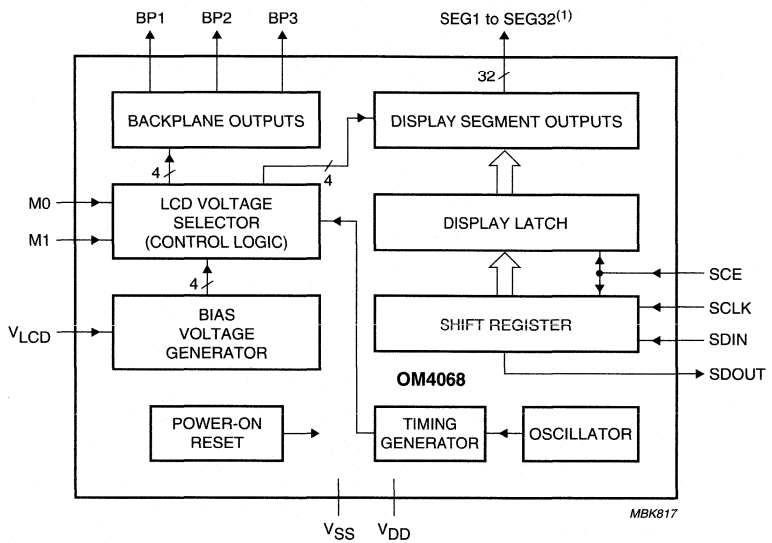
ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
OM4068H[1]	QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2
OM4068P	DIP40	plastic dual in-line package; 40 leads (600 mil)	SOT129-1
OM4068U/5[2]	die	unsawn wafer	–
OM4068U	tray	chip in tray	–

Notes

1. Gull Wing package.
2. For details see Chapter "Bonding pad locations".

BLOCK DIAGRAM



(1) SEG1, SEG6, SEG15 and SEG25 are not available in DIP40 package.

Fig.1 Block diagram.

PINNING

See notes 1 to 8.

SYMBOL	PIN		DESCRIPTION
	QFP44	DIP40	
V_{LCD}	4	19	LCD supply voltage
V_{DD}	5	20	positive supply voltage
V_{SS}	6	21	ground
M0	7	22	drive mode select input 0
M1	8	23	drive mode select input 1
SDIN	9	24	serial bus data input
SCLK	10	25	serial bus clock input
SCE	11	26	serial bus clock enable
SDOUT	12	27	serial bus data output
BP1	13	28	LCD backplane driver output 1
BP2	14	29	LCD backplane driver output 2
BP3	15	30	LCD backplane driver output 3
SEG1	16	–	LCD segment driver output 1
SEG2	17	31	LCD segment driver output 2
SEG3	18	32	LCD segment driver output 3
SEG4	19	33	LCD segment driver output 4
SEG5	20	34	LCD segment driver output 5
SEG6	21	–	LCD segment driver output 6
SEG7	22	35	LCD segment driver output 7
SEG8	23	36	LCD segment driver output 8
SEG9	24	37	LCD segment driver output 9
SEG10	25	38	LCD segment driver output 10
SEG11	26	39	LCD segment driver output 11
SEG12	27	40	LCD segment driver output 12
SEG13	28	1	LCD segment driver output 13
SEG14	29	2	LCD segment driver output 14
SEG15	30	–	LCD segment driver output 15
SEG16	31	3	LCD segment driver output 16
SEG17	32	4	LCD segment driver output 17
SEG18	33	5	LCD segment driver output 18
SEG19	34	6	LCD segment driver output 19
SEG20	35	7	LCD segment driver output 20
SEG21	36	8	LCD segment driver output 21
SEG22	37	9	LCD segment driver output 22
SEG23	38	10	LCD segment driver output 23
SEG24	39	11	LCD segment driver output 24
SEG25	40	–	LCD segment driver output 25
SEG26	41	12	LCD segment driver output 26

SYMBOL	PIN		DESCRIPTION
	QFP44	DIP40	
SEG27	42	13	LCD segment driver output 27
SEG28	43	14	LCD segment driver output 28
SEG29	44	15	LCD segment driver output 29
SEG30	1	16	LCD segment driver output 30
SEG31	2	17	LCD segment driver output 31
SEG32	3	18	LCD segment driver output 32

Notes

1. SEG1 to SEG32 (LCD segment driver outputs) output the multi-level signals for the LCD segments.
2. BP0, BP1 and BP2 (LCD backplane driver outputs) output the multi-level signals for the LCD backplanes.
3. V_{LCD} (LCD power supply): power supply for the LCD.
4. SDIN (serial data line): input for the bus data line.
5. SCL (serial clock line): input for the bus clock line.
6. SDOUT (serial data output): output of the shift register to allow serial cascading of the OM4068 with other devices.
7. SCE (serial clock enable): input for enable/disable acquisition on the data input line. If disabled, data on the serial bus are not accepted by the device.
8. M0 and M1 (display mode select inputs): inputs to select the LCD drive configurations; static, duplex or triplex.

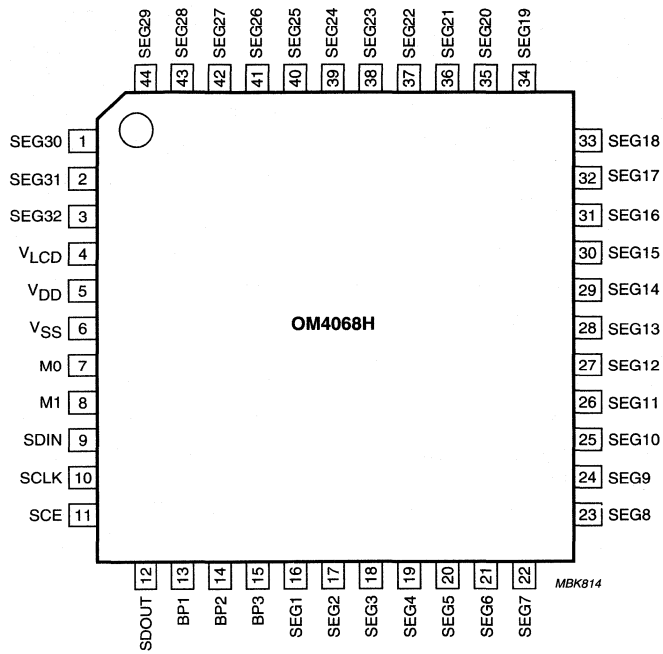


Fig.2 Pin configuration (QFP44).

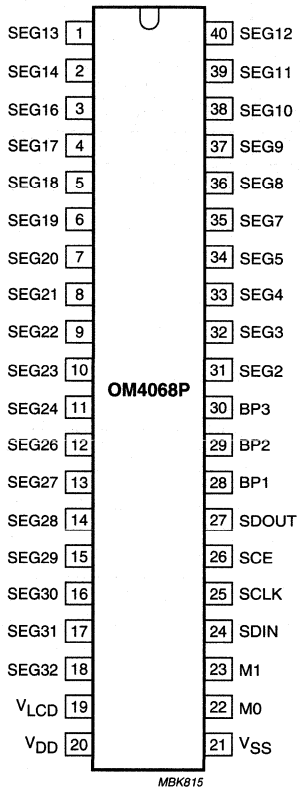


Fig.3 Pin configuration (DIP40).

FUNCTIONAL DESCRIPTION

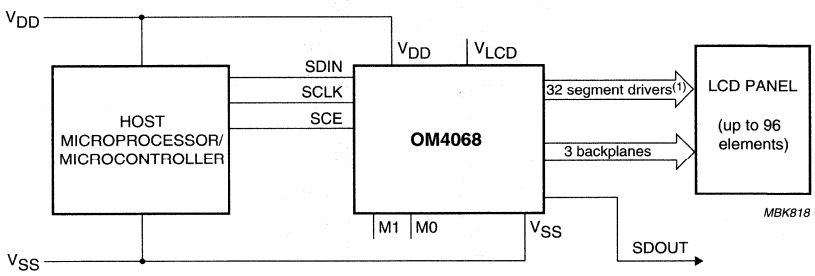
The OM4068 is a low-power LCD driver designed to interface with any microprocessor/microcontroller and a wide variety of LCDs. It can drive any static or multiplexed LCD containing up to three backplanes and up to 96 segments.

The display configurations possible with the OM4068 depend on the number of active backplane outputs required; a selection of display configurations is given in Table 1.

A typical system (MUX 1 : 3) is shown in Fig.4.

Table 1 Selection of display configurations

NUMBER OF		7-SEGMENTS NUMERIC		DOT MATRIX
BACKPLANES	DISPLAY SEGMENTS	DIGITS	INDICATOR SYMBOLS	
3	96	12	12	96 dots (3 × 32)
2	64	8	8	64 dots (2 × 32)
1	32	4	4	32 dots (1 × 32)



(1) 28 segment drivers for DIP40 package.

Fig.4 Typical system configuration.

The host microprocessor/microcontroller maintains the 3-line bus communication channel with OM4068. The internal oscillator requires no external components. The appropriate intermediate biasing voltage for the multiplexed LCD waveforms are generated on-chip.

The only other connections required to complete the system are to the power supplies (V_{SS}, V_{DD} and V_{LCD}) and suitable capacitors to decouple the V_{LCD} and V_{DD} pins to V_{SS}.

Power-on reset

The on-chip power-on reset block initializes the chip after power-on or power failures. The OM4068 resets to a starting condition as follows:

- All backplane and segment outputs are set to V_{SS} (display off)
- All shift registers and latches are set in 3-state
- SDOUT (allowing serial cascading) is set to logic 0 (with SCE LOW)
- Power-down mode.

Data transfers on the serial bus should be avoided for 0.5 ms following power-on to allow completion of the reset action.

Power-down

After power-on the chip is in power-down mode as long as the serial clock is not active. During power-down all static currents are switched off (no internal oscillator, no timing and no bias level generation) and all LCD-outputs are 3-stated. The power-on reset functions remain enabled.

The power-down mode is disabled at the first rising edge of the serial clock SCLK.

LCD bias voltage generator

The intermediate bias voltages for the LCD display are generated on-chip. This removes the need for an external resistive bias chain and significantly reduces the system power consumption. The full-scale LCD voltage V_{OP} equals $V_{LCD} - V_{SS}$. The optimum value of V_{OP} depends on the LCD threshold voltage (V_{th}) and the number of bias levels.

Fractional LCD biasing voltages are obtained from an internal voltage divider of three series resistors ($\frac{1}{3}$bias) connected between V_{LCD} and V_{SS}. The centre resistor can be switched out of the circuit to provide a $\frac{1}{2}$bias voltage level for the 1 : 2 multiplex configuration.

The bias levels depend on the multiplex rate and are selected automatically when the display configuration is selected using M1 and M0.

LCD voltage selector

The LCD voltage selector (control logic) coordinates the multiplexing of the LCD in accordance with the selected drive or display configuration. The operation of the voltage selector is controlled by the input pins M0 and M1 (see Table 2).

Table 2 Drive mode selection

M1	M0	DRIVE MODE
0	0	test mode (not user accessible)
0	1	static drive (1 : 1)
1	0	duplex drive (1 : 2)
1	1	triplex drive (1 : 3)

For multiplex rates of 1 : 2 three bias levels are used including V_{LCD} and V_{SS}. Four bias level are used for the 1 : 3 multiplex rate. The various biasing configurations together with the biasing characteristics as functions of $V_{OP} = V_{LCD} - V_{SS}$ and the resulting discrimination ratios (D), are given in Table 3.

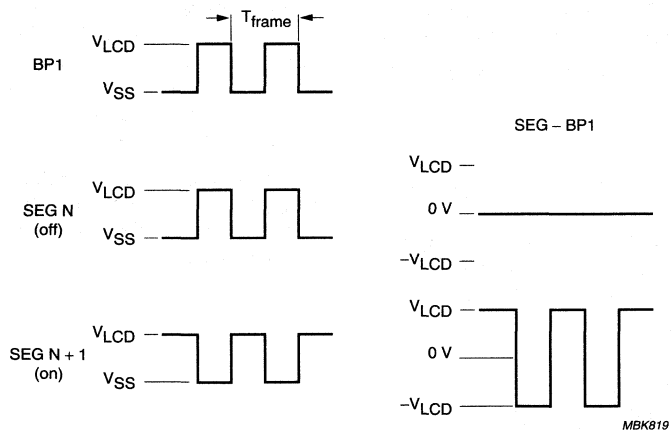
A practical value for V_{OP} is determinated by equating $V_{off(rms)}$ with a defined LCD threshold voltage (V_{th}), typically when the LCD exhibits approximately 10% contrast. In static mode a suitable choice is $V_{OP} > 3V_{th}$.

Table 3 LCD drive modes: summary of characteristics

LCD DRIVE MODE	NUMBER OF		LCD BIAS CONFIGURATION	$\frac{V_{off(rms)}}{V_{OP}}$	$\frac{V_{on(rms)}}{V_{OP}}$	$D = \frac{V_{on(rms)}}{V_{off(rms)}}$
	BACKPLANES	LEVELS				
Static	1	2	static	0	1	–
1 : 2	2	3	½	0.354	0.791	2.2236
1 : 3	3	4	⅓	0.333	0.638	1.915

LCD drive mode waveforms

The static LCD drive mode is used when a single backplane is provided in the LCD. Backplane and segment drive waveforms for this mode are shown in Fig.5.

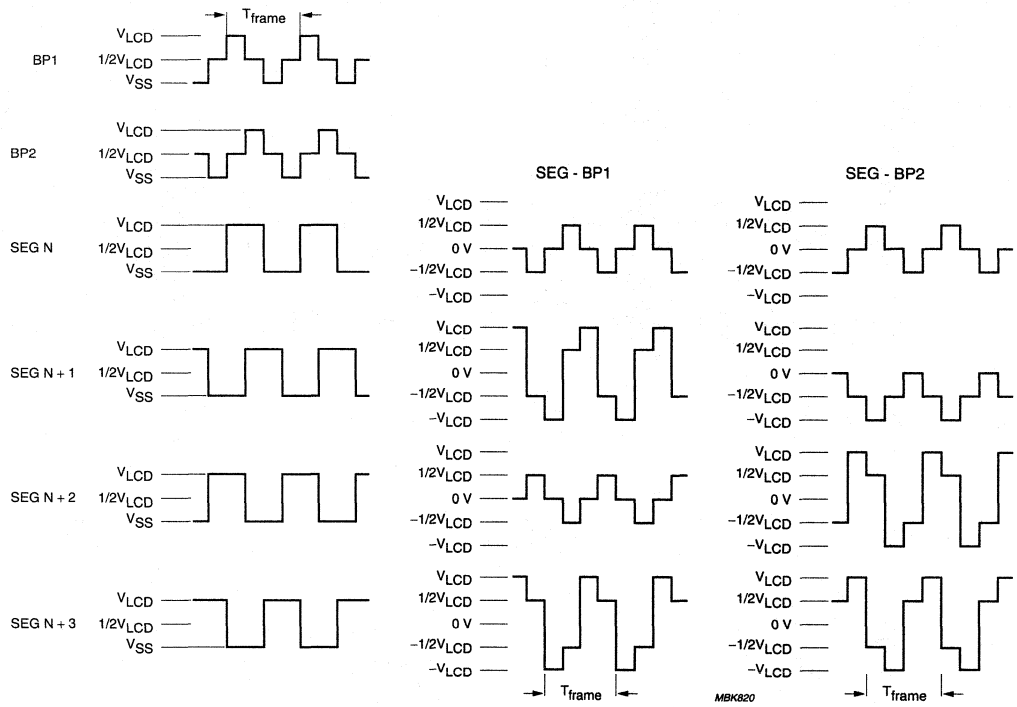


BACKPLANE DRIVER OUTPUT	SEGMENTS	
	SEG N	SEG N + 1
BP1	off	on

Fig.5 Static drive mode waveforms ($V_{OP} = V_{LCD} - V_{SS}$).

1 : 2 MULTIPLEX DRIVE MODE

When two backplanes are provided in the LCD, the 1 : 2 multiplex mode applies, as shown in Fig.6.

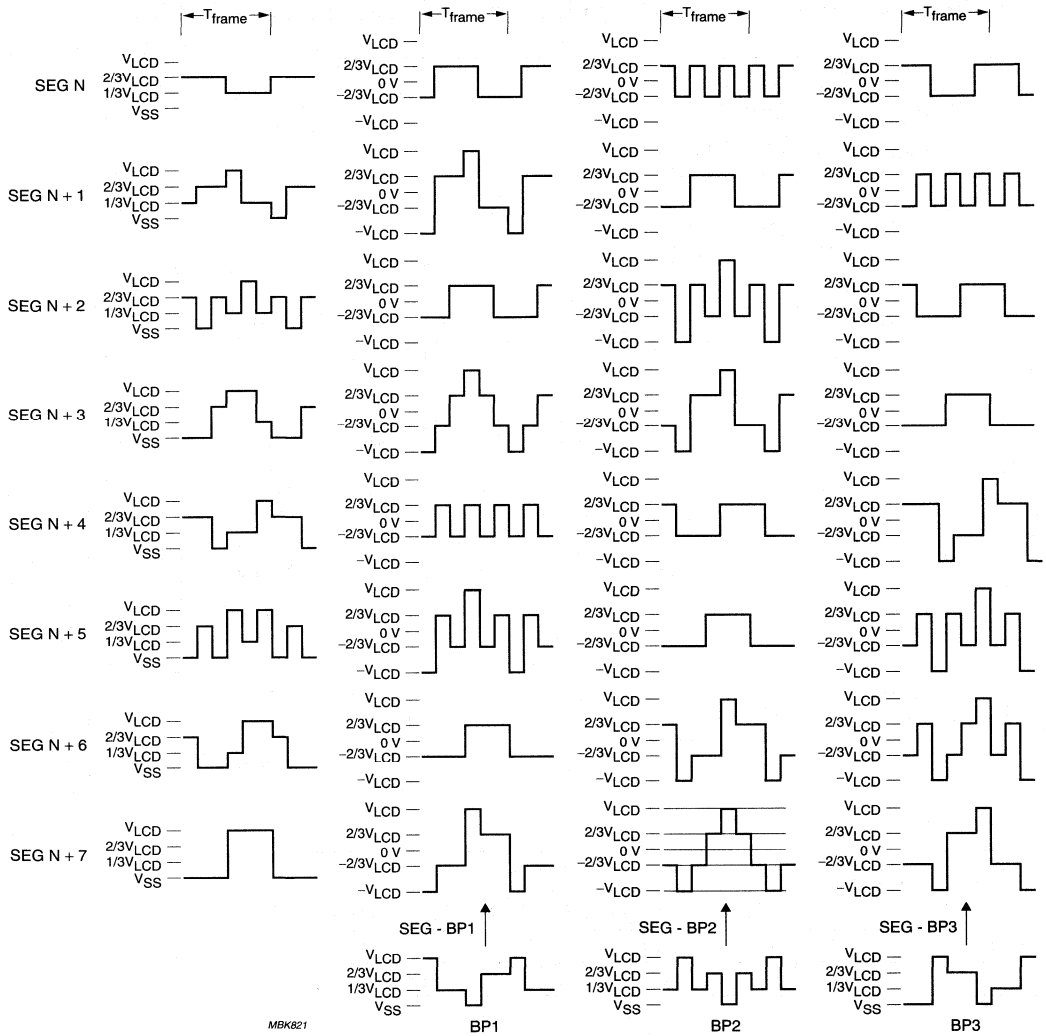


BACKPLANE DRIVER OUTPUTS	SEGMENTS			
	SEG N	SEG N + 1	SEG N + 2	SEG N + 3
BP1	off	on	off	on
BP2	off	off	on	on

Fig.6 Waveforms for 1 : 2 multiplex drive mode ($V_{OP} = V_{LCD} - V_{SS}$).

1 : 3 MULTIPLEX DRIVE MODE

When three backplanes are provided in the LCD, the 1 : 3 multiplex mode applies, as shown in Fig.7.



BACKPLANE DRIVER OUTPUTS	SEGMENTS							
	N	N + 1	N + 2	N + 3	N + 4	N + 5	N + 6	N + 7
BP1	off	on	off	on	off	on	off	on
BP2	off	off	on	on	off	off	on	on
BP3	off	off	off	off	on	on	on	on

Fig.7 Waveforms for 1 : 3 multiplex drive motive ($V_{OP} = V_{LCD} - V_{SS}$).

Oscillator

The internal logic and the multi-level LCD drive signals of the OM4068 are generated by the built-in RC oscillator. No external components are required.

In order to minimize radio frequency interference, the oscillator operates with symmetrical and slew-rate limited capacitor charge/discharge.

The oscillator runs continuously once the power down state after power-on has been left.

Interface to microprocessor unit: serial interface

A three-line bus structure enables serial unidirectional data transfer with microprocessors/microcontrollers. The three lines are a serial data input line (SDIN), a serial clock line (SCLK) and a data line enable (SCE). All inputs are CMOS compatible. These lines must always be in a defined state V_{SS} or V_{DD}. Floating inputs could damage the chip.

On the bus, one data bit is transferred during each clock pulse. The data on the SDIN line remains stable during the whole clock period. Data changes arrive with the falling edge of the serial clock SCLK (see Fig.8).

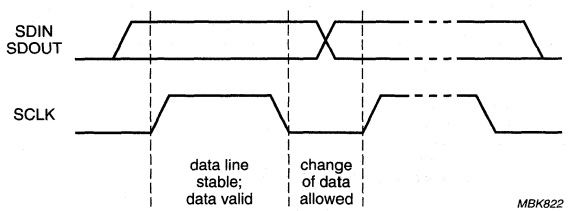


Fig.8 Bit transfer on bus.

Shift register

Data present on the SDIN pin is shifted into a shift register with the rising edge of the serial clock SCLK in a synchronous manner. The shift register serves to transfer display information from the serial bus to the (display) latch while previous data is displayed.

The shift register is organized as three 32-bit shift registers. Depending on the display driving mode selected (see Table 3), one, two or three registers are used and cascaded resulting in a shift register length of 32, 64 or 96 bits. Figure 9 shows the shift register organization with the display data bits after a shift operation is completed. The shift sequence begins with data bit D32 and finishes with data bit D1. The correspondence between the data bit numbers and the LCD display segments is shown in Table 4.

Data from the last stage of the register is supplied to the SDOUT pin to allow serial cascading of the OM4068 with other peripheral devices. Depending on the display driving mode selected, SDOUT corresponds to bit 32, 64 or 96 of the register (see Fig.10). Data on the SDOUT pin is shifted out with the falling edge of the SCLK clock. SDOUT is therefore delayed by ½SCLK cycle before it is applied to the SDIN pin of the next IC in the serial chain (see Fig.8).

The clock enable SCE signal must be HIGH in order to enable the shift operation. SDOUT output is latched with the last data after SCE returned to HIGH (shift operation terminated).

SDOUT is in 3-state mode when SCE is LOW.

Display latch

The 96-bit display latch holds the display data while the corresponding multiplex signals are generated. There is a one-to-one relationship between the data in the display latch and the LCD segment outputs. An LCD segment is activated when the corresponding data bit in the display latch is HIGH.

Display latches are in HOLD mode (SCE HIGH) during the shift operation to maintain the display data constant.

Data are latched into the display latch with the internal frame clock. Thus there is a delay of up to one half frame before new data are latched after signal SCE returns to zero.

Timing

The timing of the OM4068 organizes the internal data flow of the device. This includes the transfer of display data from the shift register to the display segments outputs. The timing also generates the LCD frame frequency which is derived from the clock frequency generated in the internal clock generator:

$$f_{fr(LCD)} = \frac{f_{osc}}{2400}$$

Shift register configuration

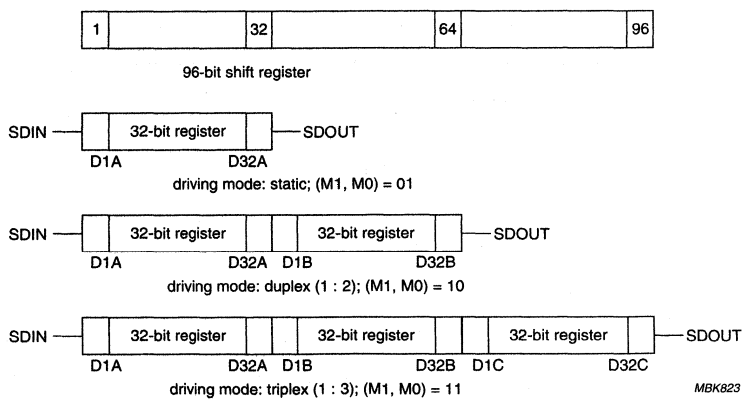


Fig.9 Display data bit position in shift register.

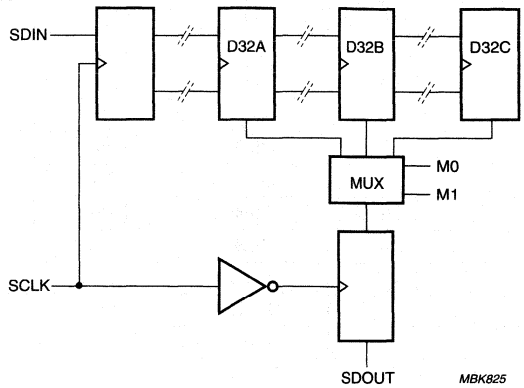


Fig.10 Shift register structure.

Table 4 Relationships between data bit numbers and the LCD segment outputs

SEGMENT NUMBER	DRIVING MODE					
	STATIC	DUPLEX		TRIPLEX		
SEG1	D1A	D1A	D1B	D1A	D1B	D1C
SEG2	D2A	D2A	D2B	D2A	D2B	D2C
SEG3	D3A	D3A	D3B	D3A	D3B	D3C
SEG4	D4A	D4A	D4B	D4A	D4B	D4C
SEG5	D5A	D5A	D5B	D5A	D5B	D5C
SEG6	D6A	D6A	D6B	D6A	D6B	D6C
SEG7	D7A	D7A	D7B	D7A	D7B	D7C
SEG8	D8A	D8A	D8B	D8A	D8B	D8C
SEG9	D9A	D9A	D9B	D9A	D9B	D9C
SEG10	D10A	D10A	D10B	D10A	D10B	D10C
SEG11	D11A	D11A	D11B	D11A	D11B	D11C
SEG12	D12A	D12A	D12B	D12A	D12B	D12C
SEG13	D13A	D13A	D13B	D13A	D13B	D13C
SEG14	D14A	D14A	D14B	D14A	D14B	D14C
SEG15	D15A	D15A	D15B	D15A	D15B	D15C
SEG16	D16A	D16A	D16B	D16A	D16B	D16C
SEG17	D17A	D17A	D17B	D17A	D17B	D17C
SEG18	D18A	D18A	D18B	D18A	D18B	D18C
SEG19	D19A	D19A	D19B	D19A	D19B	D19C
SEG20	D20A	D20A	D20B	D20A	D20B	D20C
SEG21	D21A	D21A	D21B	D21A	D21B	D21C
SEG22	D22A	D22A	D22B	D22A	D22B	D22C
SEG23	D23A	D23A	D23B	D23A	D23B	D23C
SEG24	D24A	D24A	D24B	D24A	D24B	D24C
SEG25	D25A	D25A	D25B	D25A	D25B	D25C
SEG26	D26A	D26A	D26B	D26A	D26B	D26C
SEG27	D27A	D27A	D27B	D27A	D27B	D27C
SEG28	D28A	D28A	D28B	D28A	D28B	D28C
SEG29	D29A	D29A	D29B	D29A	D29B	D29C
SEG30	D30A	D30A	D30B	D30A	D30B	D30C
SEG31	D31A	D31A	D31B	D31A	D31B	D31C
SEG32	D32A	D32A	D32B	D32A	D32B	D32C

Segment outputs

The LCD drive section includes 32 segment outputs SEG1 to SEG32 which should be connected directly to the LCD. The segment output signals are generated in accordance with the multiplex backplane signals and with data in the display latch. When less than 32 segments are required the unused segment outputs should be left open-circuit.

Backplane outputs

The LCD drive section includes three backplane outputs (BP1 to BP3) which should be connected directly to the LCD. The backplane output signals are generated in accordance with the selected LCD drive mode. If less than three backplane outputs are required the unused outputs should be left open-circuit. In 1 : 2 multiplex drive mode, BP3 is set to $\frac{1}{2}V_{LCD}$. In static drive mode BP3 and BP2 are set to V_{SS}.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		−0.5	+6.5	V
V_{LCD}	LCD supply voltage		−0.5	+7.5	V
V_I	input voltage (any input)		−0.5	V_{DD} + 0.5	V
V_O	output voltage (BP1, BP2, BP3, S1 to S32 and V_{LCD})		−0.5	V_{LCD} + 0.5	V
I_I	DC input current		−10	+10	mA
I_O	DC output current		−10	+10	mA
I_{DD}, I_{SS}, I_{LCD}	V_{DD}, V_{SS} or V_{LCD} current		−50	+50	mA
$P_{tot(pack)}$	total power dissipation per package		−	500	mW
P/out	power dissipation per output		−	10	mW
T_{amb}	operating ambient temperature		−40	+105	°C
T_{stg}	storage temperature		−65	+150	°C
T_j	junction temperature		−	150	°C
V_{es}	electrostatic handling	note 1	−2000	+2000	V
		note 2	−150	+150	V

Notes

1. Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ series resistor (human body model).
2. Equivalent to discharging a 200 pF capacitor via a 0.75 μH series inductor (machine model).

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see *"Handling MOS Devices"*).

DC CHARACTERISTICS

V_{DD} = 2.5 to 5.5 V; V_{SS} = 0 V; V_{LCD} = 3.5 to 6.5 V; T_{amb} = −40 to +105 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage		V_{SS} + 2.5	–	5.5	V
V_{LCD}	LCD supply voltage		V_{SS} + 3.5	–	6.5	V
I_{DD}	supply current	power-down state; note 1	–	4	10	μA
		normal mode; f_{osc} = intern; notes 2 and 3	–	12	25	μA
I_{LCD}	V_{LCD} current	power-down state; note 1	–	–	1.5	μA
		normal mode; f_{osc} = intern; notes 3 and 4	–	–	40	μA
V_{POR}	power-on reset voltage level	note 5	0.8	1.25	1.6	V
Logic						
V_{IL}	LOW-level input voltage		V_{SS}	–	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	–	V_{DD}	V
I_{OL}	LOW-level output current (SDOUT)	V_{OL} = 0.5 V; V_{DD} = 5 V	1.0	–	–	mA
I_{OH}	HIGH-level output current (SDOUT)	$V_{OH} = V_{DD} - 0.5$ V; V_{DD} = 5 V	–	–	−1	mA
I_{pu}	pull-up current M1 and M0	$V_I = V_{SS}$	0.04	0.15	1	μA
I_L	leakage current	$V_I = V_{DD}$ or V_{SS}	−1	–	+1	μA
Segment and backplane outputs						
$R_{(o)seg}$	segment output resistance SEG1 to SEG32	note 6	–	15	40	kΩ
$R_{(o)back}$	backplane output resistance BP1 to BP3	note 6	–	15	40	kΩ
$V_{seg(bias)(tol)}$	bias tolerance SEG1 to SEG32	note 7	−100	0	+100	mV
$V_{back(bias)(tol)}$	bias tolerance BP1, BP2 and BP3	note 7	−100	0	+100	mV

Notes

1. Power-down state. After power-on the chip is in power-down state as long as the serial clock is not activated. During power-down all static currents are switched off except the power-on reset block.
2. Output SDOUT is open-circuit; inputs at V_{DD} or V_{SS}; bus inactive.
3. Drive mode: static, duplex and triplex.
4. LCD outputs are open-circuit, C_L = 50 pF typical, inputs at V_{DD} or V_{SS}; bus inactive.
5. Resets all logic when $V_{DD} < V_{POR}$.
6. Resistance of output terminal (S1 to S32 and BP1, BP2 and BP3) with a load current of 20 μA; outputs measured one at a time.
7. LCD outputs open-circuits.

AC CHARACTERISTICS

V_{DD} = 2.5 to 5.5 V; V_{SS} = 0 V; V_{LCD} = 5.0 V; T_{amb} = −40 to +105 °C; unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
$f_{fr(LCD)}$	LCD frame frequency (internal clock)	50	84	175	Hz
f_{osc}	oscillator frequency (not available at any pin)	116	224	405	kHz
Bus timing characteristics: serial bus interface; note 1					
f_{SCLK}	SCLK clock frequency	0	–	2.1	MHz
t_{SCLKL}	SCLK clock LOW period	190	–	–	ns
t_{SCLKH}	SCLK clock HIGH period	190	–	–	ns
$t_{su(D)}$	data set-up time	100	–	–	ns
$t_{h(D)}$	data hold time	100	–	–	ns
t_r	SCLK, SDIN rise time	–	10	–	ns
t_f	SCLK, SDIN fall time	–	10	–	ns
$t_{su(en)(SDEH-SCLKH)}$	enable set-up time (SDE HIGH to SCLK HIGH)	250	–	–	ns
$t_{su(dis)(SCLKL-SDEL)}$	disable set-up time (SCLK LOW to SDE LOW)	250	–	–	ns
$t_{PHL(SDOUT)}$	SDOUT HIGH-to-LOW propagation delay	100	–	–	ns

Note

1. All timing values are valid within the operating supply voltage and ambient temperature range and are referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

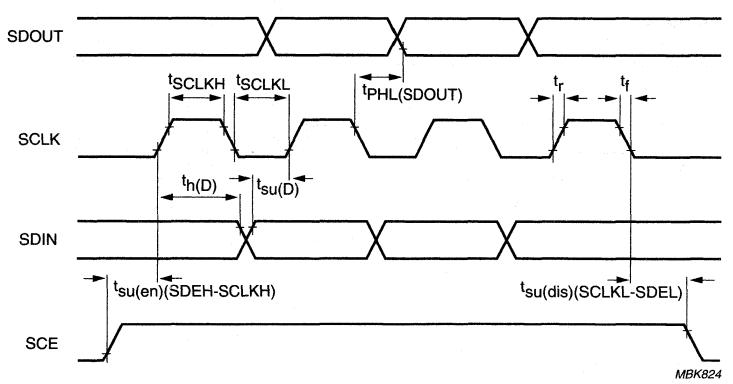
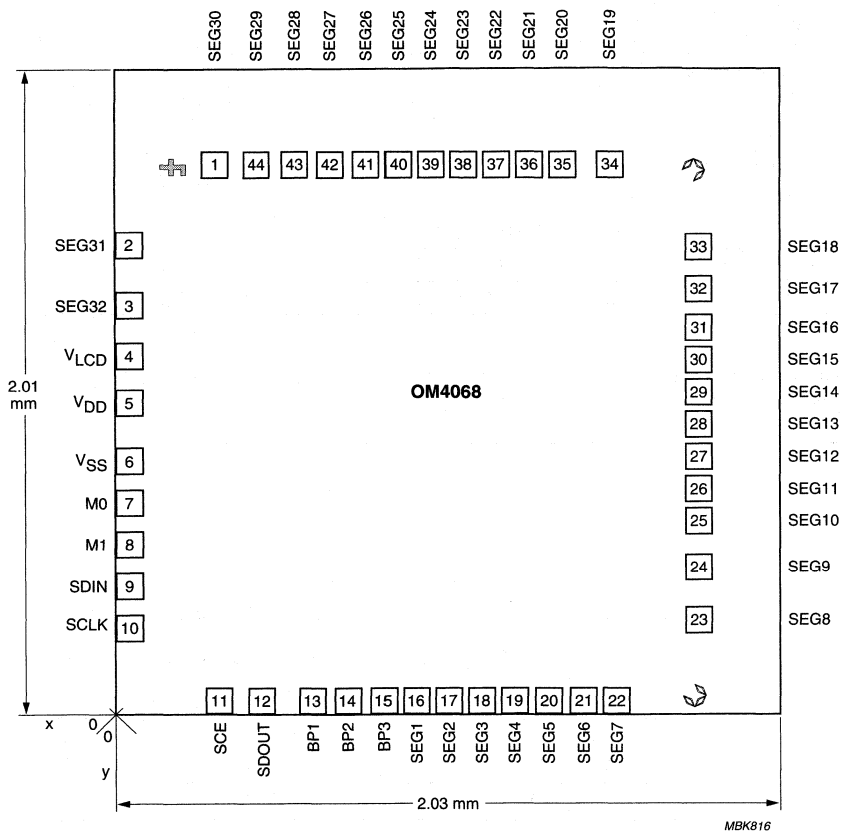


Fig.11 Serial data timing.

BONDING PAD LOCATIONS



Dimensions in mm.
Bonding pad dimensions: 80 × 80 µm.

Fig.12 Bonding pad locations.

Table 5 Bonding pad locations (dimensions in μm). All x/y coordinates are referenced to bottom left corner of chip (see Fig.12).

SYMBOL	PAD	x	y
V_{DD}	5	43.100	970.500
V_{SS}	6	42.900	791.850
M0	7	43.100	661.750
M1	8	43.100	531.750
SDIN	9	43.100	401.750
SCLK	10	43.100	271.750
SCE	11	310.450	43.100
SDOUT	12	447.350	43.100
BP1	13	604.800	43.100
BP2	14	714.850	43.100
BP3	15	824.850	43.100
SEG1	16	924.850	43.100
SEG2	17	1024.850	43.100
SEG3	18	1124.850	43.100
SEG4	19	1224.850	43.100
SEG5	20	1327.250	43.100
SEG6	21	1432.450	43.100
SEG7	22	1532.650	43.100
SEG8	23	1783.600	293.850
SEG9	24	1783.600	458.850
SEG10	25	1783.600	603.850
SEG11	26	1783.600	703.850
SEG12	27	1783.600	803.850
SEG13	28	1783.600	903.850
SEG14	29	1783.600	1003.850
SEG15	30	1783.600	1103.850
SEG16	31	1783.600	1203.850
SEG17	32	1783.600	1323.850
SEG18	33	1783.600	1453.850
SEG19	34	1514.600	1711.100
SEG20	35	1370.550	1711.100
SEG21	36	1270.500	1711.100
SEG22	37	1170.500	1711.100
SEG23	38	1070.500	1711.100
SEG24	39	970.550	1711.100
SEG25	40	870.550	1711.100
SEG26	41	770.550	1711.100
SEG27	42	660.550	1711.100
SEG28	43	550.550	1711.100
SEG29	44	430.550	1711.100
SEG30	1	300.550	1711.100
SEG31	2	43.100	1460.050
SEG32	3	43.100	1274.950
V_{LCD}	4	43.100	1158.700
Alignment marks			
C1	–	1769.6	1696.9
C2	–	1770.1	58.4
F	–	172.0	1705.2

Universal LCD driver for low multiplex rates OM4085

FEATURES

- Single-chip LCD controller/driver
- Selectable backplane drive configuration: static or 2, 3 or 4 backplane multiplexing
- Selectable display bias configuration: static, $\frac{1}{2}$ or $\frac{1}{3}$
- Internal LCD bias generation with voltage-follower buffers
- 24 segment drives: up to twelve 8-segment numeric characters; up to six 15-segment alphanumeric characters; or any graphics of up to 96 elements
- 24 × 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- LCD and logic supplies may be separated
- 2.0 to 6 V power supply range
- Low power consumption
- Power saving mode for extremely low power consumption in battery-operated and telephone applications
- I²C-bus interface
- TTL/CMOS compatible
- Compatible with any 4-bit, 8-bit or 16-bit microprocessors/microcontrollers
- May be cascaded for large LCD applications (up to 1536 segments possible)
- Cascadable with the 40 segment LCD driver PCF8576C
- Optimized pinning for single plane wiring in both single and multiple OM4085 applications
- Space-saving 40 lead plastic very small outline package (VSO40; SOT158-1)
- No external components required (even in multiple device applications)
- Manufactured in silicon gate CMOS process.

GENERAL DESCRIPTION

The OM4085 is a peripheral device which interfaces to almost any Liquid Crystal Display (LCD) having low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 24 segments and can easily be cascaded for larger LCD applications. The OM4085 is compatible with most microprocessors/microcontrollers and communicates via a two-line bidirectional I²C-bus. Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
OM4085T	VSO40	plastic very small outline package; 40 leads	SOT158-1

BLOCK DIAGRAM

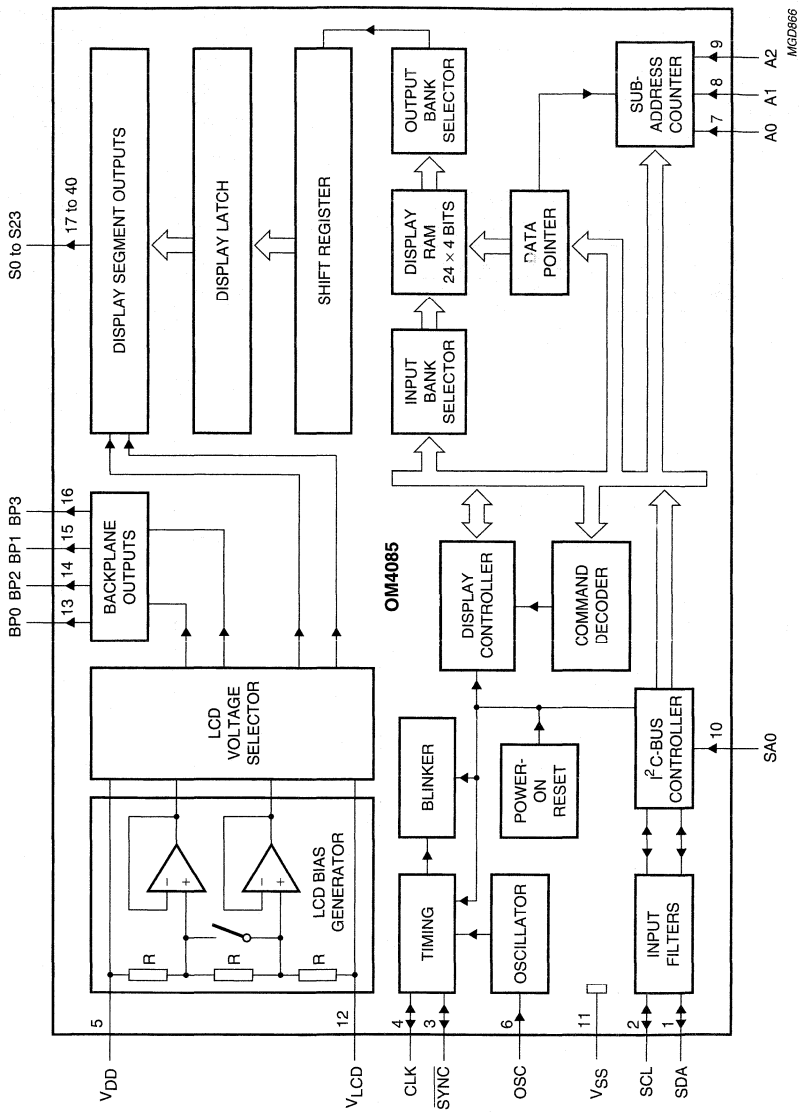


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
SDA	1	I²C-bus data input/output
SCL	2	I²C-bus clock input/output
$\overline{SYNC}$	3	cascade synchronization input/output
CLK	4	external clock input/output
V_{DD}	5	positive supply voltage
OSC	6	oscillator input
A0	7	I²C-bus subaddress inputs
A1	8	
A2	9	
SA0	10	I²C-bus slave address bit 0 input
V_{SS}	11	logic ground
V_{LCD}	12	LCD supply voltage
BP0	13	LCD backplane outputs
BP2	14	
BP1	15	
BP3	16	
S0 to S23	17 to 40	LCD segment outputs

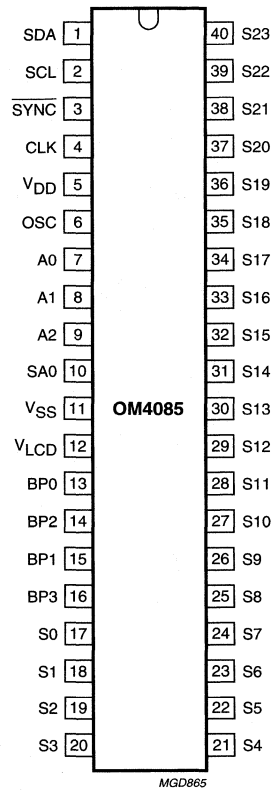


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The OM4085 is a versatile peripheral device designed to interface any microprocessor to a wide variety of LCDs. It can directly drive any static or multiplexed LCD containing up to 4 backplanes and up to 24 segments. The display configurations possible with the OM4085 depend on the number of active backplane outputs required; a selection of display configurations is given in Table 1.

All of the display configurations given in Table 1 can be implemented in the typical system shown in Fig.3. The host microprocessor/microcontroller maintains the two-line I^2C-bus communication channel with the OM4085. The internal oscillator is selected by tying OSC (pin 6) to V_{SS}. The appropriate biasing voltages for the multiplexed LCD waveforms are generated internally. The only other connections required to complete the system are to the power supplies (V_{DD}, V_{SS} and V_{LCD}) and to the LCD panel chosen for the application.

Table 1 Selection of display configurations

ACTIVE BACKPLANE OUTPUTS	NUMBER OF SEGMENTS	7-SEGMENT NUMERIC	14-SEGMENT ALPHANUMERIC	DOT MATRIX
4	96	12 digits + 12 indicator symbols	6 characters + 12 indicator symbols	96 dots (4 × 24)
3	72	9 digits + 9 indicator symbols	4 characters + 16 indicator symbols	72 dots (3 × 24)
2	48	6 digits + 6 indicator symbols	3 characters + 6 indicator symbols	48 dots (2 × 24)
1	24	3 digits + 3 indicator symbols	1 character + 10 indicator symbols	24 dots

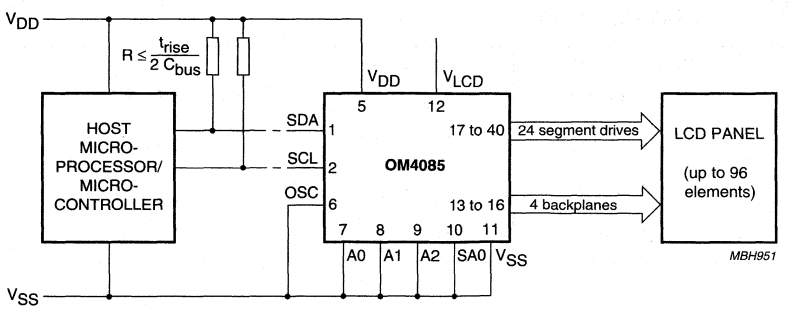


Fig.3 Typical system configuration.

Power-on reset

At power-on the OM4085 resets to a defined starting condition as follows:

1. All backplane outputs are set to V_{DD}
2. All segment outputs are set to V_{DD}
3. The drive mode '1 : 4 multiplex with ⅓bias' is selected
4. Blinking is switched off
5. Input and output bank selectors are reset (as defined in Table 5)
6. The I²C-bus interface is initialized
7. The data pointer and the subaddress counter are cleared.

Data transfers on the I²C-bus should be avoided for 1 ms following power-on to allow completion of the reset action.

LCD bias generator

The full-scale LCD voltage (V_{op}) is obtained from $V_{DD} - V_{LCD}$. The LCD voltage may be temperature compensated externally through the V_{LCD} supply to pin 12. Fractional LCD biasing voltages are obtained from an internal voltage divider of three series resistors connected between V_{DD} and V_{LCD}. The centre resistor can be switched out of circuit to provide a ½bias voltage level for the 1 : 2 multiplex configuration.

LCD voltage selector

The LCD voltage selector coordinates the multiplexing of the LCD according to the selected LCD drive configuration. The operation of the voltage selector is controlled by MODE SET commands from the command decoder. The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of $V_{op} = V_{DD} - V_{LCD}$ and the resulting discrimination ratios (D), are given in Table 2.

A practical value of V_{op} is determined by equating $V_{off(rms)}$ with a defined LCD threshold voltage (V_{th}), typically when the LCD exhibits approximately 10% contrast. In the static drive mode a suitable choice is $V_{op} \geq 3\ V_{th}$. Multiplex drive ratios of 1 : 3 and 1 : 4 with ½ bias are possible but the discrimination and hence the contrast ratios are smaller ($\sqrt{3} = 1.732$ for 1 : 3 multiplex or $\sqrt{21}/3 = 1.528$ for 1 : 4 multiplex). The advantage of these modes is a reduction of the LCD full scale voltage V_{op} as follows:

1 : 3 multiplex (½bias):

$$V_{op} = \sqrt{6}V_{op(mrs)} = 2.449V_{off(rms)}$$

1 : 4 multiplex (½bias):

$$V_{op} = \sqrt[4]{3}/3V_{off(rms)} = 2.309V_{off(rms)}$$

These compare with $V_{op} = 3\ V_{off(rms)}$ when ⅓bias is used.

Table 2 Preferred LCD drive modes: summary of characteristics

LCD DRIVE MODE	LCD BIAS CONFIGURATION	$\frac{V_{off(rms)}}{V_{op}}$	$\frac{V_{on(rms)}}{V_{op}}$	$D = \frac{V_{on(rms)}}{V_{off(rms)}}$
Static (1 BP)	static (2 levels)	0	1	∞
1 : 2 MUX (2 BP)	½ (3 levels)	$\sqrt{2}/4 = 0.354$	$\sqrt{10}/4 = 0.791$	$\sqrt{5} = 2.236$
1 : 2 MUX (2 BP)	⅓ (4 levels)	⅓ = 0.333	$\sqrt{5}/3 = 0.745$	$\sqrt{5} = 2.236$
1 : 3 MUX (3 BP)	⅓ (4 levels)	⅓ = 0.333	$\sqrt{33}/9 = 0.638$	$\sqrt{33}/3 = 1.915$
1 : 4 MUX (4 BP)	⅓ (4 levels)	⅓ = 0.333	$\sqrt{3}/3 = 0.577$	$\sqrt{3} = 1.732$

LCD drive mode waveforms

The static LCD drive mode is used when a single backplane is provided in the LCD. Backplane and segment drive waveforms for this mode are shown in Fig.4.

When two backplanes are provided in the LCD the 1 : 2 multiplex drive mode applies. The OM4085 allows use of ½ or ⅓ bias in this mode as shown in Figs 5 and 6.

The backplane and segment drive waveforms for the 1 : 3 multiplex drive mode (three LCD backplanes) and for the 1 : 4 multiplex drive mode (four LCD backplanes) are shown in Figs 7 and 8 respectively.

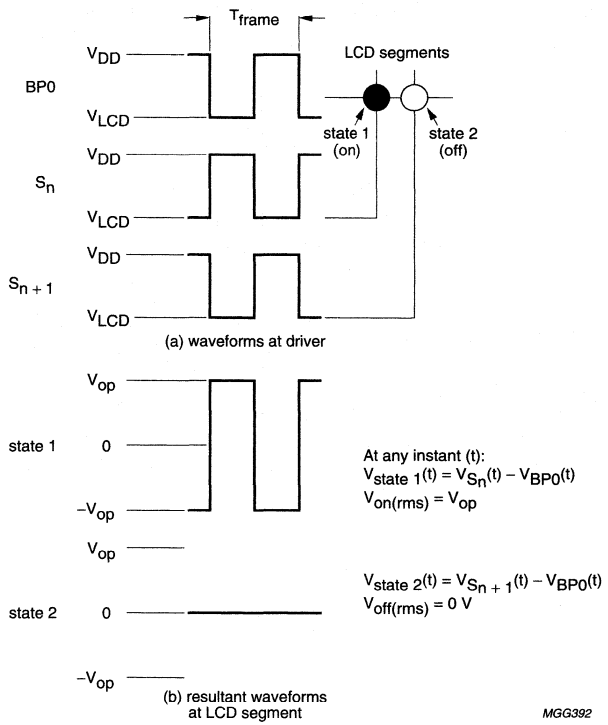


Fig.4 Static drive mode waveforms: $V_{op} = V_{DD} - V_{LCD}$.

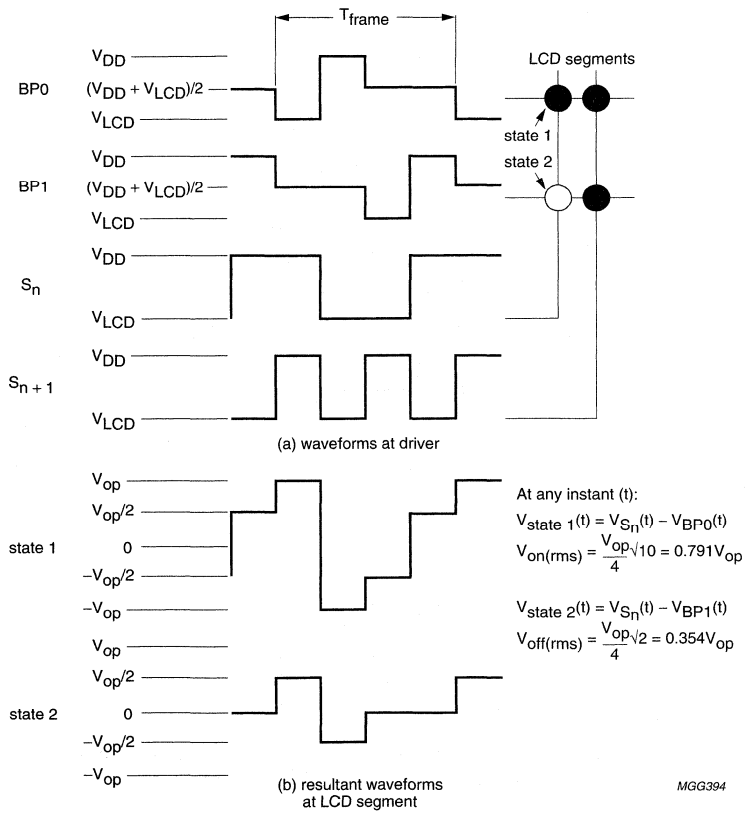


Fig.5 Waveforms for 1 : 2 multiplex drive mode with ½ bias: $V_{op} = V_{DD} - V_{LCD}$.

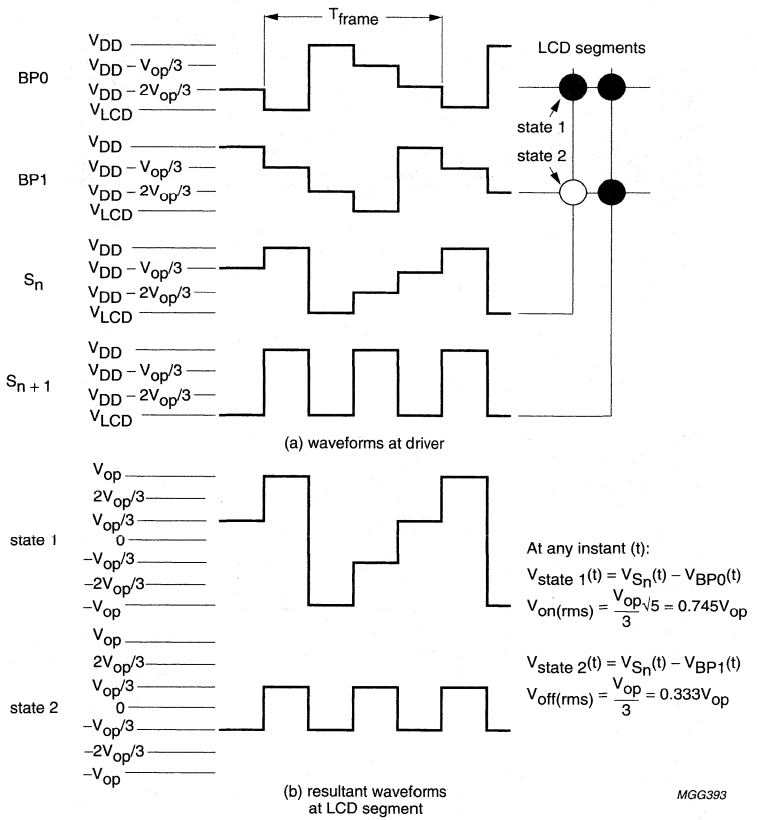


Fig.6 Waveforms for 1 : 2 multiplex drive mode with ⅓ bias: $V_{op} = V_{DD} - V_{LCD}$.

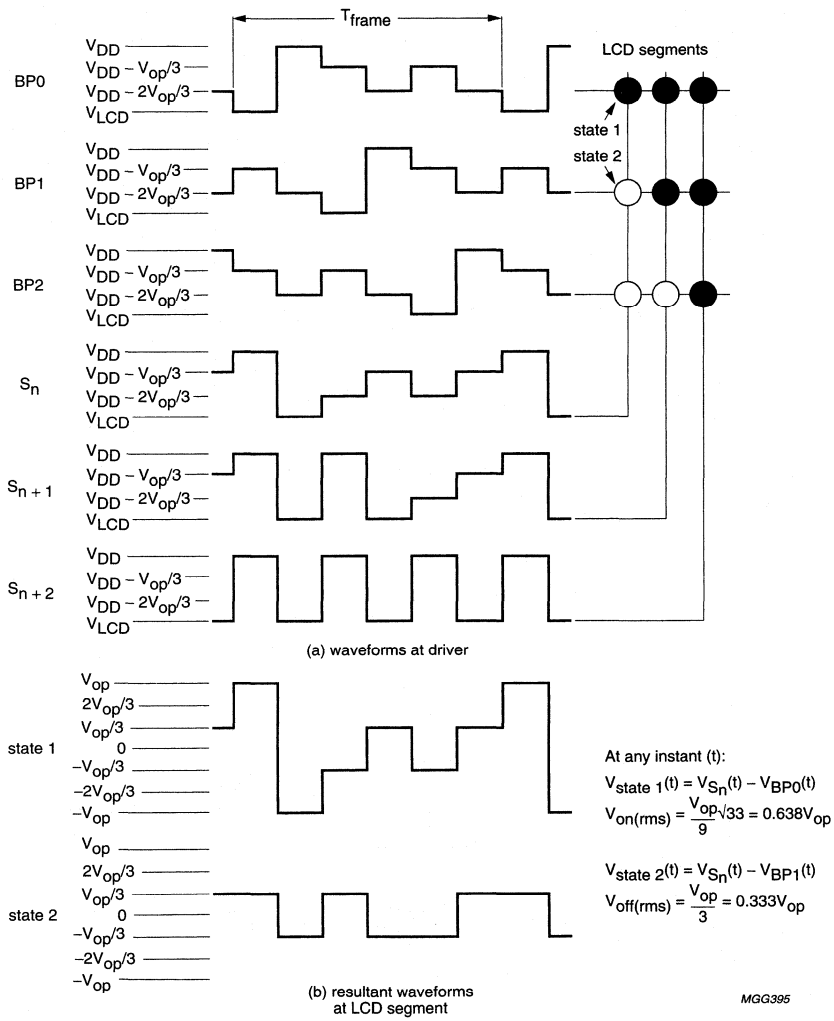


Fig.7 Waveforms for 1 : 3 multiplex drive mode: $V_{op} = V_{DD} - V_{LCD}$.

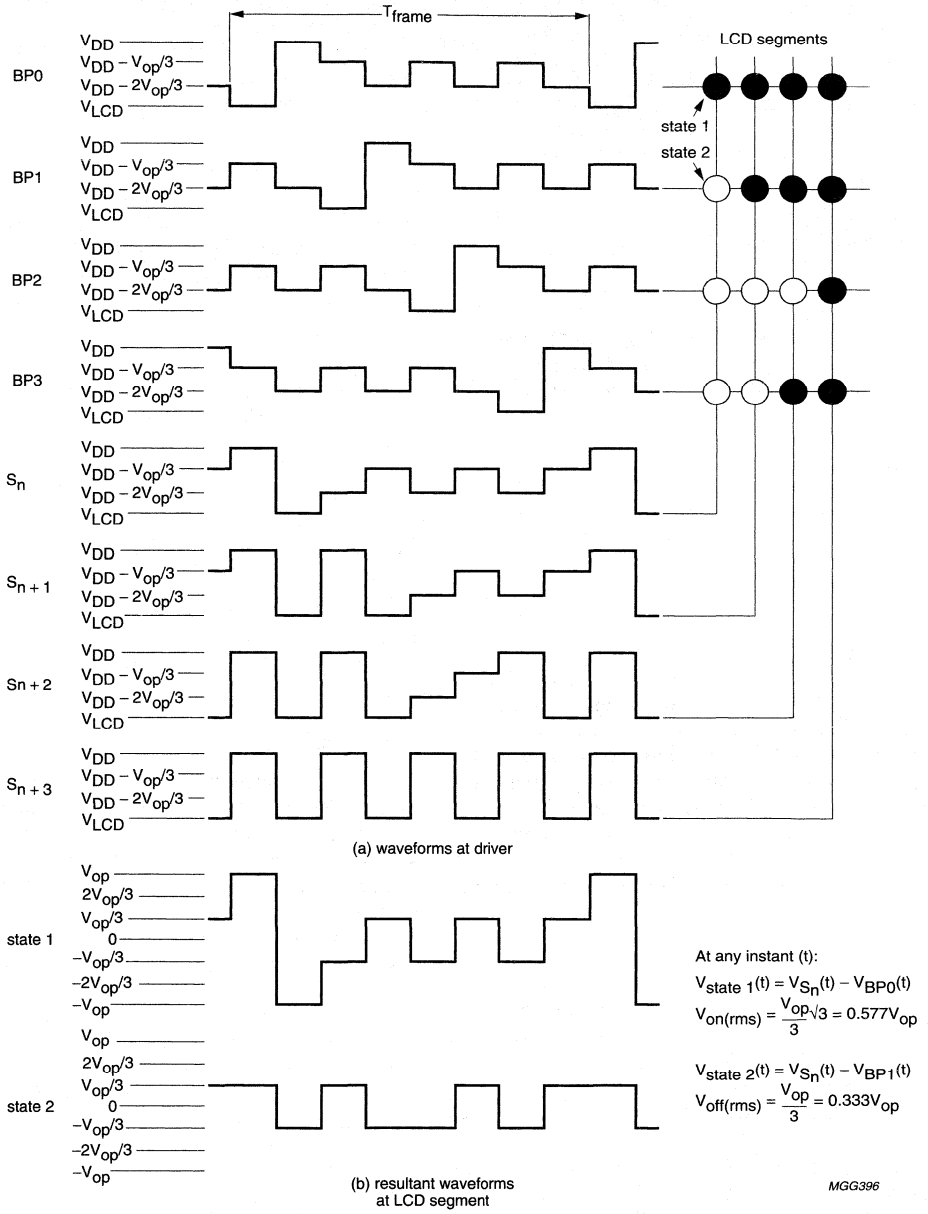


Fig.8 Waveforms for 1 : 4 multiplex drive mode: $V_{op} = V_{DD} - V_{LCD}$.

Oscillator

The internal logic and the LCD drive signals of the OM4085 or PCF8576 are timed either by the built-in oscillator or from an external clock.

The clock frequency (f_{CLK}) determines the LCD frame frequency and the maximum rate for data reception from the I²C-bus. To allow I²C-bus transmissions at their maximum data rate of 100 kHz, f_{CLK} should be chosen to be above 125 kHz.

A clock signal must always be supplied to the device; removing the clock may freeze the LCD in a DC state.

Internal clock

When the internal oscillator is used, OSC (pin 6) should be tied to V_{SS}. In this case, the output from CLK (pin 4) provides the clock signal for cascaded OM4085s and PCF8576s in the system.

External clock

The condition for external clock is made by tying OSC (pin 6) to V_{DD}; CLK (pin 4) then becomes the external clock input.

Timing

The timing of the OM4085 organizes the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. In cascaded applications, the synchronization signal $\overline{SYNC}$ maintains the correct timing relationship between the OM4085s in the system. The timing also generates the LCD frame frequency which it derives as an integer multiple of the clock frequency (Table 3). The frame frequency is set by MODE SET commands when internal clock is used, or by the frequency applied to pin 4 when external clock is used.

Table 3 LCD frame frequencies

OM4085 MODE	f_{frame}	NOMINAL f_{frame} (Hz)
Normal mode	$f_{CLK}/2880$	64
Power saving mode	$f_{CLK}/480$	64

The ratio between the clock frequency and the LCD frame frequency depends on the mode in which the device is operating. In the power saving mode the reduction ratio is six times smaller; this allows the clock frequency to be reduced by a factor of six. The reduced clock frequency results in a significant reduction in power dissipation.

The lower clock frequency has the disadvantage of increasing the response time when large amounts of display data are transmitted on the I²C-bus. When a device is unable to 'digest' a display data byte before the next one arrives, it holds the SCL line LOW until the first display data byte is stored. This slows down the transmission rate of the I²C-bus but no data loss occurs.

Display latch

The display latch holds the display data while the corresponding multiplex signals are generated. There is a one-to-one relationship between the data in the display latch, the LCD segment outputs and one column of the display RAM.

Shift register

The shift register serves to transfer display information from the display RAM to the display latch while previous data are displayed.

Segment outputs

The LCD drive section includes 24 segment outputs S0 to S23 (pins 17 to 40) which should be connected directly to the LCD. The segment output signals are generated in accordance with the multiplexed backplane signals and with the data resident in the display latch. When less than 24 segment outputs are required the unused segment outputs should be left open-circuit.

Backplane outputs

The LCD drive section includes four backplane outputs BP0 to BP3 which should be connected directly to the LCD. The backplane output signals are generated in accordance with the selected LCD drive mode. If less than four backplane outputs are required the unused outputs can be left open. In the 1 : 3 multiplex drive mode BP3 carries the same signal as BP1, therefore these two adjacent outputs can be tied together to give enhanced drive capabilities. In the 1 : 2 multiplex drive mode BP0 and BP2, BP1 and BP3 respectively carry the same signals and may also be paired to increase the drive capabilities. In the static drive mode the same signal is carried by all four backplane outputs and they can be connected in parallel for very high drive requirements.

Display RAM

The display RAM is a static 24 × 4-bit RAM which stores LCD data. A logic 1 in the RAM bit-map indicates the 'on' state of the corresponding LCD segment; similarly, a logic 0 indicates the 'off' state.

There is a one-to-one correspondence between the RAM addresses and the segment outputs, and between the individual bits of a RAM word and the backplane outputs. The first RAM column corresponds to the 24 segments operated with respect to backplane BP0 (see Fig.9). In multiplexed LCD applications the segment data of the second, third and fourth column of the display RAM are time-multiplexed with BP1, BP2 and BP3 respectively.

When display data are transmitted to the OM4085 the display bytes received are stored in the display RAM according to the selected LCD drive mode. To illustrate the filling order, an example of a 7-segment numeric display showing all drive modes is given in Fig.10; the RAM filling organization depicted applies equally to other LCD types.

With reference to Fig.10, in the static drive mode the eight transmitted data bits are placed in bit 0 of eight successive display RAM addresses. In the 1 : 2 multiplex drive mode the eight transmitted data bits are placed in bits 0 and 1 of four successive display RAM addresses. In the 1 : 3 multiplex drive mode these bits are placed in bits 0, 1 and 2 of three successive addresses, with bit 2 of the third address left unchanged. This last bit may, if necessary, be controlled by an additional transfer to this address but care should be taken to avoid overriding adjacent data because full bytes are always transmitted. In the 1 : 4 multiplex drive mode the eight transmitted data bits are placed in bits 0, 1, 2 and 3 of two successive display RAM addresses.

Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM.

The sequence commences with the initialization of the data pointer by the LOAD DATA POINTER command. Following this, an arriving data byte is stored starting at the display RAM address indicated by the data pointer thereby observing the filling order shown in Fig.10. The data pointer is automatically incremented according to the LCD configuration chosen. That is, after each byte is stored, the contents of the data pointer are incremented by eight (static drive mode), by four (1 : 2 multiplex drive mode), by three (1 : 3 multiplex drive mode) or by two (1 : 4 multiplex drive mode).

Subaddress counter

The storage of display data is conditioned by the contents of the subaddress counter. Storage is allowed to take place only when the contents of the subaddress counter agree with the hardware subaddress applied to A0, A1 and A2 (pins 7, 8, and 9). A0, A1 and A2 should be tied to V_{SS} or V_{DD}. The subaddress counter value is defined by the DEVICE SELECT command. If the contents of the subaddress counter and the hardware subaddress do not agree then data storage is inhibited but the data pointer is incremented as if data storage had taken place. The subaddress counter is also incremented when the data pointer overflows.

The storage arrangements described lead to extremely efficient data loading in cascaded applications. When a series of display bytes are being sent to the display RAM, automatic wrap-over to the next OM4085 occurs when the last RAM address is exceeded. Subaddressing across device boundaries is successful even if the change to the next device in the cascade occurs within a transmitted character.

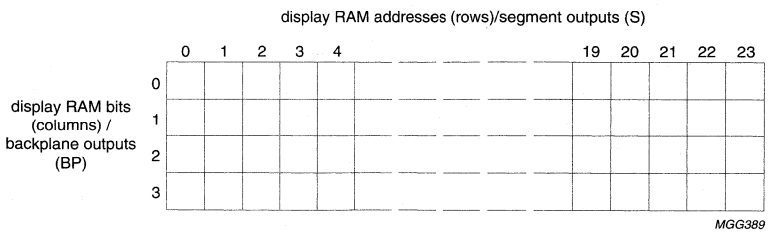


Fig.9 Display RAM bit-map showing direct relationship between display RAM addresses and segment outputs, and between bits in a RAM word and backplane outputs.

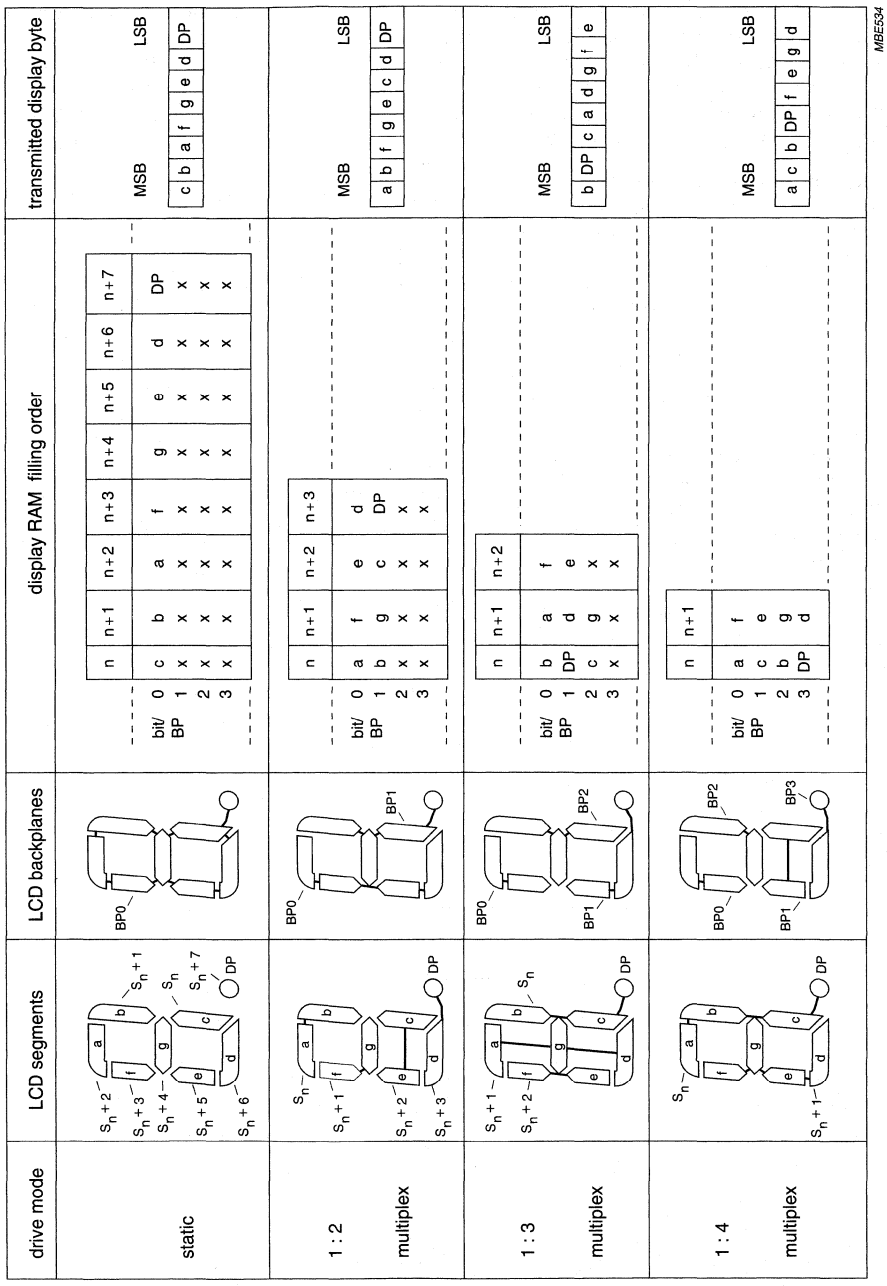


Fig.10 Relationships between LCD layout, drive mode, display RAM filling order and display data transmitted over the I²C-bus (X = data bit unchanged).

Output bank selector

This selects one of the four bits per display RAM address for transfer to the display latch. The actual bit chosen depends on the particular LCD drive mode in operation and on the instant in the multiplex sequence. In 1 : 4 multiplex, all RAM addresses of bit 0 are the first to be selected, these are followed by the contents of bit 1, bit 2 and then bit 3. Similarly in 1 : 3 multiplex, bits 0, 1 and 2 are selected sequentially. In 1 : 2 multiplex, bits 0 then 1 are selected and, in the static mode, bit 0 is selected.

The OM4085 includes a RAM bank switching feature in the static and 1 : 2 multiplex drive modes. In the static drive mode, the BANK SELECT command may request the contents of bit 2 to be selected for display instead of bit 0 contents. In the 1 : 2 drive mode, the contents of bits 2 and 3 may be selected instead of bits 0 and 1. This gives the provision for preparing display information in an alternative bank and to be able to switch to it once it is assembled.

Input bank selector

The input bank selector loads display data into the display RAM according to the selected LCD drive configuration. Display data can be loaded in bit 2 in static drive mode or in bits 2 and 3 in 1 : 2 drive mode by using the BANK SELECT command. The input bank selector functions independently of the output bank selector.

Blinker

The display blinking capabilities of the OM4085 are very versatile. The whole display can be blinked at frequencies selected by the BLINK command. The blinking frequencies are integer multiples of the clock frequency; the ratios between the clock and blinking frequencies depend on the mode in which the device is operating, as shown in Table 4.

An additional feature is for an arbitrary selection of LCD segments to be blinked. This applies to the static and 1 : 2 LCD drive modes and can be implemented without any communication overheads. By means of the output bank selector, the displayed RAM banks are exchanged with alternate RAM banks at the blinking frequency. This mode can also be specified by the BLINK command.

In the 1 : 3 and 1 : 4 multiplex modes, where no alternate RAM bank is available, groups of LCD segments can be blinked by selectively changing the display RAM data at fixed time intervals.

If the entire display is to be blinked at a frequency other than the nominal blinking frequency, this can be effectively performed by resetting and setting the display enable bit E at the required rate using the MODE SET command.

Table 4 Blinking frequencies

BLINKING MODE	NORMAL OPERATING MODE RATIO	POWER-SAVING MODE RATIO	NOMINAL BLINKING FREQUENCY f_{blink} (Hz)
Off	–	–	blinking off
2 Hz	$f_{CLK}/92160$	$f_{CLK}/15360$	2
1 Hz	$f_{CLK}/184320$	$f_{CLK}/30720$	1
0.5 Hz	$f_{CLK}/368640$	$f_{CLK}/61440$	0.5

I²C-BUS DESCRIPTION

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P).

System configuration

A device generating a message is a 'transmitter', a device receiving a message is a 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves'.

Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is not limited. Each byte is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

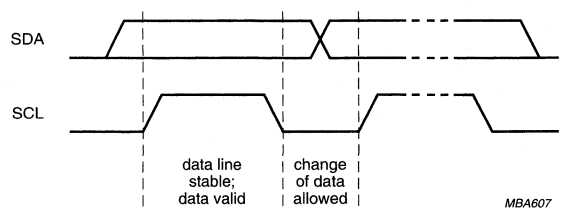


Fig.11 Bit transfer.

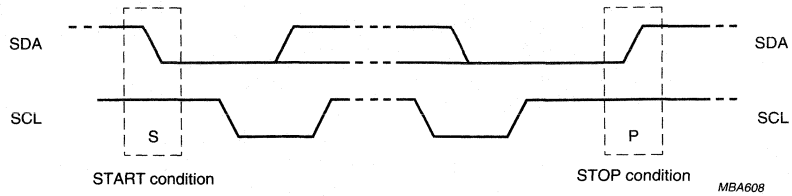


Fig.12 Definition of START and STOP conditions.

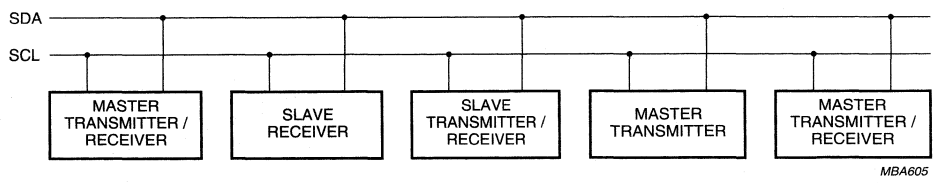


Fig.13 System configuration.

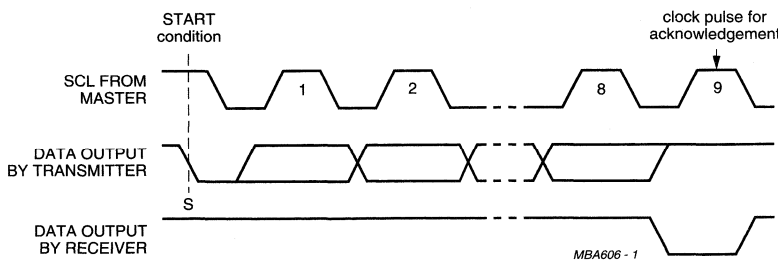


Fig.14 Acknowledgement on the I^2C-bus.

OM4085 I²C-bus controller

The OM4085 acts as an I²C-bus slave receiver. It does not initiate I²C-bus transfers or transmit data to an I²C-bus master receiver. The only data output from the OM4085 are the acknowledge signals of the selected devices. Device selection depends on the I²C-bus slave address, on the transferred command data and on the hardware subaddress.

In single device applications, the hardware subaddress inputs A0, A1 and A2 are normally left open-circuit or tied to V_{SS} which defines the hardware subaddress 0.
In multiple device applications A0, A1 and A2 are left open-circuit or tied to V_{SS} or V_{DD} according to a binary coding scheme such that no two devices with a common I²C-bus slave address have the same hardware subaddress.

In the power-saving mode it is possible that the OM4085 is not able to keep up with the highest transmission rates when large amounts of display data are transmitted. If this situation occurs, the OM4085 forces the SCL line LOW until its internal operations are completed. This is known as the 'clock synchronization feature' of the I²C-bus and serves to slow down fast transmitters. Data loss does not occur.

Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

I²C-bus protocol

Two I²C-bus slave addresses (0111110 and 0111111) are reserved for OM4085. The least-significant bit of the slave address that a OM4085 will respond to is defined by the level tied at its input SA0 (pin 10). Therefore, two types of OM4085 can be distinguished on the same I²C-bus which allows:

1. Up to 16 OM4085s on the same I²C-bus for very large LCD applications
2. The use of two types of LCD multiplex on the same I²C-bus.

The I²C-bus protocol is shown in Fig.15. The sequence is initiated with a START condition (S) from the I²C-bus master which is followed by one of the two OM4085 slave addresses available. All OM4085s with the corresponding SA0 level acknowledge in parallel the slave address but all OM4085s with the alternative SA0 level ignore the whole I²C-bus transfer. After acknowledgement, one or more command bytes (m) follow which define the status of the addressed OM4085s. The last command byte is tagged with a cleared most-significant bit, the continuation bit C. The command bytes are also acknowledged by all addressed OM4085s on the bus.

After the last command byte, a series of display data bytes (n) may follow. These display data bytes are stored in the display RAM at the address specified by the data pointer and the subaddress counter. Both data pointer and subaddress counter are automatically updated and the data are directed to the intended OM4085 device.
The acknowledgement after each byte is made only by the (A0, A1, A2) addressed OM4085. After the last display byte, the I²C-bus master issues a STOP condition (P).

Command decoder

The command decoder identifies command bytes that arrive on the I²C-bus. All available commands carry a continuation bit C in their most-significant bit position (see Fig.16). When this bit is set, it indicates that the next byte of the transfer to arrive will also represent a command.
If the bit is reset, it indicates the last command byte of the transfer. Further bytes will be regarded as display data.

The five commands available to the OM4085 are defined in Table 5.

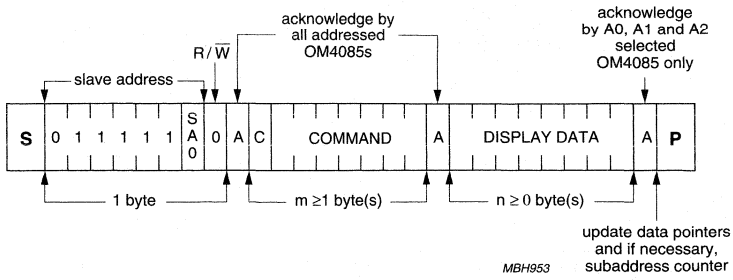


Fig.15 I²C-bus protocol.

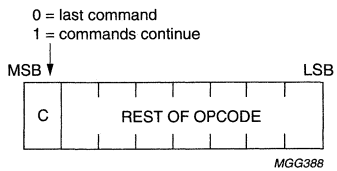


Fig.16 General format of command byte.

Table 5 Definition of OM4085 commands

COMMAND/OPCODE								OPTIONS	DESCRIPTION
Mode set									
C	1	0	LP	E	B	M1	M0	see Table 6	defines LCD drive mode
								see Table 7	defines LCD bias configuration
								see Table 8	defines display status; the possibility to disable the display allows implementation of blinking under external control
								see Table 9	defines power dissipation mode
Load data pointer									
C	0	0	P4	P3	P2	P1	P0	see Table 10	five bits of immediate data, bits P4 to P0, are transferred to the data pointer to define one of twenty-four display RAM addresses
Device select									
C	1	1	0	0	A2	A1	A0	see Table 11	three bits of immediate data, bits A0 to A2, are transferred to the subaddress counter to define one of eight hardware subaddresses
Bank select									
C	1	1	1	1	0	I	O	see Table 12	defines input bank selection (storage of arriving display data)
								see Table 13	defines output bank selection (retrieval of LCD display data)
									the BANK SELECT command has no effect in 1 : 3 and 1 : 4 multiplex drive modes
Blink									
C	1	1	1	0	A	BF1	BF0	see Table 14	defines the blinking frequency
								see Table 15	selects the blinking mode; normal operation with frequency set by bits BF1 and BF0, or blinking by alternation of display RAM banks. Alternation blinking does not apply in 1 : 3 and 1 : 4 multiplex drive modes

Table 6 LCD drive mode

LCD DRIVE MODE	BIT M1	BIT M0
Static (1 BP)	0	1
1 : 2 MUX (2 BP)	1	0
1 : 3 MUX (3 BP)	1	1
1 : 4 MUX (4 BP)	0	0

Table 7 LCD bias configuration

LCD BIAS	BIT B
1/3bias	0
1/2bias	1

Table 8 Display status

DISPLAY STATUS	BIT E
Disabled (blank)	0
Enabled	1

Table 9 Power dissipation mode

MODE	BIT LP
Normal mode	0
Power-saving mode	1

Table 10 Load data pointer

BITS	P4	P3	P2	P1	P0
5-bit binary value of 0 to 23					

Table 11 Device select

BITS	A0	A1	A2
3-bit binary value of 0 to 7			

Table 12 Input bank selection

STATIC	1 : 2 MUX	BIT 1
RAM bit 0	RAM bits 0, 1	0
RAM bit 2	RAM bits 2, 3	1

Table 13 Output bank selection

STATIC	1 : 2 MUX	BIT 0
RAM bit 0	RAM bits 0, 1	0
RAM bit 2	RAM bits 2, 3	1

Table 14 Blinking frequency

BLINK FREQUENCY	BIT BF1	BIT BF0
Off	0	0
2 Hz	0	1
1 Hz	1	0
0.5 Hz	1	1

Table 15 Blink mode selection

BLINK MODE	BIT A
Normal blinking	0
Alternation blinking	1

Display controller

The display controller executes the commands identified by the command decoder. It contains the status registers of the OM4085 and coordinates their effects.

The controller is also responsible for loading display data into the display RAM as required by the filling order.

Cascaded operation

In large display configurations, up to 16 OM4085s can be distinguished on the same I²C-bus by using the 3-bit hardware subaddress (A0, A1 and A2) and the programmable I²C-bus slave address (SA0). It is also possible to cascade up to 16 OM4085s. When cascaded, several OM4085s are synchronized so that they can share the backplane signals from one of the devices in the cascade. Such an arrangement is cost-effective in large LCD applications since the outputs of only one device need to be through-plated to the backplane electrodes of the display. The other OM4085s of the cascade contribute additional segment outputs but their backplane outputs are left open-circuit (Fig.17).

The $\overline{\text{SYNC}}$ line is provided to maintain the correct synchronization between all cascaded OM4085s. This synchronization is guaranteed after the power-on reset. The only time that $\overline{\text{SYNC}}$ is likely to be needed is if synchronization is accidentally lost (e.g. by noise in adverse electrical environments; or by the definition of a multiplex mode when OM4085s with differing SA0 levels are cascaded). $\overline{\text{SYNC}}$ is organized as an input/output pin; the output section being realized as an open-drain driver with an internal pull-up resistor. A OM4085 asserts the $\overline{\text{SYNC}}$ line at the onset of its last active backplane signal and monitors the $\overline{\text{SYNC}}$ line at all other times. Should synchronization in the cascade be lost, it will be restored by the first OM4085 to assert $\overline{\text{SYNC}}$. The timing relationships between the backplane waveforms and the $\overline{\text{SYNC}}$ signal for the various drive modes of the PCF8576 are shown in Fig.18. The waveforms are identical with the parent device PCF8576. Cascade ability between OM4085s and PCF8576s is possible, giving cost effective LCD applications.

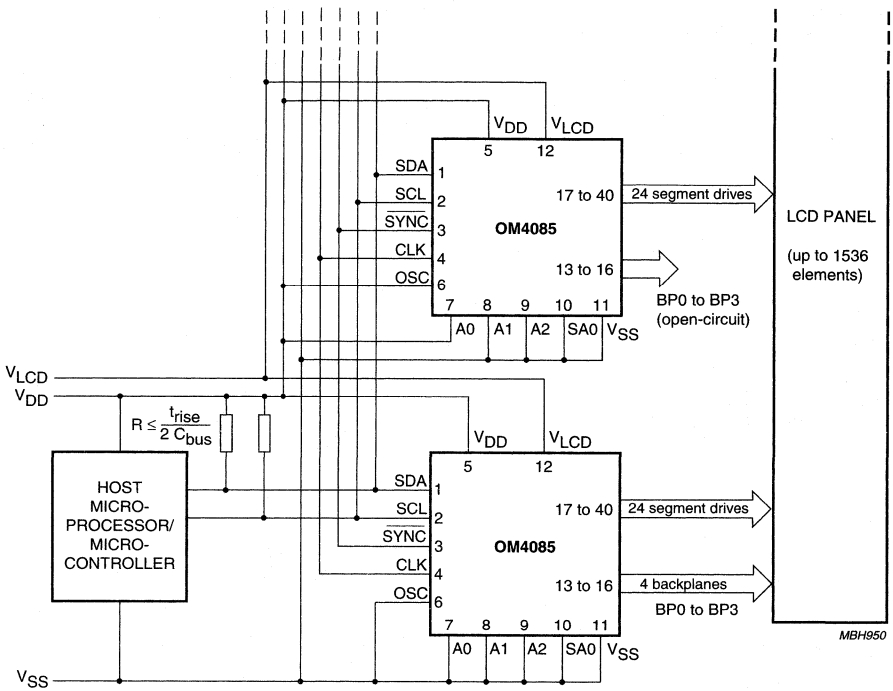


Fig.17 Cascaded OM4085 configuration.

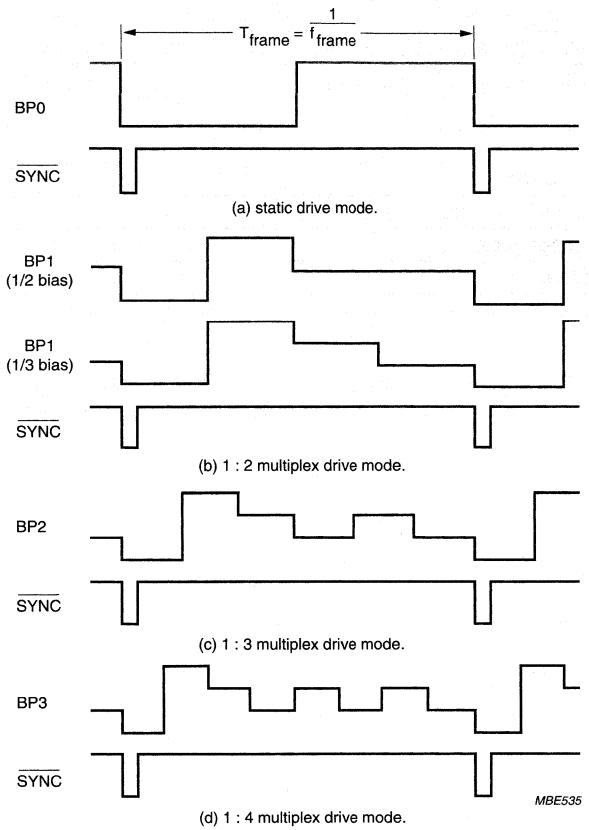


Fig.18 Synchronization of the cascade for the various OM4085 drive modes.

For single plane wiring of OM4085s, see Chapter “Application information”.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.5	+7	V
V_{LCD}	LCD supply voltage	V_{DD} − 7	V_{DD}	V
V_I	input voltage (SCL, SDA, A0 to A2, OSC, CLK, $\overline{SYNC}$ and SA0)	V_{SS} − 0.5	V_{DD} + 0.5	V
V_O	output voltage (S0 to S23 and BP0 to BP3)	V_{LCD} − 0.5	V_{DD} + 0.5	V
I_I	DC input current	−	±20	mA
I_O	DC output current	−	±25	mA
I_{DD}, I_{SS}, I_{LCD}	V_{DD}, V_{SS} or V_{LCD} current	−	±50	mA
P_{tot}	power dissipation per package	−	400	mW
P_O	power dissipation per output	−	100	mW
T_{stg}	storage temperature	−65	+150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advised to take handling precautions appropriate to handling MOS devices (see *"Handling MOS devices"*).

DC CHARACTERISTICS

V_{SS} = 0 V; V_{DD} = 2.0 to 6 V; V_{LCD} = V_{DD} − 2.0 to V_{DD} − 6 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	operating supply voltage		2.0	–	6	V
V_{LCD}	LCD supply voltage		V_{DD} − 6	–	V_{DD} − 2.0	V
I_{DD}	operating supply current (normal mode)	f_{CLK} = 200 kHz; note 1	–	30	90	μA
I_{LP}	power saving mode supply current	V_{DD} = 3.5 V; V_{LCD} = 0 V; f_{CLK} = 35 kHz; A0, A1 and A2 tied to V_{SS}; note 1	–	15	40	μA
Logic						
V_{IL}	LOW level input voltage		V_{SS}	–	0.3V_{DD}	V
V_{IH}	HIGH level input voltage		0.7V_{DD}	–	V_{DD}	V
V_{OL}	LOW level output voltage	I_O = 0 mA	–	–	0.05	V
V_{OH}	HIGH level output voltage	I_O = 0 mA	V_{DD} − 0.05	–	–	V
I_{OL1}	LOW level output current (CLK and $\overline{SYNC}$)	V_{OL} = 1 V; V_{DD} = 5 V	1	–	–	mA
I_{OH}	HIGH level output current (CLK)	V_{OH} = 4 V; V_{DD} = 5 V	–	–	−1	mA
I_{OL2}	LOW level output current (SDA and SCL)	V_{OL} = 0.4 V; V_{DD} = 5 V	3	–	–	mA
I_{LI}	leakage current (SA0, CLK, OSC, A0, A1, A2, SCL and SDA)	V_I = V_{SS} or V_{DD}	–	–	±1	μA
I_{pd}	pull-down current (A0, A1, A2 and OSC)	V_I = 1 V; V_{DD} = 5 V	15	50	150	μA
R_{puSYNC}	pull-up resistor ($\overline{SYNC}$)		15	25	60	kΩ
V_{ref}	power-on reset level	note 2	–	1.3	2	V
t_{sw}	tolerable spike width on bus		–	–	100	ns
C_i	input capacitance	note 3	–	–	7	pF
LCD outputs						
V_{BP}	DC voltage component (BP0 to BP3)	C_{BP} = 35 nF	–	±20	–	mV
V_S	DC voltage component (S0 to S23)	C_S = 5 nF	–	±20	–	mV
Z_{BP}	output impedance (BP0 to BP3)	V_{LCD} = V_{DD} − 5 V; note 4	–	1	5	kΩ
Z_S	output impedance (S0 to S23)	V_{LCD} = V_{DD} −5 V; note 4	–	3	7	kΩ

Notes

1. Outputs open; inputs at V_{SS} or V_{DD}; external clock with 50% duty factor; I^2C-bus inactive.
2. Resets all logic when V_{DD} < V_{ref}.
3. Periodically sampled, not 100% tested.
4. Outputs measured one at a time.

AC CHARACTERISTICS

V_{SS} = 0 V; V_{DD} = 2.0 to 6 V; V_{LCD} = V_{DD} − 2.0 to V_{DD} − 6 V; T_{amb} = −40 to +85 °C; unless otherwise specified; note 1.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{CLK}	oscillator frequency (normal mode)	V_{DD} = 5 V; note 2	125	200	315	kHz
f_{CLKLP}	oscillator frequency (power saving mode)	V_{DD} = 3.5 V	21	31	48	kHz
t_{CLKH}	CLK HIGH time		1	–	–	µs
t_{CLKL}	CLK LOW time		1	–	–	µs
t_{PSYNC}	$\overline{SYNC}$ propagation delay		–	–	400	ns
t_{SYNCL}	$\overline{SYNC}$ LOW time		1	–	–	µs
t_{PLCD}	driver delays with test loads	V_{LCD} = V_{DD} − 5 V	–	–	30	µs
I²C-bus						
t_{BUF}	bus free time		4.7	–	–	µs
$t_{HD;\ STA}$	START condition hold time		4	–	–	µs
t_{LOW}	SCL LOW time		4.7	–	–	µs
t_{HIGH}	SCL HIGH time		4	–	–	µs
$t_{SU;\ STA}$	START condition set-up time (repeated start code only)		4.7	–	–	µs
$t_{HD;\ DAT}$	data hold time		0	–	–	µs
$t_{SU;\ DAT}$	data set-up time		250	–	–	ns
t_r	rise time		–	–	1	µs
t_f	fall time		–	–	300	ns
$t_{SU;\ STO}$	STOP condition set-up time		4.7	–	–	µs

Notes

1. All timing values referred to V_{IH} and V_{IL} levels with an input voltage swing of V_{SS} to V_{DD}.
2. At f_{CLK} < 125 kHz, I²C-bus maximum transmission speed is derated.

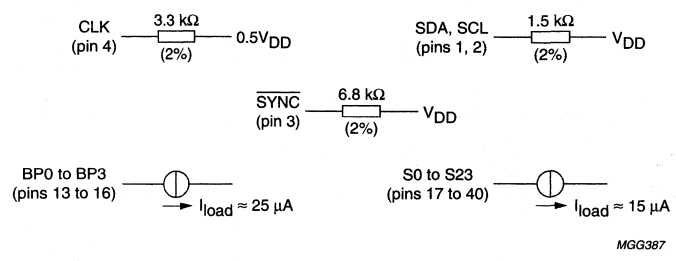


Fig.19 Test loads.

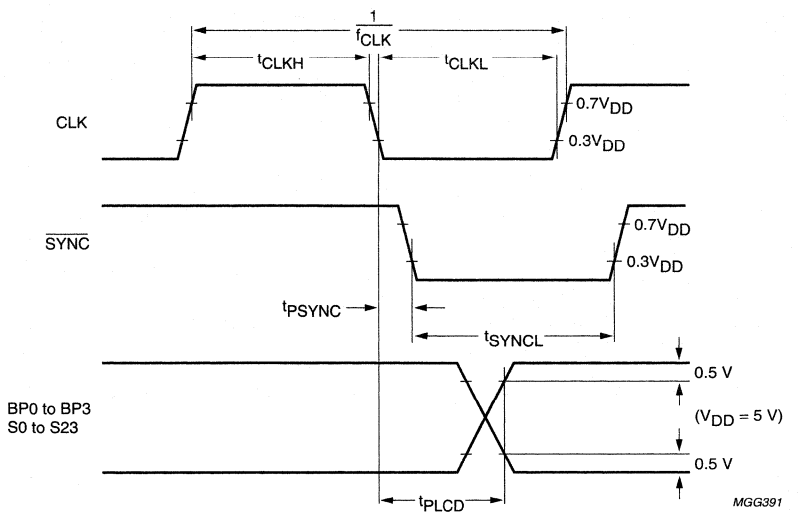


Fig.20 Driver timing waveforms.

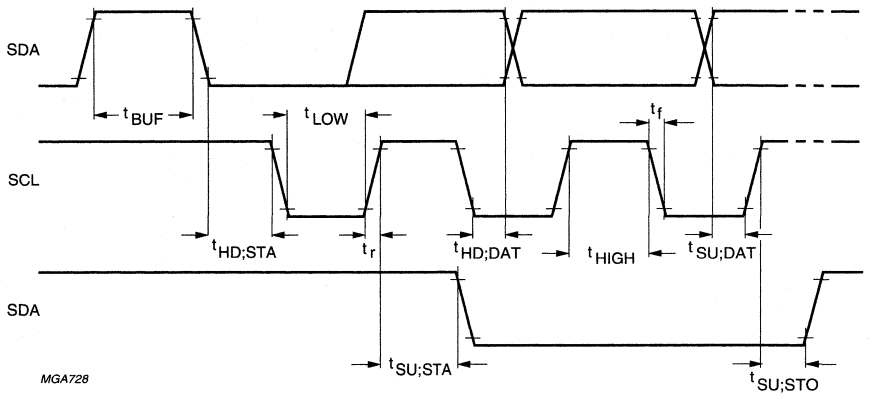
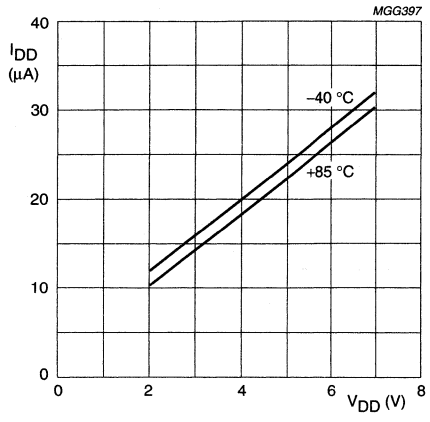
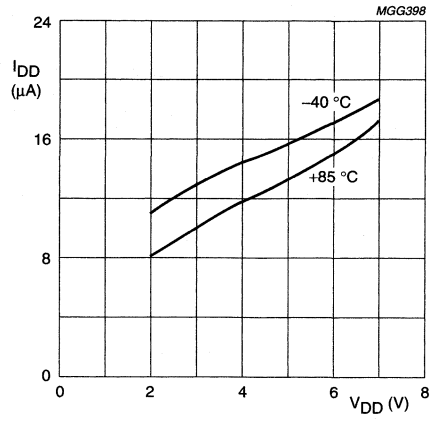


Fig.21 I²C-bus timing waveforms.

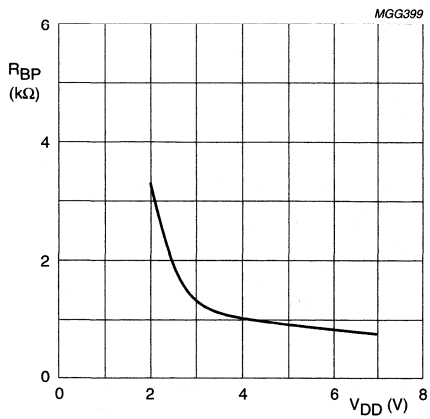


a. Normal mode; V_{LCD} = 0 V; external clock = 200 kHz.

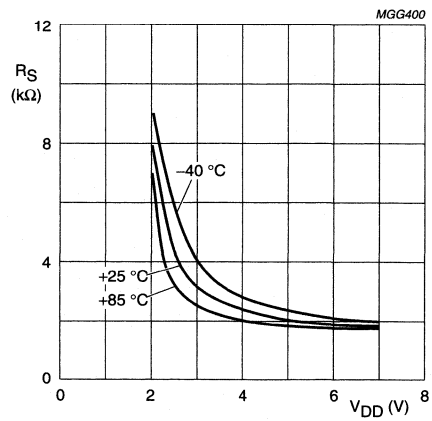


b. Low power mode; V_{LCD} = 0 V; external clock = 35 kHz.

Fig.22 Typical supply current characteristics.



a. Backplane output impedance BP0 to BP3 (R_{BP}); V_{DD} = 5 V; T_{amb} = −40 to +85 °C.



b. Segment output impedance S0 to S23 (R_S); V_{DD} = 5 V.

Fig.23 Typical characteristics of LCD outputs.

APPLICATION INFORMATION

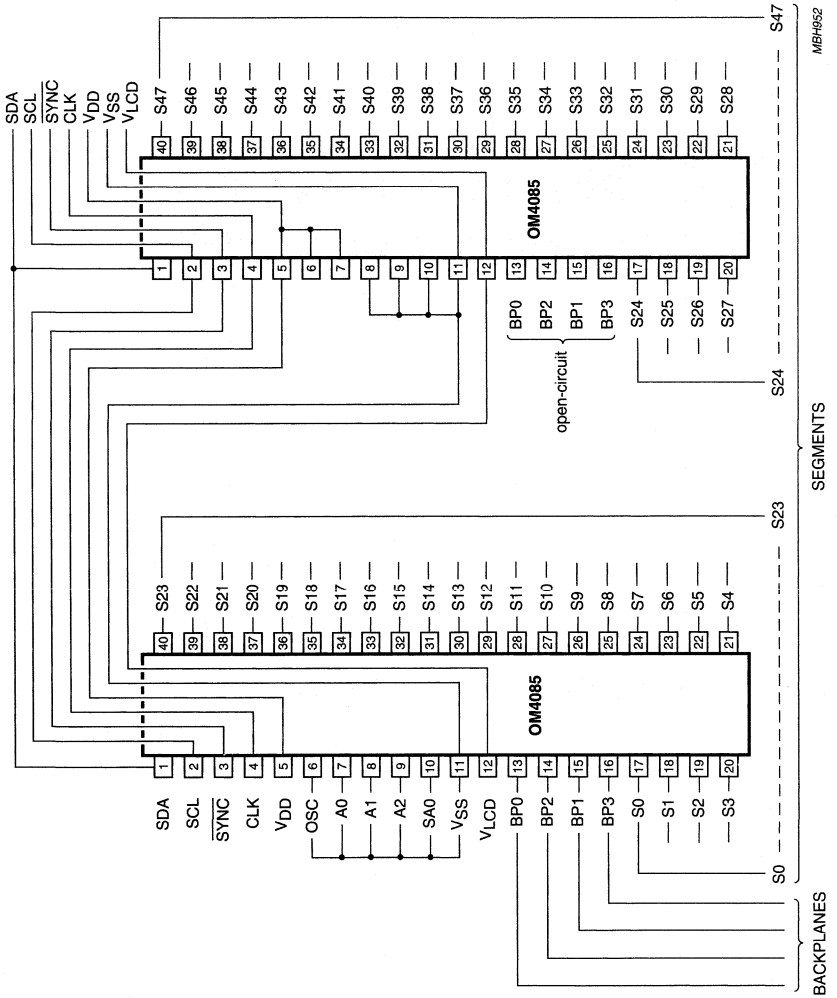
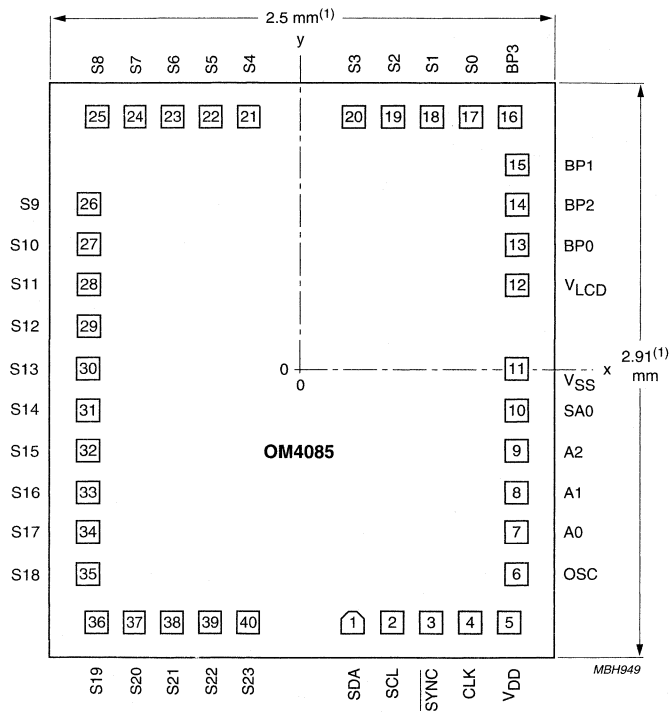


Fig.24 Single plane wiring of package OM4085s.

CHIP DIMENSIONS AND BONDING PAD LOCATIONS



(1) Typical value.
Pad size: 120 × 120 μm
Chip area: 7.27 mm.
The numbers given in the small squares refer to the pad numbers.

Fig.25 Bonding pad locations.

Table 16 Bonding pad locations (dimensions in mm)
All x/y coordinates are referenced to centre of chip, (see Fig.25)

PAD NUMBER	SYMBOL	x	y	PIN
1	SDA	200	−1235	1
2	SCL	400	−1235	2
3	$\overline{SYNC}$	605	−1235	3
4	CLK	856	−1235	4
5	V_{DD}	1062	−1235	5
6	OSC	1080	−1025	6
7	A0	1080	−825	7
8	A1	1080	−625	8
9	A2	1080	−425	9
10	SA0	1080	−225	10
11	V_{SS}	1080	−25	11
12	V_{LCD}	1080	347	12
13	BP0	1080	547	13
14	BP2	1080	747	14
15	BP1	1080	947	15
16	BP3	1074	1235	16
17	S0	674	1235	17
18	S1	674	1235	18
19	S2	474	1235	19
20	S3	274	1235	20
21	S4	−274	1235	21
22	S5	−474	1235	22
23	S6	−674	1235	23
24	S7	−874	1235	24
25	S8	−1074	1235	25
26	S9	−1080	765	26
27	S10	−1080	565	27
28	S11	−1080	365	28
29	S12	−1080	165	29
30	S13	−1080	−35	30
31	S14	−1080	−235	31
32	S15	−1080	−435	32
33	S16	−1080	−635	33
34	S17	−1080	−835	34
35	S18	−1080	−1035	35
36	S19	−1056	−1235	36
37	S20	−830	−1235	37
38	S21	−630	−1235	38
39	S22	−430	−1235	39
40	S23	−230	−1235	40

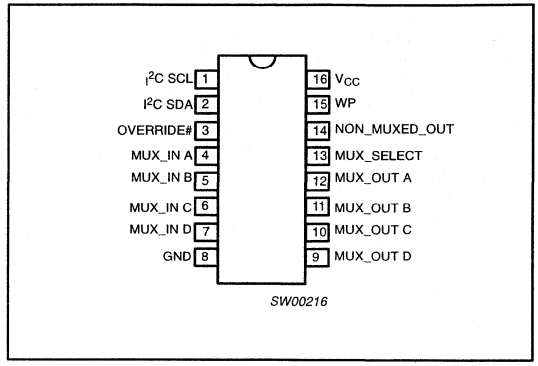
4-bit multiplexed/1-bit latched 5-bit I²C EEPROM PCA8550

FEATURES

- 4-bit 2-to-1 multiplexer, 1-bit latch
- 5-bit internal non-volatile register
- Override input forces all outputs to logic 0
- Internal non-volatile register write/readable via I²C bus
- Write-protect pin enables/disables I²C writes to register
- 2.5V multiplexed outputs
- 3.3V non-multiplexed output (latched)
- 5V tolerant inputs
- Useful for 'jumperless' configuration of PC motherboards
- Designed for use in Pentium Pro/Pentium II™ systems

Pentium II is a registered trademark of Intel Corporation

PIN CONFIGURATION



DESCRIPTION

The primary function of the 4-bit 2-to-1 I²C multiplexer is to select either a 4-bit input or data from a non-volatile register and drive this value onto the output pins. One additional non-multiplexed register output is also provided. The non-multiplexed output is latched to prevent output value changes during I²C writes to the non-volatile register. A write protect input is provided to enable/disable the ability to write to the non-volatile register. An "override" input feature forces all outputs to logic 0.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DRAWING NUMBER
16-Pin Plastic SO	0°C to +70°C	PCA8550D	PCA8550D	SOT109-1
16-Pin Plastic SSOP	0°C to +70°C	PCA8550DB	PCA8550DB	SOT338-1
16-Pin Plastic TSSOP	0°C to +70°C	PCA8550PW	PCA8550PW DH	SOT403-1

FUNCTIONAL DESCRIPTION

When the MUX_SELECT signal is logic 0, the multiplexer will select the data from the non-volatile register to drive on the MUX_OUT pins. When the MUX_SELECT signal is logic 1, the multiplexer will select the MUX_IN lines to drive on the MUX_OUT pins. The MUX_SELECT signal is also used to latch the NON_MUXED_OUT signal which outputs data from the non-volatile register. The NON_MUXED_OUT signal latch is transparent when MUX_SELECT is in a logic 0 state, and will latch data when MUX_SELECT is in a logic 1 state. When the active-LOW OVERRIDE# signal is set to logic 0 and the MUX_SELECT signal is at a logic 0, all outputs will be driven to logic 0. This information is summarized in Table 1.

The write protect (WP) input is used to control the ability to write the contents of the 5-bit non-volatile register. If the WP signal is logic 0, the I²C bus will be able to write the contents of the non-volatile register. If the WP signal is logic 1, data will not be allowed to be written into the non-volatile register.

The factory default for the contents of the non-volatile register are all logic 0. These stored values can be read or written using the I²C bus (described in the next section).

The OVERRIDE#, WP, MUX_IN, and MUX_SELECT signals have internal pullup resistors. See the DC and AC Characteristics for hysteresis and signal spike suppression figures.

PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	I²C SCL	I²C bus clock
2	I²C SDA	Bi-directional I²C bus data
3	OVERRIDE#	Forces all outputs to logic 0
4	MUX_IN A	External inputs to multiplexer
5	MUX_IN B	
6	MUX_IN C	
7	MUX_IN D	
8	GND	Common ground voltage rail
9	MUX_OUT D	2.5V multiplexed output
10	MUX_OUT C	
11	MUX_OUT B	
12	MUX_OUT A	
13	MUX_SELECT	Selects MUX_IN inputs or register contents for MUX_OUT outputs
14	NON_MUXED_OUT	TTL-level output from non-volatile memory
15	WP	Non-volatile register write-protect
16	V_{CC}	Positive voltage rail

FUNCTION TABLE

Table 1. Function table

OVERRIDE #	MUX_SELECT	MUX_OUT OUTPUTS	NON_MUXED_OUT OUTPUT
0	0	All 0's	All 0's
0	1	MUX_IN inputs	Latched NON_MUXED_OUT[1]
1	0	From non-volatile register	From non-volatile register
1	1	MUX_IN inputs	From non-volatile register

NOTE

1. Latched NON_MIXED_OUT state will be the value present on the NON_MUXED_OUT output at the time of the MUX_SELECT input transitioned from a logic 0 to a logic 1 state.

I²C Interface

Communicating with this device is initiated by sending a valid address on the I²C bus. The address format (see FIgure 1) is a fixed unique 7-bit value followed by a 1-bit read/write value which determines the direction of the data transfer.

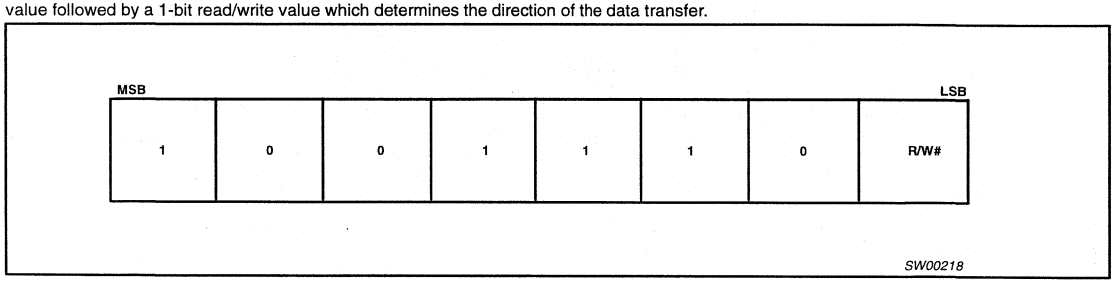


Figure 1. I²C Address Byte

Following the address and acknowledge bit are 8 data bits which, depending on the read/write bit in the address, will read data from or write data to the non-volatile register. Data will be written to the register if the read/write bit is logic 0 and the WP input is logic 0. Data will be read from the register if the bit is logic 1. The three high-order bits (see FIgure 2) are logic 0. The next bit is data which is non-multiplexed. The low four bits are the data which will be multiplexed. A write with any of the first three bits non-zero will be aborted.

NOTE:

1. To ensure data integrity, the non-volatile register must be internally write protected when V_{CC} to the I²C bus is powered down or V_{CC} to the component is dropped below normal operating levels.

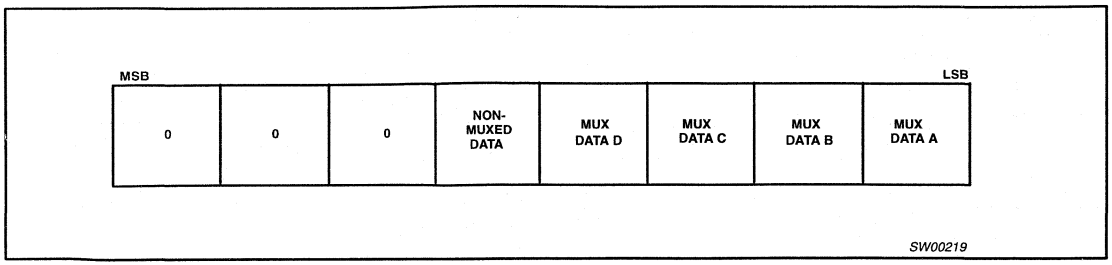
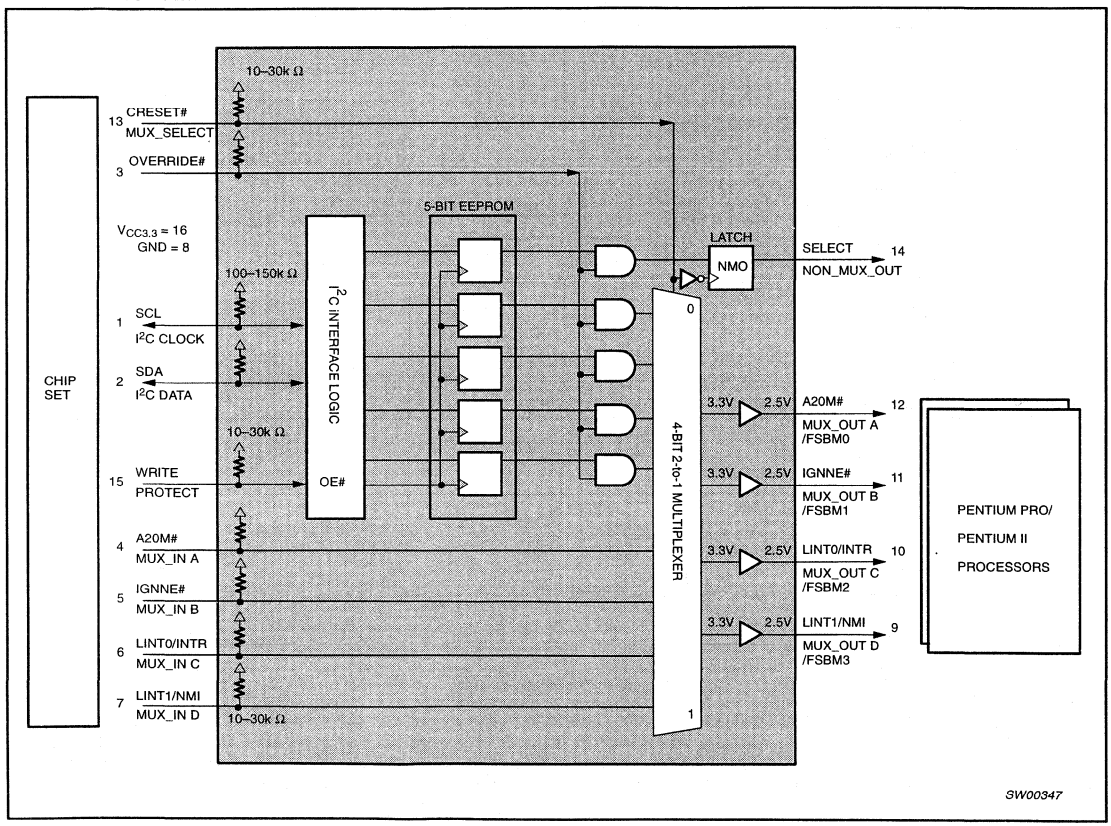


Figure 2. I²C Data Byte

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +4.6	V
V_I	DC input voltage	Note 3	−1.5 to V_{CC} +1.5	V
V_{OUT}	DC output voltage	Note 3	−0.5 to V_{CC} +0.5	V
T_{stg}	Storage temperature range		−60 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage		3.0	3.6	V
SCL, SDA	V_{IL} V_{IH} V_{OL}	I_{OL}= 3mA	−0.5 2.7	0.9 4.0 0.4	V
OVERRIDE#, MUX_IN, MUX_SELECT	V_{IL} V_{IH}		−0.5 2.0	0.8 4.0	V
MUX_OUT, NON_MUXED_OUT	I_{OL} I_{OH}			2.0 −2.0	mA
dt/dv	Input transition rise or fall time		0	10	ns/V
T_A	Operating temperature		0	70	°C

DC CHARACTERISTICS

SYMBOL	PARAMETER	LIMITS		UNIT
		Temp = 0°C to +70°C 3.0V < V_{CC} ≤ 3.6V		
		MIN	MAX	
SCL, SDA	V_{OL} I_{OL} (V_{OL} = 0.4V) I_{OL} (V_{OL} = 0.6V) I_{IL} (V_{IL} = 0.4V) I_{IH} (V_{IH} = 2.4V) V_{HYS}[1]	0 –7 –1.5 0.19	0.6 3.0 6.0 –32 –12 	V mA mA µA µA V
OVERRIDE#, WP, MUX_SELECT	I_{IL} I_{IH}	–86 –20	–267 –100	µA
MUX A ⇒ D	I_{IL} (V_{IL} = 0.4V) I_{IH} (V_{IH} = 2.4V)	–0.72 –0.166	–2.0 –0.75	mA
MUX_OUT	V_{OL} (I_{OL} = 100µA) V_{OL} (I_{OL} = 2.0mA) V_{OH} (I_{OH} = –100µA) V_{OH} (I_{OH} = –1.0mA)	–0.3 –0.3 2.0 1.7	0.4 0.7 2.625 2.625	V
NON_MUXED_OUT	V_{OL} (I_{OL} = 100µA) V_{OL} (I_{OL} = 2.0mA) V_{OH} (I_{OH} = –100µA) V_{OH} (I_{OH} = –2.0mA)	–0.5 –0.5 2.4 2.0	0.4 0.7 3.6 3.6	V
I_{CC}	Quiescent supply current (V_{CC} = 3.3V) V_I = 0V to V_{CC}		10	mA
I_{CC}	Quiescent supply current V_I = V_{CC}		500	µA
C_{IN}	All inputs		10	pF
	ESD protection	2.0		KV
	Input diode clamp voltage	–1.5		V

NOTES:
1. V_{HYS} is the hysteresis of Schmitt-Trigger inputs
2. Human body model

NON-VOLATILE STORAGE SPECIFICATIONS

Parameter	Specification
Memory cell data retention	10 years min
Number of memory cell write cycles	1,000 cycles min

AC CHARACTERISTICS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
T_{MPD}	Mux input to output propagation delay		20.0	ns
T_{SOV}	MUX_SELECT to output valid		22	ns
T_{OVN}	OVERRIDE# to NON_MUX output delay		15.0	ns
T_{OVM}	OVERRIDE# to mux output delay		25.0	ns
T_R	Output rise time	1.0	3.0	ns/V
T_F	Output fall time	1.0	3.0	ns/V
C_L	Test load capacitance on Muxed/Non-Muxed outputs		15	pF
	I²C BUS			
f_{SCL}	I²C clock frequency	10	400	KHz
T_{SCH}	I²C clock high time	600		ns
T_{SCL}	I²C clock low time	1.3		ns
T_{DSP}	I²C data spike time	0	50	ns
T_{SDS}	I²C data setup time	100		ns
T_{SDH}	I²C data hold time	0		ns
T_{ICR}	I²C input rise time (10–400pF bus)	20	300	ns
T_{ICF}	I²C input fall time (10–400pF bus)	20	300	ns
T_{BUF}	I²C bus free time between start and stop	1.3		ns
T_{STS}	I²C repeated start condition setup	600		ns
T_{STH}	I²C repeated start condition hold	600		ns
T_{SPS}	I²C stop condition setup	600		ns
C_B	I²C bus capacitive load		400	pF
T_W	Write cycle time[1]	TYPICAL = 15		ms

NOTE:
1. WRITE CYCLE time can only be measured indirectly during write cycle. The device will not acknowledge its I²C address.

CONTENTS

1 FEATURES

- Operating supply voltage:
  - 4.5 to 5.5 V (PCA8581)
  - 2.5 to 6.0 V (PCA8581C)
- Integrated voltage multiplier and timer for writing (no external components required)
- Automatic erase before write
- Low standby current; maximum 10 μA
- 8-byte page write mode
- Serial input/output bus (I²C-bus)
- Address by 3 hardware address pins
- Automatic word address incrementing
- Designed for minimum 10000 write cycles per byte
- 10 years minimum non-volatile data retention
- Infinite number of read cycles
- Pin and address compatibility to PCF8570C and PCF8582
- Operating ambient temperature: –25 to +85 °C.

2 GENERAL DESCRIPTION

The PCA8581 and PCA8581C are low power CMOS EEPROMs with standard and wide operating voltages:

4.5 to 5.5 V (PCA8581)

2.5 to 6.0 V (PCA8581C).

In the following text, the generic term 'PCA8581' is used to refer to both types in all packages except when otherwise specified.

The PCA8581 is organized as 128 words of 8-bytes.

Addresses and data are transferred serially via a two-line bidirectional bus (I²C-bus). The built-in word address register is incremented automatically after each written or read data byte. All bytes can be read in a single operation. Up to 8 bytes can be written in one operation, reducing the total write time per byte. Three address pins, A0, A1 and A2 are used to define the hardware address, allowing the use of up to 8 devices connected to the bus without additional hardware.

3 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage				
	PCA8581		4.5	5.5	V
	PCA8581C		2.5	6.0	V
I_{DD}	supply current (standby)	f_{SCL} = 0 Hz	–	10	μA
T_{amb}	operating ambient temperature		–25	+85	°C
T_{stg}	storage temperature	without EEPROM retention	–65	+150	°C
		with EEPROM retention	–65	+85	°C

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCA8581P	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1
PCA8581CP	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1
PCA8581T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1
PCA8581CT	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

5 BLOCK DIAGRAM

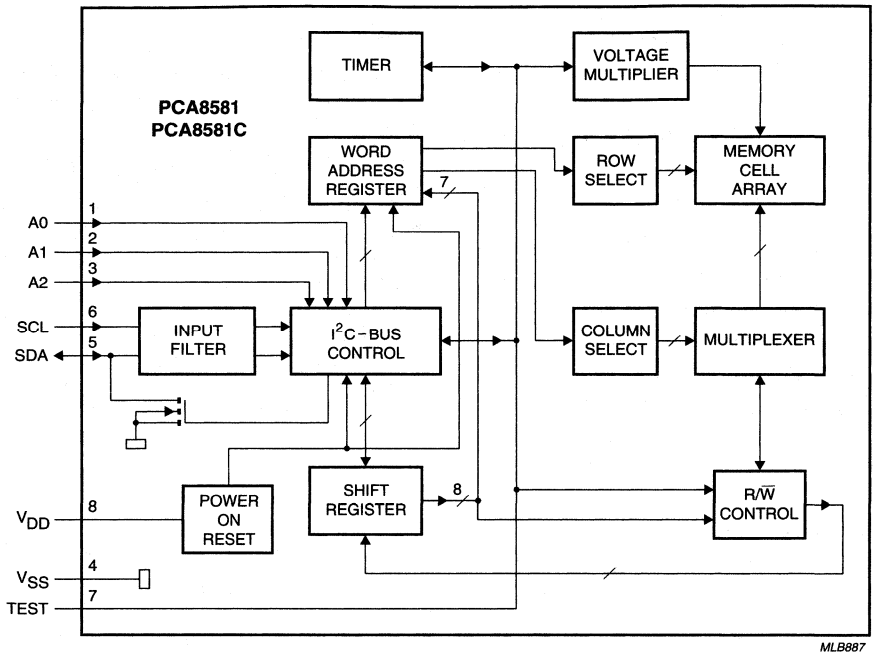


Fig.1 Block diagram.

6 PINNING

SYMBOL	PIN	DESCRIPTION
A0	1	hardware address input 0
A1	2	hardware address input 1
A2	3	hardware address input 2
V_{SS}	4	negative supply
SDA	5	serial data input/output
SCL	6	serial clock input
TEST	7	test output can be connected to V_{SS}, V_{DD} or left open-circuit
V_{DD}	8	positive supply

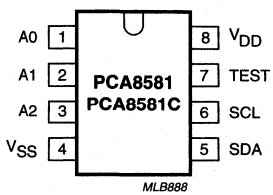


Fig.2 Pin configuration.

7 CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

7.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

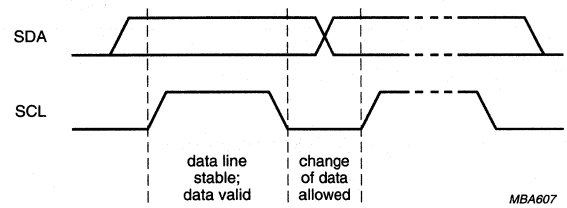


Fig.3 Bit transfer.

7.2 Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

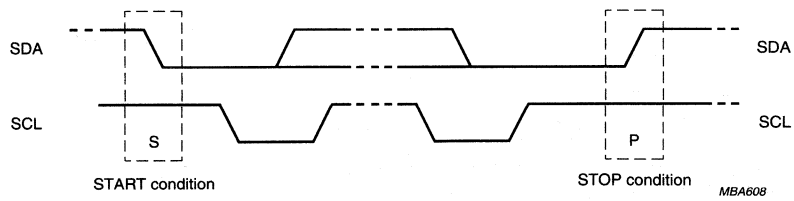


Fig.4 Definition of START and STOP conditions.

7.3 System configuration

A device generating a message is a 'transmitter', a device receiving a message is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves'.

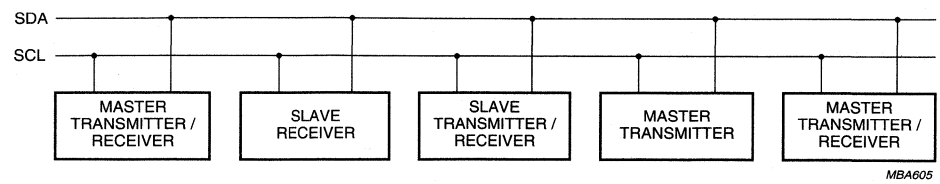


Fig.5 System configuration.

7.4 Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

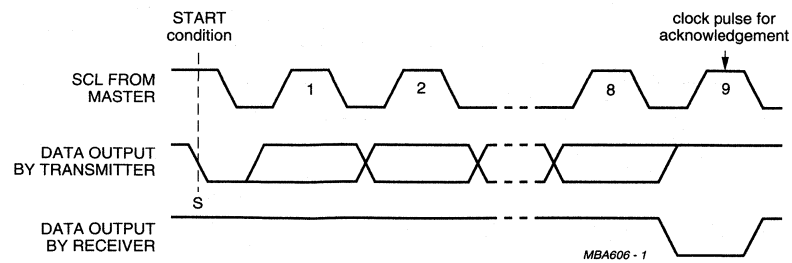


Fig.6 Acknowledgement on the I²C-bus.

7.5 I²C-bus protocol

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always carried out with the first byte transmitted after the start procedure. The I²C-bus configuration for the different PCA8581 WRITE and READ cycles is shown in Figs 7, 9 and 10.

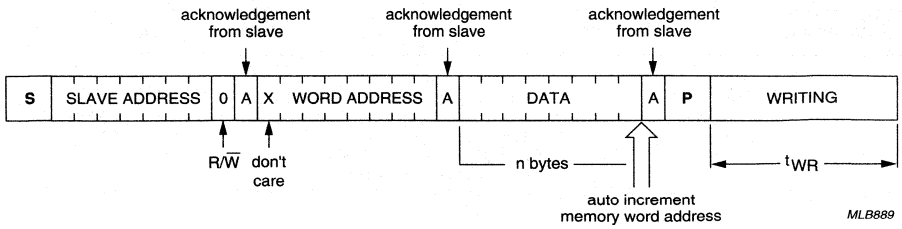
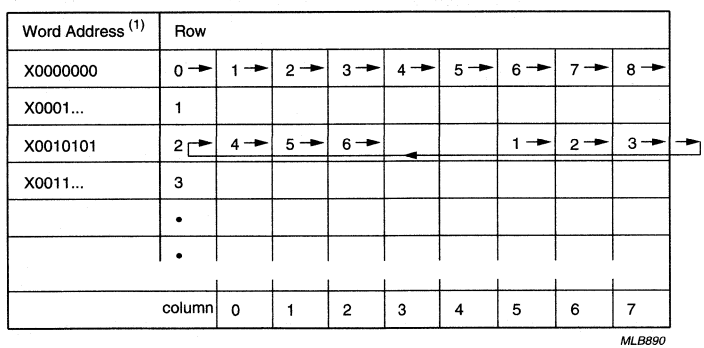


Fig.7 Master transmits to slave receiver (WRITE) mode.

After the word address, one-to-eight data bytes can be sent. The address is automatically incremented, but the four highest address bits (row) are internally latched. Therefore all bytes are written in the same row.

An example of writing eight bytes with word address X 0 0 0 0 0 0 0 and six bytes with word address X 0 0 1 0 1 0 1 is shown in Fig.8.



(1) X = don't care.

Fig.8 Writing eight and six bytes with different word addresses.

To transmit eight bytes in sequential order, begin with the lowest address bits 0 0 0. The data is written after a stop is detected. The data is only written if complete bytes have been received and acknowledged. Writing takes a time t_{WR} (6 to 10 ms) during which the device will not respond to its slave address. Note that to write the next row, a new write operation is required (start, slave address, row address, data and stop).

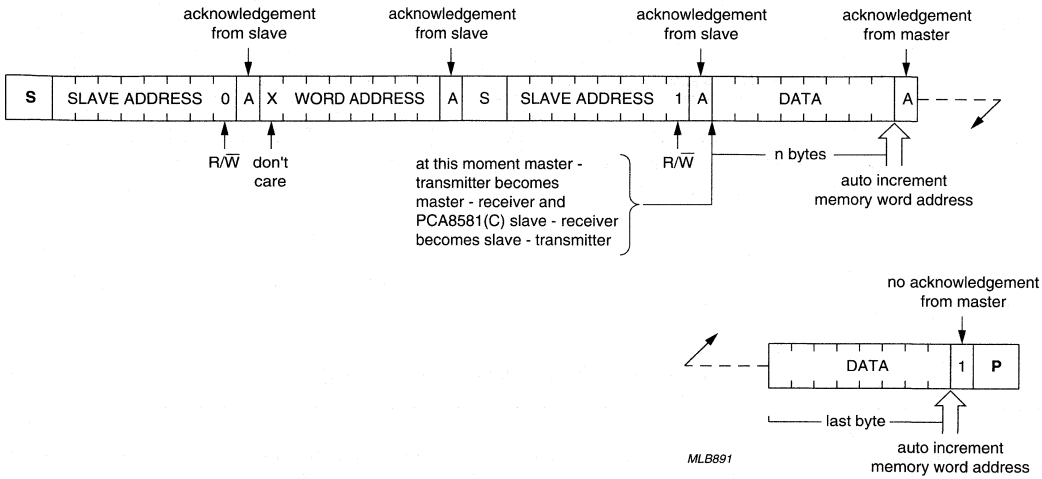


Fig.9 Master reads after setting word address (WRITE word address; READ data).

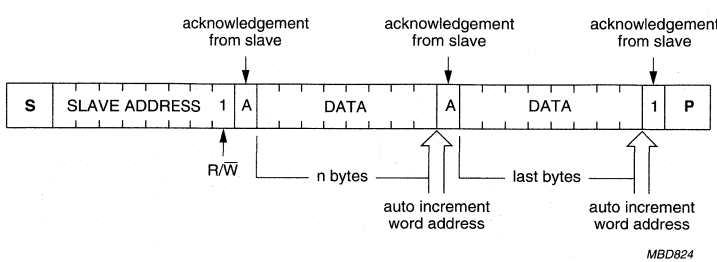


Fig.10 Master reads slave immediately after first byte (READ mode).

An unlimited number of data bytes can be read in one operation. The address is automatically incremented. If a read without setting the word address is performed after a write operation, the address pointer may point at a byte in the row after the previously written row. This occurs if, during writing, the three lowest address bits (column) rolled over.

8 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage (pin 8)		−0.3	+7.0	V
V_I	input voltage (any input)	measured via a 500 Ω resistor	−0.8	V_{DD} + 0.8	V
I_I	DC input current		–	±10	mA
I_O	DC output current		–	±10	mA
P_{tot}	total power dissipation per package		–	150	mW
P_O	power dissipation per output		–	50	mW
T_{amb}	operating ambient temperature		−25	+85	°C
T_{stg}	storage temperature	without EEPROM retention	−65	+150	°C
		with EEPROM retention	−65	+85	°C

9 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take precautions appropriate to handling MOS devices. Advice can be found in Data Handbook IC12 under *"Handling MOS Devices"*.

10 DC CHARACTERISTICS

V_{DD} = 2.5 to 6.0 V (PCA8581C); V_{DD} = 4.5 to 5.5 V (PCA8581); V_{SS} = 0 V; T_{amb} = −25 to +85 °C; note 1; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage					
	PCA8581C		2.5	–	6.0	V
	PCA8581		4.5	–	5.5	V
I_{DD}	supply current					
	standby mode	f_{SCL} = 0 Hz; V_{IL} = 0 V; V_{IH} = V_{DD}	–	–	10	µA
	during read cycle	f_{SCL} = 100 Hz; V_{IL} = 0 V; V_{IH} = V_{DD}	–	–	400	µA
	during write cycle	V_{IL} = 0 V; V_{IH} = V_{DD}	–	–	1000	µA
Inputs A0, A1, A2, SDA and SCL						
V_{IL}	LOW level input voltage		–	–	0.3V_{DD}	V
V_{IH}	HIGH level input voltage		0.7V_{DD}	–	–	V
I_{LI}	input leakage current	V_I = V_{DD} or V_{SS}	–	–	1	µA
C_i	input capacitance	V_I = V_{SS}	–	–	7	pF
Output SDA						
I_{OL}	LOW level output current	V_{OL} = 0.4 V	3	–	–	mA
Erase/write data						
t_{WR}	write time		–	7	10	ms
t_{RET}	data retention time		10	–	–	years

Note

1. The PCA8581C is guaranteed to be programmed with all locations 'FF' (hexadecimal) provided the device has been stored within the temperature limits −65 to +85 °C.

11 AC CHARACTERISTICS

All timing values are valid within the operating supply voltage and ambient temperature range and reference to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
I²C-bus timing (see Fig.11; note 1)					
f_{SCL}	SCL clock frequency	–	–	100	kHz
t_{SP}	tolerable spike width on bus	–	–	100	ns
t_{BUF}	bus free time	4.7	–	–	µs
$t_{SU;STA}$	START condition set-up time	4.7	–	–	µs
$t_{HD;STA}$	START condition hold time	4.0	–	–	µs
t_{LOW}	SCL LOW time	4.7	–	–	µs
t_{HIGH}	SCL HIGH time	4.0	–	–	µs
t_r	SCL and SDA rise time	–	–	1.0	µs
t_f	SCL and SDA fall time	–	–	0.3	µs
$t_{SU;DAT}$	data set-up time	250	–	–	ns
$t_{HD;DAT}$	data hold time	0	–	–	ns
$t_{VD;DAT}$	SCL LOW to data out valid	–	–	3.4	µs
$t_{SU;STO}$	STOP condition set-up time	4.0	–	–	µs

Note

1. A detailed description of the I²C-bus specification, with applications, is given in brochure *"The I²C-bus and how to use it"*. This brochure may be ordered using the code 9398 393 40011.

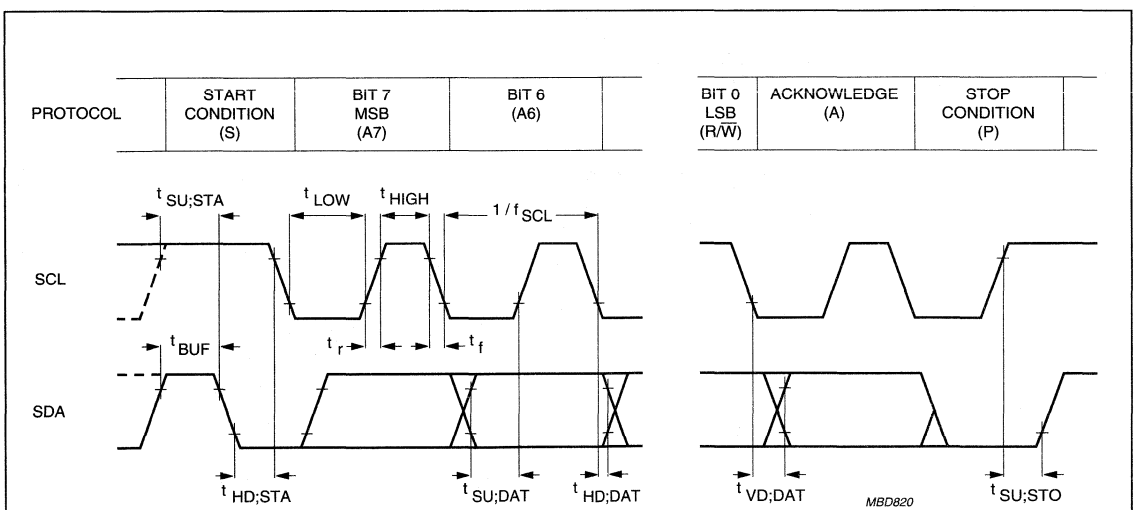
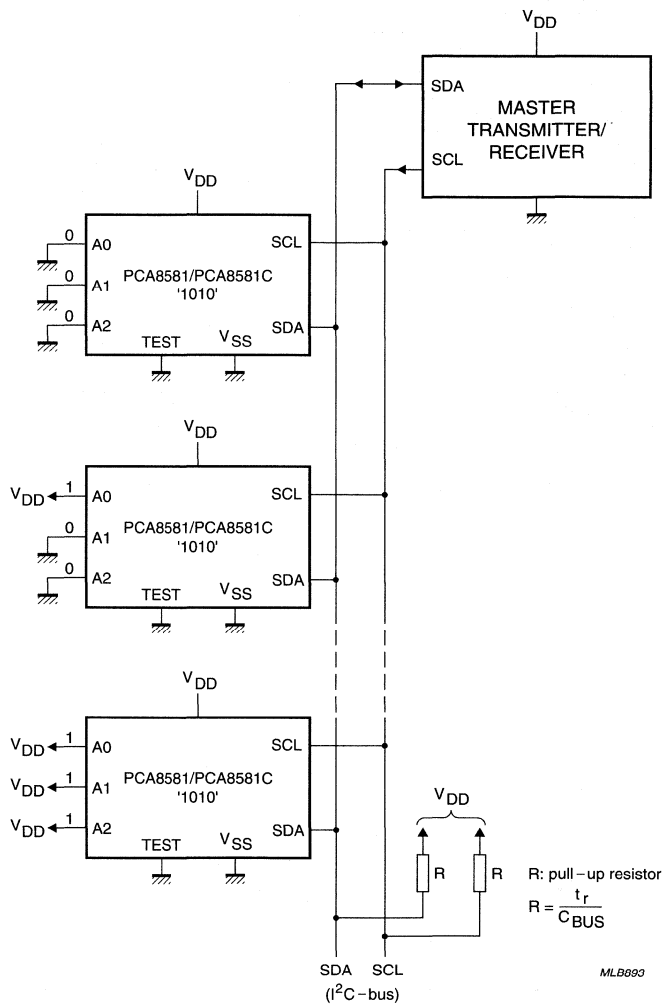


Fig.11 I²C-bus timing diagram; rise and fall times refer to V_{IL} and V_{IH}.

12 APPLICATION INFORMATION

12.1 Application example



Inputs A0, A1 and A2 must be connected to V_{DD} of V_{SS} but not left open-circuit.

Fig.12 Application diagram.

12.2 Slave address

The PCA8581 has a fixed combination 1 0 1 0 as group 1, while group 2 is fully programmable (see Fig.13).

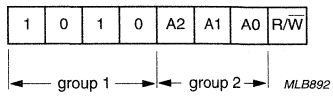
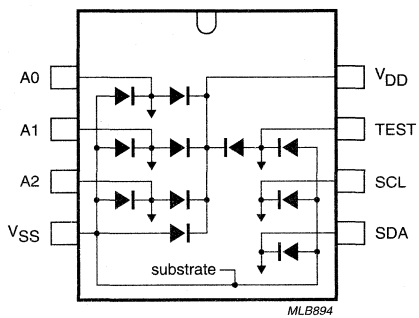


Fig.13 Slave address.

12.3 Diode protection



There is no connection between SCL and V_{DD}, and SDA and V_{DD}; this allows powering down the device without affecting I²C-bus operation.

Fig.14 Device diode protection.

Octal SMBus Registered Interface PCA9556

FEATURES

- SMBus compliance with fixed 3.3V voltage levels
- Operating power supply voltage range of 3.0V – 3.6V
- Active high polarity inverter register
- Write protect register
- Active low reset pin
- Low leakage current on power-down
- Noise filter on SCL/SDA inputs
- No glitch on power-up
- Internal power-on reset
- 8 I/O pins which default to 8 inputs
- High impedance open drain on I/O

DESCRIPTION

The PCA9556 is a silicon CMOS circuit which provides parallel input/output expansion for SMBus applications. The PCA9556 consists of an 8-bit input port register, 8-bit output port register, and an SMBus interface. It has low current consumption and a high impedance open drain output pin, I/O0.

The SMBus system master can reset the PCA9556 in the event of a timeout by asserting a LOW on the reset input. The SMBus system master can also invert the PCA9556 inputs by writing to their active HIGH polarity inversion bits. Finally, the SMBus system master can enable the PCA9556's I/Os as either inputs or outputs by writing to their I/O configuration bits.

The power-on reset sets the registers to their default values and initializes the SMBus state machine. The $\overline{\text{RESET}}$ pin causes the same reset/initialization to occur without depowering the part.

PIN CONFIGURATION

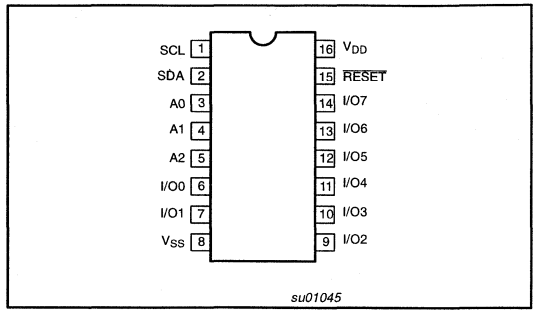


Figure 1. Pin configuration

PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	SCL	Serial clock line
2	SDA	Serial data line
3	A0	Address input 0
4	A1	Address input 1
5	A2	Address input 2
6	I/O0	I/O0 (open drain)
7	I/O1	I/O1
8	V_{SS}	Supply GROUND
9	I/O2	I/O2
10	I/O3	I/O3
11	I/O4	I/O4
12	I/O5	I/O5
13	I/O6	I/O6
14	I/O7	I/O7
15	$\overline{\text{RESET}}$	External reset (active LOW)
16	V_{DD}	Supply voltage

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	DRAWING NUMBER
16-Pin Plastic TSSOP16 Type I	0°C to +70°C	PCA9556 PW	SOT403-1

BLOCK DIAGRAM

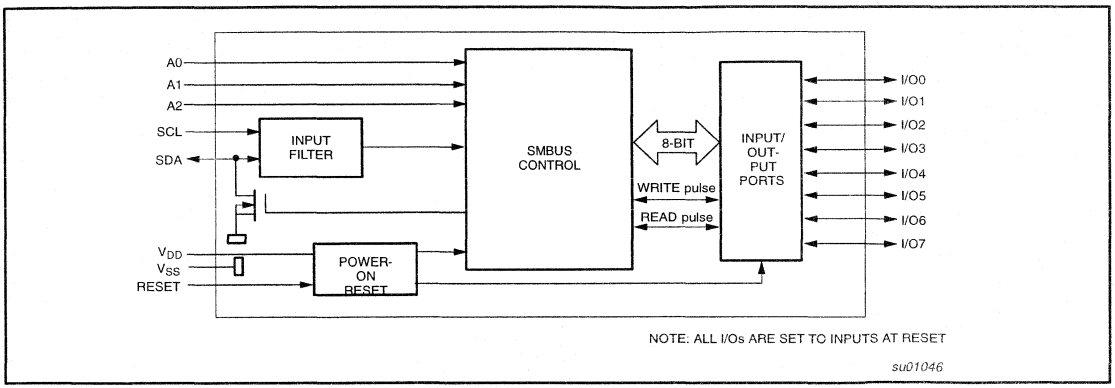


Figure 2. Block diagram

REGISTERS

Command Byte

Command	Protocol	Function
0	Read byte	Input port register
1	Read/write byte	Output port register
2	Read/write byte	Polarity inversion register
3	Read/write byte	I/O configuration register

The command byte is the first byte to follow the address byte during a write transmission. It is used as a pointer to determine which of the following registers will be written or read.

Register 0 – Input Port Register

I7	I6	I5	I4	I3	I2	I1	I0

This register is an input-only port. It reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by register 3. Writes to this register have no effect.

Register 1 – Output Port Register

bit	O7	O6	O5	O4	O3	O2	O1	O0
default	0	0	0	0	0	0	0	0

This register is an output-only port. It reflects the outgoing logic levels of the pins defined as outputs by register 3. Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, NOT the actual pin value.

Register 2 – Polarity Inversion Register

bit	N7	N6	N5	N4	N3	N2	N1	N0
default	1	1	1	1	0	0	0	0

This register enables polarity inversion of pins defined as inputs by register 3. If a bit in this register is set (written with '1'), the corresponding port pin's polarity is inverted. If a bit in this register is cleared (written with a '0'), the corresponding port pin's original polarity is retained.

Register 3 – Input/Output Configuration Register

bit	C7	C6	C5	C4	C3	C2	C1	C0
default	1	1	1	1	1	1	1	1

This register configures the directions of the I/O pins. If a bit in this register is set (written with '1'), the corresponding port pin is enabled as an input with high impedance output driver. If a bit in this register is cleared (written with '0'), the corresponding port pin is enabled as an output.

RESET

Power-on Reset

When power is applied to V_{DD}, an internal power-on reset holds the PCA9556 in a reset state until V_{DD} has reached V_{POR}. At that point, the reset condition is released and the PCA9556 registers and SMBus state machine will initialize to their default states.

External Reset

A reset can be accomplished by holding the $\overline{\text{RESET}}$ pin low for a minimum of T_W. The PCA9556 registers and SMBus state machine will be held in their default state until the $\overline{\text{RESET}}$ input is once again high. This input contains an internal pull-up, therefore, it may be left open if not used.

SIMPLIFIED SCHEMATIC OF I/O0

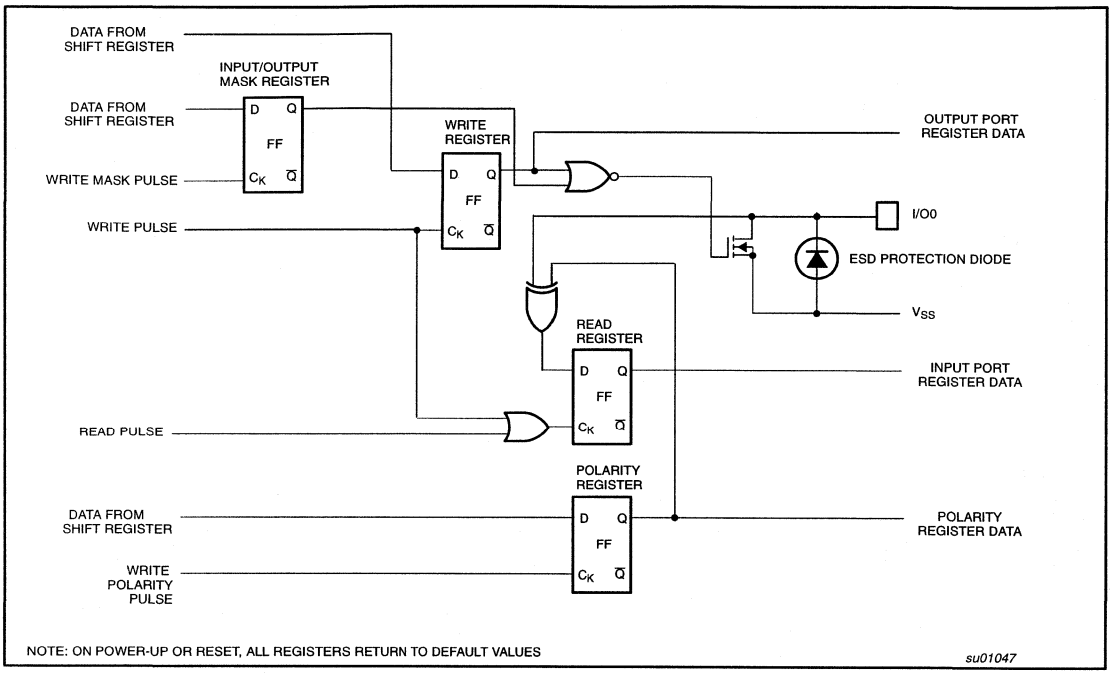


Figure 3. Simplified schematic of I/O0

SIMPLIFIED SCHEMATIC OF I/O1 TO I/O7

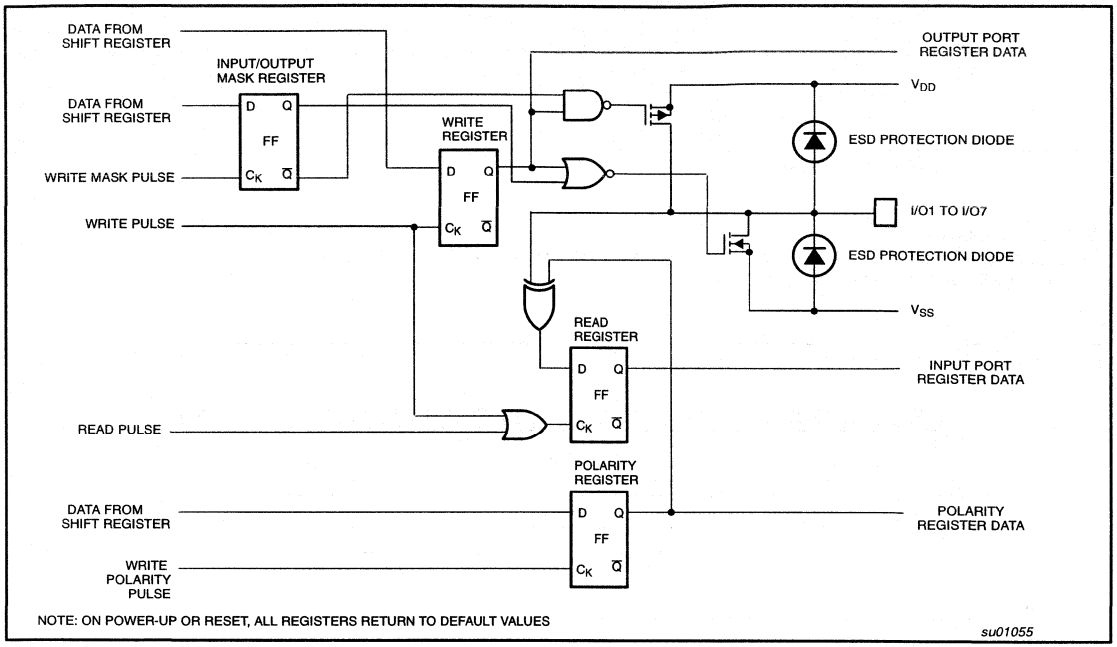


Figure 4. Simplified schematic of I/O1 to I/O7

SMBus Address

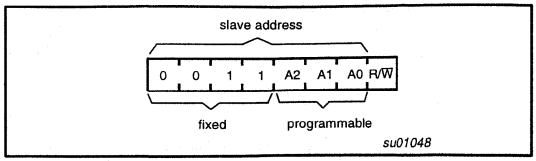


Figure 5. PCA9556 address

SMBus Transactions

Data is transmitted to the PCA9556 registers using Write Byte transfers (see Figures 6 and 7). Data is read from the PCA9556 registers using Read and Receive Byte transfers (see FIgures 8 and 9).

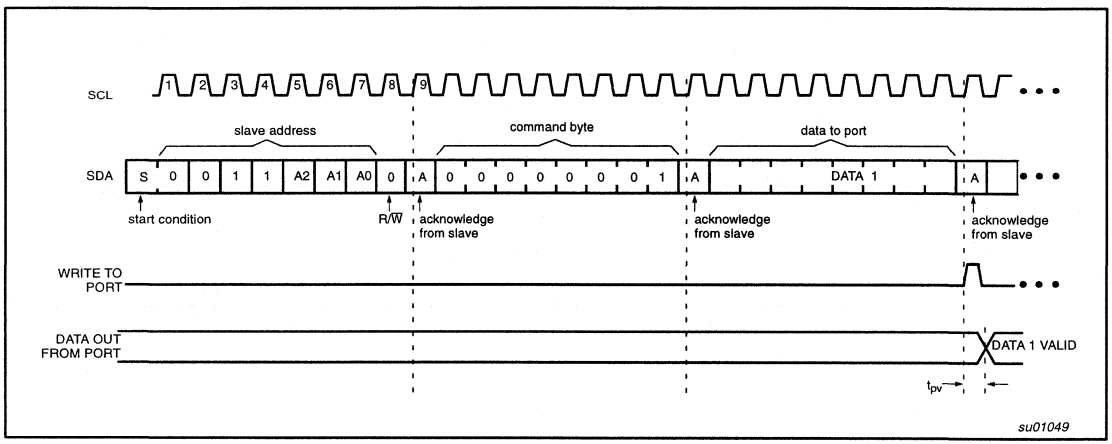


Figure 6. WRITE to output port register via Write Byte Protocol

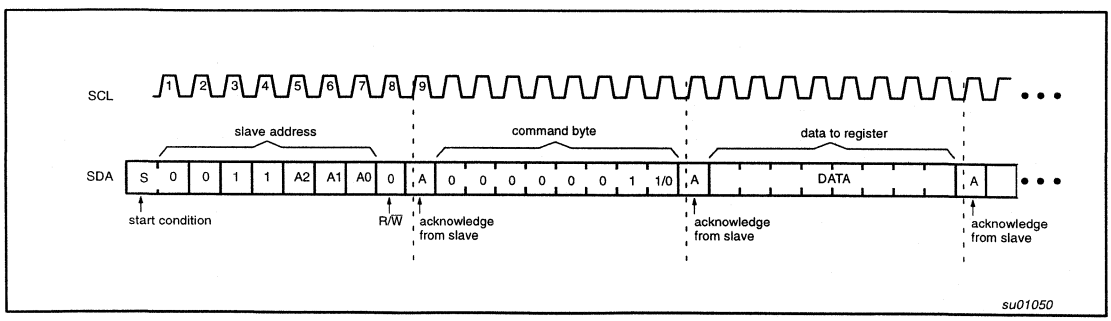


Figure 7. WRITE to I/O configuration or polarity inversion registers via Write Byte Protocol

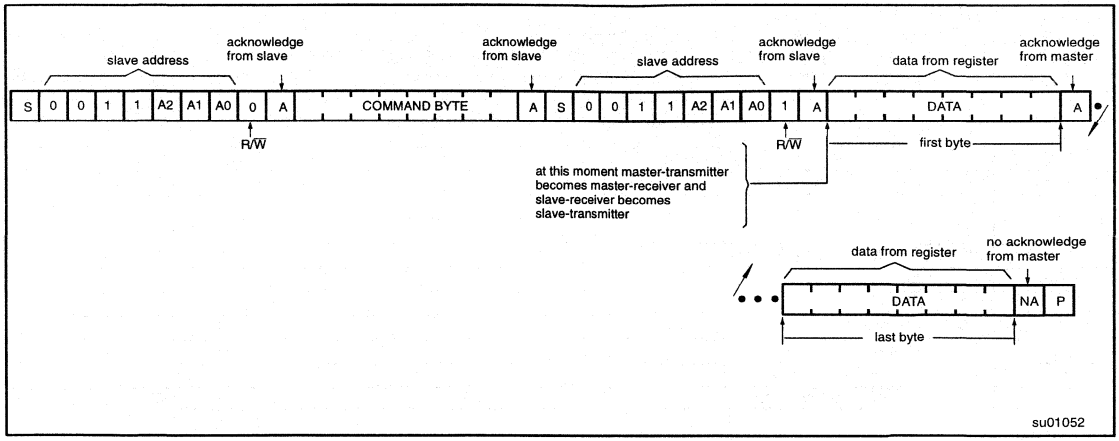


Figure 8. READ from register via Read byte protocol

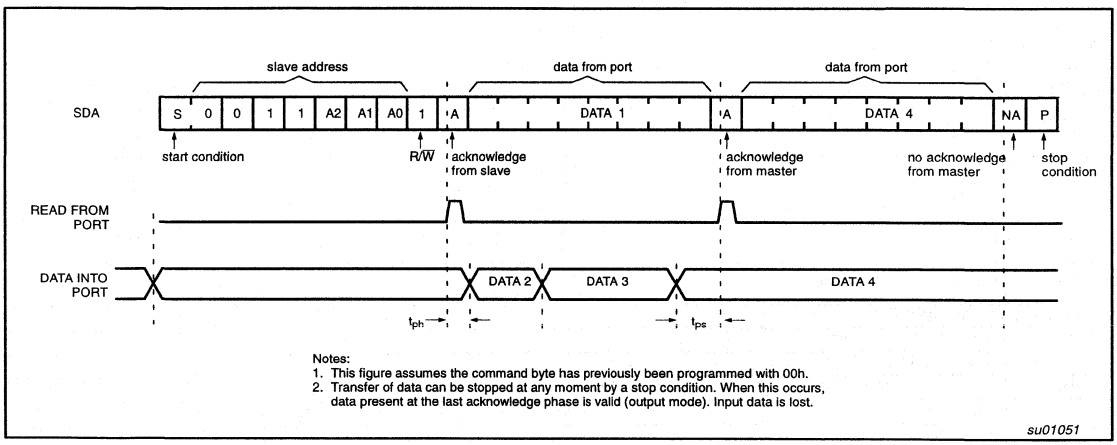


Figure 9. READ input port register via Receive byte protocol

ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{DD}	Supply voltage		−0.5	+4.6	V
V_I	Input voltage		V_{SS} − 0.5	V_{DD} + 0.5	V
I_I	DC input current		−	± 20	mA
$V_{I/O}$	DC voltage on an I/O as an input other than I/O0		V_{SS} − 0.5	V_{DD} + 0.5	V
$V_{I/O0}$	DC voltage on I/O0 as an input		V_{SS} − 0.5	4.6	V
$I_{I/O0}$	DC input current on I/O0		−	+400	µA
			−	−20	mA
$I_{I/O}$	DC output current on an I/O		−	± 20	mA
I_{DD}	Supply current		−		mA
I_{SS}	Supply current		−		mA
P_{tot}	Total power dissipation		−		mW
P_O	Power dissipation per output		−		mW
T_{stg}	Storage temperature range		−65	+150	°C
T_{amb}	Operating ambient temperature		0	+70	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take precautions appropriate to handling MOS devices. Advice can be found in Data Handbook IC24 under "*Handling MOS devices*".

DC CHARACTERISTICS

V_{DD} = 3.0 to 3.6 V; V_{SS} = 0 V; T_{amb} = 0 to +70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Supplies						
V_{DD}	Supply voltage		3.0		3.6	V
I_{DD}	Supply current	Operating mode; V_{DD} = 3.3 V; no load; V_I = V_{DD} or V_{SS}; f_{SCL} = 100 kHz		300	425	µA
I_{stb}	Standby current	Standby mode; V_{DD} = 3.3 V no load; V_I = V_{DD} or V_{SS}		25	50	µA
V_{POR}	Power-on reset voltage	V_{DD} = 3.3 V no load; V_I = V_{DD} or V_{SS}; note 1		1.3	2.4	V
input SCL; input/output SDA						
V_{IL}	LOW level input voltage		−0.5		0.8	V
V_{IH}	HIGH level input voltage		2.1		V_{DD} + 0.5	V
I_{OL}	LOW level output current	V_{OL} = 0.4V	3		−	mA
I_L	Leakage current	V_I = V_{DD} = V_{SS}	−1		+1	µA
C_I	Input capacitance	V_I = V_{SS}	−		10	pF
I/Os						
V_{IL}	LOW level input voltage		−0.5	−	0.8	V
V_{IH}	HIGH level input voltage		2.0	−	V_{DD} + 0.5	V
$I_{IHL(max)}$	Maximum allowed input current through protection diode (I/O1 – I/O7)	$V_I \geq V_{DD}$ or $V_I \leq V_{SS}$	−	−	±400	µA
I_{OL}	LOW level output current	V_{OL} = 0.55V; V_{DD} = 3.3V	8	10	−	mA
I_{OH}	HIGH level output current except I/O0	V_{OH} = 2.4V; V_{DD} = 3.3V	4	−		mA
	HIGH level output current on I/O0	V_{DD} = 3.6V; V_{OH} = 4.6V		−	1	µA
		V_{DD} = 0V; V_{OH} = 3.3V		−	1	
I_L	Input leakage current	V_{DD} = 3.6V; V_I = 0 or V_{DD}	−1		1	µA
C_I	Input capacitance		−	−	10	pF
C_O	Output capacitance		−	−	10	pF
Select Inputs A0, A1, A2, and RESET						
V_{IL}	LOW level input voltage		−0.5		0.8	V
V_{IH}	HIGH level input voltage		2.0		V_{DD} + 0.5	V
I_{LI}	Input leakage current		−1		1	µA

NOTE:

1. The power-on reset circuit resets the SMBus logic with $V_{DD} < V_{POR}$ and sets all I/Os to their default values

AC SPECIFICATIONS

SYMBOL	PARAMETER	LIMITS		UNITS
		MIN	MAX	
F_{SBM}	SMB operating frequency	10	100	KHz
T_{BUF}	Bus free time between stop and start conditions	4.7		µs
$T_{HO:STA}$	Hold time after (repeated) start condition	4.0		µs
$T_{SU:STA}$	Repeated start condition setup time	4.7		µs
$T_{HO:DAT}$	Data hold time	300		ns
$T_{SU:DAT}$	Data setup time	250		ns
T_{LOW}	Clock LOW period	4.7		µs
T_{HIGH}	Clock HIGH period	4.0		µs
T_F	Clock/Data fall time		300	ns
T_R	Clock/Data rise time		1000	ns
Port Timing				
T_{PV}	Output data valid		4	µs
T_{PS}	Input data setup time	0		µs
T_{PH}	Input data hold time	4		µs
Reset				
T_W	Reset pulse width	2		ns

CONTENTS

1K dual mode serial EEPROM PCB2421

1 FEATURES

- Single supply with operation 4.5 to 5.5 V
- Completely implements DDC1/DDC2B interface for monitor identification
- Low power CMOS technology
- Two-wire I^2C-bus interface
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 8 bytes
- Write-protect pin
- 100 kHz I^2C-bus compatibility
- Designed for 10000 erase/write cycles minimum
- Data retention greater than 10 years
- 8-pin DIP and SO package
- Temperature range 0 to +70 °C.

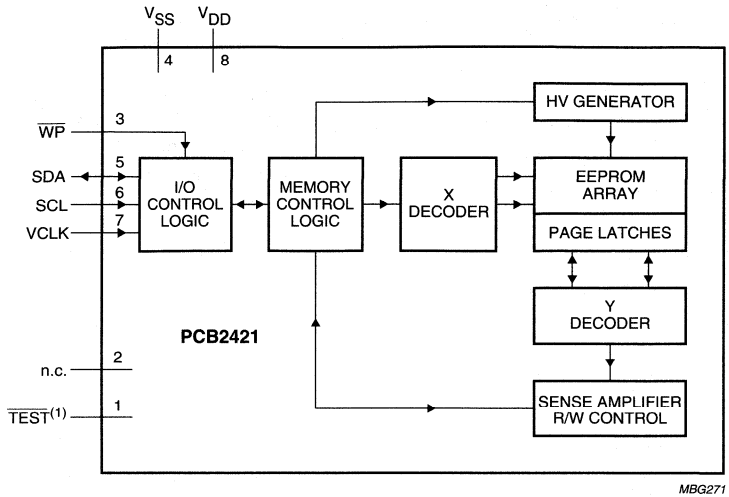
2 GENERAL DESCRIPTION

The Philips PCB2421 is a 128 × 8-bit dual mode serial Electrically Erasable PROM (EEPROM).
This device is designed for use in applications requiring storage and serial transmission of configuration and control information. Two modes of operation have been implemented: transmit-only mode (DDC1 mode) and bidirectional mode (DDC2B, or I^2C-bus mode). Upon power-up, the device will be in the transmit-only mode, sending a serial bitstream of the entire memory array contents, clocked by the VCLK pin. A valid HIGH-to-LOW transition on the SCL pin will cause the device to enter the bidirectional mode, with byte selectable read/write capability of the memory array. The PCB2421 is available in a standard 8-pin dual in-line and 8-pin small outline package operating in a commercial temperature range.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCB2421P	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1
PCB2421T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

4 BLOCK DIAGRAM



(1) Factory use only.

Fig.1 Block diagram.

5 PINNING

SYMBOL	PIN	DESCRIPTION
$\overline{TEST}$	1	factory use only: must be tied to V_{DD}; may not be left open-circuit
n.c.	2	may be tied to V_{SS}, V_{DD}, or left open-circuit
$\overline{WP}$	3	write protect input (LOW = write protected, HIGH = not write protected); may not be left open-circuit
V_{SS}	4	ground
SDA	5	serial data input/output
SCL	6	serial clock input/output (DDC2B)
VCLK	7	serial clock input (transmit-only mode, DDC1)
V_{DD}	8	supply voltage

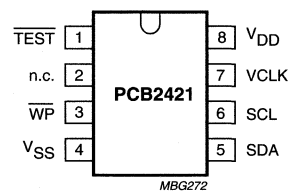


Fig.2 Pin configuration.

6 FUNCTIONAL DESCRIPTION

The PCB2421 operates in two modes, the transmit-only mode (DDC1) and the bidirectional mode (DDC2, or I²C-bus mode). There is a separate two-wire protocol to support each mode, each having a separate clock input and sharing a common data line (SDA). The device enters the transmit-only mode (DDC1) upon power-up. In this mode the device transmits data bits on the SDA pin in response to a clock signal on the VCLK pin. The device will remain in this mode until a valid HIGH-to-LOW transition is placed on the SCL input. When a valid transition on SCL is recognized, the device will switch into the bidirectional mode (see Fig.3). The only way to switch the device back to the transmit-only mode (DDC1) is to remove power from the device.

6.1 Transmit-only mode (DDC1)

The device will power-up in the transmit-only mode. This mode supports a unidirectional two-wire protocol for transmission of the contents of the memory array (see Fig.12). The PCB2421 requires that it be initialized prior to valid data being sent in the transmit-only mode (see Section "Initialization procedure", and Fig.4).

In this mode, data is transmitted on the SDA pin in 8-bit bytes, each byte followed by a ninth clock pulse during which time SDA is left high-impedance. The clock source for the transmit-only mode is provided on the VCLK pin; a data bit is output on the rising edge on this pin. The 8 bits in each byte are transmitted most significant bit first. Each byte within the memory array will be output in sequence. When the last byte in the memory array is transmitted, the output will wrap around to the first location and continue. The bidirectional mode clock (SCL) pin must be held HIGH for the device to remain in the transmit-only mode.

6.2 Initialization procedure

At power-on, after V_{DD} has stabilized, the device will be in the transmit-only mode. Nine clock cycles on the VCLK pin must be given to the device for it to perform internal synchronization. During this period, the SDA pin will be in a high-impedance state. On the rising edge of the tenth clock cycle, the device will output the first valid data bit which will be the most significant bit of a byte. The device will power-up with address pointer at 00H (see Fig.4).

6.3 Bidirectional mode (DDC2B, I²C-bus mode)

The PCB2421 can be switched into the bidirectional mode (see Fig.3) by applying a valid HIGH-to-LOW transition on the bidirectional mode clock (SCL).

When the device has been switched into the bidirectional mode, the VCLK input is disregarded. This mode supports a two-wire bidirectional data transmission protocol (I²C-bus protocol). In the I²C-bus protocol, a device that sends data on the bus is defined to be the transmitter, and a device that receives data from the bus is defined to be the receiver. The bus must be controlled by a master device that generates the bidirectional mode clock, controls access to the bus, and generates the START and STOP conditions, while the PCB2421 acts as slave. Both master and slave can operate as transmitter or receiver, but the master device determines which mode is activated.

6.3.1 BIDIRECTIONAL MODE BUS CHARACTERISTICS

The following bus protocol has been defined:

- Data transfer may be initiated only when the bus is not busy
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (see Fig.6).

6.3.2 BUS NOT BUSY (A)

Both data (SDA) and clock (SCL) lines remain HIGH.

6.3.3 START CONDITION (B)

A HIGH-to-LOW transition of the SDA line while SCL is HIGH determines a START condition. All commands must be preceded by a START condition.

6.3.4 STOP CONDITION (C)

A LOW-to-HIGH transition of the SDA line while SCL is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

6.3.5 DATA VALID (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data. Each data transfer is initiated with a START condition and terminated with a STOP condition. The maximum number of data bytes transferred between the START and STOP conditions during a write operation is 8 bytes (see Section "Page write" and Fig.5).

The maximum number of data bytes transferred between START and STOP conditions during a read operation is unlimited.

6.3.6 ACKNOWLEDGE

The PCB2421, when addressed in DDC2B mode, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra (9th) clock pulse which is associated with this acknowledge bit. The PCB2421 does not generate an acknowledge if an internal programming cycle is in progress (SDA line is left HIGH during the 9th clock pulse). The PCB2421 generates an acknowledge by pulling down the SDA line during the acknowledge pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Set-up and hold times must also be taken into account. The master receiver must signal an end of data to the PCB2421 by **not** generating an acknowledge bit on the last byte that has been clocked out of the slave transmitter. In this case, the slave transmitter PCB2421 must leave the data line HIGH to enable the master to generate the STOP condition.

6.3.7 SLAVE ADDRESS

After generating a START condition, the bus master transmits the slave address (MSB first) consisting of a 7-bit device address (1010000) for the PCB2421. The eighth bit of the slave address determines if the master device wants to read or write to the PCB2421 ($R/\overline{W}$ bit) (see Fig.7). The PCB2421 monitors the bus for its corresponding slave address all the time. It generates an acknowledge bit if the slave address was true and it is not in a programming mode.

Table 1 Slave address

OPERATION	SLAVE ADDRESS	$R/\overline{W}$
Read	1010000	1
Write	1010000	0

6.4 Write operation

6.4.1 BYTE WRITE

Following the START condition from the master, the device address (7 bits), and the $R/\overline{W}$ bit (logic LOW for write) is placed on the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore the next byte transmitted by the master is the word address and will be written into the address pointer of the PCB2421. After receiving another acknowledge signal from the PCB2421, the master device will transmit the data word to be written into the addressed memory location. The PCB2421 acknowledges again and the master generates a STOP condition. This initiates the internal write cycle, and during this time the PCB2421 will not generate acknowledge signals.

6.4.2 PAGE WRITE

For a page write, the write control byte, word address, and the first data byte are transmitted to the PCB2421 in the same way as in a single byte write. But instead of generating a STOP condition the master transmits up to eight data bytes to the PCB2421 which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a STOP condition. After the receipt of each word, the three lower order address pointer bits are internally incremented by one. The higher order four bits of the word address remain constant. A maximum of 8 bytes can be written in one operation. As with the byte write operation, once the STOP condition is received an internal write cycle will begin (see Figs 5 and 8).

6.5 Acknowledge polling

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the STOP condition for a write command has been issued from the master, the device initiates the internally timed write cycle. Acknowledge (ACK) polling can be initiated immediately. This involves the master sending a START condition followed by the control byte for a write command ($R/\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Fig.9 for flow diagram.

6.6 Write protection

Pin 3 is a write protect input ($\overline{WP}$). In the DDC1 mode, the PCB2421 can only be read according to the DDC1 protocol, hence the $\overline{WP}$ input has no effect in this mode. In the DDC2B mode, when $\overline{WP}$ is connected to ground, the entire EEPROM is write-protected, regardless of other pin states. When connected to V_{DD}, write-protection is disabled and the EEPROM may be programmed. $\overline{WP}$ may not be left open-circuit.

Table 2 Mode configurations

DDC	$\overline{WP}$	MODE
DCC1	X[1]	R
DCC2	1	R/W
	0	R

Note

1. Where X = don't care.

6.7 Read operation

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to logic 1. There are three basic types of read operations: current address read, random read, and sequential read.

6.7.1 CURRENT ADDRESS READ

The PCB2421 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address 'n', the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/W set to logic 1, the PCB2421 issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a STOP condition and the PCB2421 discontinues transmission (see Fig.10).

6.7.2 RANDOM READ

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, the word address must first be set. This is done by sending the word address to the PCB2421 as part of a normal write operation. After the word address is sent, the master generates a REPEATED START condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. The master then issues the control byte again but with the R/W bit set to logic 1. The PCB2421 will then issue an acknowledge and transmits the 8-bit data word. The master will not acknowledge the transfer but does generate a STOP condition and the PCB2421 discontinues transmission (see Fig.11).

6.7.3 SEQUENTIAL READ

Sequential reads are initiated in the same way as a random read except that after the PCB2421 transmits the first data byte, the master issues an acknowledge as opposed to a STOP condition in a random read. This directs the PCB2421 to transmit the next sequentially addressed 8-bit word. To provide sequential reads the PCB2421 contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation.

6.8 Pin description

6.8.1 SDA

This pin is used to transfer addresses and data into and out of the device, when the device is in the bidirectional (I^2C-bus, DDC2B) mode. In the transmit-only mode (DDC1), which only allows data to be read from the device, data is also transferred on the SDA pin. This pin is an open-drain terminal, therefore the SDA bus requires a pull-up resistor connected to V_{DD} (typically 10 kΩ for 100 kHz). See brochure *"The I^2C-bus and how to use it"* (order no. 9398 393 40011) or *"Data Handbook IC12"*.

6.8.2 SCL

This pin is the clock input for the bidirectional mode (I^2C-bus, DDC2B), and is used to synchronize data transfer to and from the device. It is also used as the signalling input to switch the device from the transmit-only mode to the bidirectional mode. It must remain HIGH for the chip to continue operation in the transmit-only mode (DDC1).

6.8.3 VCLK

This pin is the clock input for the transmit-only mode (DDC1). In the transmit-only mode, each bit is clocked out on the rising edge of this signal. In DDC2B mode, this input is a don't care.

6.8.4 $\overline{WP}$

This pin is used to inhibit writing of the EEPROM. When this pin is connected to ground, writing of the EEPROM is inhibited. When connected to V_{DD} (and VCLK = V_{DD}), the EEPROM can be programmed. $\overline{WP}$ may not be left open-circuit. $\overline{WP}$ input is a 'don't care' in DDC1 mode.

6.8.5 $\overline{TEST}$

Pins 1 is a $\overline{TEST}$ pin for factory use only. It must be connected to V_{DD} in the application.

6.8.6 N.C.

This pin has no connection and may be tied to V_{SS}, V_{DD} or left open-circuit.

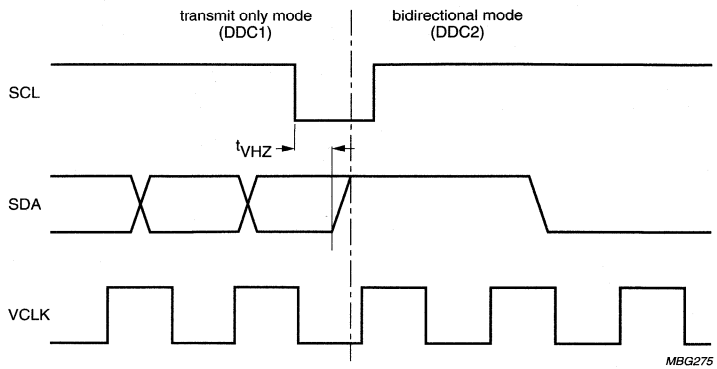


Fig.3 Mode transition diagram.

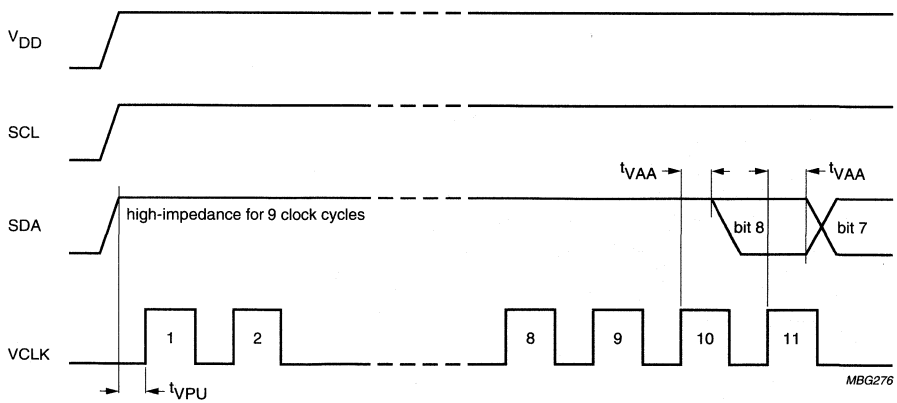


Fig.4 Device initialization diagram.

Word Address	Row								
X0000000	0 →	1 →	2 →	3 →	4 →	5 →	6 →	7 →	8 →
X0001...	1								
X0010101	2 →	4 →	5 →	6			1 →	2 →	3 →
X0011...	3								
	•								
	•								
column	0	1	2	3	4	5	6	7	

MBG277

X = don't care.

Fig.5 Example of writing 8 bytes with word address X0000000 and 6 bytes with word address X0010101.

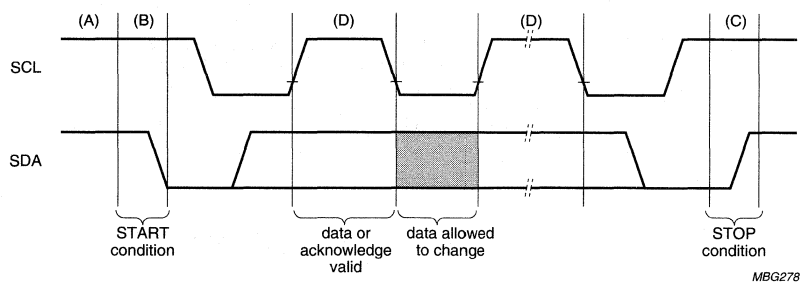


Fig.6 DDC2B data transfer sequence on the I²C-bus.

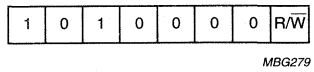


Fig.7 Slave address.

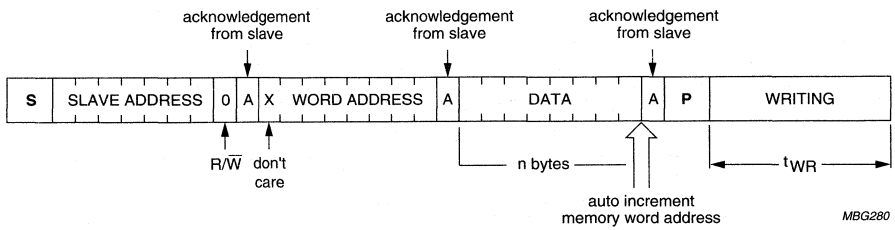


Fig.8 I²C-bus write protocol (n = maximum 8 bytes).

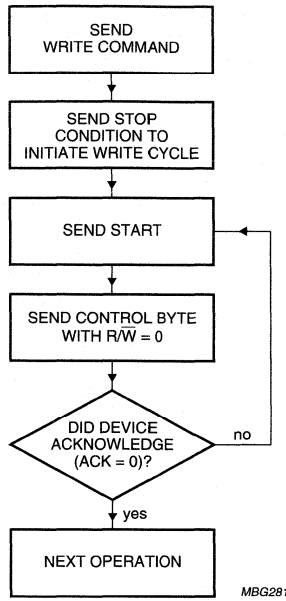


Fig.9 Acknowledge polling.

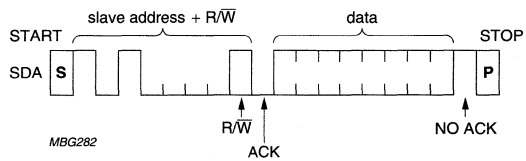


Fig.10 Current address read.

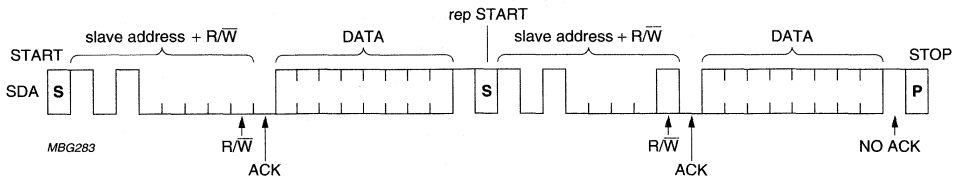


Fig.11 Random read.

7 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		−0.3	+7.0	V
V_n	input voltage on any pin	measured via 500 Ω resistor	−0.5	$V_{DD(max)}$ + 0.5	V
I_I	DC input current		−10	+10	mA
I_O	DC output current		−10	+10	mA
P_{tot}	total power dissipation		−	150	mW
P_o	power dissipation per output		−	50	mW
T_{stg}	storage temperature	without EEPROM retention	−65	+150	°C
		with EEPROM retention	−65	+70	°C
T_{amb}	operating ambient temperature		0	+70	°C
V_{es}	electrostatic discharge	note 1	−2000	+2000	V

Note

1. Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

8 DC CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; V_{SS} = 0 V; T_{amb} = 0 to +70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		4.5	−	5.5	V
V_{IH}	HIGH level input voltage (pins 3, 5 and 6)		0.7V_{DD}	−	−	V
V_{IL}	LOW level input voltage (pins 3, 5 and 6)		−	−	0.3V_{DD}	V
$V_{IH(7)}$	HIGH level input voltage (pin 7)		2.0	−	−	V
$V_{IL(7)}$	LOW level input voltage (pin 7)		−	−	0.8	V
V_{OL}	LOW level output voltage	I_{OL} = 3 mA; V_{DD} = 4.5 V	−	−	0.4	V
I_{LI}	input leakage current	V_I = 0 to 5.5 V	−10	−	+10	µA
I_{LO}	output leakage current	V_O = 0 to 5.5 V	−10	−	+10	µA
$I_{DD(write)}$	operating write current	f_{SCL} = 100 kHz; V_{DD} = 5.5 V	−	−	1000	µA
$I_{DD(read)}$	operating read current	f_{SCL} = 100 kHz; V_{DD} = 5.5 V	−	−	400	µA
$I_{DD(st)}$	standby current	V_{DD} = 5.5 V; DDC2B mode; VCLK = SDA = SCL = V_{DD}	−	−	30	µA

9 EEPROM CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; V_{SS} = 0 V; T_{amb} = 0 to +70 °C; unless otherwise specified.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{WR}	EEPROM write time	−	20	ms
N_{CYC}	EEPROM endurance	10000	−	E/W cycles
t_{RET}	EEPROM retention	10	−	years

10 AC CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; V_{SS} = 0 V; T_{amb} = 0 to +70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DDC1 mode (transmit-only; unidirectional)						
t_{VAA}	output valid from VCLK	see Fig.12; note 1	–	1	–	µs
t_{VHIGH}	VCLK HIGH time	see Fig.12	20	–	–	µs
t_{VLOW}	VCLK LOW time	see Fig.12	20	–	–	µs
t_{VHZ}	mode transition time	see Fig.3; note 1	–	500	–	ns
t_{SP}	input filter spike suppression time		–	–	100	ns
t_{vpu}	DDC1 mode power-up time	see Fig.4	–	5	–	µs
DDC2B mode (bidirectional; I²C-bus mode); see Fig.13						
f_{SCL}	serial clock frequency		0	–	100	kHz
t_{HIGH}	serial clock HIGH time		4	–	–	µs
t_{LOW}	serial clock LOW time		4.7	–	–	µs
t_r	SCL and SDA rise time		–	–	1	µs
t_f	SCL and SDA fall time		–	–	0.3	µs
$t_{HD;STA}$	START condition hold time		4	–	–	µs
$t_{SU;STA}$	START condition set-up time		4.7	–	–	µs
$t_{HD;DAT}$	data input hold time		0	–	–	µs
$t_{SU;DAT}$	data input set-up time		250	–	–	ns
$t_{SU;STO}$	STOP condition set-up time		4	–	–	µs
t_{BUF}	bus free time	note 2	4.7	–	–	µs
t_{SP}	input filter spike suppression		–	–	100	ns

Notes

1. The rise time for SDA returning HIGH must be observed after this period.
2. This is the time that the bus must be free before a new transmission can start.

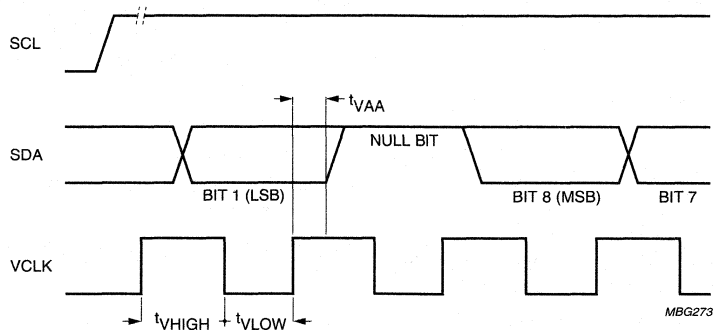


Fig.12 Transmit-only mode (DDC1).

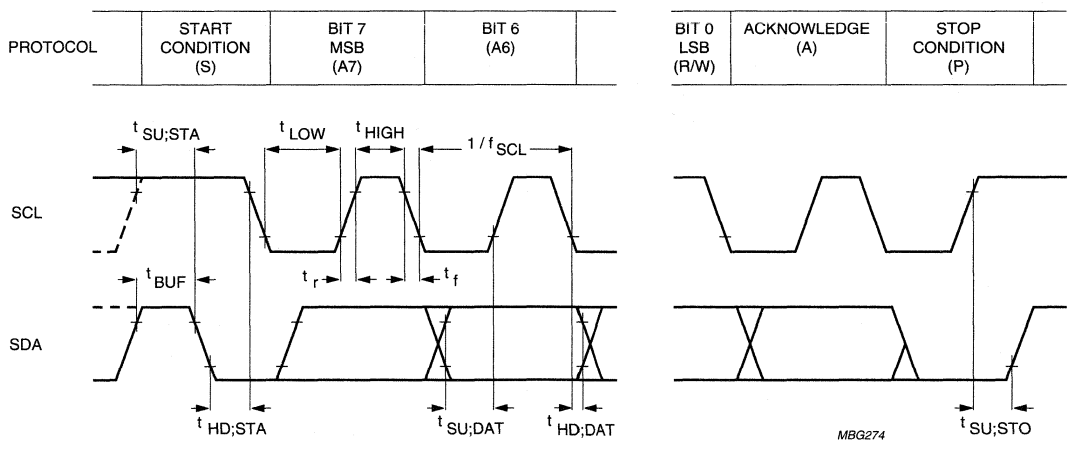


Fig.13 DDC2B (I^2C-bus timing).

11 APPLICATION INFORMATION

11.1 Diode protection

There is no diode connection between VCLK and V_{DD}, SCL and V_{DD} and SDA and V_{DD} (see Fig.14). This allows powering-down the device without affecting the I^2C-bus operation or loading the VCLK driver.

11.2 Functional compatibility with microchip 24CL21 dual mode EEPROM

The Philips PCB2421 is pin and function compatible with the 24CL21 providing the following measures are taken in the application.

1. Pin 1 ($\overline{TEST}$) must be tied to V_{DD}
2. Pin 3 ($\overline{WP}$) must be tied to V_{DD}. This inhibits the write protection function which does not exist on the 24CL21 at this time
3. Maximum 100 kHz DDC2B clock frequency
4. Maximum 25 kHz DDC1 VCLK clock frequency
5. During EEPROM programming a maximum write time of 20 ms must be observed
6. 8-byte maximum during page write must be observed
7. During operation V_{DD} must be between 4.5 and 5.5 V
8. An operating temperature between 0 and +70 °C must be observed
9. Output valid from VCLK (t_{VAA}) typical 1 µs must be observed
10. DDC1 mode power-up time (t_{VPU}) typical 5 µs should be observed.

Remark: VCLK is 'don't care' in the DDC2B mode.

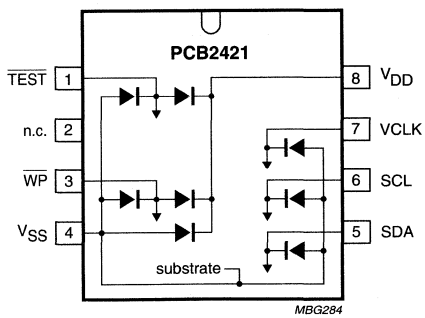
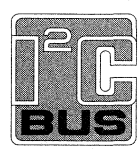


Fig.14 PCB2421 diode protection.

CONTENTS



1 FEATURES

- DTMF, modem and musical tone generation
- Stabilized output voltage level
- Low output distortion with on-chip filtering conforming to CEPT recommendations
- Latched inputs for data bus applications
- I^2C-bus compatible
- Selection of parallel or serial (I^2C-bus) data input (PCD3311C).

2 GENERAL DESCRIPTION

The PCD3311C and PCD3312C are single-chip silicon gate CMOS integrated circuits. They are intended principally for use in telephone sets to provide the dual-tone multi-frequency (DTMF) combinations required for tone dialling systems. The various audio output frequencies are generated from an on-chip 3.58 MHz quartz crystal-controlled oscillator. A separate crystal is used, and a separate microcontroller is required to control the devices.

Both the devices can interface to I^2C-bus compatible microcontrollers for serial input. The PCD3311C can also interface directly to all standard microcontrollers, accepting a binary coded parallel input.

With their on-chip voltage reference the PCD3311C and PCD3312C provide constant output amplitudes which are independent of the operating supply voltage and ambient temperature.

An on-chip filtering system assures a very low total harmonic distortion in accordance with CEPT recommendations.

In addition to the standard DTMF frequencies the devices can also provide:

- Twelve standard frequencies used in simplex modem applications for data rates from 300 to 1200 bits per second
- Two octaves of musical scales in steps of semitones.

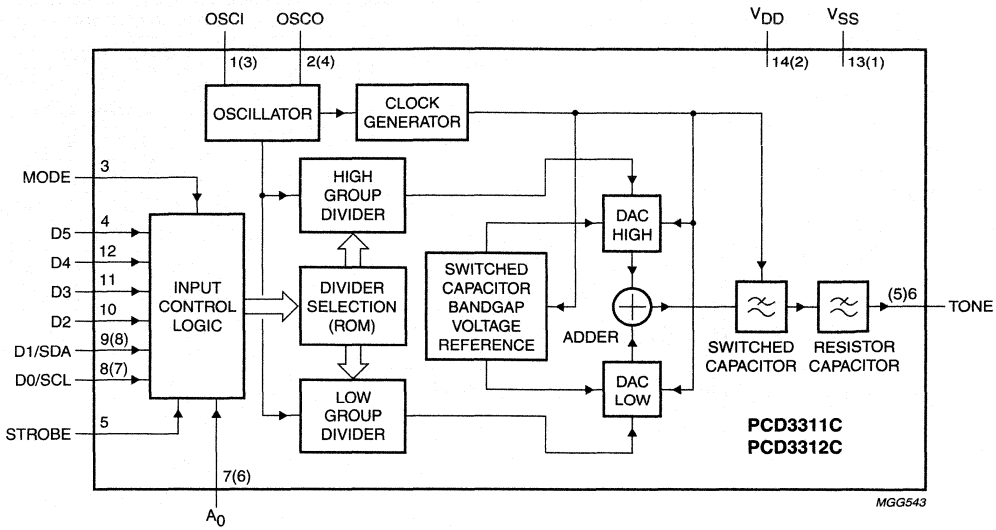
3 QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	operating supply voltage	2.5	–	6.0	V
I_{DD}	operating supply current	–	–	0.9	mA
I_{stb}	standby current	–	–	3	µA
$V_{HG(RMS)}$	DTMF HIGH group output voltage level (RMS value)	158	192	205	mV
$V_{LG(RMS)}$	DTMF LOW group output voltage level (RMS value)	125	150	160	mV
G_v	pre-emphasis (voltage gain) of group	1.85	2.10	2.35	dB
THD	total harmonic distortion	–	–25	–	dB
T_{amb}	operating ambient temperature	–25	–	+70	°C

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCD3311CP	DIP14	plastic dual in-line package; 14 leads (300 mil)	SOT27-1
PCD3311CT	SO16	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1
PCD3312CP	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1
PCD3312CT	SO8	plastic small outline package; 8 leads; body width 7.5 mm	SOT176-1

5 BLOCK DIAGRAM



The un-parenthesised numbers are for the PCD3311CP, those in parenthesis for the PCD3312C.

Fig.1 Block diagram.

6 PINNING INFORMATION

6.1 Pinning PCD3311CP

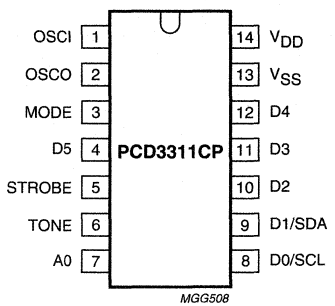


Fig.2 Pin configuration PCD3311CP.

6.2 Pin description PCD3311CP

SYMBOL	PIN	TYPE	DESCRIPTION
OSCI	1	I	oscillator input
OSCO	2	O	oscillator output
MODE	3	I	mode select input (selects I^2C or parallel data input)
D5	4	I	parallel data input
STROBE	5	I	strobe input (for loading data in parallel mode)
TONE	6	O	frequency output (DTMF, modem, musical tones)
A0	7	I	slave address input (to be connected to V_{DD} or V_{SS})
D0/SCL	8	I	parallel data input or I^2C-bus clock line
D1/SDA	9	I	parallel data input or I^2C-bus data line
D2 – D4	10 – 12	I	parallel data inputs
V_{SS}	13	P	negative supply
V_{DD}	14	P	positive supply

6.3 Pinning PCD3311CT

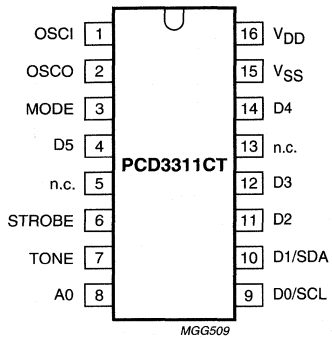


Fig.3 Pin configuration PCD3311CT.

6.4 Pin description PCD3311CT

SYMBOL	PIN	TYPE	DESCRIPTION
OSCI	1	I	oscillator input
OSCO	2	O	oscillator output
MODE	3	I	mode select input (selects I²C or parallel data input)
D5	4	I	parallel data input
n.c.	5	–	not connected
STROBE	6	I	strobe input (for loading data in parallel mode)
TONE	7	O	frequency output (DTMF, modem, musical tones)
A0	8	I	slave address input (to be connected to V_{DD} or V_{SS})
D0/SCL	9	I	parallel data input or I²C-bus clock line
D1/SDA	10	I	parallel data input or I²C-bus data line
D2, D3	11, 12	I	parallel data inputs
n.c.	13	–	not connected
D4	14	I	parallel data input
V_{SS}	15	P	negative supply
V_{DD}	16	P	positive supply

6.5 Pinning PCD3312C

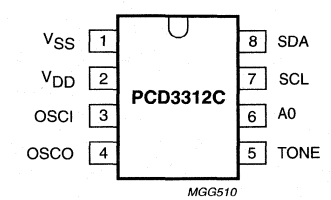


Fig.4 Pin configuration PCD3312C.

6.6 Pin description PCD3312C

SYMBOL	PIN	TYPE	DESCRIPTION
V_{SS}	1	P	negative supply
V_{DD}	2	P	positive supply
OSCI	3	I	oscillator input
OSCO	4	O	oscillator output
TONE	5	O	frequency output (DTMF, modem, musical tones)
A0	6	I	slave address input (to be connected to V_{DD} or V_{SS})
SCL	7	I	I²C-bus clock line
SDA	8	I	I²C-bus data line

7 FUNCTIONAL DESCRIPTION

7.1 General (see Fig.1)

The Input Control Logic decodes the input data to determine whether DTMF, modem or musical tones are selected; and which particular tone or combination of tones is required.

A code representing the required tones is sent to the Divider Selection ROM which selects the correct division ratio in both of the Frequency Dividers (or in one divider, if only a single tone is required).

The Oscillator circuit provides a square wave of frequency 3.58 MHz. Each Frequency Divider divides the frequency of the Oscillator to give a serial digital square wave with a frequency simply related to that of the required tone.

The output from each Frequency Divider goes to a DAC, which is also fed by a clock derived from the oscillator. Using these two signals, the DAC produces an approximate sine wave of the required frequency, with an amplitude derived from the Voltage Reference.

The output from the DAC goes to an Adder where, for DTMF, it is combined with the output from the other DAC.

The output from the Adder goes through two stages of Low Pass Filters to give a smoothed tone (single or dual), and finally to the TONE output.

7.2 Clock/oscillator connection

The timebase for the PCD3311C and PCD3312C is a crystal-controlled oscillator, requiring a 3.58 MHz quartz crystal to be connected between OSCI and OSCO. Alternatively, the OSCI input can be driven from an external clock of 3.58 MHz.

7.3 Mode selection (PCD3311C)

The MODE input selects the data input mode for the PCD3311C. When MODE is connected to V_{DD} (HIGH), data can be received in the parallel mode. When connected to V_{SS} (LOW) or left open, data can be received via the serial I^2C-bus.

PCD 3312C has no MODE input as data input is via the I^2C-bus only.

7.4 Data inputs (PCD3311C)

Inputs D0, D1, D2, D3, D4 and D5 are used in the parallel data input mode of the PCD3311C. Inputs D0 and D1 are also used in serial input mode when they act as the SCL and SDA inputs respectively. Inputs D0 and D1 have no internal pull-down or pull-up resistors and must not be left open in any application. Inputs D2, D3, D4 and D5 have internal pull-down.

D4 and D5 are used to select between DTMF dual, DTMF single, modem and musical tones (see Table 1). D0, D1, D2 and D3 select the tone combination or single tone within the selected application. They also, in combination with D4, select the standby mode. See Tables 2, 3, 4 and 5.

PCD 3312C has no parallel data pins as data input is via the I^2C-bus.

Table 1 Use of D5 and D4 to select application

D5	D4	APPLICATION
LOW	LOW	DTMF single tones; musical tones; standby
LOW	HIGH	DTMF dual tones (all 16 combinations)
HIGH	LOW	modem tones
HIGH	HIGH	musical tones

7.5 Strobe input (PCD3311C)

The STROBE input (with internal pull-down) allows the loading of parallel data into D0 to D5 when MODE is HIGH.

The data inputs must be stable preceding the positive-going edge of the strobe pulse (active HIGH). Input data are loaded at the negative-going edge of the strobe pulse and then the corresponding tone (or standby mode) is provided at the TONE output. The output remains unchanged until the negative-going edge of the next STROBE pulse (for new data) is received. Figure 5 is an example of the timing relationship between STROBE and the data inputs.

When MODE is LOW, data is received serially via the I^2C-bus.

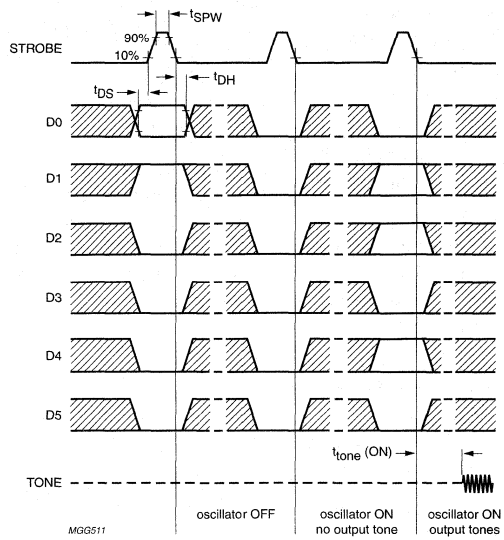


Fig.5 Timing of STROBE, parallel data inputs and TONE output (770 Hz + 1477 Hz in example) in the parallel mode (MODE = HIGH).

7.6 I²C-bus clock and data inputs

SCL and SDA are the serial clock and serial data inputs according to the I²C-bus specification, see Chapter 8. SCL and SDA must be pulled up externally to V_{DD}.

For the PCD3311C, SCL and SDA are combined with parallel inputs D0 and D1 respectively - D0/SCL and D1/SDA operate serially only when MODE is LOW.

7.7 Address input

Address input A0 defines the least significant bit of the I²C-bus address of the device (see Fig.6). The first 6 bits of the address are fixed internally. By tying the A0 of each device to V_{DD} (HIGH) and V_{SS} (LOW) respectively, two different PCD3311C or PCD3312C devices can be individually addressed on the bus.

Whether one or two devices are used, A0 must be connected to V_{DD} or V_{SS}.

7.8 I²C-bus data configuration (see Fig.6)

The PCD3311C and PCD3312C are always slave receivers in the I²C-bus configuration. The R/$\overline{W}$ bit in is thus always LOW, indicating that the master (microcontroller) is writing.

The slave address in the serial mode consists of 7 bits: 6 bits internally fixed, 1 externally set via A0. in the serial mode, the same input data codes are used as in the parallel mode. See Tables 2, 3, 4 and 5.

7.9 Tone output

The single and dual tones provided at the TONE output are first filtered by an on-chip switched-capacitor filter, followed by an active RC low-pass filter. The filtered tones fulfil the CEPT recommendations for total harmonic distortion of DTMF tones. An on-chip reference voltage provides output tone levels independent of the supply voltage. Tables 3, 4 and 5 give the frequency deviation of the output tones with respect to the standard DTMF, modem and music frequencies.

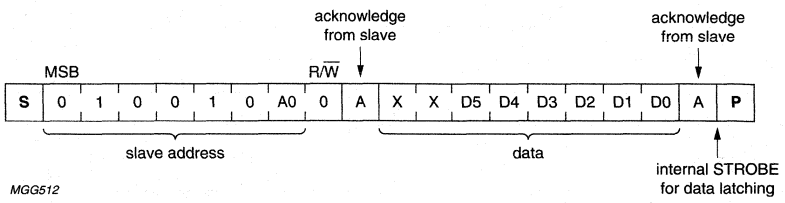


Fig.6 I²C-bus data format.

7.10 Power-on reset

In order to avoid an undefined state when the power is switched ON, the devices have an internal reset circuit which sets the standby mode (oscillator OFF).

7.11 TABLES OF INPUT AND OUTPUT

The specified output tones are obtained when a 3.579545 MHz crystal is used.

In each table, the logical states for the input data lines are related to voltage levels as follows:

1 = HIGH = V_{DD}

0 = LOW = V_{SS}

X = don't care

Table 2 Input data for no output tone, TONE in 3-state

D5	D4	D3	D2	D1	D0	HEX(1)	OSCILLATOR
X	0	0	0	0	0	00 or 20	ON
X	0	0	0	0	1	01 or 21	OFF
X	0	0	0	1	0	02 or 22	OFF
X	0	0	0	1	1	03 or 23	OFF

Note

1. The alternative HEX values depend on the value of D5.

Table 3 Input data and output for DTMF tones

D5	D4	D3	D2	D1	D0	HEX	SYMBOL	STANDARD FREQUENCY	TONE OUTPUT FREQ.	FREQUENCY DEVIATION	
								Hz	Hz	%	Hz
0	0	1	0	0	0	08	–	697	697.90	+0.13	+0.90
0	0	1	0	0	1	09	–	770	770.46	+0.06	+0.46
0	0	1	0	1	0	0A	–	852	850.45	–0.18	–1.55
0	0	1	0	1	1	0B	–	941	943.23	+0.24	+2.23
0	0	1	1	0	0	0C	–	1209	1206.45	–0.21	–2.55
0	0	1	1	0	1	0D	–	1336	1341.66	+0.42	+5.66
0	0	1	1	1	0	0E	–	1477	1482.21	+0.35	+5.21
0	0	1	1	1	1	0F	–	1633	1638.24	+0.32	+5.24
0	1	0	0	0	0	10	0	941+1336	–	–	–
0	1	0	0	0	1	11	1	697+1209	–	–	–
0	1	0	0	1	0	12	2	697+1336	–	–	–
0	1	0	0	1	1	13	3	697+1477	–	–	–
0	1	0	1	0	0	14	4	770+1209	–	–	–
0	1	0	1	0	1	15	5	770+1336	–	–	–
0	1	0	1	1	0	16	6	770+1477	–	–	–
0	1	0	1	1	1	17	7	852+1209	–	–	–
0	1	1	0	0	0	18	8	852+1336	–	–	–
0	1	1	0	0	1	19	9	852+1477	–	–	–
0	1	1	0	1	0	1A	A	697+1633	–	–	–
0	1	1	0	1	1	1B	B	770+1633	–	–	–
0	1	1	1	0	0	1C	C	852+1633	–	–	–
0	1	1	1	0	1	1D	D	941+1633	–	–	–
0	1	1	1	1	0	1E	*	941+1209	–	–	–
0	1	1	1	1	1	1F	#	941+1477	–	–	–

Table 4 Input data and output for modem tones

D5	D4	D3	D2	D1	D0	HEX	STANDARD FREQUENCY	TONE OUTPUT FREQ.	FREQUENCY DEVIATION		TELECOM. STANDARD
							Hz	Hz	%	Hz	
1	0	0	1	0	0	24	1300	1296.94	–0.24	–3.06	V.23
1	0	0	1	0	1	25	2100	2103.14	+0.15	+3.14	
1	0	0	1	1	0	26	1200	1197.17	–0.24	–2.83	Bell 202
1	0	0	1	1	1	27	2200	2192.01	–0.36	–7.99	
1	0	1	0	0	0	28	980	978.82	–0.12	–1.18	V.21
1	0	1	0	0	1	29	1180	1179.03	–0.08	–0.97	

D5	D4	D3	D2	D1	D0	HEX	STANDARD FREQUENCY	TONE OUTPUT FREQ.	FREQUENCY DEVIATION		TELECOM. STANDARD
							Hz	Hz	%	Hz	
1	0	1	0	1	0	2A	1070	1073.33	+0.31	+3.33	Bell 103
1	0	1	0	1	1	2B	1270	1265.30	−0.37	−4.70	
1	0	1	1	0	0	2C	1650	1655.66	+0.34	+5.66	V.21
1	0	1	1	0	1	2D	1850	1852.77	+0.15	+2.77	
1	0	1	1	1	0	2E	2025	2021.20	−0.19	−3.80	Bell 103
1	0	1	1	1	1	2F	2225	2223.32	−0.08	−1.68	

Table 5 Input/output for musical tones

D5	D4	D3	D2	D1	D0	HEX	NOTE	STD. FREQ. BASED ON A4 = 440 Hz	TONE OUTPUT FREQUENCY
								Hz	Hz
1	1	0	0	0	0	30	D#5	622.3	622.5
1	1	0	0	0	1	31	E5	659.3	659.5
1	1	0	0	1	0	32	F5	698.5	697.9
1	1	0	0	1	1	33	F#5	740.0	741.1
1	1	0	1	0	0	34	G5	784.0	782.1
1	1	0	1	0	1	35	G#5	830.6	832.3
1	1	0	1	1	0	36	A5	880.0	879.3
1	1	0	1	1	1	37	A#5	932.3	931.9
1	1	1	0	0	0	38	B5	987.8	985.0
1	1	1	0	0	1	39	C6	1046.5	1044.5
1	1	1	0	1	0	3A	C#6	1108.7	1111.7
1	0	1	0	0	1	29	D6	1174.7	1179.0
1	1	1	0	1	1	3B	D#6	1244.5	1245.1
1	1	1	1	0	0	3C	E6	1318.5	1318.9
1	1	1	1	0	1	3D	F6	1396.9	1402.1
0	0	1	1	1	0	0E	F#6	1480.0	1482.2
1	1	1	1	1	0	3E	G6	1568.0	1572.0
1	0	1	1	0	0	2C	G#6	1661.2	1655.7
1	1	1	1	1	1	3F	A6	1760.0	1768.5
0	0	0	1	0	0	04	A#6	1864.7	1875.1
0	0	0	1	0	1	05	B6	1975.5	1970.0
1	0	0	1	0	1	25	C7	2093.0	2103.1
1	0	1	1	1	1	2F	C#7	2217.5	2223.3
0	0	1	1	1	0	06	D7	2349.3	2358.1
0	0	0	1	1	1	07	D#7	2489.0	2470.4

8 I²C-BUS INTERFACE

The I²C-bus is for two-way communication between different ICs or modules. It uses only two lines, a serial data line (SDA) and a serial clock line (SCL), both of which are bi-directional. Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

8.1 **Bit transfer** (see Fig.7)

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

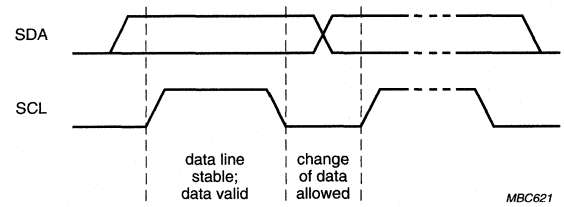


Fig.7 Bit transfer.

8.2 **Start and stop conditions** (see Fig.8)

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

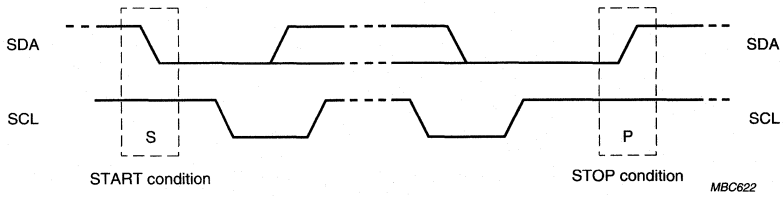


Fig.8 Start and stop conditions.

8.3 System configuration (see Fig.9)

A device generating a message is a 'transmitter', a device receiving a message is the 'receiver'. The device that controls message transfer is the 'master' and the devices that are controlled by the master are the 'slaves'.

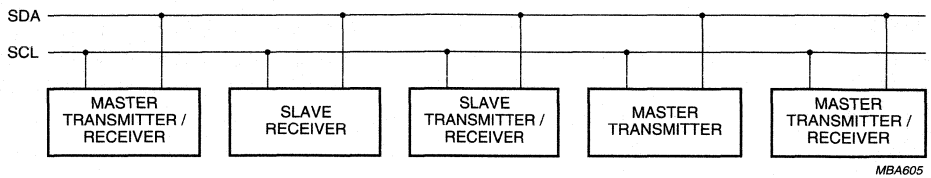


Fig.9 System configuration.

8.4 Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge after the reception of each byte. Also a master must generate an acknowledge after reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge-related clock pulse. Set-up and hold times must be taken into account to ensure that the SDA line is stable LOW during the whole HIGH period of the acknowledge-related clock pulse. A master receiver must signal an end of data to the transmitter by **not** generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate the stop condition.

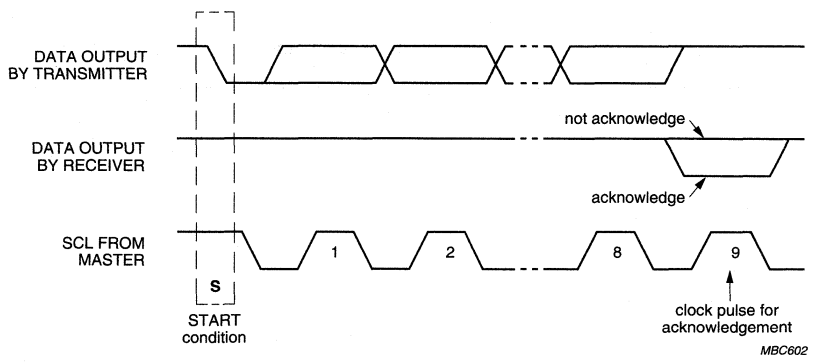


Fig.10 Acknowledgment on the I²C-bus.

8.5 Timing specifications

The PCD3311C and PCD3312C accept data input from a microcontroller and are 'slave receivers' when operating via the I²C-bus. They support the 'standard' and 'low-speed' modes of the I²C-bus, but not the 'fast' mode detailed in *"The I²C-bus and how to use it"* document order no. 9398 393 40011. The timing requirements for the devices are described in Sections 8.5.1 and 8.5.2.

8.5.1 STANDARD MODE

Masters generate a bus clock with a maximum frequency of 100 kHz. Detailed timing is shown in Fig.11, where the two signal levels are LOW = V_{IL} and HIGH = V_{IH}, see Chapter 11. Figure 12 shows a complete data transfer in standard mode. The time symbols are explained in Table 6.

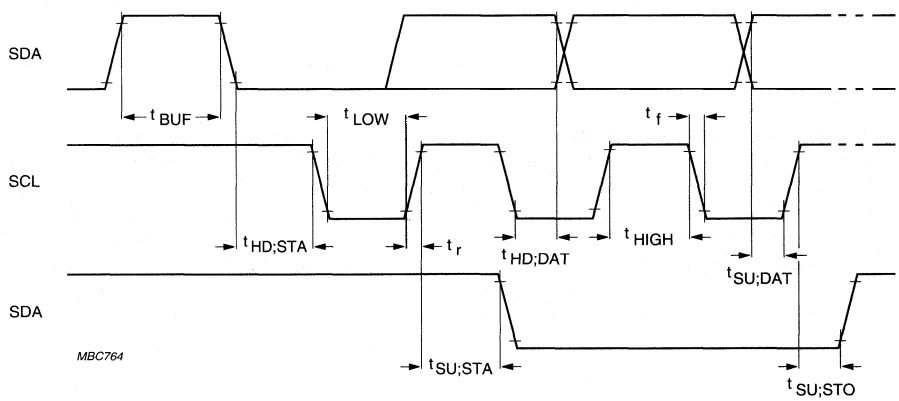
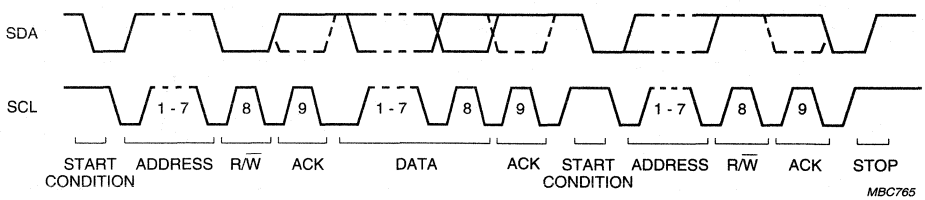


Fig.11 Standard mode timing.



Clock LOW minimum = 4.7 μs; clock HIGH minimum = 4 μs.
The dashed line is the acknowledgment of the receiver.
Mark-to-space ratio = 1 : 1 (LOW-to-HIGH).
Maximum number of bytes is unrestricted.
Premature termination of transfer is allowed by generation of STOP condition.
Acknowledge clock bit must be provided by master.

Fig.12 Complete data transfer in standard mode.

Table 6 Explanation of time symbols used in Fig.11

SYMBOL	PARAMETER	REMARKS	MIN.	MAX.	UNIT
f_{SCL}	SCL clock frequency		0	100	kHz
t_{SW}	tolerable pulse spike width		–	100	ns
t_{BUF}	bus free time	The time that the bus is free (SDA is HIGH) before a new transmission is initiated by SDA going LOW.	4.7	–	μs
$t_{SU;STA}$	set-up time repeated START	Only valid for repeated start code.	4.7	–	μs
$t_{HD;STA}$	hold time START condition	The time between SDA going LOW and the first valid negative-going transition of SCL.	4.0	–	μs
t_{LOW}	SCL LOW time	The LOW period of the SCL clock.	4.7	–	μs
t_{HIGH}	SCL HIGH time	The HIGH period of the SCL clock.	4.0	–	μs
t_r	rise time SDA and SCL		–	1.0	μs
t_f	fall time SDA and SCL		–	0.3	μs
$t_{SU;DAT}$	data set-up time		250	–	ns
$t_{HD;DAT}$	data hold time		0	–	ns
$t_{SU;STO}$	set-up time STOP condition		4.0	–	μs

8.5.2 LOW-SPEED MODE

Masters generate a bus clock with a maximum frequency of 2 kHz; a minimum LOW period of 105 μs and a minimum HIGH period of 365 μs. The mark-to-space ratio is 1 : 3 LOW-to-HIGH. Detailed timing is shown in Fig.13, where the two signal levels are LOW = V_{IL} and HIGH = V_{IH}, see Chapter 11. Figure 14 shows a complete data transfer in low-speed mode.The time symbols are explained in Table 7.

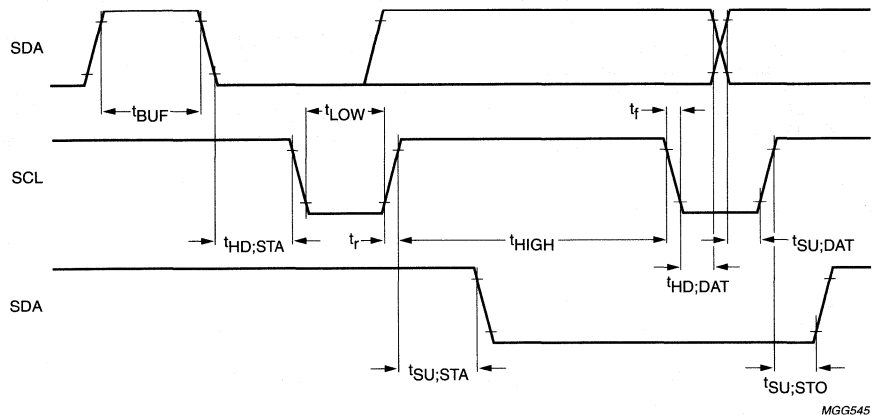
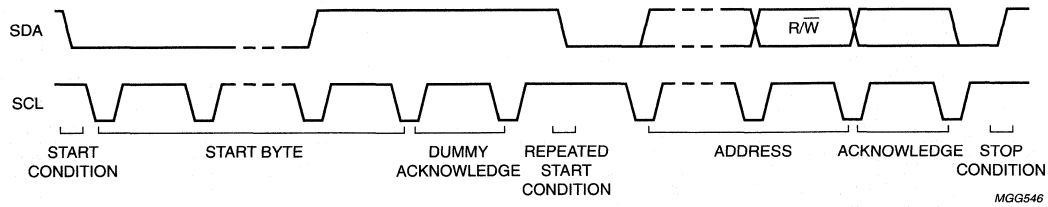


Fig.13 Low-speed mode timing.



Clock LOW minimum = 130 μs ±25 μs; clock HIGH minimum 390 μs ±25 μs.
Mark-to-space ratio = 1 : 3 (LOW-to-HIGH).
Start byte 0000 0001.
Maximum number of bytes = 6.
Premature termination of transfer not allowed.
Acknowledge clock bit must be provided by master.

Fig.14 Complete data transfer in low speed mode.

Table 7 Explanation of time symbols used in Fig.13

SYMBOL	PARAMETER	REMARKS	MIN.	MAX.	UNIT
f_{SCL}	SCL clock frequency		0	2	kHz
t_{SW}	tolerable pulse spike width		–	100	ns
t_{BUF}	bus free time	The time that the bus is free (SDA is HIGH) before a new transmission is initiated by SDA going LOW.	105	–	µs
$t_{SU;STA}$	set-up time repeated START	Only valid for repeated start code.	105	155	µs
$t_{HD;STA}$	hold time START condition	The time between SDA going LOW and the first valid negative-going transition of SCL.	365	415	µs
t_{LOW}	SCL LOW time	The LOW period of the SCL clock.	105	155	µs
t_{HIGH}	SCL HIGH time	The HIGH period of the SCL clock.	365	–	µs
t_r	rise time SDA and SCL		–	1.0	µs
t_f	fall time SDA and SCL		–	0.3	µs
$t_{SU;DAT}$	data set-up time		250	–	ns
$t_{HD;DAT}$	data hold time		0	–	ns
$t_{SU;STO}$	set-up time STOP condition		105	155	µs

9 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, it is good practice to take normal precautions appropriate to handling MOS devices (see *"Handbook IC03, Section: General, Handling MOS devices"*).

10 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.8	+8.0	V
V_I	all input voltages	−0.8	V_{DD} + 0.8	V
I_I	DC input current	−10	+10	mA
I_O	DC output current	−10	+10	mA
P_{tot}	total power dissipation	−	300	mW
P_O	power dissipation per output	−	50	mW
I_{DD}	supply current through pin V_{DD}	−50	+50	mA
I_{SS}	supply current through pin V_{SS}	−50	+50	mA
T_{stg}	storage temperature	−65	+150	°C
T_{amb}	operating ambient temperature	−25	+70	°C

11 CHARACTERISTICS

V_{DD} = 2.5 to 6.0 V; V_{SS} = 0 V; T_{amb} = −25 to +70 °C; all voltages with respect to V_{SS}; f_{xtal} = 3.58 MHz (g_{mL}); maximum series resistance = 50 Ω; unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT
V_{DD}	operating supply voltage	2.5	−	6.0	V
I_{DD}	operating supply current (note 1)				
	no output tone	−	50	100	µA
	single output tone	−	0.5	0.8	mA
	dual output tone	−	0.6	0.9	mA
I_{stb}	static standby current (note 2)	−	−	3	µA
Inputs/outputs (SDA)					
D0 TO D5; MODE; STROBE					
V_{IL}	LOW level input voltage	0	−	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage	$0.7V_{DD}$	−	V_{DD}	V
D2 TO D5 MODE; STROBE; A0					
I_{IL}	pull-down input current; $V_I = V_{DD}$	−30	−150	−300	nA
SCL (D0); SDA (D1)					
I_{OL}	LOW level output current (SDA); V_{OL} = 0.4 V	3	−	−	mA
f_{SCL}	SCL clock frequency	−	−	100	kHz
C_i	input capacitance; $V_I = V_{SS}$	−	−	7	pF
t_i	allowable input spike pulse width	−	−	100	ns

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT
TONE output (see test circuit, Fig.15)					
$V_{HG(RMS)}$	DTMF output voltage (RMS), HIGH group	158	192	205	mV
$V_{LG(RMS)}$	DTMF output voltage (RMS), LOW group	125	150	160	mV
V_{DC}	DC voltage level	–	$\frac{1}{2} V_{DD}$	–	V
G_v	voltage gain (pre-emphasis) of group	1.85	2.10	2.35	dB
THD	Total Harmonic Distortion; T_{amb} = 25 °C				
	dual tone (note 3)	–	–25	–	dB
	modem tone (note 4)	–	–29	–	dB
$\|Z_o\|$	output impedance	–	0.1	0.5	kΩ
OSCI input					
$V_{OSC(p-p)}$	maximum allowable amplitude at OSCI	–	–	$V_{DD} - V_{SS}$	V
Timing (V_{DD} = 3 V)					
$t_{OSC(ON)}$	oscillator start-up time	–	3	–	ms
$t_{TONE(ON)}$	TONE start-up time (note 5)	–	0.5	–	ms
t_{SPW}	STROBE pulse width (note 6)	400	–	–	ns
t_{DS}	data set-up time (note 6)	150	–	–	ns
t_{DH}	data hold time (note 6)	100	–	–	ns

Notes

1. Oscillator ON; V_{DD} = 3 V; crystal connected between OSCI and OSCO; D0/SCL and D1/SDA connected via resistance of 5.6 kΩ to V_{DD}; all other pins left open.
2. As note 1, but with oscillator OFF.
3. Related to the level of the LOW group frequency component, according to CEPT recommendations.
4. Related to the level of the fundamental frequency.
5. Oscillator must be running.
6. Values are referenced to the 10% and 90% levels of the relevant pulse amplitudes, with a total voltage swing from V_{SS} to V_{DD}.

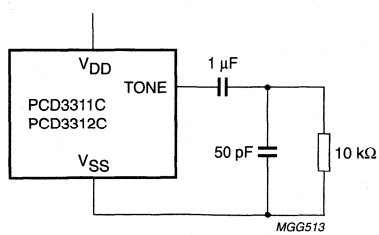


Fig.15 TONE output test circuit.

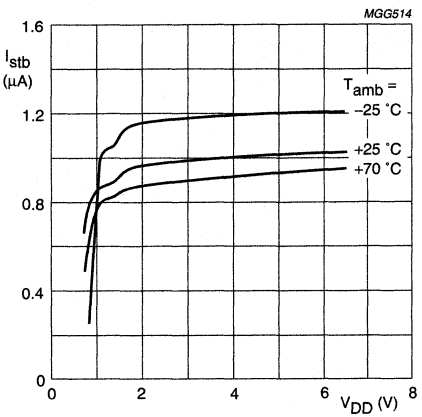


Fig.16 Standby supply current as a function of supply voltage; oscillator OFF.

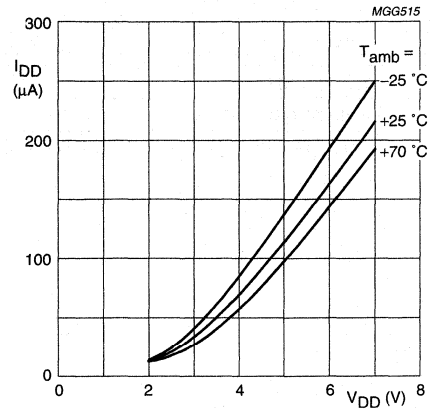


Fig.17 Operating supply current as a function of supply voltage; oscillator ON, no output at TONE.

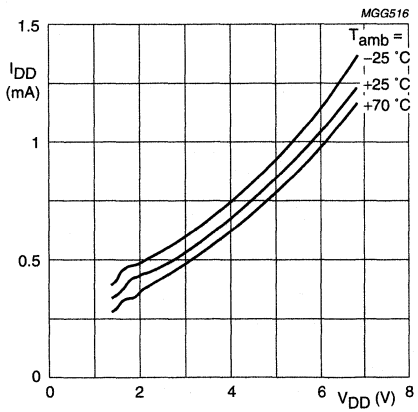


Fig.18 Operating supply current as a function of supply voltage; oscillator ON, dual tone at TONE.

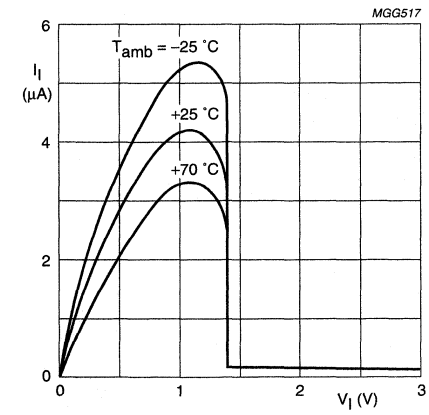


Fig.19 Pull-down input current as a function of input voltage; V_{DD} = 3 V.

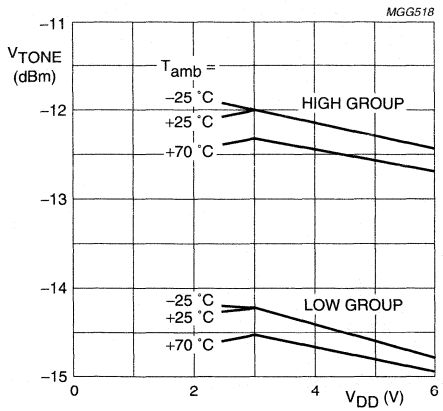


Fig.20 DTMF output voltage levels as a function of operating supply voltage; R_L = 1 MΩ.

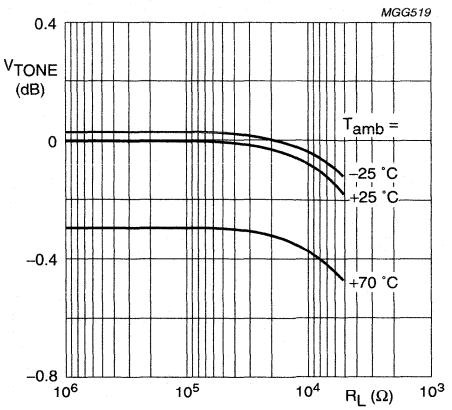


Fig.21 Dual tone output voltage level as a function of output load resistance.

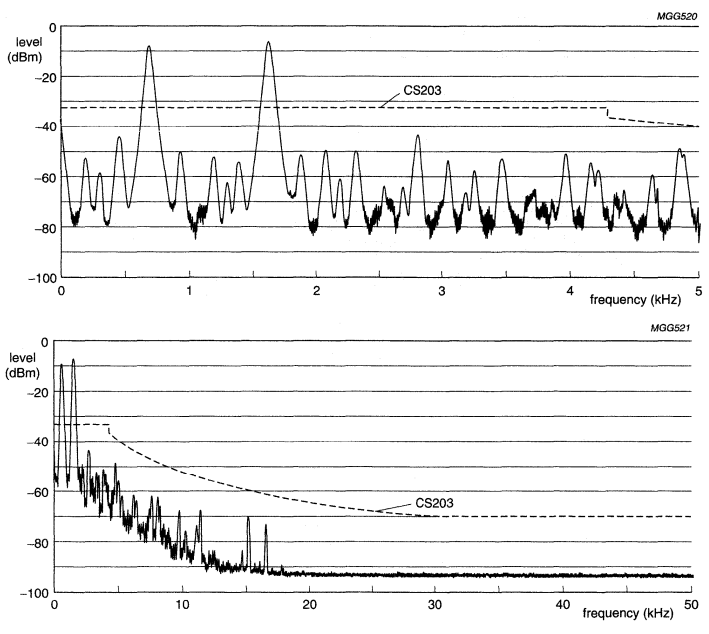


Fig.22 Typical frequency spectrum of a dual tone signal after flat-band amplification of 6 dB.

12 APPLICATION INFORMATION

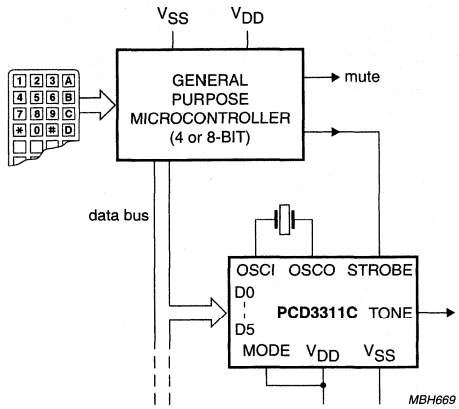


Fig.23 PCD3311C driven by microcontroller with parallel data bus.

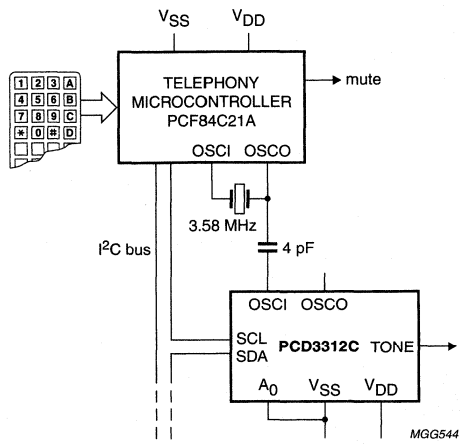


Fig.24 PCD3312C driven by microcontroller PCF84C21A. The PCF84C21A is a single-chip 8-bit microcontroller with 2 kbytes ROM and I²C-bus. The same application is possible with the PCD3311C with MODE = V_{SS}.

PCD3316

Caller-ID on Call Waiting (CIDCW) receiver

11 March 1999 **Product specification**

1. General description

The PCD3316 is a low power mixed signal CMOS integrated circuit for receiving physical layer signals like Bellcore's 'CPE[1] Alerting Signal (CAS)' and the signals used in similar services. The device is capable of a very high precision detection of the dual tone (2130 and 2750 Hz) by using a patented digital algorithm. The PCD3316 can be used for on-hook and off-hook Caller-ID (CID), Caller-ID on Call Waiting (CIDCW) and Caller-Name (CNAM) applications.

For timing purposes the PCD3316 can be programmed to generate an interrupt signal to the microcontroller every second or every minute. These timings are derived from an on-chip 32.768 kHz oscillator.

Also incorporated in the device are a Frequency Shift Keying (FSK) receiver/demodulator and a 'Ring or polarity change detector'. The status of the PCD3316, the received FSK data bytes and the ringer period can be read and many options can be selected via the I²C-bus serial interface. Two on-chip oscillators are available. One 3.58 MHz oscillator for all internal functions and a low frequency 32.768 kHz oscillator for the 1 second or 1 minute timing.

In Power-down mode only the polarity comparators and the 32.768 kHz oscillator are active. The CAS detection, the FSK receiver and the 3.58 MHz oscillator can be enabled separately. Detection of a polarity change on the inputs POL0 or POL1, the reception of an FSK data byte, the detection of a CAS tone or a timebase interrupt is signalled to the microcontroller by an interrupt request signal (IRQ). The microcontroller can communicate with the PCD3316 device via the serial interface.

The PCD3316 is designed for use in a microcontroller controlled system. The device is available in a SO16 package.

A demonstration board OM5843 and an application note *AN98071* are available.

1. CPE = Customer Premises Equipment.

2. Features

- Bellcore's 'CPE Alerting Signal (CAS)' and British Telecom's (BT) 'Loop State Tone Alert Signal' detection
- BT's 'Idle State Tone Alert Signal' by means of monitoring the input signal level
- 1200 baud FSK demodulator conform Bell 202 and CCITT V23 standards
- Ring or polarity change detector
- Ring period measurement
- Low battery comparator
- Signal level detector
- On-hook and off-hook applications according to *Bellcore TR-NWT-000030* and *SR-TSV-002476* specifications
- Receive sensitivity of –37.8 dBm (in 600 Ω) for CAS
- 2.5 to 3.6 V supply; low power standby mode
- Selectable 1 second or 1 minute timebase interrupt
- 3.58 MHz and 32.768 kHz crystal oscillators
- SO16 package.

3. Applications

- Analog Display Services Interface (ADSI) phones
- Feature phones and adjunct boxes with Bellcore CID, CIDCW and CNAM systems
- Computer Telephony Integrated (CTI) systems.

4. Ordering information

Table 1: Ordering information

Type number	Package		
	Name	Description	Version
PCD3316T	SO16	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1

5. Block diagram

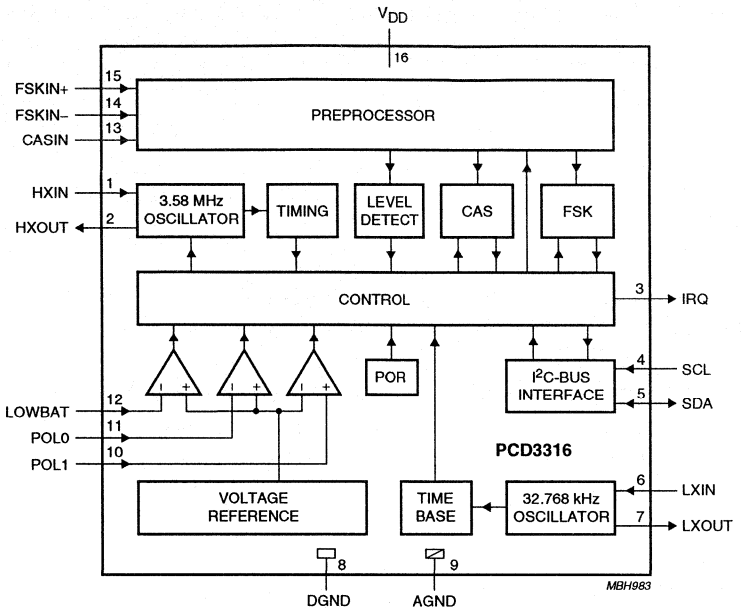


Fig 1. Block diagram.

6. Pinning information

6.1 Pinning

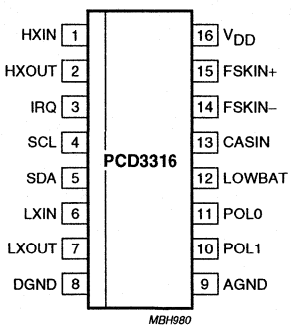


Fig 2. Pin configuration.

6.2 Pin description

Table 2: Pin description

Symbol	Pin	I/O	Description
HXIN	1	I	3.58 MHz crystal oscillator input
HXOUT	2	O	3.58 MHz crystal oscillator output
IRQ	3	O	interrupt output; programmable active HIGH or active LOW
SCL	4	I	serial clock line of I^2C-bus
SDA	5	I/O	serial data line of I^2C-bus
LXIN	6	I	32.768 kHz crystal oscillator input
LXOUT	7	O	32.768 kHz crystal oscillator output
DGND	8	–	digital ground
AGND	9	–	analog ground
POL1	10	I	polarity detector input 1
POL0	11	I	polarity detector input 0
LOWBAT	12	I	low battery detector input
CASIN	13	I	input pin for CAS signal
FSKIN–	14	I	negative input for FSK signal
FSKIN+	15	I	positive input for FSK signal
V_{DD}	16	–	supply

7. Functional description

7.1 Preprocessor and analog inputs

The preprocessor for the CAS detection and the FSK receiver incorporates an Analog-to-Digital Converter (ADC) and a digital bandpass filter.

The LOWBAT input of the PCD3316 can be used for low battery detection. The voltage on the LOWBAT pin is compared with an internal voltage reference circuit. When the LOWBAT voltage drops below the reference voltage, the Status register, bit 5 is set to logic 1.

The PCD3316 can be forced in a Power-down state by switching off the 3.58 MHz system clock and the ADC. This is done by setting Mode register 2, bit 7 (CIDMD2.7) to logic 0. To guarantee correct operation the following order of actions must be performed (see also Section 7.8 about interrupts):

1. Switch off CAS and FSK detection (if turned on)
2. Read the interrupt register (thus clearing pending interrupts generated by the CAS and FSK detector)
3. Switch off the 3.58 MHz oscillator by clearing bit 7 of Mode register 2.

The two low power comparators (inputs POL0 and POL1) and the 32.768 kHz clock are always active.

They can be used for ring or line polarity reversal detection. The POL on/off bit (Mode register 1, bit 4) must be set to enable generation of an interrupt when a polarity change occurs. The result of the two comparators can be read in bits 7 and 6 (POL0 and POL1) of the Status register (see Section 7.4). The 3.58 MHz clock is not needed for the generation of a polarity interrupt.

7.2 CAS detection

After a power-on reset or after enabling the CAS detector the internal registers of the CAS detection function are initialized. The initialization takes a maximum of 100 periods of the 3.58 MHz clock.

If the CAS detection is enabled the PCD3316 will generate an interrupt (Interrupt register, bit 1 is set) when a correct dual tone (2130 and 2750 Hz) is detected. Interrupts will be blocked when the signal level on the CAS input is below the threshold in the level detector.

7.3 FSK reception

The FSK receiver function can be enabled by setting the FSK on/off bit (Mode register 1, bit 7).

In the FSK transmission specification of BT and Bellcore a channel seizure is transmitted first (sequence of 1010..). After the channel seizure a block of marks and finally the data pattern are sent (see Figure 3). These mark bits are detected by the PCD3316 which sets the FSK-BOM Indication bit (Status register, bit 4). The FSK-BOM Indication bit is reset when the FSK receiver is disabled.

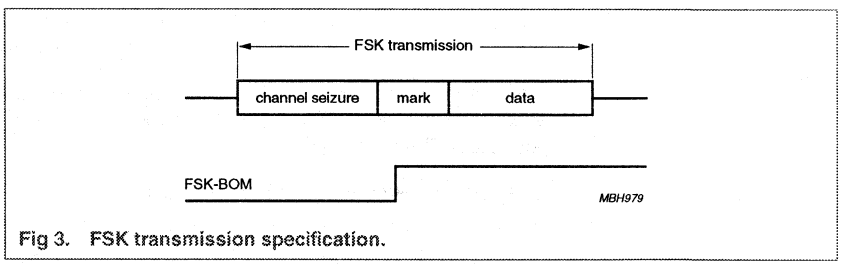


Fig 3. FSK transmission specification.

If the FSK-BOM Indication bit is set, the FSK receiver will generate an interrupt after it has received a complete data word. An FSK data word consists of one start bit (space), followed by eight data bits and one stop bit (mark). Interrupts will therefore not be generated during the channel seizure and during the block of marks. When a valid data word has been received, FSK data is available in the FSK data register.

By clearing the FSK-BOM-mask on/off bit (Mode register 1, bit 6), the FSK receiver will not wait with the generation of interrupts until a Begin Of Mark (BOM) has been detected but will handle the channel seizure as normal data. The block of marks which is a string of logic 1 will still not generate interrupts because there are no start bits.

After the generation of an interrupt the IRQ pin will become active (see Figure 4), and the FSK Interrupt bit is set (Interrupt register, bit 5). The received data is available in the FSK data register.

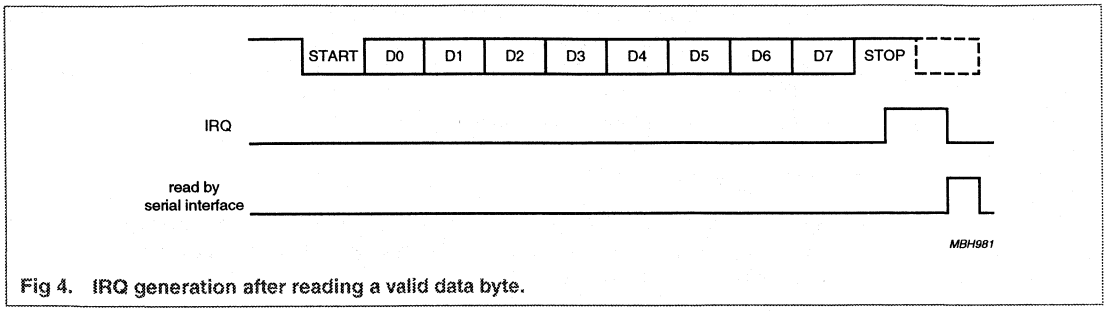


Fig 4. IRQ generation after reading a valid data byte.

The FSK-OVR Error bit (Status register, bit 3) indicates that a previous byte is lost due to an overrun. The FSK-FRM Error bit (Status register, bit 2) indicates an incorrect start- or stop-bit. These frame errors indicate that there are synchronization problems. The on-chip level detector can be used to detect a carrier loss during FSK transmission. FSK data can be rejected when the signal level is below the reference level, this to avoid that noise is interpreted as data (Interrupt register, bit 4 is logic 1).

7.4 Ring or polarity change detector

For ring and polarity change detection two comparators are available in the PCD3316. The reference level of the comparators is set internally by the reference voltage generator. The voltage levels on the two polarity comparator inputs, POL0 and POL1, are compared with the reference voltage V_{ref}. If POL0 < V_{ref} or POL1 > V_{ref}, POL0 and POL1 (Status register, bit 7 and 6) are set respectively and reset if POL0 > V_{ref} and POL1 < V_{ref}. Every time the POL0 status bit changes from logic 1 to logic 0, a POL0 interrupt is generated. Every time the POL1 status bit changes from logic 0 to logic 1, a POL1 interrupt is generated.

The period time of a POL1-POL0-POL1 sequence is available in the Ringer period register. It is preset to 255 on power-on and updated every time a POL1 interrupt is generated. The sequence is:

1. Power-on: Ringer period register = 255
2. First POL1 interrupt: Ringer period register = 255
3. First POL1 interrupt after a POL0 interrupt: Ringer period register = new time
4. First POL1 interrupt after more than $^{255}/_{2048}$ s: Ringer period register = 255.

The period is given in multiples of $^{1}/_{2048}$ s. The maximum value is 255.

The POL1-POL0-POL1 sequence is recognized when one or more POL1 interrupts are generated followed by one or more POL0 interrupts, followed by a POL1 interrupt. The 32.768 kHz clock is needed for the generation of a polarity interrupt.

7.5 Low battery detection

The low battery voltage detection input (pin LOWBAT) is connected to the positive input of a comparator. The negative input is connected to the internal reference voltage. If the voltage on the LOWBAT input pin is less than the reference voltage V_{ref}, the LOW-BAT Indication (Status register, bit 5) is set. If the LOWBAT input rises above V_{ref} again, the LOW-BAT Indication is cleared.

The 32.768 kHz clock signal must be available. The LOW-BAT Indication bit does not generate interrupts, thus the bit should be polled.

7.6 Level detect

When the input signal level on the FSK or the CAS input (the one that is selected) is below a threshold of typically –40 dBm, the Low Level Status bit will be set (Interrupt register, bit 4). The level detector can be used to observe a carrier loss during FSK transmission and to detect the 'Idle State Tone Alert Signal' for British Telecom. The signal power on the input can be monitored by polling the register bit since it will not generate an interrupt. Signal power is measured in a frequency band corresponding to the selected operation mode, FSK (1000 to 2200 Hz) or CAS (2000 to 2800 Hz).

The Low Level Status bit will be updated every 8 ms. When FSK and CAS are both disabled the signal level on the FSK input is measured. The 32.768 kHz clock signal must be available.

7.7 Time base

The 32.768 kHz oscillator is used to generate either a 1 second or a 1 minute interrupt signal. If the TB on/off bit is set (Mode register 2, bit 6) every second or minute an interrupt is generated and MIN Interrupt and/or SEC Interrupt bits (Interrupt register, bit 7 and 6) are set. After reading the Interrupt register the interrupt is cleared.

The SEC/MIN (Mode register 2, bit 5) selects whether every second (SEC/MIN is set) or every minute (SEC/MIN is cleared) an interrupt is generated. All possible selections are shown in Table 3. Resetting bit TB on/off in Mode register 2 (bit 6) will only disable time base interrupts, and the 32.768 kHz oscillator will continue to run.

7.8 Interrupt

The interrupt request output (IRQ) is active HIGH by default. The polarity of the IRQ output can be made active LOW by the INT Polarity HIGH/LOW bit (Mode register 1, bit 3). The IRQ pin is in 3-state when not active, so an external pull-up or pull-down resistor is required. The interrupt cause is indicated by the flags in the Interrupt register. Interrupt flags are set by hardware but must be reset by software. All flags of the Interrupt register are reset when the register is read via I^2C-bus interface.

The IRQ pin is deactivated at the positive edge of SCL which reads the first data bit of the Interrupt register. The IRQ pin will stay inactive for one SCL cycle. IRQ can handle a next interrupt after the next positive edge of SCL.

Table 3: Selection of interrupt modes

Mode register 2 (CIDMD2)		Interrupt register (CIDINT)		Interrupt
TB on/off (CIDMD2.6)	SEC/MIN (CIDMD2.5)	MIN Interrupt (CIDINT.7)	SEC Interrupt (CIDINT.6)	
0	X[1]	0	0	no time base interrupt (time base is reset)
1	0	1	0	every minute an interrupt is generated; no second interrupt
1	1	1	1	every second an interrupt is generated; every minute an interrupt is generated

[1] X = don't care.

7.9 The internal Power-on reset (POR)

The device contains an on-chip Power-on reset circuitry which activates a reset as long as V_{DD} is below a predefined level $V_{POR(H)}$. If V_{DD} exceeds $V_{POR(H)}$, the 3.58 MHz oscillator will start. The PCD3316 is initialized and the internal registers are set to the default value (see Section 7.13). It takes a maximum of 100 cycles of the 3.58 MHz clock to initialize all internal functions. The POR circuitry also ensures, that the chip will be switched off as soon as a falling V_{DD} reaches a predefined level ($V_{POR(L)}$).

7.10 3.58 MHz oscillator circuitry

The 3.58 MHz oscillator is needed for the FSK receiver and the CAS detection. This on-chip Amplitude Controlled Oscillator (ACO) circuitry is a single-stage inverting amplifier biased by an internal feedback resistor R_{fb}. The oscillator circuit is shown in Figure 5. When using a quartz resonator to drive the oscillator, normally no external components are needed.

When using ceramic resonators to drive the oscillator, in some cases external components are needed; refer to the ceramic resonator product specifications. Two different configurations are shown in Figure 6a and Figure 6b.

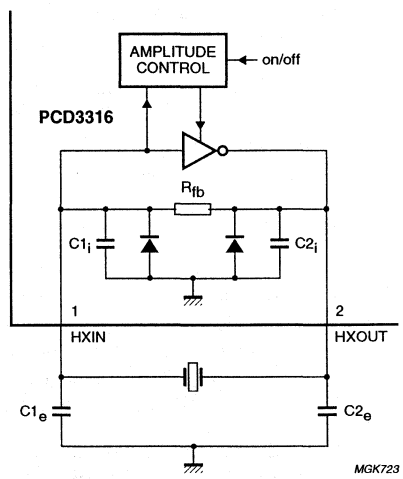
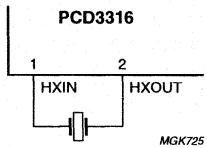


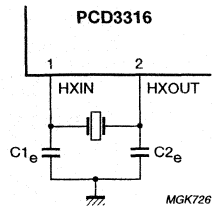
Fig 5. Oscillator.

To drive the device with an external clock source, apply the external clock signal to HXIN, and leave HXOUT to float, as shown in Figure 6c. If the amplitude of the input signal is less than V_{DD} to DGND or a sine wave is applied, capacitive decoupling is needed as shown in Figure 6d.

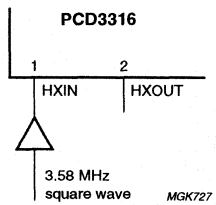
In the Power-down mode (Mode register 2, bit 7 = 0), the oscillator is stopped and HXIN and HXOUT are internally pulled LOW. The current of the whole oscillator is switched off.



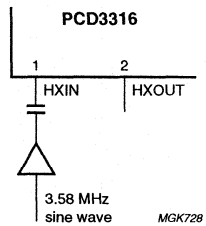
a. Standard oscillator: quartz or PXE.



b. Oscillator: quartz or PXE with external capacitors.

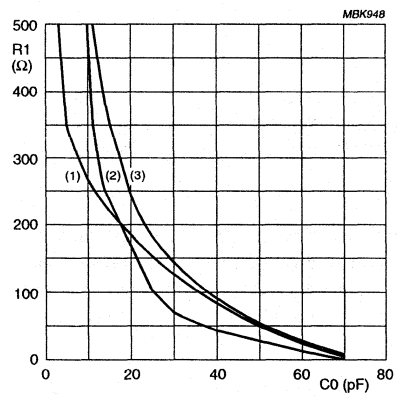


c. External clock: square wave.



d. External clock: sine wave.

Fig 6. 3.58 MHz oscillator configurations.



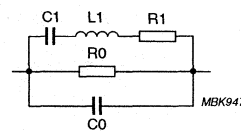
$C1_e$ and $C2_e$ are the external load capacitances (see Figure 6b). Normally, they are not needed due to integrated load capacitances of 10 pF; see curve (2).

(1) $C1_e = C2_e = 22$ pF.

(2) $C1_e = C2_e = 0$ pF.

(3) $C1_e = C2_e = 12$ pF.

a. Resonator requirements for the ACO.



For correct function of the oscillator, the values of R1 and C0 of the chosen resonator (quartz or PXE) must be below the related curve lines shown in Figure 7a. The value of the parallel resistor R0 must be less than 47 kΩ.

The wiring between chip and resonator should be kept as short as possible.

b. Resonator equivalent circuit.

Fig 7. Resonator requirements and equivalent circuit.

7.11 32 kHz oscillator

The 32.768 kHz oscillator is enabled permanently and is used to generate either a 1 second or 1 minute interrupt. The 32.768 kHz clock is also used for the 'Ring or polarity change detector', the 'Low battery detection' and the 'Level detect' function.

An external 32.768 kHz signal may be applied to pin LXIN while leaving pin LXOUT not connected.

The 32 kHz oscillator requires an external 32.768 kHz quartz crystal and an external feedback resistor (4.7 MΩ) between the LXIN and LXOUT pins (see Figure 8).

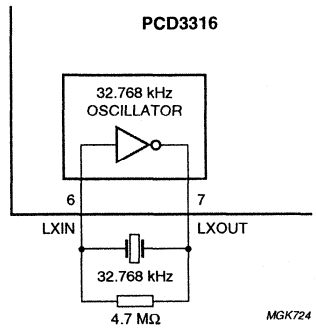


Fig 8. Connections of the 32 kHz oscillator.

7.12 Serial interface

The serial interface of the PCD3316 is the I²C-bus. A detailed description of the I²C-bus specification, including applications, is given in the brochure: *The I²C-bus and how to use it*, order no. 9398 393 40011 or *I²C Peripherals Data Handbook IC12*.

7.12.1 Characteristics of the I²C-bus

For the I²C-bus configuration see Figure 9. A device generating a message is a 'transmitter', a device receiving a message is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are called the 'slaves'. The PCD3316 operates in the slave transmitter/receiver mode only.

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

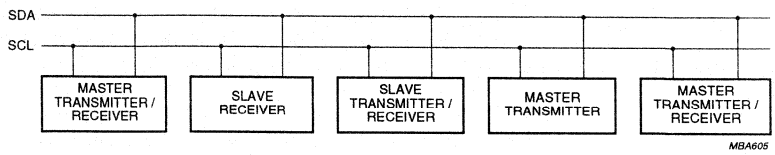


Fig 9. I²C-bus configuration.

7.12.2 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as a STOP condition (P); see Figure 10.

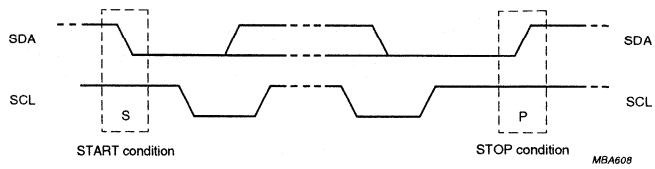


Fig 10. START and STOP conditions for the I²C-bus.

7.12.3 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal; see Figure 11.

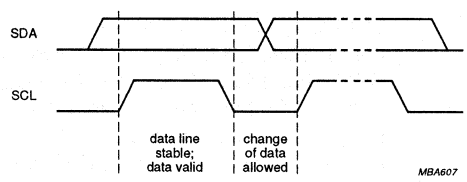


Fig 11. I²C-bus bit transfer.

7.12.4 Acknowledge

The number of data bytes transferred between the START and the STOP conditions from the transmitter to the receiver is unlimited. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledge-related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges must pull down the SDA line during the acknowledge clock period immediately after the 8th SCL pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration).

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

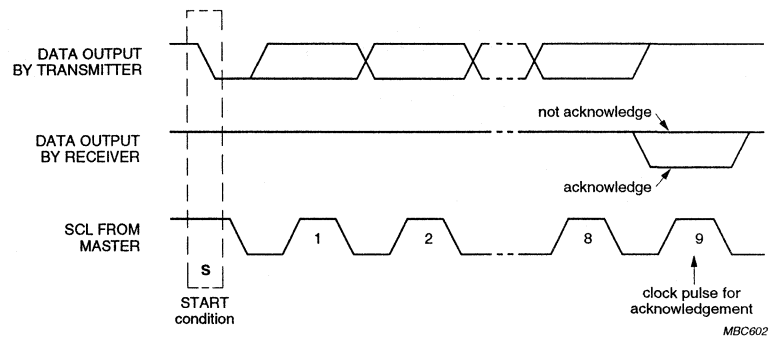


Fig 12. I²C-bus acknowledge.

7.12.5 I²C-bus protocol

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always carried out with first byte transmitted after the START procedure. One I²C-bus slave address is reserved for the PCD3316, E0H (1110 0000 for write and 1110 0001 for read).

The I²C-bus protocol is shown in Figure 13. Two different sequences are considered, the write sequence and the read sequence. Both sequences are initiated with a START condition (S) from the I²C-bus master which is followed by the PCD3316 slave address with the read bit cleared. The first byte after the I²C-bus address is interpreted as the address of a PCD3316 register.During the write sequence the register address of the PCD3316 is auto-incremented on each acknowledge. The write sequence is ended with a STOP condition from the master. If the addressed register is read-only or non-existent, nothing will be changed.

For the read sequence the bus master issues a repeated START condition followed by the PCD3316 slave address with the read bit set. Then data is read from previously set address and sent out. When the master responds with an acknowledge the address of the register is auto incremented and the slave will put the data from the next register on the bus. The read sequence is stopped when the master stops giving an acknowledge and generates a STOP condition.

When a non-existing register is addressed the PCD3316 will return FFH. Existing register addresses are shown in Section 7.13. An additional register address (73H) is reserved for test purposes. This address cannot be reached with the auto-increment function of the I²C-bus interface.

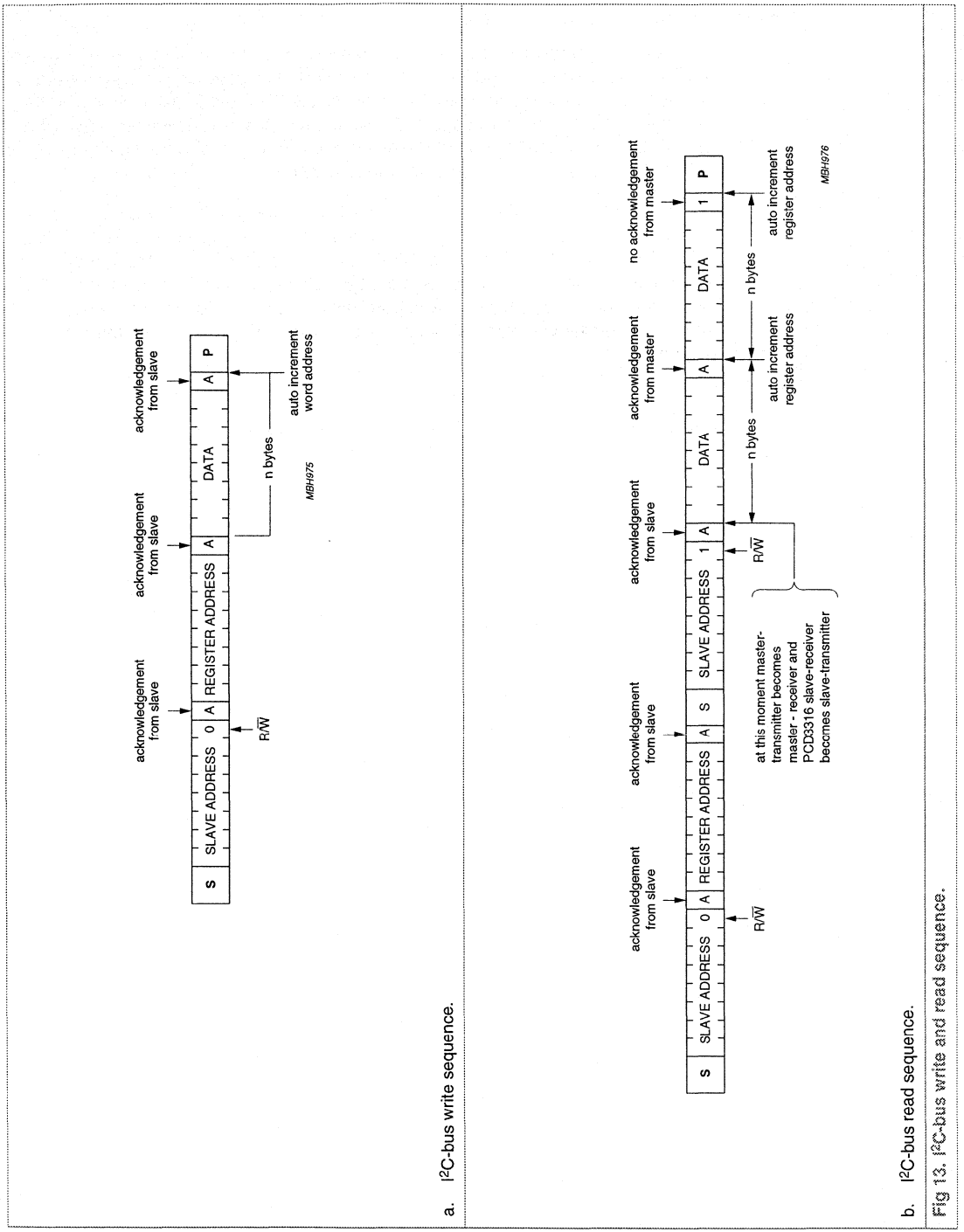


Fig 13. I²C-bus write and read sequence.

7.12.6 I²C-bus bit rate

When a microcontroller is used that implements an I²C-bus in software, the bit rate of the I²C-bus can be critical during reception of FSK. The collection of the interrupt data and FSK-data from the PCD3316 takes 48 bits on the I²C-bus. With an FSK baud rate of 1200 (corresponds to 1200 bits per second) the minimal speed of the I²C-bus should be 5.76 kbits/s. Additional interrupts generated by the time base of the PCD3316 will cause the processor to collect extra information from the PCD3316.

As a consequence, the FSK-data can be overrun in the PCD3316 and one data byte will be lost. In this case, the time base interrupt should be suppressed while FSK is active. This can be done by setting the 'INT-SUP on/off' bit (bit 4 in Mode register 2). The 'TB on/off' bit (bit 6 in Mode register 2) will still be set but the IRQ output will not be activated by the time base interrupt. Any time base interrupt can be detected by the microcontroller when an FSK interrupt is processed by reading the Interrupt register.

7.13 Registers

Table 4: Register overview

Address	Name	Function	Read/Write	Default value
00H	CIDINT	Interrupt register	read only	0000 0000
01H	CIDFSK	FSK data register	read only	–
02H	CIDSTA	Status register	read only	–
03H	CIDRNG	Ringer period register	read only	–
04H	CIDMD1	Mode register 1	read/write	0101 1000
05H	CIDMD2	Mode register 2	read/write	1101 0000

7.13.1 Interrupt register (CIDINT)

Table 5: Interrupt register
Address: 00H; read only.

7	6	5	4	3	2	1	0
MIN Interrupt	SEC Interrupt	FSK Interrupt	Low Level Status	POL1 Interrupt	POL0 Interrupt	CAS Interrupt	–

Table 6: Description of CIDINT bits

Bit	Symbol	Description
CIDINT.7	MIN Interrupt	MIN Interrupt = 0: no interrupt request; MIN Interrupt = 1: one minute interrupt request
CIDINT.6	SEC Interrupt	SEC Interrupt = 0: no interrupt request; SEC Interrupt = 1: one second interrupt request
CIDINT.5	FSK Interrupt	FSK Interrupt = 0: no FSK interrupt or FSK disabled; FSK Interrupt = 1: FSK interrupt, one byte received
CIDINT.4	Low Level Status	Low Level Status = 0: signal level on selected input above power reference (no interrupt); Low Level Status = 1: signal level on selected input below power reference (no interrupt)
CIDINT.3	POL1 Interrupt	POL1 Interrupt = 0: no zero to one changes on POL1 input or polarity interrupt disabled; POL1 Interrupt = 1: a one to zero input change on the POL1 input is detected
CIDINT.2	POL0 Interrupt	POL0 Interrupt = 0: no one to zero changes on POL0 input or polarity interrupt disabled; POL0 Interrupt = 1: a zero to one input change on the POL0 input is detected
CIDINT.1	CAS Interrupt	CAS Interrupt = 0: no CAS signal detected or CAS disabled; CAS Interrupt = 1: CAS signal detected
CIDINT.0	–	reserved bit

7.13.2 FSK data register (CDFSK)

Table 7: Interrupt register
Address: 01H; read only.

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Table 8: Description of CDFSK bits

Bit	Symbol	Description
CDFSK.7 to CDFSK.0	D7 to D0	If an FSK interrupt has occurred and no FSK error is detected, the FSK data register contains valid data.

7.13.3 Status register (CIDSTA)

Table 9: Status register
Address: 02H; read only.

7	6	5	4	3	2	1	0
POL1	POL0	LOW-BAT Indication	FSK-BOM Indication	FSK-OVR Error	FSK-FRM Error	–	–

Table 10: Description of CIDSTA bits

Bit	Symbol	Description
CIDSTA.7	POL1	POL1 = 0: voltage on input POL1 < V_{ref}; POL1 = 1: voltage on input POL1 > V_{ref}
CIDSTA.6	POL0	POL0 = 0: voltage on input POL0 > V_{ref}; POL0 = 1: voltage on input POL0 < V_{ref}
CIDSTA.5	LOW-BAT Indication	LOW-BAT Indication = 0: voltage on input LOWBAT > V_{ref}; LOW-BAT Indication = 1: voltage on input LOWBAT < V_{ref}
CIDSTA.4	FSK-BOM Indication	FSK-BOM Indication = 0: begin of mark period not yet detected; FSK-BOM Indication = 1: begin of mark period detected
CIDSTA.3	FSK-OVR Error	FSK-OVR Error = 0: no FSK overrun error; FSK-OVR Error = 1: FSK overrun error, data byte(s) lost
CIDSTA.2	FSK-FRM Error	FSK-FRM Error = 0: no FSK frame error; FSK-FRM Error = 1: FSK frame error, stop bit was wrong
CIDSTA.1 and CIDSTA.0	–	reserved bits

7.13.4 Ringer period register (CIDRNG)

Table 11: Register format
Address: 03H; read only.

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Table 12: Description of CIDRNG bits

Bit	Symbol	Description
CIDRNG.7 to CIDRNG.0	D7 to D0	The value held in this byte denotes the time between two positive edges of the POL1 comparator output (between two positive edges of POL1 one positive edge of POL0 must have been detected).

7.13.5 Mode register 1 (CIDMD1)

Table 13: Mode register 1
Address: 04H; read/write.

7	6	5	4	3	2	1	0
FSK on/off	FSK-BOM-mask on/off	CAS on/off	POL on/off	INT polarity HIGH/LOW	–	–	–

Table 14: Description of CIDMD1 bits

Bit	Symbol	Description
CIDMD1.7	FSK on/off	FSK on/off = 0: FSK receiver disabled; FSK on/off = 1: FSK receiver enabled
CIDMD1.6	FSK-BOM-mask on/off	FSK-BOM-mask on/off = 0: FSK interrupts will be generated when a data word was received even before mark period (data from channel seizure); FSK-BOM-mask on/off = 1: FSK interrupts will only be generated after the mark period was detected (no interrupts from channel seizure)
CIDMD1.5	CAS on/off	CAS on/off = 0: CAS detector disabled; CAS on/off = 1: CAS detector enabled
CIDMD1.4	POL on/off	POL on/off = 0: disable interrupts due to polarity change; POL on/off = 1: enable interrupts due to polarity change
CIDMD1.3	INT polarity HIGH/LOW	INT polarity HIGH/LOW = 0: interrupt pin active LOW; INT polarity HIGH/LOW = 1: interrupt pin active HIGH
CIDMD1.2 to CIDMD1.0	–	reserved bits

7.13.6 Mode register 2 (CIDMD2)

Table 15: Mode register 2
Address: 05H; read/write.

7	6	5	4	3	2	1	0
XTAL on/off	TB on/off	SEC/MIN	INT-SUP on/off	–	–	–	–

Table 16: Description of CIDMD2 bits

Bit	Symbol	Description
CIDMD2.7	XTAL on/off	XTAL on/off = 0: disable 3.58 MHz oscillator; XTAL on/off = 1: enable 3.58 MHz oscillator
CIDMD2.6	TB on/off	TB on/off = 0: disable 32.768 kHz timebase; TB on/off = 1: enable 32.768 kHz timebase
CIDMD2.5	SEC/MIN	SEC/MIN = 0: every minute a timebase interrupt; SEC/MIN = 1: every second a timebase interrupt
CIDMD2.4	INT-SUP on/off	INT-SUP on/off = 0: enable SEC/MIN interrupts during FSK reception; INT-SUP on/off = 1: disable SEC/MIN interrupts during FSK reception
CIDMD2.3 to CIDMD2.0	–	reserved bits

8. Limiting values

Table 17: Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		–0.5	+5.0	V
I_{DD}	supply current		–	50	mA
I_I	DC input current at any input		–10	+10	mA
I_O	DC output current at any output		–10	+10	mA
V_I	input voltage on all inputs		–0.5	V_{DD} + 0.5 [1]	V
P_{tot}	total power dissipation		–	300	mW
P_O	power dissipation per output		–	10	mW
T_{amb}	operating ambient temperature		–25	+70	°C
T_{stg}	storage temperature		–65	+150	°C

[1] $V_{I(max)}$ = 5.0 V.

9. Characteristics

Table 18: Characteristics
V_{DD} = 2.5 to 3.6 V; T_{amb} = –25 to +70 °C; HXIN = 3.579545 MHz ±0.05%; LXIN = 32.768 kHz ±0.1%; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DD}	supply voltage		[1]	2.5	3.3	3.6	V
$V_{POR(H)}$	power-on reset HIGH voltage			1.85	2.05	2.25	V
$V_{hys(POR)}$	power-on reset hysteresis voltage		[2]	50	100	150	mV
I_{DD}	supply currents	V_{DD} = 2.5 V					
	Power-down mode		[3]	–	30	70	µA
	operating		[3][4]	–	2.0	2.3	mA
Low voltage and polarity comparators (pins LOWBAT, POL0 and POL1)							
V_{hys}	hysteresis voltage			–	20	–	mV
I_{LI}	input leakage current		[5]	–	–	1	µA
Internal reference							
V_{ref}	reference voltage level			1.125	1.25	1.375	V
$P_{i(ref)}$	input signal reference power for Low Level Status bit	in 600 Ω load	[6]	–43.8	–	–37.8	dBm
$t_{r(level)}$	input signal to Low Level Status bit rise time	input signal power < $P_{i(ref)}$		–	–	8	ms
$t_{f(level)}$	input signal to Low Level Status bit fall time	input signal power > $P_{i(ref)}$		–	–	8	ms
Logical output (pin IRQ) [7]							
I_{OL}	LOW-level output current	V_{IRQ} = 0.4 V		2	–	–	mA
I_{OH}	HIGH-level output current	V_{IRQ} = V_{DD} – 0.4 V		2	–	–	mA

Table 18: Characteristics *...continued*

V_{DD} = 2.5 to 3.6 V; T_{amb} = −25 to +70 °C; HXIN = 3.579545 MHz ±0.05%; LXIN = 32.768 kHz ±0.1%; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
FSK receiver (pins FSKIN+ and FSKIN−)							
Z_i	input impedance FSKIN+ to FSKIN−			–	1.4	–	MΩ
$Z_{source(max)}$	maximum source impedance			–	–	200	kΩ
$P_{i(FSKIN)}$	input signal power	in 600 Ω load	[8]	−50	–	0	dBm
S/N_{FSK}	signal-to-noise ratio	200 to 3400 Hz		20	–	–	dB
$\|V_{dif}\|$	differential voltage between mark and space (twist)			–	–	10	dB
$f_{(D)}$	data transmission rate frequency			1180	1200	1212	bits/s
f_s	space frequency			2068	–	2222	Hz
f_m	mark frequency			1188	–	1320	Hz
CAS detector (pin CASIN)							
Z_i	input impedance CASIN to V_{ref}			–	1.4	–	MΩ
$Z_{source(max)}$	maximum source impedance			–	–	200	kΩ
P_i	input signal power	in 600 Ω load	[6]	−37.8	–	0	dBm
$TH_{ns(CAS)}$	no signal threshold (CAS)	in 600 Ω load		−43.8	–	−37.8	dBm
f_l	low tone frequency			–	2130	–	Hz
f_h	high tone frequency			–	2750	–	Hz
Δf_{max}	maximum frequency deviation		[9]	−0.5	–	+0.5	%
V_{dif}	differential voltage level (twist)		[9]	–	–	6	dB
t_{dt}	dual tone detection time			60	–	–	ms
I^2C-bus interface (pins SCL and SDA)[10]; see Figure 14							
V_{IL}	LOW-level input voltage		[11]	0	–	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		[11]	$0.7V_{DD}$	–	V_{DD}	V
I_{OL1}	LOW-level output current for pin SDA	$V_{O(SDA)}$ = 0.4 V		2	–	–	mA
C_i	input capacitance for each I/O pin			–	–	10	pF
f_{SCL}	SCL clock frequency			–	–	100	kHz
t_{BUF}	bus free time			4.7	–	–	µs
$t_{SU;STA}$	START condition set-up time			4.7	–	–	µs
$t_{HD;STA}$	START condition hold time			4.0	–	–	µs
t_{LOW}	SCL LOW time			4.7	–	–	µs
t_{HIGH}	SCL HIGH time			4.0	–	–	µs
t_r	maximum SCL and SDA rise time		[12]	–	–	1000	ns
t_f	maximum SCL and SDA fall time		[12]	–	–	300	ns
$t_{SU;DAT}$	data set-up time			250	–	–	ns
$t_{HD;DAT}$	data hold time			0	–	–	ns
$t_{VD;DAT}$	SCL LOW to data out valid time			–	–	3.4	µs
$t_{SU;STO}$	STOP condition set-up time			4.0	–	–	µs

Table 18: Characteristics...*continued*

V_{DD} = 2.5 to 3.6 V; T_{amb} = −25 to +70 °C; HXIN = 3.579545 MHz ±0.05%; LXIN = 32.768 kHz ±0.1%; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
3.58 MHz oscillator (pins HXIN and HXOUT)						
$V_{HXIN(p-p)}$	external clock signal amplitude (peak-to-peak value) on pin HXIN		0.5	–	V_{DD}	V
$Z_{i(HXIN)}$	input impedance on pin HXIN		300	1000	–	kΩ
$C1_i$; $C2_i$	input capacitance on pins HXIN and HXOUT [13]		–	10	–	pF
32 kHz oscillator (pins LXIN and LXOUT)						
g_m	transconductance	$V_{i(p-p)} < 50$ mV	2	4	10	µS
$C_{i(LXIN)}$	LXIN input capacitance		–	13	–	pF
$C_{o(LXOUT)}$	LXOUT output capacitance		–	10	–	pF

[1] Except for FSK and CAS detection, all circuitry works already when $V_{DD} > V_{POR(H)}$. Since the I²C-bus interface will work (starts to acknowledge), the application can start reading the LOW-BAT Indication bit (Status register, bit 5) to check whether the supply voltage has reached the operating voltage level. A voltage divider network can be connected to pins V_{DD}, LOWBAT and AGND/DGND such that $V_{LOWBAT} = V_{ref}$ if $V_{DD} = V_{DD(min)}$.

[2] The power-on reset LOW level is defined as $V_{POR(L)} = V_{POR(H)} - V_{hys(POR)}$. By design $V_{POR(L)}$ is always lower than $V_{POR(H)}$.

[3] 32 kHz oscillator on (MIN Interrupt, SEC Interrupt, Polarity change, Low battery and Level detect available).

[4] 3.58 MHz oscillator on (device fully operational).

[5] $GND < V_I < V_{DD}$. The leakage currents are generally very small, <1 nA. The value given here, 1 µA, is a maximum that can occur after an Electrostatic Stress on the pin.

[6] When FSK is selected the signal power is measured between 1000 and 2200 Hz. When CAS is selected signal levels are measured between 2000 and 2800 Hz.

[7] The IRQ pin is implemented as a 3-state pin which is only active (either HIGH or LOW) when an interrupt occurs. A pull-up or pull-down has to be connected to define the line when no interrupt is generated.

[8] Verified on sampling basis.

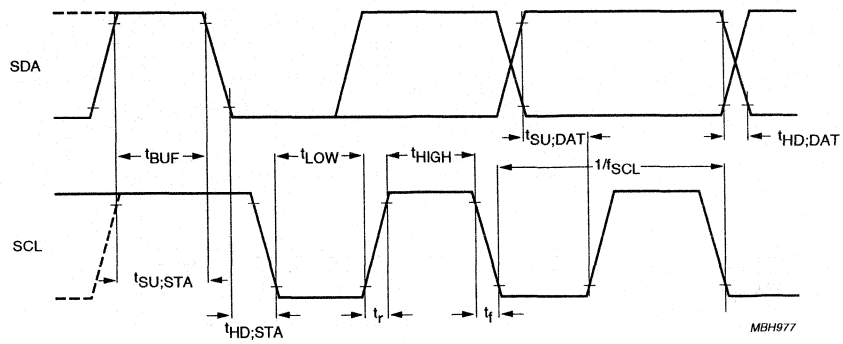
[9] According to Bellcore specification: near end speech level ≤ −7 dBm ASL (ASL = Active Speech Level), referenced to 600 Ω, according to method B of recommendation P.56.

[10] Pins SCL and SDA are equipped with an open-drain output buffer. The pins have no clamp diode to V_{DD}.

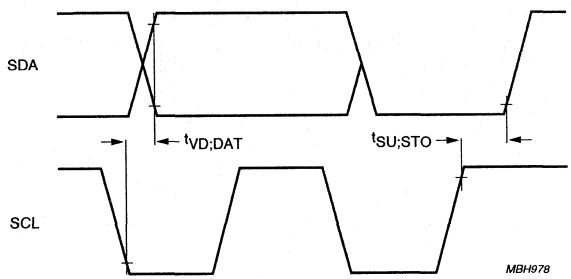
[11] The input threshold voltage of SCL and SDA meet the I²C-bus specification. Therefore, an input voltage below $0.3V_{DD}$ will be recognized as a logic 0 and an input voltage above $0.7V_{DD}$ will be recognized as a logic 1

[12] Maximum capacitive load for each bus line is 400 pF.

[13] $C1_i$ and $C2_i$ are the total internal capacitances (including gate capacitance and leadframe capacitance).



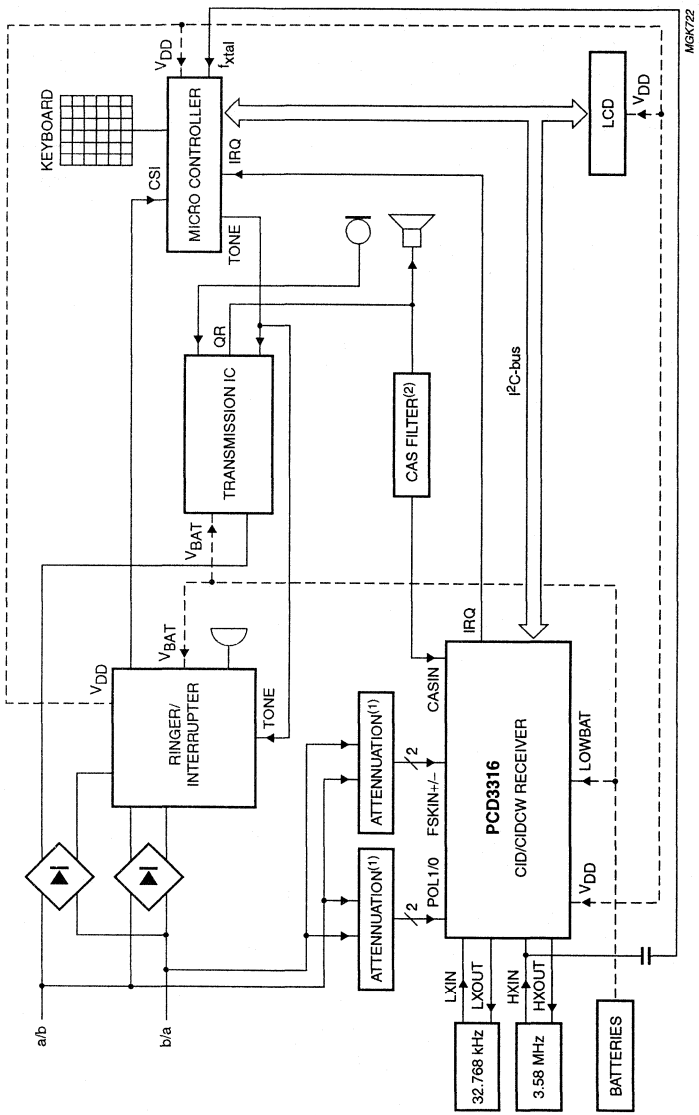
a. Timing diagram 1.



b. Timing diagram 2.

Fig 14. I²C-bus timing.

10. Application information

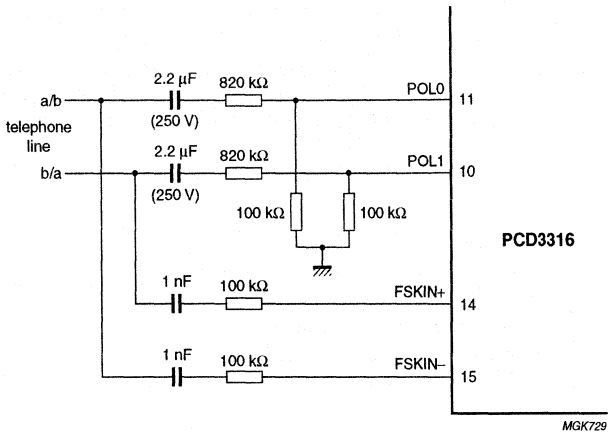


A demo-board (OM5843) of this configuration is available. Please contact your Philips sales office.

(1) See Figure 16a.

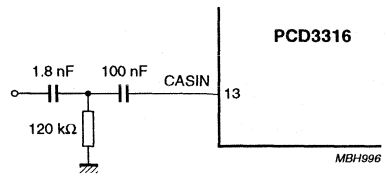
(2) See Figure 16b.

Fig 15. Application diagram for a telephone with CID/CIDCW functionality.



Attenuation networks to connect the polarity and FSK inputs to the telephone line.

a. Attenuation networks.



High-pass filter (cut-off frequency ≈ 1 kHz) to improve performance of CAS detection.

b. High-pass filter.

Fig 16. Application diagrams.

11. Test information

11.1 Application note on Customer Premises Equipment (CPE) testing

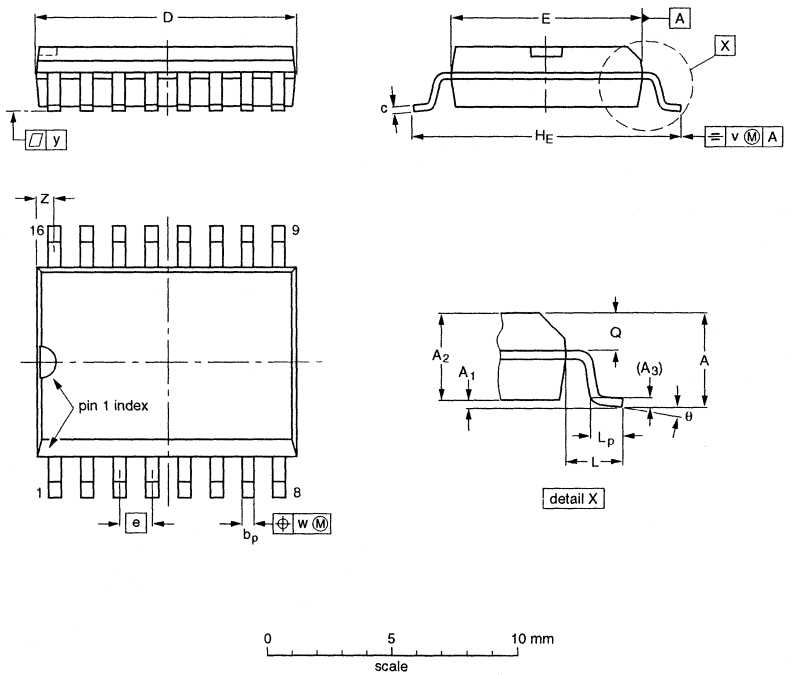
Under certain circumstances, some external CIDCW test equipment may generate incorrect pulses after the ringing signal becomes inactive. These pulses may cause the FSK detector of the PCD3316 to respond. Note that this is by no means an incorrect behaviour of the PCD3316 chip, but a correct detection of incorrect test stimuli. However, if not known, it may lead to confusing results during testing of the CPE.

To avoid the issue described above, following work-around can be used:

1. Disable the FSK detection of PCD3316, before and during the ringing signal detection.
2. Switch on the FSK detection only after a certain period, e.g. 100 ms after the ringing signal goes inactive.
3. When the first FSK data is detected, e.g '55H' (possible part of channel seizure), switch off the FSK detection and on again. This will force the FSK detector to resynchronize and detect the normal FSK data correctly. It may be necessary to repeat this sequence a number of times to ensure that the data detected really comes from the channel seizure. Thus, it is recommended to wait for a multiple number of bytes '55H' to be detected to validate a correct channel seizure.

12. Package outline

SO16: plastic small outline package; 16 leads; body width 7.5 mm **SOT162-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	10.5 10.1	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.41 0.40	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT162-1	075E03	MS-013AA				~~95-01-24~~ 97-05-22

Fig 17. SOT162-1.

13. Soldering

13.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

13.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

13.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C. A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

13.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

13.5 Package related soldering information

Table 19: Suitability of surface mount IC packages for wave and reflow soldering methods

Package	Soldering method	
	Wave	Reflow [1]
BGA, SQFP	not suitable	suitable
HLQFP, HSQFP, HSOP, HTSSOP, SMS	not suitable [2]	suitable
PLCC, SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended [3] [4]	suitable
SSOP, TSSOP, VSO	not recommended [5]	suitable

[1] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods.*

[2] These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).

[3] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[4] Wave soldering is only suitable for LQFP, QFP and TQFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[5] Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

14. Revision history

Rev	Date	CPCN	Description
01	990311	-	**This data sheet supersedes the version of 1998 May 14 (9397 750 03525):** • The format of this specification has been redesigned to comply with Philips Semiconductors' new presentation and information standard • Section 1 "General description" on page 1: reference to application note AN98701 added • Section 7.6 "Level detect" on page 7: Added text regarding the frequency band for signal power measurement • Section 7.10 "3.58 MHz oscillator circuitry" on page 8: recommended resonator indication removed • Section 7.13 "Registers" on page 15: new register presentation in this section • Table 14 " Description of CIDMD1 bits" on page 17: Description of bit CIDMD1.6 and CIDMD1.5 adjusted • Application diagram Figure 16a on page 23: diodes removed • Added Section 11.1 "Application note on Customer Premises Equipment (CPE) testing" on page 23.

Data sheet status

Datasheet status	Product status	Definition[1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued data sheet before initiating or completing a design.

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Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Contents

Date of release: 11 March 1999 **Document order number: 9397 750 04824**

CONTENTS

48 × 84 pixels matrix LCD controller/driver PCD8544

1 FEATURES

- Single chip LCD controller/driver
- 48 row, 84 column outputs
- Display data RAM 48 × 84 bits
- On-chip:
  - Generation of LCD supply voltage (external supply also possible)
  - Generation of intermediate LCD bias voltages
  - Oscillator requires no external components (external clock also possible).
- External $\overline{RES}$ (reset) input pin
- Serial interface maximum 4.0 Mbits/s
- CMOS compatible inputs
- Mux rate: 48
- Logic supply voltage range V_{DD} to V_{SS}: 2.7 to 3.3 V
- Display supply voltage range V_{LCD} to V_{SS}
  - 6.0 to 8.5 V with LCD voltage internally generated (voltage generator enabled)
  - 6.0 to 9.0 V with LCD voltage externally supplied (voltage generator switched-off).
- Low power consumption, suitable for battery operated systems
- Temperature compensation of V_{LCD}
- Temperature range: –25 to +70 °C.

2 GENERAL DESCRIPTION

The PCD8544 is a low power CMOS LCD controller/driver, designed to drive a graphic display of 48 rows and 84 columns. All necessary functions for the display are provided in a single chip, including on-chip generation of LCD supply and bias voltages, resulting in a minimum of external components and low power consumption.

The PCD8544 interfaces to microcontrollers through a serial bus interface.

The PCD8544 is manufactured in n-well CMOS technology.

3 APPLICATIONS

- Telecommunications equipment.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCD8544U	–	chip with bumps in tray; 168 bonding pads + 4 dummy pads	–

5 BLOCK DIAGRAM

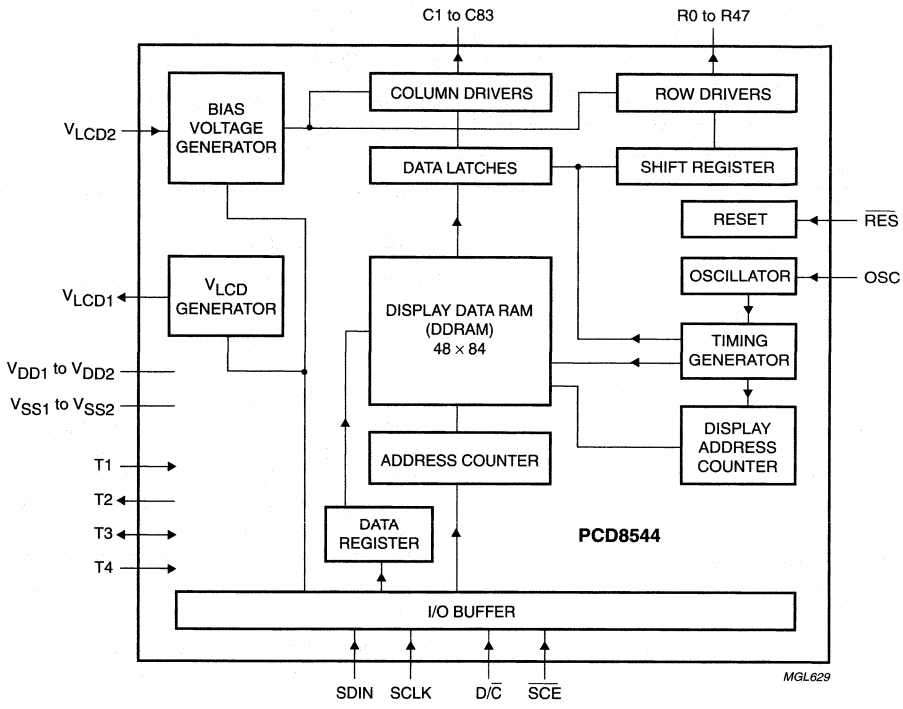


Fig.1 Block diagram.

6 PINNING

SYMBOL	DESCRIPTION
R0 to R47	LCD row driver outputs
C0 to C83	LCD column driver outputs
V_{SS1}, V_{SS2}	ground
V_{DD1}, V_{DD2}	supply voltage
V_{LCD1}, V_{LCD2}	LCD supply voltage
T1	test 1 input
T2	test 2 output
T3	test 3 input/output
T4	test 4 input
SDIN	serial data input
SCLK	serial clock input
D/$\overline{C}$	data/$\overline{command}$
$\overline{SCE}$	chip enable
OSC	oscillator
$\overline{RES}$	external reset input
dummy1, 2, 3, 4	not connected

Note

1. For further details, see Fig.18 and Table 7.

6.1 Pin functions

6.1.1 R0 TO R47 ROW DRIVER OUTPUTS

These pads output the row signals.

6.1.2 C0 TO C83 COLUMN DRIVER OUTPUTS

These pads output the column signals.

6.1.3 V_{SS1}, V_{SS2}: NEGATIVE POWER SUPPLY RAILS

Supply rails V_{SS1} and V_{SS2} must be connected together.

6.1.4 V_{DD1}, V_{DD2}: POSITIVE POWER SUPPLY RAILS

Supply rails V_{DD1} and V_{DD2} must be connected together.

6.1.5 V_{LCD1}, V_{LCD2}: LCD POWER SUPPLY

Positive power supply for the liquid crystal display. Supply rails V_{LCD1} and V_{LCD2} must be connected together.

6.1.6 T1, T2, T3 AND T4: TEST PADS

T1, T3 and T4 must be connected to V_{SS}, T2 is to be left open. Not accessible to user.

6.1.7 SDIN: SERIAL DATA LINE

Input for the data line.

6.1.8 SCLK: SERIAL CLOCK LINE

Input for the clock signal: 0.0 to 4.0 Mbits/s.

6.1.9 D/$\overline{C}$: MODE SELECT

Input to select either command/address or data input.

6.1.10 $\overline{SCE}$: CHIP ENABLE

The enable pin allows data to be clocked in. The signal is active LOW.

6.1.11 OSC: OSCILLATOR

When the on-chip oscillator is used, this input must be connected to V_{DD}. An external clock signal, if used, is connected to this input. If the oscillator and external clock are both inhibited by connecting the OSC pin to V_{SS}, the display is not clocked and may be left in a DC state. To avoid this, the chip should always be put into Power-down mode before stopping the clock.

6.1.12 $\overline{RES}$: RESET

This signal will reset the device and must be applied to properly initialize the chip. The signal is active LOW.

7 FUNCTIONAL DESCRIPTION

7.1 Oscillator

The on-chip oscillator provides the clock signal for the display system. No external components are required and the OSC input must be connected to V_{DD}. An external clock signal, if used, is connected to this input.

7.2 Address Counter (AC)

The address counter assigns addresses to the display data RAM for writing. The X-address X_6 to X_0 and the Y-address Y_2 to Y_0 are set separately. After a write operation, the address counter is automatically incremented by 1, according to the V flag.

7.3 Display Data RAM (DDRAM)

The DDRAM is a 48 × 84 bit static RAM which stores the display data. The RAM is divided into six banks of 84 bytes (6 × 8 × 84 bits). During RAM access, data is transferred to the RAM through the serial interface. There is a direct correspondence between the X-address and the column output number.

7.4 Timing generator

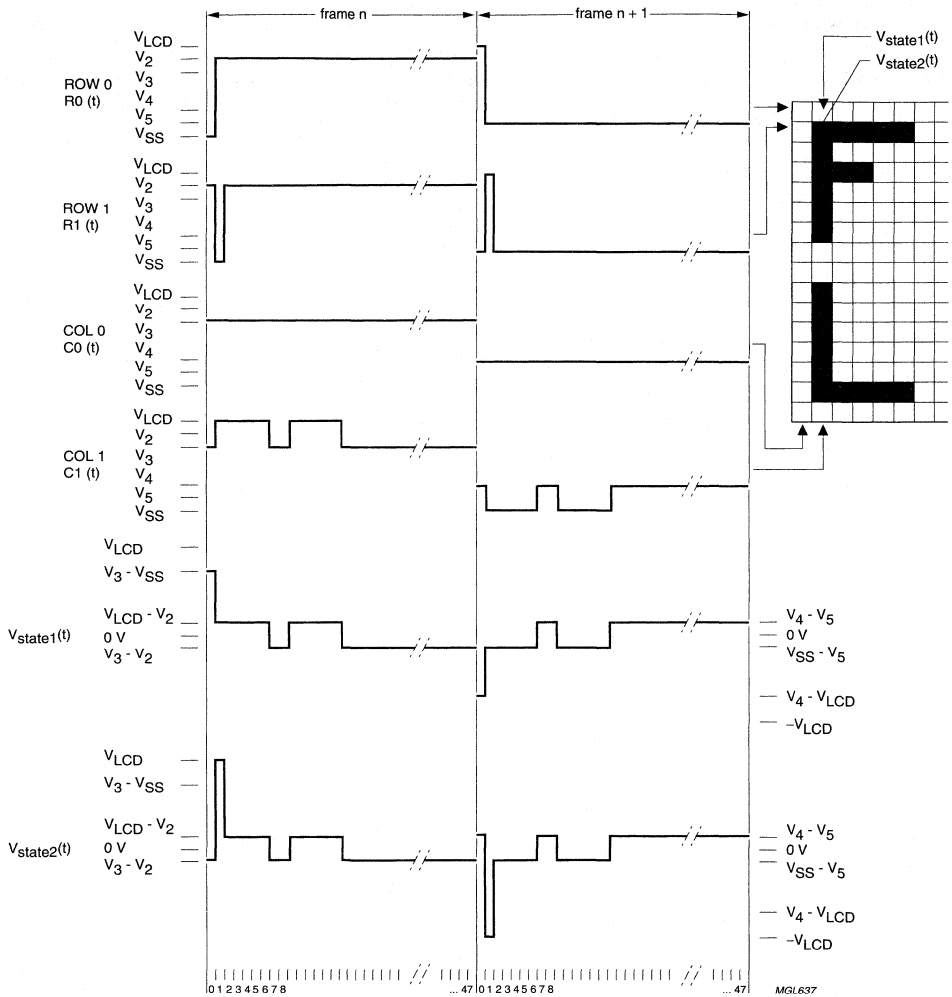
The timing generator produces the various signals required to drive the internal circuits. Internal chip operation is not affected by operations on the data buses.

7.5 Display address counter

The display is generated by continuously shifting rows of RAM data to the dot matrix LCD through the column outputs. The display status (all dots on/off and normal/inverse video) is set by bits E and D in the 'display control' command.

7.6 LCD row and column drivers

The PCD8544 contains 48 row and 84 column drivers, which connect the appropriate LCD bias voltages in sequence to the display in accordance with the data to be displayed. Figure 2 shows typical waveforms. Unused outputs should be left unconnected.



$V_{state1}(t) = C1(t) - R0(t)$.
$V_{state2}(t) = C1(t) - R1(t)$.

Fig.2 Typical LCD driver waveforms.

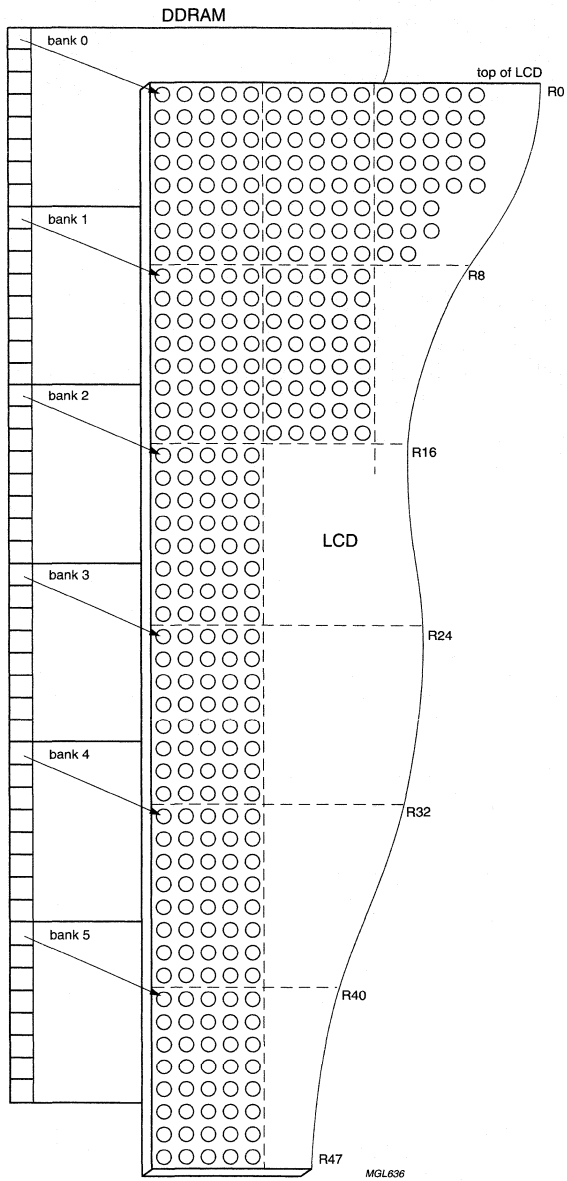


Fig.3 DDRAM to display mapping.

7.7 Addressing

Data is downloaded in bytes into the 48 by 84 bits RAM data display matrix of PCD8544, as indicated in Figs. 3, 4, 5 and 6. The columns are addressed by the address pointer. The address ranges are: X 0 to 83 (1010011), Y 0 to 5 (101). Addresses outside these ranges are not allowed. In the vertical addressing mode (V = 1), the Y address increments after each byte (see Fig.5). After the last Y address (Y = 5), Y wraps around to 0 and X increments to address the next column. In the horizontal addressing mode (V = 0), the X address increments after each byte (see Fig.6). After the last X address (X = 83), X wraps around to 0 and Y increments to address the next row. After the very last address (X = 83 and Y = 5), the address pointers wrap around to address (X = 0 and Y = 0).

7.7.1 DATA STRUCTURE

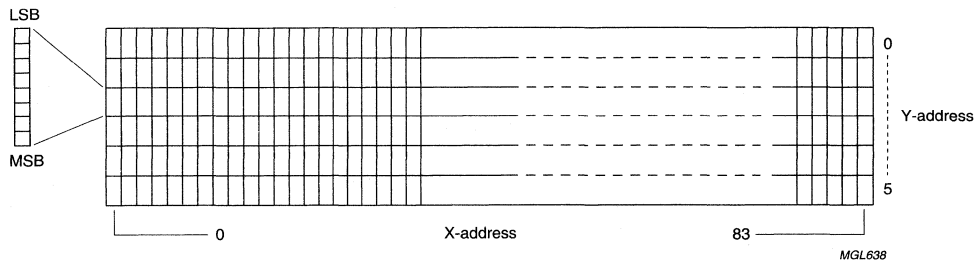


Fig.4 RAM format, addressing.

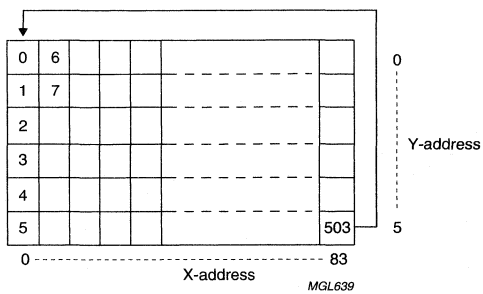


Fig.5 Sequence of writing data bytes into RAM with vertical addressing (V = 1).

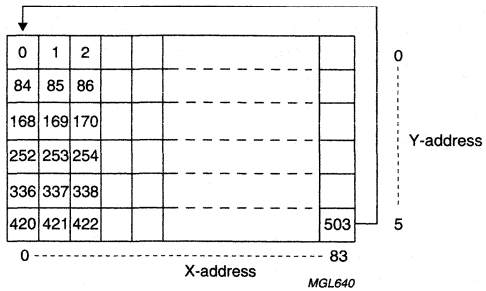
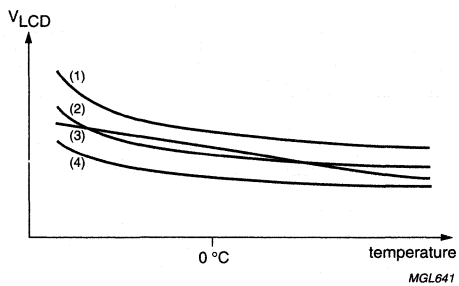


Fig.6 Sequence of writing data bytes into RAM with horizontal addressing (V = 0).

7.8 Temperature compensation

Due to the temperature dependency of the liquid crystals' viscosity, the LCD controlling voltage V_{LCD} must be increased at lower temperatures to maintain optimum contrast. Figure 7 shows V_{LCD} for high multiplex rates. In the PCD8544, the temperature coefficient of V_{LCD}, can be selected from four values (see Table 2) by setting bits TC_1 and TC_0.



(1) Upper limit.
(2) Typical curve.
(3) Temperature coefficient of IC.
(4) Lower limit.

Fig.7 V_{LCD} as function of liquid crystal temperature (typical values).

8 INSTRUCTIONS

The instruction format is divided into two modes: If D/$\overline{C}$ (mode select) is set LOW, the current byte is interpreted as command byte (see Table 1). Figure 8 shows an example of a serial data stream for initializing the chip. If D/$\overline{C}$ is set HIGH, the following bytes are stored in the display data RAM. After every data byte, the address counter is incremented automatically.

The level of the D/$\overline{C}$ signal is read during the last bit of data byte.

Each instruction can be sent in any order to the PCD8544. The MSB of a byte is transmitted first. Figure 9 shows one possible command stream, used to set up the LCD driver.

The serial interface is initialized when $\overline{SCE}$ is HIGH. In this state, SCLK clock pulses have no effect and no power is consumed by the serial interface. A negative edge on $\overline{SCE}$ enables the serial interface and indicates the start of a data transmission.

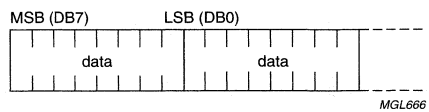


Fig.8 General format of data stream.

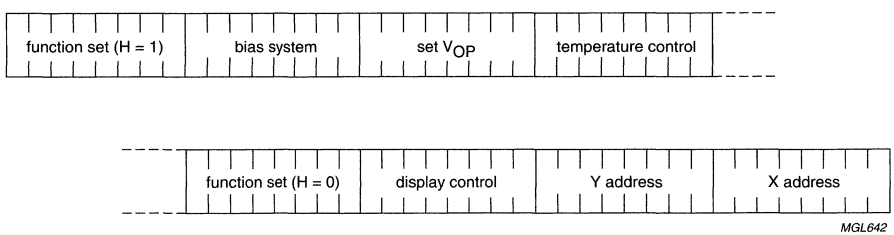


Fig.9 Serial data stream, example.

Figures 10 and 11 show the serial bus protocol.

- When $\overline{SCE}$ is HIGH, SCLK clock signals are ignored; during the HIGH time of $\overline{SCE}$, the serial interface is initialized (see Fig.12)
- SDIN is sampled at the positive edge of SCLK
- D/$\overline{C}$ indicates whether the byte is a command (D/$\overline{C}$ = 0) or RAM data (D/$\overline{C}$ = 1); it is read with the eighth SCLK pulse
- If $\overline{SCE}$ stays LOW after the last bit of a command/data byte, the serial interface expects bit 7 of the next byte at the next positive edge of SCLK (see Fig.12)
- A reset pulse with $\overline{RES}$ interrupts the transmission. No data is written into the RAM. The registers are cleared. If $\overline{SCE}$ is LOW after the positive edge of $\overline{RES}$, the serial interface is ready to receive bit 7 of a command/data byte (see Fig.13).

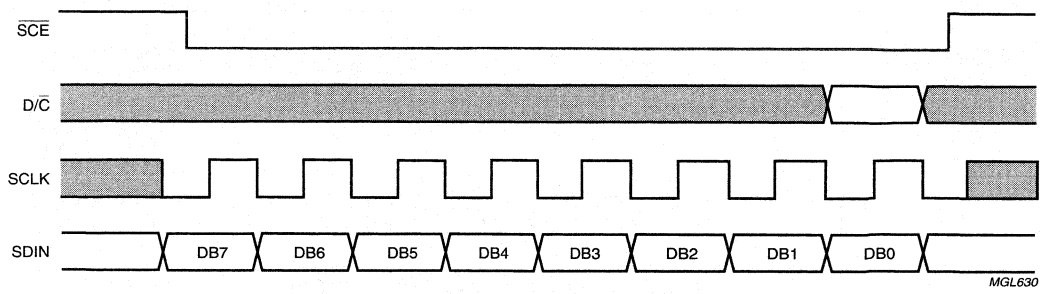


Fig.10 Serial bus protocol - transmission of one byte.

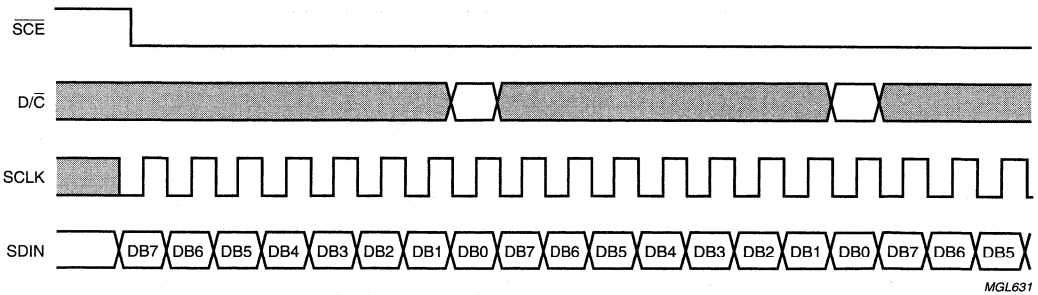


Fig.11 Serial bus protocol - transmission of several bytes.

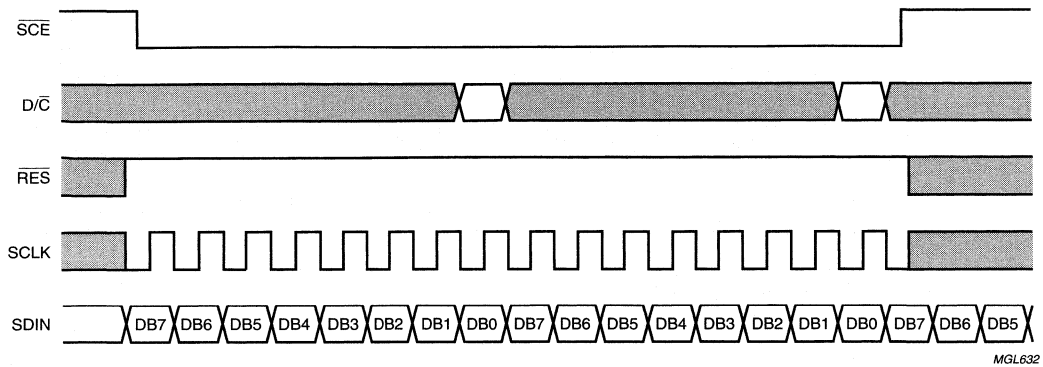


Fig.12 Serial bus reset function ($\overline{SCE}$).

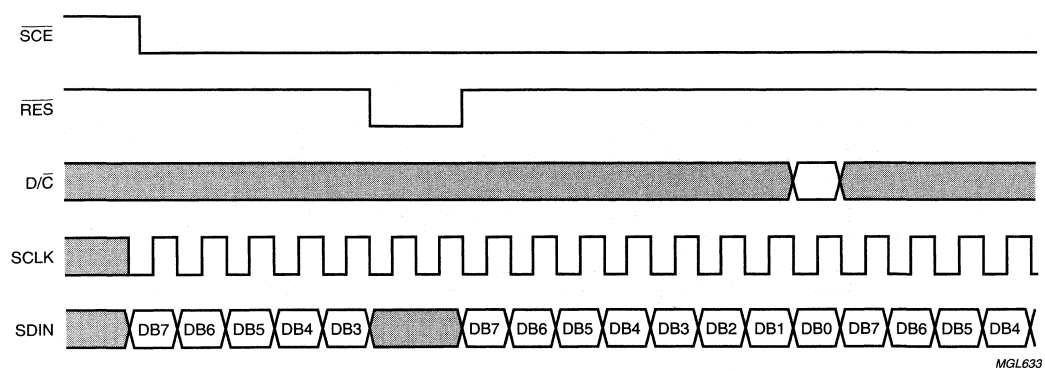


Fig.13 Serial bus reset function ($\overline{RES}$).

Table 1 Instruction set

INSTRUCTION	D/$\overline{C}$	COMMAND BYTE								DESCRIPTION
		DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
(H = 0 or 1)										
NOP	0	0	0	0	0	0	0	0	0	no operation
Function set	0	0	0	1	0	0	PD	V	H	power down control; entry mode; extended instruction set control (H)
Write data	1	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	writes data to display RAM
(H = 0)										
Reserved	0	0	0	0	0	0	1	X	X	do not use
Display control	0	0	0	0	0	1	D	0	E	sets display configuration
Reserved	0	0	0	0	1	X	X	X	X	do not use
Set Y address of RAM	0	0	1	0	0	0	Y_2	Y_1	Y_0	sets Y-address of RAM; $0 \leq Y \leq 5$
Set X address of RAM	0	1	X_6	X_5	X_4	X_3	X_2	X_1	X_0	sets X-address part of RAM; $0 \leq X \leq 83$
(H = 1)										
Reserved	0	0	0	0	0	0	0	0	1	do not use
	0	0	0	0	0	0	0	1	X	do not use
Temperature control	0	0	0	0	0	0	1	TC_1	TC_0	set Temperature Coefficient (TC_x)
Reserved	0	0	0	0	0	1	X	X	X	do not use
Bias system	0	0	0	0	1	0	BS_2	BS_1	BS_0	set Bias System (BS_x)
Reserved	0	0	1	X	X	X	X	X	X	do not use
Set V_{OP}	0	1	V_{OP6}	V_{OP5}	V_{OP4}	V_{OP3}	V_{OP2}	V_{OP1}	V_{OP0}	write V_{OP} to register

Table 2 Explanations of symbols in Table 1

BIT	0	1
PD	chip is active	chip is in Power-down mode
V	horizontal addressing	vertical addressing
H	use basic instruction set	use extended instruction set
D and E		
00	display blank	
10	normal mode	
01	all display segments on	
11	inverse video mode	
TC_1 and TC_0		
00	V_{LCD} temperature coefficient 0	
01	V_{LCD} temperature coefficient 1	
10	V_{LCD} temperature coefficient 2	
11	V_{LCD} temperature coefficient 3	

8.1 Initialization

Immediately following power-on, the contents of all internal registers and of the RAM are undefined. **A $\overline{\text{RES}}$ pulse must be applied**. Attention should be paid to the possibility that the **device may be damaged** if not properly reset.

All internal registers are reset by applying an external $\overline{\text{RES}}$ pulse (active LOW) at pad 31, within the specified time. However, the RAM contents are still undefined. The state after reset is described in Section 8.2.

The $\overline{\text{RES}}$ input must be $\leq 0.3V_{DD}$ when V_{DD} reaches V_{DDmin} (or higher) within a maximum time of 100 ms after V_{DD} goes HIGH (see Fig.16).

8.2 Reset function

After reset, the LCD driver has the following state:

- Power-down mode (bit PD = 1)
- Horizontal addressing (bit V = 0) normal instruction set (bit H = 0)
- Display blank (bit E = D = 0)
- Address counter X_6 to X_0 = 0; Y_2 to Y_0 = 0
- Temperature control mode (TC_1 TC_0 = 0)
- Bias system (BS_2 to BS_0 = 0)
- V_{LCD} is equal to 0, the HV generator is switched off (V_{OP6} to V_{OP0} = 0)
- After power-on, the RAM contents are undefined.

8.3 Function set

8.3.1 Bit PD

- All LCD outputs at V_{SS} (display off)
- Bias generator and V_{LCD} generator off, V_{LCD} can be disconnected
- Oscillator off (external clock possible)
- Serial bus, command, etc. function
- Before entering Power-down mode, the RAM needs to be filled with '0's to ensure the specified current consumption.

8.3.2 Bit V

When V = 0, the horizontal addressing is selected. The data is written into the DDRAM as shown in Fig.6. When V = 1, the vertical addressing is selected. The data is written into the DDRAM, as shown in Fig.5.

8.3.3 Bit H

When H = 0 the commands 'display control', 'set Y address' and 'set X address' can be performed; when H = 1, the others can be executed. The 'write data' and 'function set' commands can be executed in both cases.

8.4 Display control

8.4.1 Bits D and E

Bits D and E select the display mode (see Table 2).

8.5 Set Y address of RAM

Y_n defines the Y vector addressing of the display RAM.

Table 3 Y vector addressing

Y_2	Y_1	Y_0	BANK
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5

8.6 Set X address of RAM

The X address points to the columns. The range of X is 0 to 83 (53H).

8.7 Temperature control

The temperature coefficient of V_{LCD} is selected by bits TC_1 and TC_0.

8.8 Bias value

The bias voltage levels are set in the ratio of R - R - nR - R - R, giving a 1/(n + 4) bias system. Different multiplex rates require different factors n (see Table 4). This is programmed by BS_2 to BS_0. For Mux 1 : 48, the optimum bias value n, resulting in 1/8 bias, is given by:

$$n = \sqrt{48} - 3 = 3.928 = 4 \quad (1)$$

Table 4 Programming the required bias system

BS_2	BS_1	BS_0	n	RECOMMENDED MUX RATE
0	0	0	7	1 : 100
0	0	1	6	1 : 80
0	1	0	5	1 : 65/1 : 65
0	1	1	4	1 : 48
1	0	0	3	1 : 40/1 : 34
1	0	1	2	1 : 24
1	1	0	1	1 : 18/1 : 16
1	1	1	0	1 : 10/1 : 9/1 : 8

Table 5 LCD bias voltage

SYMBOL	BIAS VOLTAGES	BIAS VOLTAGE FOR 1/8 BIAS
V1	V_{LCD}	V_{LCD}
V2	(n + 3)/(n + 4)	$^7/_8 \times V_{LCD}$
V3	(n + 2)/(n + 4)	$^6/_8 \times V_{LCD}$
V4	2/(n + 4)	$^2/_8 \times V_{LCD}$
V5	1/(n + 4)	$^1/_8 \times V_{LCD}$
V6	V_{SS}	V_{SS}

8.9 Set V_{OP} value

The operation voltage V_{LCD} can be set by software. The values are dependent on the liquid crystal selected. V_{LCD} = a + (V_{OP6} to V_{OP0}) × b [V]. In the PCD8544, a = 3.06 and b = 0.06 giving a program range of 3.00 to 10.68 at room temperature.

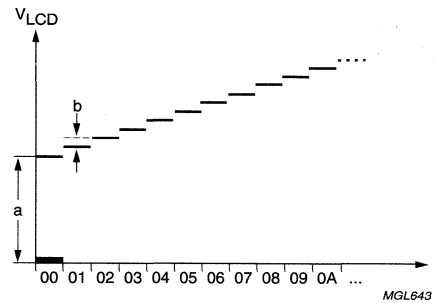
Note that the charge pump is turned off if V_{OP6} to V_{OP0} is set to zero.

For Mux 1 : 48, the optimum operation voltage of the liquid can be calculated as:

$$V_{LCD} = \frac{1+\sqrt{48}}{\sqrt{2\cdot\left(1-\frac{1}{\sqrt{48}}\right)}}\cdot V_{th} = 6.06\cdot V_{th} \qquad (2)$$

where V_{th} is the threshold voltage of the liquid crystal material used.

Caution, as V_{OP} increases with lower temperatures, care must be taken not to set a V_{OP} that will exceed the maximum of 8.5 V when operating at −25 °C.



a = 3.06.
b = 0.06.
V_{OP6} to V_{OP0} (programmed) [00 to 7FH].

Fig.14 V_{OP} programming.

9 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); see notes 1 and 2.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage	note 3	−0.5	+7	V
V_{LCD}	supply voltage LCD	note 4	−0.5	+10	V
V_I	all input voltages		−0.5	V_{DD} + 0.5	V
I_{SS}	ground supply current		−50	+50	mA
I_I, I_O	DC input or output current		−10	+10	mA
P_{tot}	total power dissipation		−	300	mW
P_O	power dissipation per output		−	30	mW
T_{amb}	operating ambient temperature		−25	+70	°C
T_j	operating junction temperature		−65	+150	°C
T_{stg}	storage temperature		−65	+150	°C

Notes

1. Stresses above those listed under limiting values may cause permanent damage to the device.
2. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.
3. With external LCD supply voltage externally supplied (voltage generator disabled). V_{DDmax} = 5 V if LCD supply voltage is internally generated (voltage generator enabled).
4. When setting V_{LCD} by software, take care not to set a V_{OP} that will exceed the maximum of 8.5 V when operating at −25 °C, see Caution in Section 8.9.

10 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see *"Handling MOS devices"*).

11 DC CHARACTERISTICS

V_{DD} = 2.7 to 3.3 V; V_{SS} = 0 V; V_{LCD} = 6.0 to 9.0 V; T_{amb} = −25 to +70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD1}	supply voltage 1	LCD voltage externally supplied (voltage generator disabled)	2.7	–	3.3	V
V_{DD2}	supply voltage 2	LCD voltage internally generated (voltage generator enabled)	2.7	–	3.3	V
V_{LCD1}	LCD supply voltage	LCD voltage externally supplied (voltage generator disabled)	6.0	–	9.0	V
V_{LCD2}	LCD supply voltage	LCD voltage internally generated (voltage generator enabled); note 1	6.0	–	8.5	V
I_{DD1}	supply current 1 (normal mode) for internal V_{LCD}	V_{DD} = 2.85 V; V_{LCD} = 7.0 V; f_{SCLK} = 0; T_{amb} = 25 °C; display load = 10 µA; note 2	–	240	300	µA
I_{DD2}	supply current 2 (normal mode) for internal V_{LCD}	V_{DD} = 2.70 V; V_{LCD} = 7.0 V; f_{SCLK} = 0; T_{amb} = 25 °C; display load = 10 µA; note 2	–	–	320	µA
I_{DD3}	supply current 3 (Power-down mode)	with internal or external LCD supply voltage; note 3	–	1.5	–	µA
I_{DD4}	supply current external V_{LCD}	V_{DD} = 2.85 V; V_{LCD} = 9.0 V; f_{SCLK} = 0; notes 2 and 4	–	25	–	µA
I_{LCD}	supply current external V_{LCD}	V_{DD} = 2.7 V; V_{LCD} = 7.0 V; f_{SCLK} = 0; T = 25 °C; display load = 10 µA; notes 2 and 4	–	42	–	µA
Logic						
V_{IL}	LOW level input voltage		V_{SS}	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}	V
I_L	leakage current	$V_I = V_{DD}$ or V_{SS}	−1	–	+1	µA
Column and row outputs						
$R_{o(C)}$	column output resistance C0 to C83		–	12	20	kΩ
$R_{o(R)}$	row output resistance R0 to R47		–	12	20	kΩ
$V_{bias(tol)}$	bias voltage tolerance on C0 to C83 and R0 to R47		−100	0	+100	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
LCD supply voltage generator						
V_{LCD}	V_{LCD} tolerance internally generated	V_{DD} = 2.85 V; V_{LCD} = 7.0 V; f_{SCLK} = 0; display load = 10 μA; note 5	–	0	300	mV
TC0	V_{LCD} temperature coefficient 0	V_{DD} = 2.85 V; V_{LCD} = 7.0 V; f_{SCLK} = 0; display load = 10 μA	–	1	–	mV/K
TC1	V_{LCD} temperature coefficient 1	V_{DD} = 2.85 V; V_{LCD} = 7.0 V; f_{SCLK} = 0; display load = 10 μA	–	9	–	mV/K
TC2	V_{LCD} temperature coefficient 2	V_{DD} = 2.85 V; V_{LCD} = 7.0 V; f_{SCLK} = 0; display load = 10 μA	–	17	–	mV/K
TC3	V_{LCD} temperature coefficient 3	V_{DD} = 2.85 V; V_{LCD} = 7.0 V; f_{SCLK} = 0; display load = 10 μA	–	24	–	mV/K

Notes

1. The maximum possible V_{LCD} voltage that may be generated is dependent on voltage, temperature and (display) load.
2. Internal clock.
3. RAM contents equal '0'. During power-down, all static currents are switched off.
4. If external V_{LCD}, the display load current is not transmitted to I_{DD}.
5. Tolerance depends on the temperature (typically zero at 27 °C, maximum tolerance values are measured at the temperate range limit).

12 AC CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{OSC}	oscillator frequency		20	34	65	kHz
$f_{clk(ext)}$	external clock frequency		10	32	100	kHz
f_{frame}	frame frequency	f_{OSC} or $f_{clk(ext)}$ = 32 kHz; note 1	–	67	–	Hz
t_{VHRL}	V_{DD} to $\overline{RES}$ LOW	Fig.16	0[2]	–	30	ms
$t_{WL(RES)}$	$\overline{RES}$ LOW pulse width	Fig.16	100	–	–	ns
Serial bus timing characteristics						
f_{SCLK}	clock frequency	V_{DD} = 3.0 V ±10%	0	–	4.00	MHz
T_{cy}	clock cycle SCLK	All signal timing is based on 20% to 80% of V_{DD} and maximum rise and fall times of 10 ns	250	–	–	ns
t_{WH1}	SCLK pulse width HIGH		100	–	–	ns
t_{WL1}	SCLK pulse width LOW		100	–	–	ns
t_{su2}	$\overline{SCE}$ set-up time		60	–	–	ns
t_{h2}	$\overline{SCE}$ hold time		100	–	–	ns
t_{WH2}	$\overline{SCE}$ min. HIGH time		100	–	–	ns
t_{h5}	$\overline{SCE}$ start hold time; note 3		100	–	–	ns
t_{su3}	D/$\overline{C}$ set-up time		100	–	–	ns
t_{h3}	D/$\overline{C}$ hold time		100	–	–	ns
t_{su4}	SDIN set-up time		100	–	–	ns
t_{h4}	SDIN hold time		100	–	–	ns

Notes

1. $T_{frame} = \frac{f_{clk(ext)}}{480}$
2. $\overline{RES}$ may be LOW before V_{DD} goes HIGH.
3. t_{h5} is the time from the previous SCLK positive edge (irrespective of the state of $\overline{SCE}$) to the negative edge of $\overline{SCE}$ (see Fig.15).

12.1 Serial interface

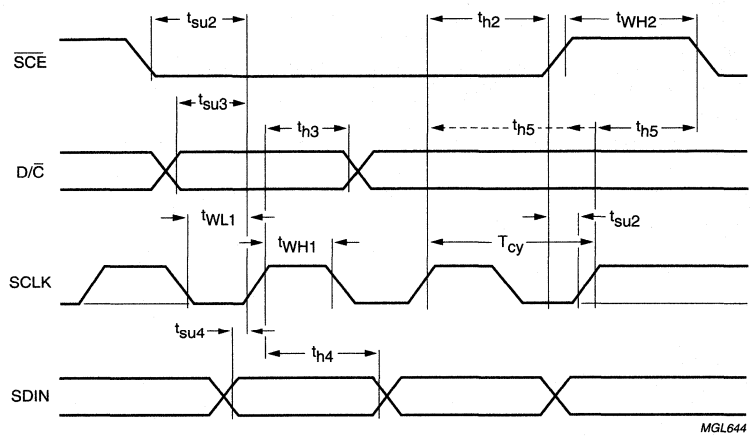


Fig.15 Serial interface timing.

12.2 Reset

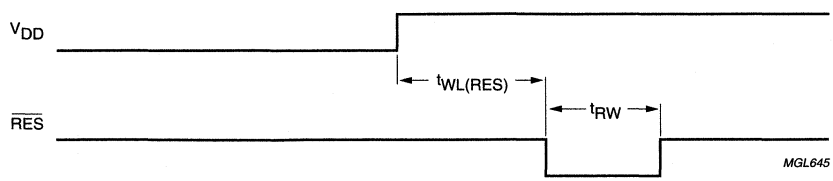
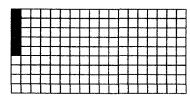
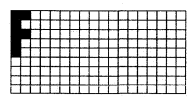
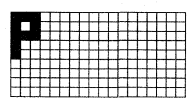
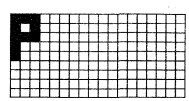
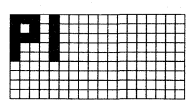
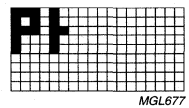
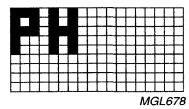
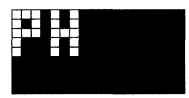
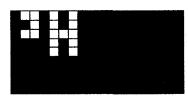


Fig.16 Reset timing.

13 APPLICATION INFORMATION

Table 6 Programming example

STEP	SERIAL BUS BYTE									DISPLAY	OPERATION
	D/$\overline{C}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
1	start										$\overline{SCE}$ is going LOW
2	0	0	0	1	0	0	0	0	1		function set PD = 0 and V = 0, select extended instruction set (H = 1 mode)
3	0	1	0	0	1	0	0	0	0		set V_{OP}; V_{OP} is set to a +16 × b [V]
4	0	0	0	1	0	0	0	0	0		function set PD = 0 and V = 0, select normal instruction set (H = 0 mode)
5	0	0	0	0	0	1	1	0	0		display control set normal mode (D = 1 and E = 0)
6	1	0	0	0	1	1	1	1	1	 MGL673	data write Y and X are initialized to 0 by default, so they are not set here
7	1	0	0	0	0	0	1	0	1	 MGL674	data write
8	1	0	0	0	0	0	1	1	1	 MGL675	data write
9	1	0	0	0	0	0	0	0	0	 MGL675	data write
10	1	0	0	0	1	1	1	1	1	 MGL676	data write

STEP	SERIAL BUS BYTE									DISPLAY	OPERATION
	D/$\overline{C}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
11	1	0	0	0	0	0	1	0	0	 MGL677	data write
12	1	0	0	0	1	1	1	1	1	 MGL678	data write
13	0	0	0	0	0	1	1	0	1	 MGL679	display control; set inverse video mode (D = 1 and E = 1)
14	0	1	0	0	0	0	0	0	0	 MGL679	set X address of RAM; set address to '0000000'
15	1	0	0	0	0	0	0	0	0	 MGL680	data write

The pinning is optimized for single plane wiring e.g. for chip-on-glass display modules. Display size: 48 × 84 pixels.

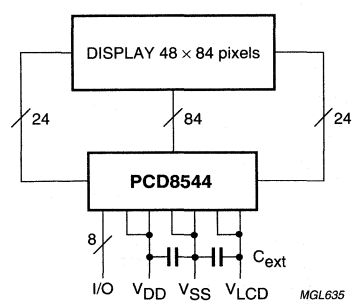


Fig.17 Application diagram.

The required minimum value for the external capacitors is: C_{ext} = 1.0 µF.

Higher capacitor values are recommended for ripple reduction.

14 BONDING PAD LOCATIONS

14.1 Bonding pad information (see Fig.18)

PARAMETER	SIZE
Pad pitch	min. 100 µm
Pad size, aluminium	80 × 100 µm
Bump dimensions	59 × 89 × 17.5 (±5) µm
Wafer thickness	max. 380 µm

14.2 Bonding pad location

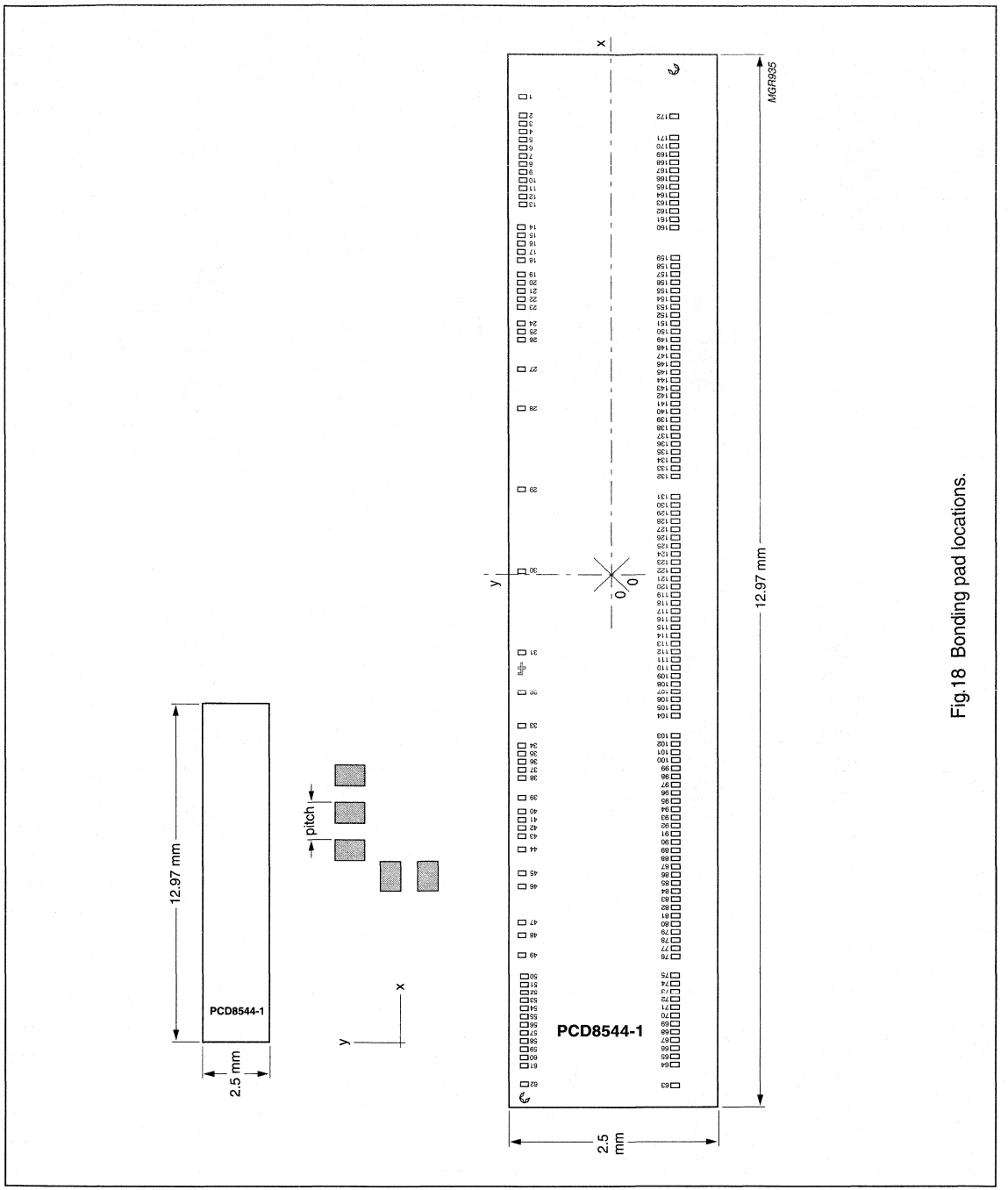


Fig.18 Bonding pad locations.

Table 7 Bonding pad locations (dimensions in μm). All X/Y coordinates are referenced to the centre of chip (see Fig.18)

PAD	PAD NAME	x	y
1	dummy1	+5932	+1060
2	R36	+5704	+1060
3	R37	+5604	+1060
4	R38	+5504	+1060
5	R39	+5404	+1060
6	R40	+5304	+1060
7	R41	+5204	+1060
8	R42	+5104	+1060
9	R43	+5004	+1060
10	R44	+4904	+1060
11	R45	+4804	+1060
12	R46	+4704	+1060
13	R47	+4604	+1060
14	V_{DD1}	+4330	+1085
15	V_{DD1}	+4230	+1085
16	V_{DD1}	+4130	+1085
17	V_{DD1}	+4030	+1085
18	V_{DD1}	+3930	+1085
19	V_{DD2}	+3750	+1085
20	V_{DD2}	+3650	+1085
21	V_{DD2}	+3550	+1085
22	V_{DD2}	+3450	+1085
23	V_{DD2}	+3350	+1085
24	V_{DD2}	+3250	+1085
25	V_{DD2}	+3150	+1085
26	V_{DD2}	+3050	+1085
27	SCLK	+2590	+1085
28	SDIN	+2090	+1085
29	D/$\overline{C}$	+1090	+1085
30	$\overline{SCE}$	+90	+1085
31	$\overline{RES}$	−910	+1085
32	OSC	−1410	+1085
33	T3	−1826	+1085
34	V_{SS2}	−2068	+1085
35	V_{SS2}	−2168	+1085
36	V_{SS2}	−2268	+1085
37	V_{SS2}	−2368	+1085
38	V_{SS2}	−2468	+1085
39	T4	−2709	+1085
40	V_{SS1}	−2876	+1085
41	V_{SS1}	−2976	+1085
42	V_{SS1}	−3076	+1085
43	V_{SS1}	−3176	+1085
44	T1	−3337	+1085
45	V_{LCD2}	−3629	+1085
46	V_{LCD2}	−3789	+1085
47	V_{LCD1}	−4231	+1085
48	V_{LCD1}	−4391	+1085
49	T2	−4633	+1085
50	R23	−4894	+1060
51	R22	−4994	+1060
52	R21	−5094	+1060
53	R20	−5194	+1060
54	R19	−5294	+1060
55	R18	−5394	+1060
56	R17	−5494	+1060
57	R16	−5594	+1060
58	R15	−5694	+1060
59	R14	−5794	+1060
60	R13	−5894	+1060
61	R12	−5994	+1060
62	dummy2	−6222	+1060
63	dummy3	−6238	−738
64	R0	−5979	−738
65	R1	−5879	−738
66	R2	−5779	−738
67	R3	−5679	−738
68	R4	−5579	−738
69	R5	−5479	−738
70	R6	−5379	−738
71	R7	−5279	−738
72	R8	−5179	−738
73	R9	−5079	−738
74	R10	−4979	−738
75	R11	−4879	−738
76	C0	−4646	−746

PAD	PAD NAME	x	y
77	C1	−4546	−746
78	C2	−4446	−746
79	C3	−4346	−746
80	C4	−4246	−746
81	C5	−4146	−746
82	C6	−4046	−746
83	C7	−3946	−746
84	C8	−3846	−746
85	C9	−3746	−746
86	C10	−3646	−746
87	C11	−3546	−746
88	C12	−3446	−746
89	C13	−3346	−746
90	C14	−3246	−746
91	C15	−3146	−746
92	C16	−3046	−746
93	C17	−2946	−746
94	C18	−2846	−746
95	C19	−2746	−746
96	C20	−2646	−746
97	C21	−2546	−746
98	C22	−2446	−746
99	C23	−2346	−746
100	C24	−2246	−746
101	C25	−2146	−746
102	C26	−2046	−746
103	C27	−1946	−746
104	C28	−1696	−746
105	C29	−1596	−746
106	C30	−1496	−746
107	C31	−1396	−746
108	C32	−1296	−746
109	C33	−1196	−746
110	C34	−1096	−746
111	C35	−996	−746
112	C36	−896	−746
113	C37	−796	−746
114	C38	−696	−746
115	C39	−596	−746
116	C40	−496	−746
117	C41	−396	−746

PAD	PAD NAME	x	y
118	C42	−296	−746
119	C43	−196	−746
120	C44	−96	−746
121	C45	+4	−746
122	C46	+104	−746
123	C47	+204	−746
124	C48	+304	−746
125	C49	+404	−746
126	C50	+504	−746
127	C51	+604	−746
128	C52	+704	−746
139	C53	+804	−746
130	C54	+904	−746
131	C55	+1004	−746
132	C56	+1254	−746
133	C57	+1354	−746
134	C58	+1454	−746
135	C59	+1554	−746
136	C60	+1654	−746
137	C61	+1754	−746
138	C62	+1854	−746
139	C63	+1954	−746
140	C64	+2054	−746
141	C65	+2154	−746
142	C66	+2254	−746
143	C67	+2354	−746
144	C68	+2454	−746
145	C69	+2554	−746
146	C70	+2654	−746
147	C71	+2754	−746
148	C72	+2854	−746
149	C73	+2954	−746
150	C74	+3054	−746
151	C75	+3154	−746
152	C76	+3254	−746
153	C77	+3354	−746
154	C78	+3454	−746
155	C79	+3554	−746
156	C80	+3654	−746
157	C81	+3754	−746
158	C82	+3854	−746

PAD	PAD NAME	x	y
159	C83	+3954	−746
160	R35	+4328	−738
161	R34	+4428	−738
162	R33	+4528	−738
163	R32	+4628	−738
164	R31	+4728	−738
165	R30	+4828	−738
166	R29	+4928	−738
167	R28	+5028	−738
168	R27	+5128	−738
169	R26	+5228	−738
170	R25	+5328	−738
171	R24	+5428	−738
172	dummy4	+5694	−738

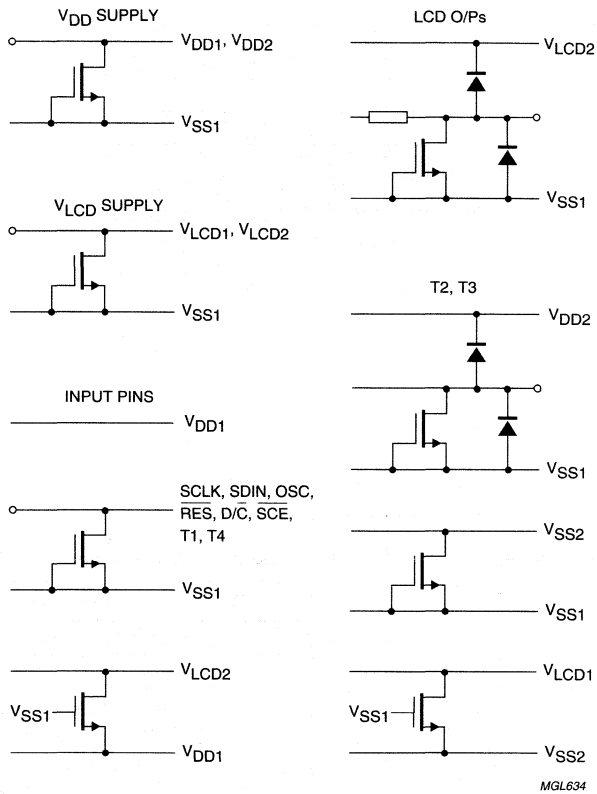
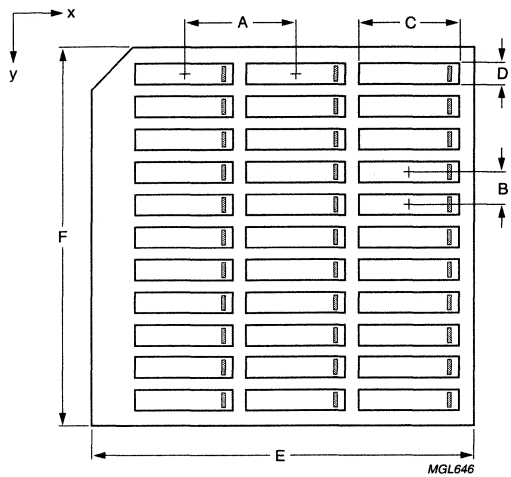


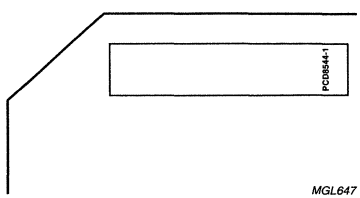
Fig.19 Device protection diagram.

15 TRAY INFORMATION



For the dimensions of x, y and A to F, see Table 8.

Fig.20 Tray details.



The orientation of the IC in a pocket is indicated by the position of the IC type name on the die surface with respect to the chamfer on the upper left corner of the tray. Refer to the bonding pad location diagram for the orientation and position of the type name on the die surface.

Fig.21 Tray alignment.

Table 8 Dimensions

DIM.	DESCRIPTION	VALUE
A	pocket pitch, in the x direction	14.82 mm
B	pocket pitch, in the y direction	4.39 mm
C	pocket width, in the x direction	13.27 mm
D	pocket width, in the y direction	2.8 mm
E	tray width, in the x direction	50.67 mm
F	tray width, in the y direction	50.67 mm
x	no. of pockets in the x direction	3
y	no. of pockets in the y direction	11

CONTENTS

1 FEATURES

- Single-chip LCD controller/driver
- 2-line display of up to 12 characters + 120 icons, or 1-line display of up to 24 characters + 120 icons
- 5 × 7 character format plus cursor; 5 × 8 for kana (Japanese syllabary) and user defined symbols
- Icon mode: reduced current consumption while displaying icons only(1)
- Icon blink function
- On-chip:
  - Generation of intermediate LCD bias voltages
  - Oscillator requires no external components (external clock also possible)
- Display data RAM: 80 characters
- Character generator ROM: 240, 5 × 8 characters
- Character generator RAM: 16, 5 × 8 characters; 3 characters used to drive 120 icons, 6 characters used if icon blink feature is used in application
- 4 or 8-bit parallel bus and 2-wire I²C-bus interface
- CMOS compatible
- 18 row, 60 column outputs
- Mux rates 1 : 18 (for normal operation) and 1 : 2 (for icon-only mode)
- Uses common 11 code instruction set (extended)
- Logic supply voltage range, $V_{DD} - V_{SS}$ = 1.8 to 5.5 V; chip may be driven with two battery cells
- Display supply voltage range, $V_{LCD} - V_{SS}$ = 2.2 to 6.5 V
- Very low current consumption (20 to 120 μA):
  - Icon mode: <25 μA
  - Power-down mode: <2.5 μA.

(1) Icon mode is used to save current. When only icons are displayed, a much lower operating voltage V_{LCD} can be used and the switching frequency of the LCD outputs is reduced. In most applications it is possible to use V_{DD} as V_{LCD}.

2 APPLICATIONS

- Telecom equipment
- Portable instruments
- Point-of-sale terminals.

3 GENERAL DESCRIPTION

The PCF2103 family is a low power CMOS LCD controller and driver, designed to drive a dot matrix LCD display of 2 line by 12 or 1 line by 24 characters with 5 × 8 dot format. All necessary functions for the display are provided in a single chip, including on-chip generation of LCD bias voltages, resulting in a minimum of external components and lower system current consumption. The PCF2103 interfaces to most microcontrollers via a 4 or 8-bit bus or via the 2-wire I²C-bus. The chip contains a character generator and displays alphanumeric and kana (Japanese) characters. The letter 'X' in PCF2103X characterizes the built-in character set. Various character sets can be manufactured on request.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF2103EU/2/F2	–	chip with bumps in tray	–

5 BLOCK DIAGRAM

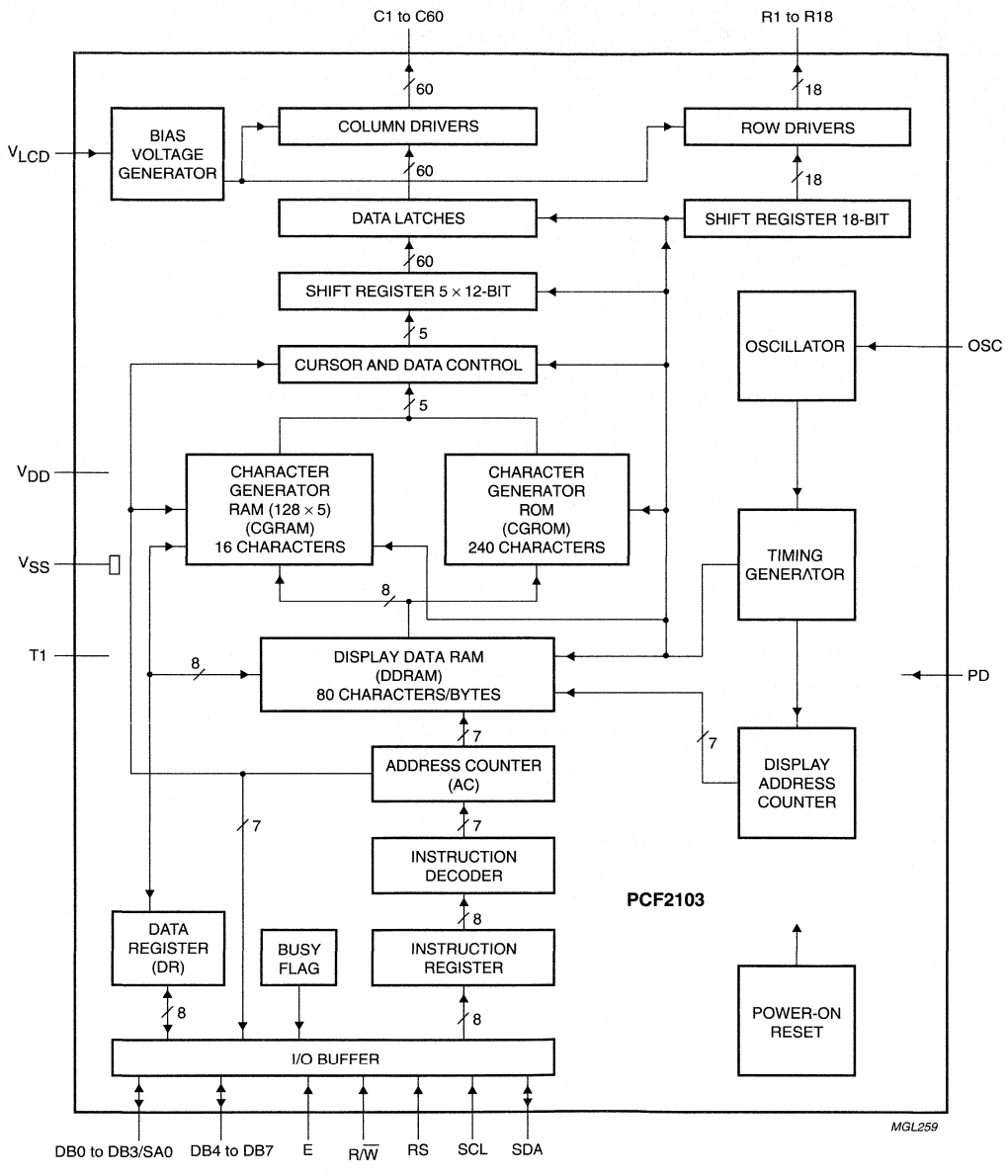


Fig.1 Block diagram.

6 PINNING

SYMBOL	DIE PAD	DESCRIPTION
V_{DD}	1	supply voltage
OSC	2	oscillator/external clock input
PD	3	power-down pad input
T1	4	test pad (connected to V_{SS})
V_{SS}	5	ground
V_{LCD}	6	V_{LCD} input; note 1
R9 to R16	7 to 14	LCD row driver outputs 9 to 16
R18	15	LCD row driver output 18
C60 to C1	16 to 23, 26 to 50, 53 to 77, 80, 81	LCD column driver outputs 60 to 1
R8 to R1	82 to 89	LCD row driver outputs 8 to 1
R17	90	LCD row driver output 17
SCL	91	I^2C-bus serial clock input
SDA	92	I^2C-bus serial data input/output
E	93	data bus clock input
RS	94	register select input
R/$\overline{W}$	95	read/write input
DB7	96	bit of bi-directional data bus
DB6	97	bit of bi-directional data bus
DB5	98	bit of bi-directional data bus
DB4	99	bit of bi-directional data bus
DB3/SA0	100	bit of bi-directional data bus/I^2C-bus address pin
DB2	101	bit of bi-directional data bus
DB1	102	bit of bi-directional data bus
DB0	103	bit of bi-directional data bus

Note

1. This is the voltage used for the generation of LCD bias levels.

Table 1 Pin functions; note 1

NAME	FUNCTION	DESCRIPTION
RS	register select	RS selects the register to be accessed for read and write; there is an internal pull-up on this pin RS = 0 selects the instruction register for write and the busy flag and address counter for read RS = 1 selects the data register for both read and write
R/$\overline{W}$	read/write	R/$\overline{W}$ selects either the read (R/$\overline{W}$ = 1) or write (R/$\overline{W}$ = 0) operation; there is an internal pull-up on this pin
E	data bus clock	pin E is set HIGH to signal the start of a read or write operation; data is clocked in or out of the chip on the negative edge of the clock
DB7 to DB0	data bus	the bi-directional, 3-state data bus transfers data between the system controller and the PCF2103; DB7 may be used as the busy flag, signalling that internal operations are not yet completed; in 4-bit operations the 4 higher order lines DB7 to DB4 are used; DB3 to DB0 must be left open-circuit; there is an internal pull-up on each of the data lines
C1 to C60	column driver outputs	these pins output the data for columns
R1 to R18	row driver outputs	these pins output the row select waveforms to the display; R17 and R18 drive the icons
V_{LCD}	LCD power supply	positive power supply for the liquid crystal display
OSC	oscillator	when the on-chip oscillator is used this pin must be connected to V_{DD}; an external clock signal, if used, is input at this pin
SCL	serial clock line	input for the I^2C-bus clock signal
SDA	serial data line	I/O for the I^2C-bus data line
SA0	address pin	the hardware sub-address line is used to program the device sub-address for two different PCF2103s on the same I^2C-bus
T1	test pad	must be connected to V_{SS}; not user accessible
PD	power-down pad	PD selects chip power-down mode; for normal operation PD = 0

Note

1. When the I^2C-bus is used, the parallel interface pin E must be defined as E = 0. In I^2C-bus read mode DB7 to DB0 should be connected to V_{DD} or left open-circuit.
   a) When the parallel bus is used, pins SCL and SDA must be connected to V_{SS} or V_{DD}; they may not be left unconnected.
   b) If the 4-bit interface is used without reading out from the PCF2103 (i.e. R/$\overline{W}$ is set permanently to logic 0), the unused ports DB0 to DB3 can either be set to V_{SS} or V_{DD} instead of leaving them open.

7 FUNCTIONAL DESCRIPTION

7.1 LCD bias voltage generator

The intermediate bias voltages for the LCD display are generated on-chip. This removes the need for an external resistive bias chain and significantly reduces the system current consumption. The optimum value of V_{LCD} depends on the multiplex rate, the LCD threshold voltage (V_{th}) and the number of bias levels and is given by the relationships given in Tables 2 and 3. Using a 5-level bias scheme for 1 : 18 maximum rate allows V_{LCD} <5 V for most LCD liquids.

Table 2 Optimum/maximum values for V_{OP} (off pixels start darkening; $V_{off} = V_{th}$)

MUX RATE	NUMBER OF LEVELS	V_{on}/V_{th}	V_{OP}/V_{th}	V_{OP} (typical; for V_{th} = 1.4 V)
1 : 18	5	1.272	3.7	5.2 V
1 : 2	3	2.236	2.283	3.9 V

Table 3 Minimum values for V_{OP} (on pixels clearly visible; $V_{on} > V_{th}$)

MUX RATE	NUMBER OF LEVELS	V_{on}/V_{th}	V_{OP}/V_{th}	V_{OP} (typical; for V_{th} = 1.4 V)
1 : 18	5	1.12	3.2	4.6 V
1 : 2	3	1.2	1.5	2.1 V

7.2 Oscillator

The on-chip oscillator provides the clock signal for the display system. No external components are required and pin OSC must be connected to V_{DD}.

7.3 External clock

If an external clock is to be used, it is input at the OSC pin. The resulting display frame frequency is given by

$$f_{frame} = \frac{f_{osc}}{3072}$$

Only in the power-down state is the clock allowed to be stopped (OSC connected to V_{SS}), otherwise the LCD is frozen in a DC state.

7.4 Power-on reset

The on-chip power-on reset block initializes the chip after power-on or power failure. This is a synchronous reset and requires 3 oscillator cycles to be executed. Afterwards, a clear display is initiated.

7.5 Power-down mode

The chip can be put into power-down mode where all static currents are switched off (no internal oscillator, no bias level generation, all LCD outputs are internally connected to V_{SS}) when PD = 1.

During power-down, the whole chip is being reset and will restart with a clear display after power-down. Therefore, the whole chip has to be initialized after a power-down as after an initial power-up.

7.6 Registers

The PCF2103 has two 8-bit registers, an Instruction Register (IR) and a Data Register (DR). The Register Select signal (RS) determines which register will be accessed. The instruction register stores instruction codes such as 'display clear' and 'cursor shift', and address information for the Display Data RAM (DDRAM) and Character Generator RAM (CGRAM). The instruction register can be written from but not read by the system controller. The data register temporarily stores data to be read from the DDRAM and CGRAM. When reading, data from the DDRAM or CGRAM corresponding to the address in the instruction register is written to the data register prior to being read by the 'read data' instruction.

7.7 Busy flag

The busy flag indicates the internal status of the PCF2103. Logic 1 indicates that the chip is busy and further instructions will not be accepted. The busy flag is output at pin DB7 when RS = 0 and R/$\overline{W}$ = 1. Instructions should only be written after checking that the busy flag is logic 0 or waiting for the required number of cycles.

7.8 Address Counter (AC)

The address counter assigns addresses to the DDRAM and CGRAM for reading and writing and is set by the commands 'set CGRAM address' and 'set DDRAM address'. After a read/write operation the address counter is automatically incremented or decremented by 1. The address counter contents are output to the bus (DB6 to DB0) when RS = 0 and R/$\overline{W}$ = 1.

7.9 Display Data RAM (DDRAM)

The DDRAM stores up to 80 characters of display data represented by 8-bit character codes. RAM locations which are not used for storing display data can be used as general purpose RAM. The basic RAM-to-display addressing scheme is shown in Fig.2. With no display shift the characters represented by the codes in the first 24 RAM locations starting at address 00 in line 1 are displayed. Figures 3 and 4 show the display mapping for right and left shift respectively.

When data is written to or read from the DDRAM wrap-around occurs from the end of one line to the start of the next line. When the display is shifted each line wraps around within itself, independently of the others. Thus all lines are shifted and wrapped around together. The address ranges and wrap-around operations for the various modes are shown in Table 4.

7.10 Character Generator ROM (CGROM)

The Character Generator ROM (CGROM) generates 240 character patterns in 5 × 8 dot format from 8-bit character codes. Figure 6 shows the character set that is currently implemented.

7.11 Character Generator RAM (CGRAM)

Up to 16 user defined characters may be stored in the CGRAM. Some CGRAM characters (see Fig.14) are also used to drive icons (6 if icons blink and both icon rows are used in application; 3 if no blink but both icon rows are used in application; 0 if no icons are driven by the icon rows). The CGROM and CGRAM use a common address space, of which the first column is reserved for the CGRAM (see Fig.6). Figure 7 shows the addressing principle for the CGRAM.

7.12 Cursor control circuit

The cursor control circuit generates the cursor (underline and/or cursor blink as shown in Fig.5) at the DDRAM address contained in the address counter. When the address counter contains the CGRAM address the cursor will be inhibited.

7.13 Timing generator

The timing generator produces the various signals required to drive the internal circuitry. Internal chip operation is not disturbed by operations on the data buses.

7.14 LCD row and column drivers

The PCF2103 contains 18 row and 60 column drivers, which connect the appropriate LCD bias voltages in sequence to the display in accordance with the data to be displayed. R17 and R18 drive the icon rows.

The bias voltages and the timing are selected automatically when the number of lines in the display is selected. Figures 8, 9 and 10 show typical waveforms. Unused outputs should be left unconnected.

Table 4 Address space and wrap-around operation

MODE	ADDRESS SPACE	READ/WRITE WRAP-AROUND[1]	DISPLAY SHIFT WRAP-AROUND[2]
1 × 24	00H to 4FH	4FH to 00H	4FH to 00H
2 × 12	00H to 27H; 40H to 67H	27H to 40H; 67H to 00H	27H to 00H; 67H to 40H

Notes

1. Moves to next line.
2. Stays within line.

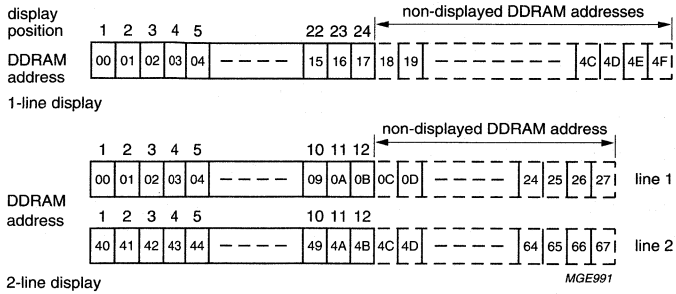


Fig.2 DDRAM-to-display mapping: no shift.

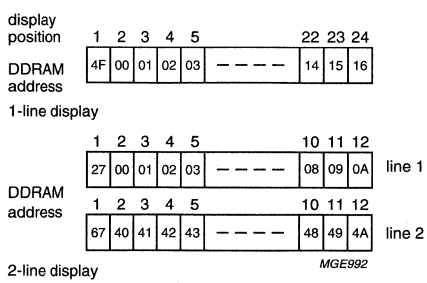


Fig.3 DDRAM-to-display mapping: right shift.

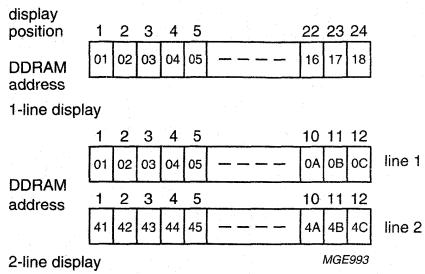


Fig.4 DDRAM-to-display mapping: left shift.

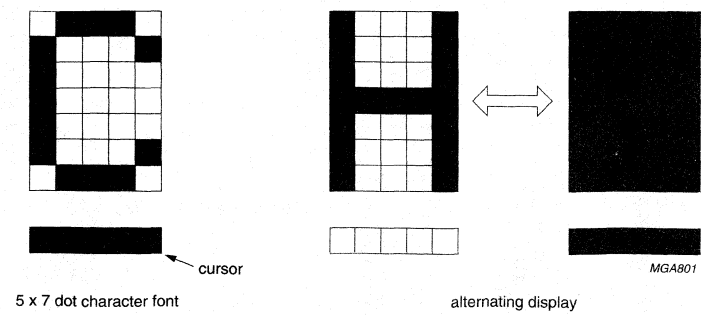
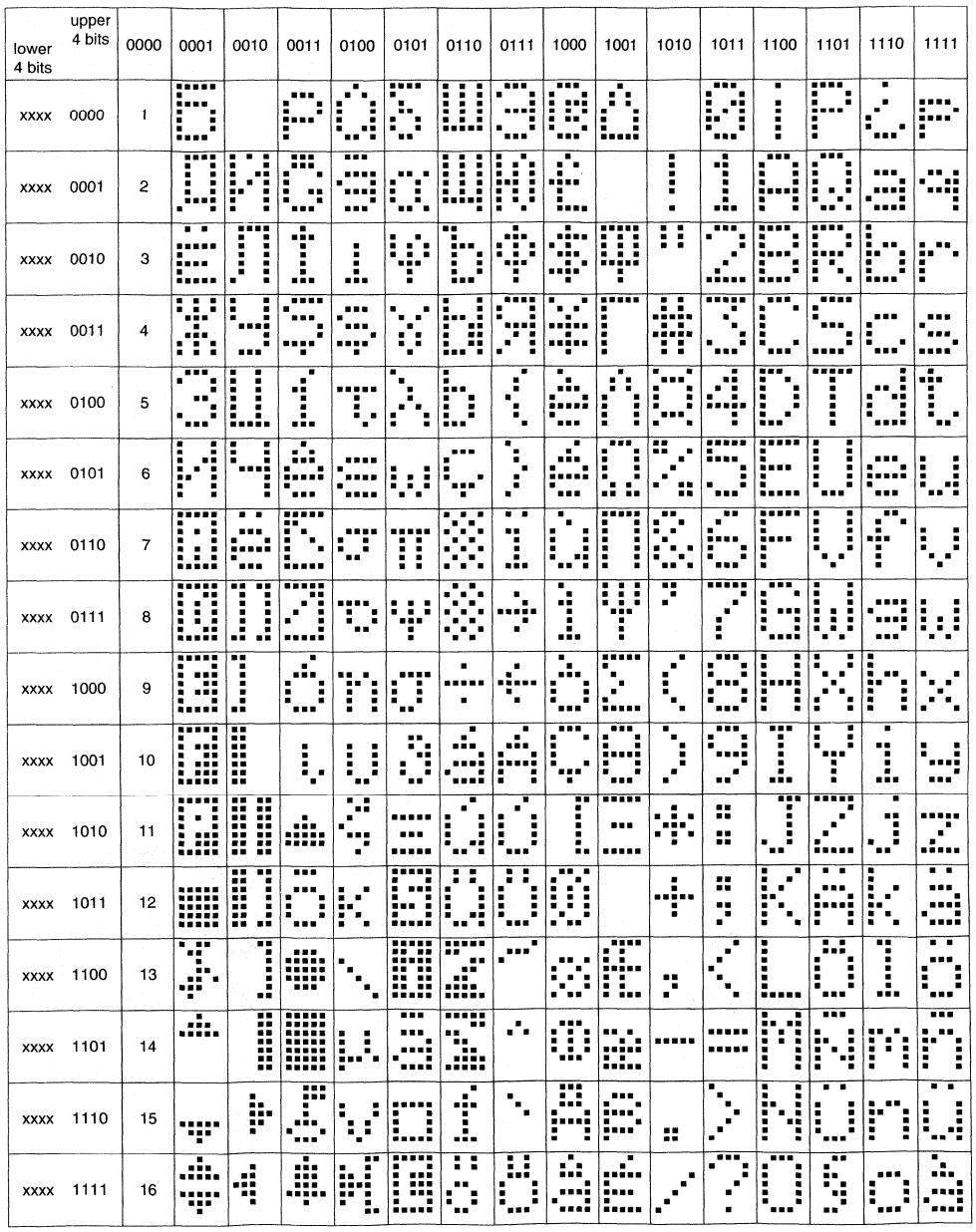


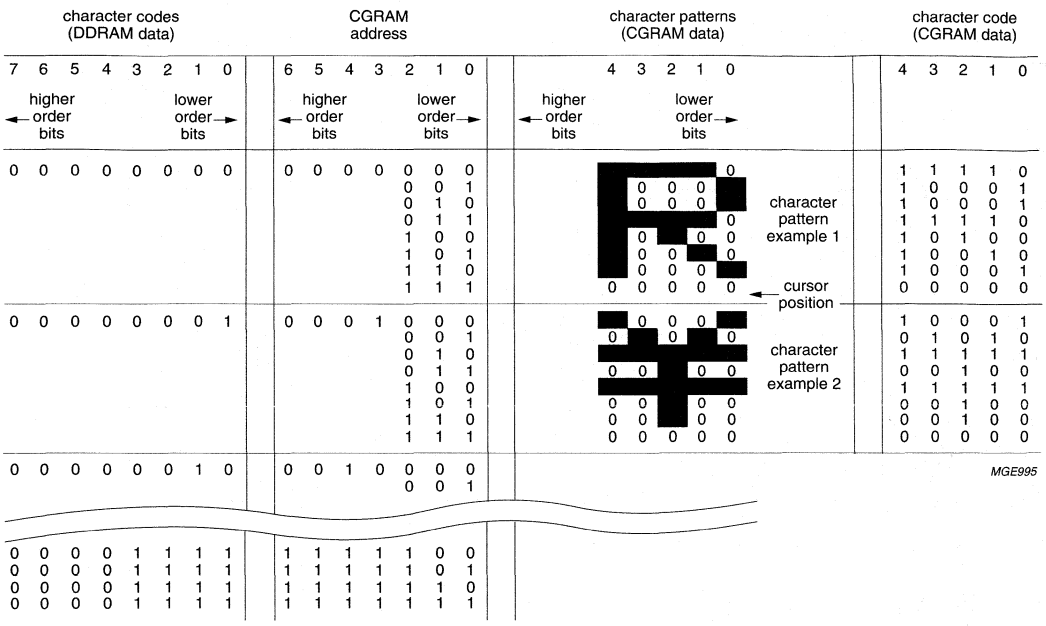
Fig.5 Cursor and blink display examples.

lower 4 bits	upper 4 bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
xxxx	0000	1															
xxxx	0001	2															
xxxx	0010	3															
xxxx	0011	4															
xxxx	0100	5															
xxxx	0101	6															
xxxx	0110	7															
xxxx	0111	8															
xxxx	1000	9															
xxxx	1001	10															
xxxx	1010	11															
xxxx	1011	12															
xxxx	1100	13															
xxxx	1101	14															
xxxx	1110	15															
xxxx	1111	16															



MGD689

Fig.6 Character set 'E' in CGROM.



Character code bits 0 to 3 correspond to CGRAM address bits 3 to 6.

CGRAM address bits 0 to 2 designate the character pattern line position. The 8th line is the cursor position and display is performed by logical OR with the cursor. Data in the 8th position will appear in the cursor position.

Character pattern column positions correspond to CGRAM data bits 0 to 4, as shown in Fig.6.

As shown in Figs 6 and 7, CGRAM character patterns are selected when character code bits 4 to 7 are all logic 0. CGRAM data = logic 1 corresponds to selection for display.

Only bits 0 to 5 of the CGRAM address are set by the 'set CGRAM address' command. Bit 6 can be set using the 'set DDRAM address' command in the valid address range or by using the auto-increment feature during CGRAM write. All bits 0 to 6 can be read using the 'read busy flag and address counter' command; see Table 7.

Fig.7 Relationship between CGRAM addresses and data and display patterns.

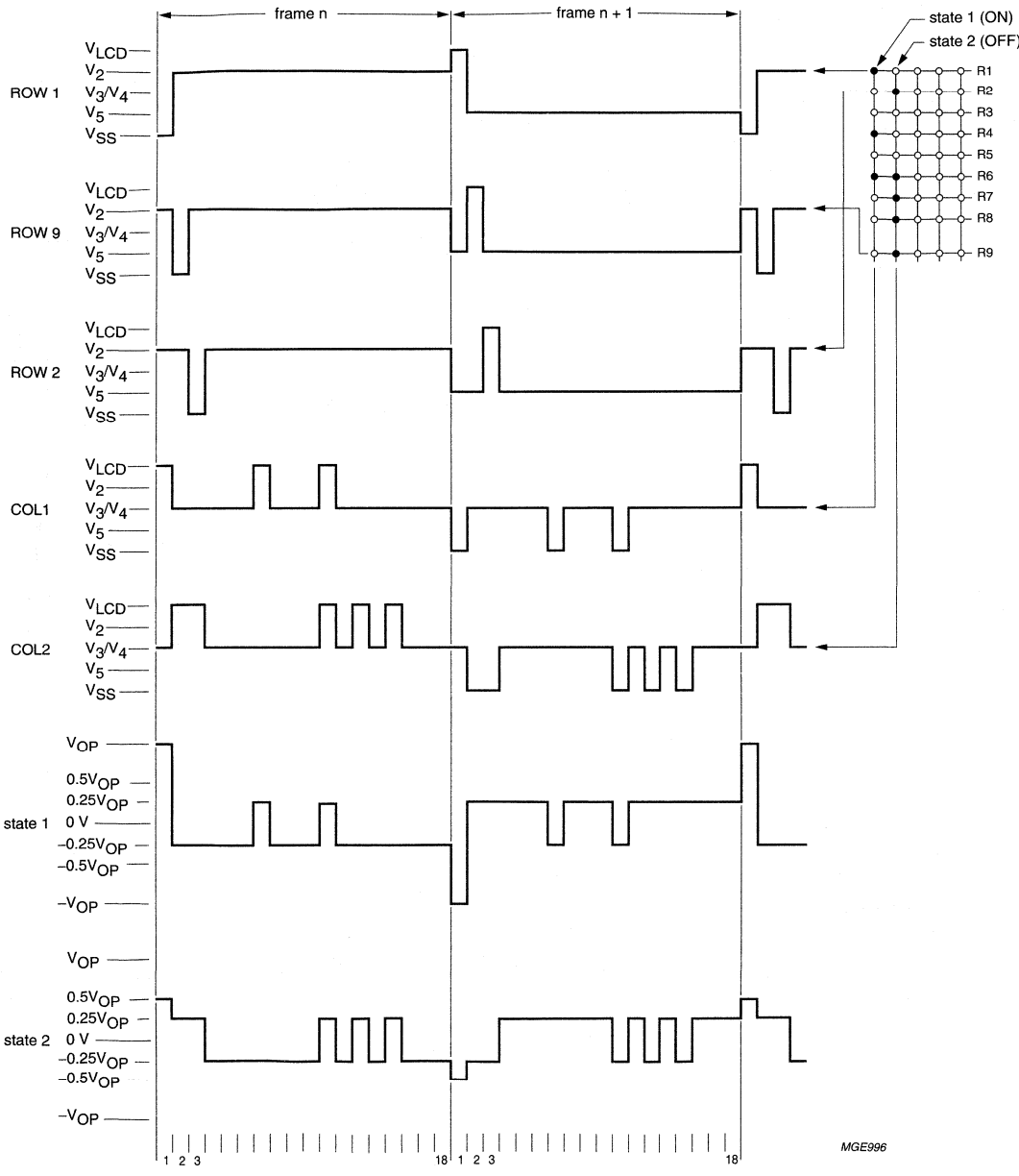


Fig.8 Typical LCD waveforms; character mode.

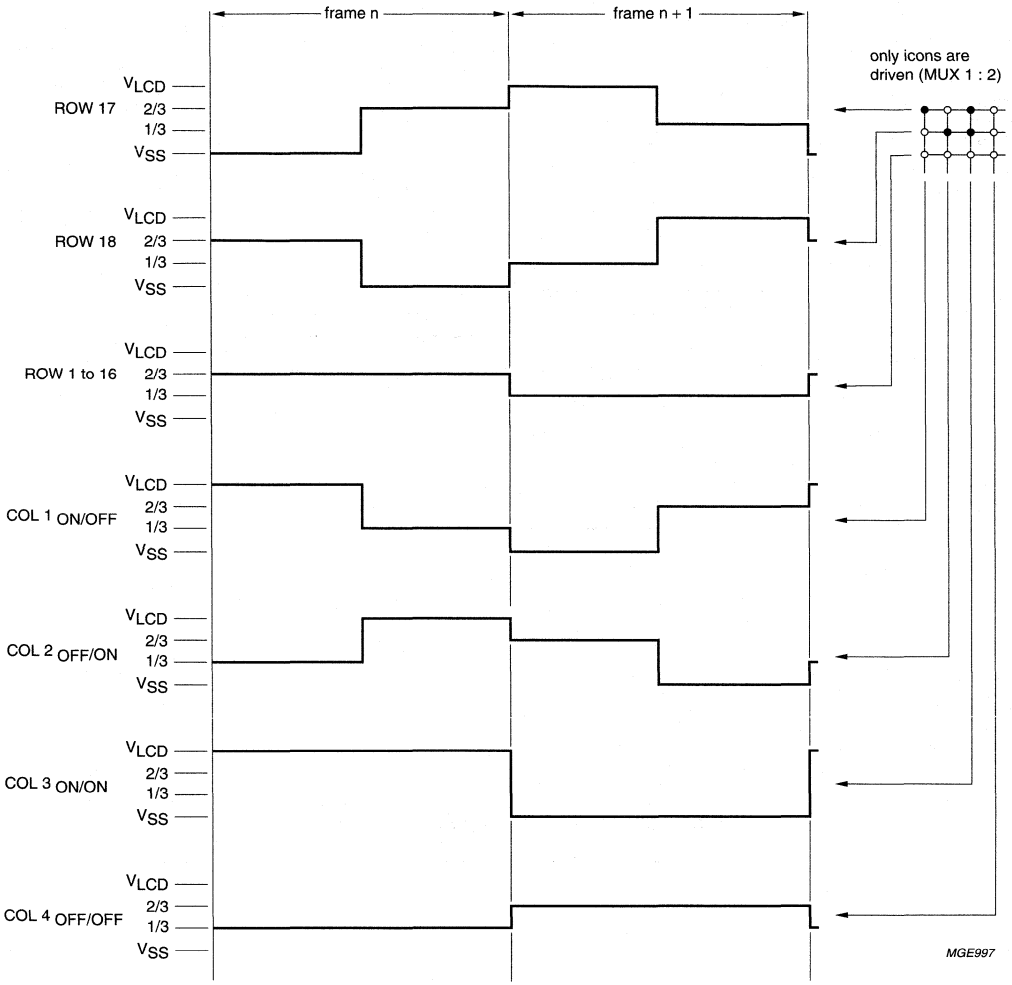
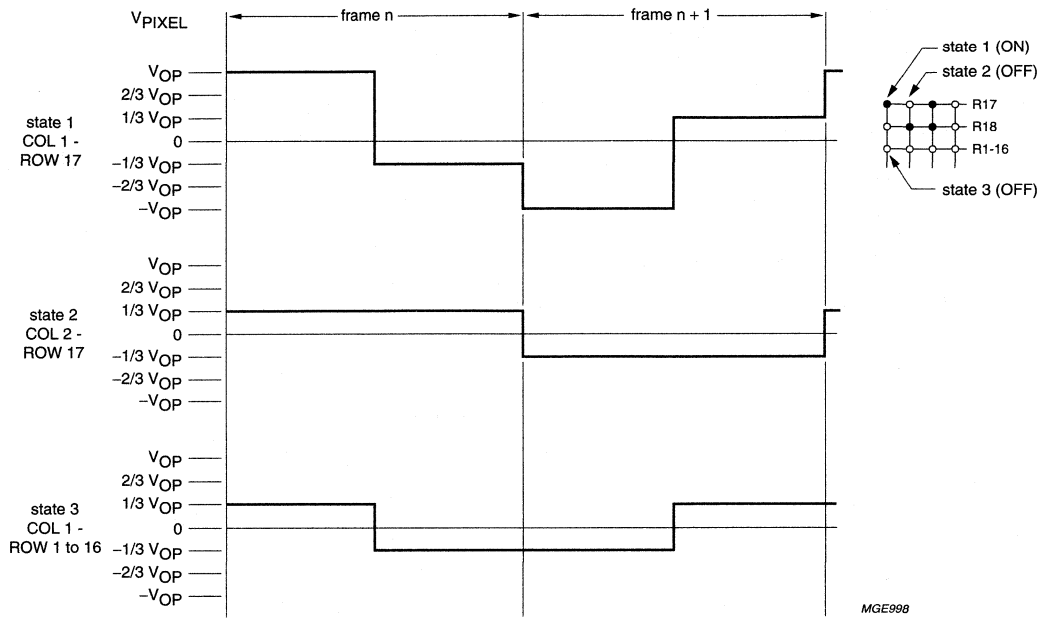


Fig.9 Mux 1 : 2 LCD waveforms; icon mode.



$V_{ON(rms)} = 0.745\ V_{OP}$.

$V_{OFF(rms)} = 0.333\ V_{OP}$.

$$D = \frac{V_{ON}}{V_{OFF}} = 2.23$$

Fig.10 Mux 1 : 2 LCD waveforms; icon mode.

7.15 Reset function

The PCF2103 automatically initializes (resets) when power is turned on. The reset executes a 'clear display' instruction, requiring 165 oscillator cycles. After the reset the chip has the state shown in Table 5.

Table 5 State after reset

STEP	INSTRUCTION	RESET STATE (BIT/REGISTER)	RESET STATE (DESCRIPTION)
1	clear display		
2	entry mode set	I/D = 1	+1 (increment)
		S = 0	no shift
3	display control	D = 0	display off
		C = 0	cursor off
		B = 0	cursor character blink off
4	function set	DL = 1	8-bit interface
		M = 0	1-line display
		H = 0	normal instruction set
5	default address pointer to DDRAM; the Busy Flag (BF) indicates the busy state (BF = 1) until initialization ends; the busy state lasts 2 ms; the chip may also be initialized by software; see Tables 16 and 17		
6	icon control	IM, IB = 00	icons/icon blink disabled
7	display/screen configuration	L, P, Q = 000	default configurations
8	I^2C-bus interface reset		

8 INSTRUCTIONS

Only two PCF2103 registers, the Instruction Register (IR) and the Data Register (DR) can be directly controlled by the microcontroller. Before internal operation, control information is stored temporarily in these registers to allow interface to various types of microcontrollers which operate at different speeds or to allow interface to peripheral control ICs. The format for instructions when I²C-bus control is used is shown in Table 6. The PCF2103 operation is controlled by the instructions given in Table 7 together with their execution time. Details are explained in subsequent sections.

Instructions are of 4 types, those that:

1. Designate PCF2103 functions such as display format, data length, etc.
2. Set internal RAM addresses
3. Perform data transfer with internal RAM
4. Others.

In normal use, instructions that perform data transfer with internal RAM are used most frequently. However, automatic incrementing by 1 (or decrementing by 1) of internal RAM addresses after each data write lessens the microcontroller program load. The display shift in particular can be performed concurrently with display data write, enabling the designer to develop systems in minimum time with maximum programming efficiency.

During internal operation, no instruction other than the 'read busy flag and address counter' instruction will be executed. Because the busy flag is set to logic 1 while an instruction is being executed, the user should verify that the busy flag is at logic 0 before sending the next instruction or wait for the maximum instruction execution time, as given in Table 7. An instruction sent while the busy flag is logic 1 will not be executed.

Table 6 Instruction set for I²C-bus commands

CONTROL BYTE								COMMAND BYTE								I²C-BUS COMMANDS
Co	RS	0	0	0	0	0	0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	note 1

Note

1. R/$\overline{W}$ is set together with the slave address.

...ds commands; note 1

INSTRUCTION	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DESCRIPTION	REQUIRED CLOCK CYCLES
H = 0 or 1												
NOP	0	0	0	0	0	0	0	0	0	0	no operation	3
Function set	0	0	0	0	1	DL	0	M	0	H	sets interface Data Length (DL) and number of display lines (M); extended instruction set control (H)	3
Read busy flag and address counter	0	1	BF	AC							reads the Busy Flag (BF) indicating internal operating is being performed and reads address counter contents	0
Read data	1	1	read data								reads data from CGRAM or DDRAM	3
Write data	1	0	write data								writes data from CGRAM or DDRAM	3
H = 0												
Clear display	0	0	0	0	0	0	0	0	0	1	clears entire display and sets DDRAM address 0 in address counter	165
Return home	0	0	0	0	0	0	0	0	1	0	sets DDRAM address 0 in address counter; also returns shifted display to original position; DDRAM contents remain unchanged	3
Entry mode set	0	0	0	0	0	0	0	1	I/D	S	sets cursor move direction and specifies shift of display; these operations are performed during data write and read	3
Display control	0	0	0	0	0	0	1	D	C	B	sets entire display on/off (D), cursor on/off (C) and blink of cursor position character (B); D = 0 (display off) puts chip into power-down mode	3
Cursor/display shift	0	0	0	0	0	1	S/C	R/L	0	0	moves cursor and shifts display without changing DDRAM contents	3
Set CGRAM address	0	0	0	1	A_{CG}						sets CGRAM address; bit 6 is to be set by the command 'set DDRAM address'; look at the description of the commands	3
Set DDRAM address	0	0	1	A_{DD}							sets DDRAM address	3

INSTRUCTION	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DESCRIPTION	REQUIRED CLOCK CYCLES
H = 1												
Reserved	0	0	0	0	0	0	0	0	0	1	do not use	–
Screen configuration	0	0	0	0	0	0	0	0	1	L	set screen configuration	3
Display configuration	0	0	0	0	0	0	0	1	P	Q	set display configuration	3
Icon control	0	0	0	0	0	0	1	IM	IB	0	set icon mode (IM), icon blink (IB)	3
Reserved	0	0	0	0	0	1	X	X	X	X	do not use	–
Reserved	0	0	0	1	X	X	X	X	X	X	do not use	–
Reserved	0	0	1	X	X	X	X	X	X	X	do not use	–

Note

1. X = don't care.

Table 8 Specification of mnemonics used in Table 7

BIT	LOGIC 0	LOGIC 1
I/D	decrement	increment
S	display freeze	display shift
D	display off	display on
C	cursor off	cursor on
B	cursor character blink off: character at cursor position does not blink	cursor character blink on: character at cursor position blinks
S/C	cursor move	display shift
R/L	left shift	right shift
DL	4 bits	8 bits
H	use basic instruction set	use extended instruction set
L (ignored, if M = 1)	left/right screen: standard connection (as in PCF2114); 1st 12 characters of 24: columns are from 1 to 60; 2nd 12 characters of 24: columns are from 1 to 60	left/right screen: mirrored connection (as in PCF2116); 1st 12 characters of 24: columns are from 1 to 60; 2nd 12 characters of 24: columns are from 60 to 1
P	column data: left to right (as in PCF2116); column data is displayed from 1 to 60	column data: right to left; column data is displayed from 60 to 1
Q	row data: top to bottom (as in PCF2116); row data is displayed from 1 to 16 and icon row data is in 17 and 18	row data: bottom to top; row data is displayed from 16 to 1 and icon row data is in 18 and 17
IM	character mode; full display	icon mode; only icons displayed
IB	icon blink disabled	icon blink enabled
M	1-line by 24 display	2-line by 12 display
C_0	last control byte; see Table 6	another control byte follows after data/command

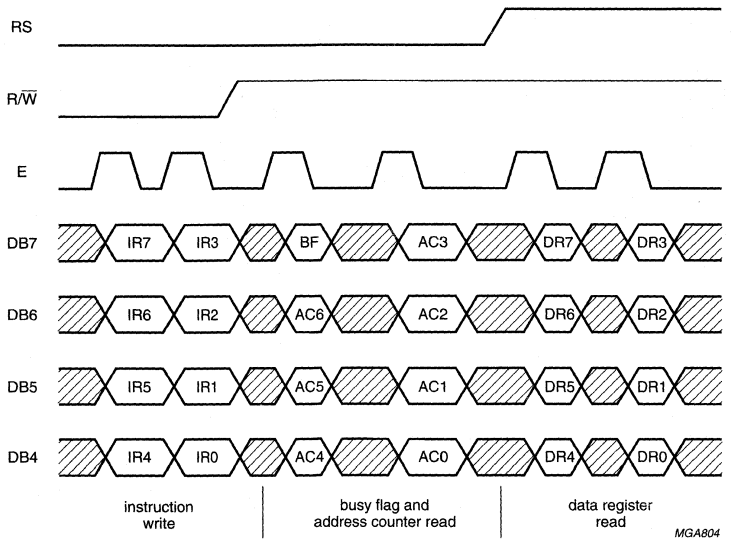
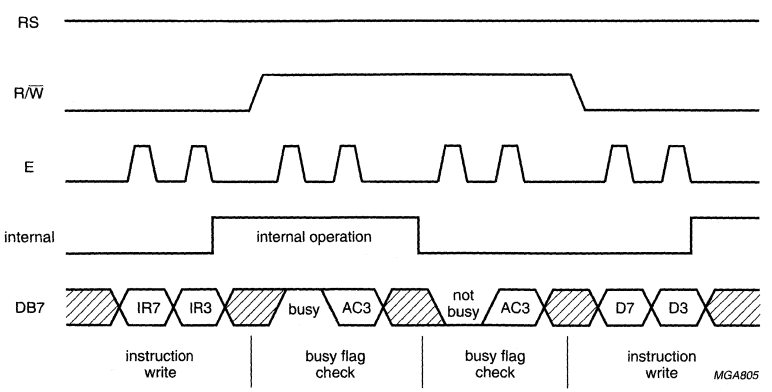


Fig.11 4-bit transfer example.



IR7 and IR3: instruction 7th and 3rd bit.
AC3: address counter 3rd bit.
D7 and D3: data 7th and 3rd bit.

Fig.12 An example of 4-bit data transfer timing sequence.

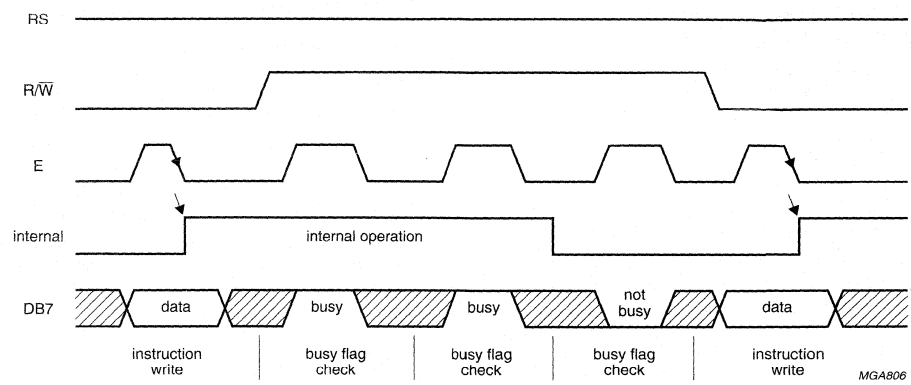


Fig.13 Example of busy flag checking timing sequence.

8.1 Clear display

'Clear display' writes character code 20H into all DDRAM addresses (the character pattern for character code 20H must be a blank pattern), sets the DDRAM address counter to logic 0 and returns display to its original position if it was shifted. Thus, the display disappears and the cursor or blink position goes to the left edge of the display. Sets entry mode I/D = 1 (increment mode). S of entry mode does not change.

The instruction 'clear display' requires extra execution time. This may be allowed by checking the Busy Flag (BF) or by waiting until the 165 clock cycles have elapsed. The latter must be applied where no read-back options are foreseen, as in some Chip-On-Glass (COG) applications.

8.2 Return home

'Return home' sets the DDRAM address counter to logic 0 and returns display to its original position if it was shifted. DDRAM contents do not change. The cursor or blink position goes to the left of the first display line. I/D and S of entry mode do not change.

8.3 Entry mode set

8.3.1 I/D

When I/D = 1 (0) the DDRAM or CGRAM address increments (decrements) by 1 when data is written into or read from the DDRAM or CGRAM. The cursor or blink position moves to the right when incremented and to the left when decremented. The cursor underline and cursor character blink are inhibited when the CGRAM is accessed.

8.3.2 S

When S = 1, the entire display shifts either to the right (I/D = 0) or to the left (I/D = 1) during a DDRAM write. Thus it looks as if the cursor stands still and the display moves. The display does not shift when reading from the DDRAM, or when writing into or reading out of the CGRAM. When S = 0 the display does not shift.

8.4 Display control (and partial power-down mode)

8.4.1 D

The display is on when D = 1 and off when D = 0. Display data in the DDRAM are not affected and can be displayed immediately by setting D to logic 1.

When the display is off (D = 0) the chip is in partial power-down mode:

- The LCD outputs are connected to V_{SS}
- Bias generator is turned off.

3 oscillator cycles are required after sending the 'display off' instruction to ensure all outputs are at V_{SS}, afterwards OSC can be stopped. If the oscillator is running during partial power-down mode ('display off') the chip can still execute instructions. Even lower current consumption is obtained by inhibiting the oscillator (OSC = V_{SS}).

To ensure $I_{DD} < 2\ \mu A$ the parallel bus pins DB7 to DB0 should be connected to V_{DD}; RS and R/$\overline{W}$ to V_{DD} or left open-circuit and PD to V_{DD}. Recovery from power-down mode: put PD back to logic 0, if necessary put OSC back to V_{DD} and send a 'display control' instruction with D = 1 to enable the display again.

8.4.2 C

The cursor is displayed when C = 1 and inhibited when C = 0. Even if the cursor disappears, the display functions I/D, etc. remain in operation during display data write. The cursor is displayed using 5 dots in the 8th line (see Fig.5).

8.4.3 B

The character indicated by the cursor blinks when B = 1. The cursor character blink is displayed by switching between display characters and all dots on with a period of approximately 1 s, with $f_{BLINK} = \frac{f_{osc}}{52224}$

The cursor underline and the cursor character blink can be set to display simultaneously.

8.5 Cursor or display shift

'Cursor/display shift' moves the cursor position or the display to the right or left without writing or reading display data. This function is used to correct a character or move the cursor through the display. In 2-line displays, the cursor moves to the next line when it passes the last position (40) of the line. When the displayed data is shifted repeatedly all lines shift at the same time; displayed characters do not shift into the next line.

The Address Counter (AC) content does not change if the only action performed is shift display, but increments or decrements with the 'cursor shift'.

8.6 Function set

8.6.1 DL (PARALLEL MODE ONLY)

Sets interface data width. Data is sent or received in bytes (DB7 to DB0) when DL = 1 or in two nibbles (DB7 to DB4) when DL = 0. When 4-bit width is selected, data is transmitted in two cycles using the parallel bus. In a 4-bit application DB3 to DB0 should be left open-circuit (internal pull-ups). Hence in the first 'function set' instruction after power-on N and H are set to logic 1. A second 'function set' must then be sent (2 nibbles) to set N and H to their required values.

'Function set' from the I²C-bus interface sets the DL bit to logic 1.

8.6.2 M

Chooses either 1-line by 24 display (M = 0) or 2-line by 12 display (M = 1).

8.6.3 H

When H = 0 the chip can be programmed via the standard 11 instruction codes used in the PCF2116 and other LCD controllers.

When H = 1 the extended range of instructions will be used. These are mainly for controlling the display configuration and the icons.

8.7 Set CGRAM address

'Set CGRAM address' sets bits 5 to 0 of the CGRAM address A_{CG} into the address counter (binary A[5] to A[0]). Data can then be written to or read from the CGRAM.

Attention: the CGRAM address uses the same address register as the DDRAM address and consists of 7 bits (binary A[6] to A[0]). With the 'set CGRAM address' command, only bits 5 down to 0 are set. Bit 6 can be set using the 'set DDRAM address' command first, or by using the auto-increment feature during CGRAM write.
All bits 6 to 0 can be read using the 'read busy flag and address counter' command.

When writing to the lower part of the CGRAM, ensure that bit 6 of the address is not set (e.g. by an earlier DDRAM write or read action).

8.8 Set DDRAM address

'Set DDRAM address' sets the DDRAM address A_{DD} into the address counter (binary A[6] to A[0]). Data can then be written to or read from the DDRAM.

8.9 Read busy flag and address counter

'Read busy flag and address counter' reads the Busy Flag (BF) and Address Counter (AC). BF = 1 indicates that an internal operation is in progress. The next instruction will not be executed until BF = 0, so BF should be checked before sending another instruction.

At the same time, the value of the address counter expressed in binary A[6] to A[0] is read out. The address counter is used by both CGRAM and DDRAM, and its value is determined by the previous instruction.

8.10 Write data to CGRAM or DDRAM

'Write data' writes binary 8-bit data D[7] to D[0] to the CGRAM or the DDRAM.

Whether the CGRAM or DDRAM is to be written into is determined by the previous 'set CGRAM address' or 'set DDRAM address' command. After writing, the address automatically increments or decrements by 1, in accordance with the entry mode. Only bits D[4] to D[0] of CGRAM data are valid, bits D[7] to D[5] are 'don't care'.

8.11 Read data from CGRAM or DDRAM

'Read data' reads binary 8-bit data D[7] to D[0] from the CGRAM or DDRAM.

The most recent 'set address' command determines whether the CGRAM or DDRAM is to be read.

The 'read data' instruction gates the content of the Data Register (DR) to the bus while pin E is HIGH. After pin E goes LOW again, internal operation increments (or decrements) the AC and stores RAM data corresponding to the new AC into the DR.

It should be noted that there are only three instructions that update the Data Register (DR). These are:

- 'set CGRAM address'
- 'set DDRAM address'
- 'read data' from CGRAM or DDRAM.

Other instructions (e.g. 'write data', 'cursor/display shift', 'clear display', 'return home') do not modify the data register content.

8.12 Extended function set instructions and features

8.12.1 NEW INSTRUCTIONS

H = 1 sets the chip into alternate instruction set mode.

8.12.2 ICON CONTROL

The PCF2103 can drive up to 120 icons. See Fig.14 for CGRAM to icon mapping.

8.12.3 IM

When IM = 0 the chip is in character mode. In character mode characters and icons are driven (mux 1 : 18).

When IM = 1 the chip is in icon mode. In icon mode only the icons are driven (mux 1 : 2).

8.12.4 IB

Icon blink control is independent of the cursor/character blink function.

When IB = 0 icon blink is disabled. Icon data is stored in CGRAM character 0 to 2 ($3 \times 8 \times 5 = 120$ bits for 120 icons).

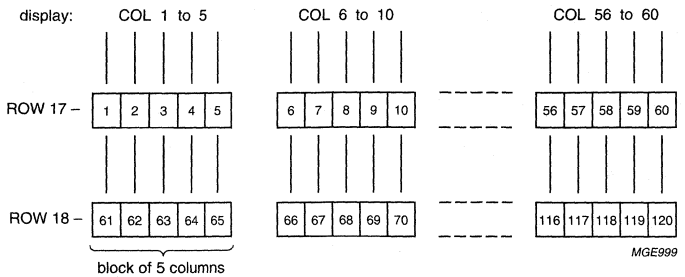
When IB = 1 icon blink is enabled. In this case each icon is controlled by two bits. Blink consists of two half phases (corresponding to the cursor on and off phases called even and odd phases hereafter).

Icon states for the even phase are stored in CGRAM characters 0 to 2 ($3 \times 8 \times 5 = 120$ bits for 120 icons). These bits also define the icon state when the icon blink is not used.

Icon states for the odd phase are stored in CGRAM character 4 to 6 (another 120 bits for the 120 icons). When icon blink is disabled CGRAM characters 4 to 6 may be used as normal CGRAM characters.

Table 9 Blink effect for icons and cursor character blink

PARAMETER	EVEN PHASE	ODD PHASE
Cursor underline	on	off
Cursor character blink	block (all on)	normal (display character)
Icons	state 1: CGRAM characters 0 to 2	state 2: CGRAM characters 4 to 6



icon no.	phase	ROW/COL	character codes	CGRAM address	CGRAM data	icon view
			7 6 5 4 3 2 1 0 MSB LSB	6 5 4 3 2 1 0 MSB LSB	4 3 2 1 0 MSB LSB	
1-5	even	17/1-5	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0	1 0 1 0 1	
6-10	even	17/6-10	0 0 0 0 0 0 0 0	0 0 0 0 0 0 1	0 1 0 1 0	
11-15	even	17/11-15	0 0 0 0 0 0 0 0	0 0 0 0 0 1 0	0 1 1 1 0	
⋮	⋮	⋮	⋮	⋮	⋮	⋮
56-60	even	17/56-60	0 0 0 0 0 0 0 1	0 0 0 1 0 1 1	1 1 1 1 1	
61-65	even	18/1-5	0 0 0 0 0 0 0 1	0 0 0 1 1 0 0	1 1 0 0 0	
⋮	⋮	⋮	⋮	⋮	⋮	⋮
116-120	even	18/56-60	0 0 0 0 0 0 1 0	0 0 1 0 1 1 1	1 1 1 0 1	
1-5	odd (blink)	17/1-5	0 0 0 0 0 1 0 0	0 1 0 0 0 0 0	0 0 0 0 0	
⋮	⋮	⋮	⋮	⋮	⋮	⋮
116-120	odd (blink)	18/56-60	0 0 0 0 0 1 1 0	0 1 1 0 0 1 1	0 0 1 1 0	

MGG001

CGRAM data bit = logic 1 turns the icon on, data bit = logic 0 turns the icon off.
Data in character codes 0 to 2 define the icon states when icon blink is disabled or during the even phase when icon blink is enabled.
Data in character codes 4 to 6 define the icon state during the odd phase when icon blink is enabled (not used for icons when icon blink is disabled).

Fig.14 CGRAM-to-icon mapping.

8.12.5 SCREEN CONFIGURATION

The default value for L is logic 0. In the event of L = 0 the two halves of a split screen are connected in a standard way i.e. column 1/61, 2/62 to 60/120. In the event of L = 1 the two halves of a split screen are connected in a mirrored way i.e. column 1/120, 2/119 to 60/61. This allows single layer PCB or glass layout.

8.12.6 DISPLAY CONFIGURATION

The default value for P and Q is logic 0. P = 1 mirrors the column data whereas Q = 1 mirrors the row data.

8.12.7 REDUCING CURRENT CONSUMPTION

Reducing current consumption can be achieved by one of the options mentioned in Table 10.

Table 10 Reducing current consumption

ORIGINAL MODE	ALTERNATIVE MODE
Character mode	icon mode (control bit IM)
Display on	display off (control bit D)

9 INTERFACE TO MICROCONTROLLER

9.1 Parallel interface

The PCF2103 can send data in either two 4-bit operations or one 8-bit operation and can thus interface to 4-bit or 8-bit microcontrollers.

In 8-bit mode data is transferred as 8-bit bytes using the 8 data lines DB7 to DB0. Three further control lines E, RS and R/$\overline{W}$ are required; see Table 1.

In 4-bit mode data is transferred in two cycles of 4 bits each using pins DB7 to DB4 for transaction. The higher order bits (corresponding to DB7 to DB4 in 8-bit mode) are sent in the first cycle and the lower order bits (DB3 to DB0 in 8-bit mode) in the second. Data transfer is complete after two 4-bit data transfers. Note that two cycles are also required for the busy flag check. 4-bit operation is selected by instruction. See Figs 11 to 14 for examples of bus protocol.

In 4-bit mode pins DB3 to DB0 must be left open-circuit. They are pulled up to V_{DD} internally.

9.2 I²C-bus interface

9.2.1 CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a Serial Clock Line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH-level signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

9.2.2 I²C-BUS PROTOCOL

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always carried out with the first byte transmitted after the start procedure. The I²C-bus configuration for the different PCF2103 read and write cycles is shown in Figs 20 to 21. The slow down feature of the I²C-bus protocol (receiver holds SCL low during internal operations) is not used in the PCF2103.

9.2.3 DEFINITIONS

- Transmitter: the device which sends the data to the bus
- Receiver: the device which receives the data from the bus
- Master: the device which initiates a transfer, generates clock signals and terminates a transfer
- Slave: the device addressed by a master
- Multi-master: more than one master can attempt to control the bus at the same time without corrupting the message
- Arbitration: procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted
- Synchronization: procedure to synchronize the clock signals of two or more devices.

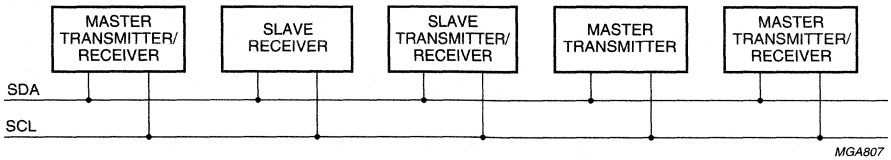


Fig.15 System configuration.

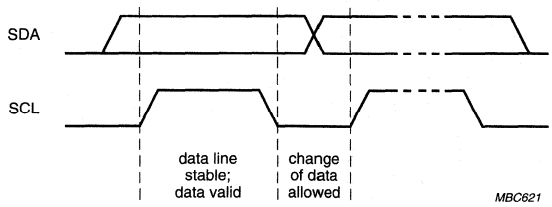


Fig.16 Bit transfer.

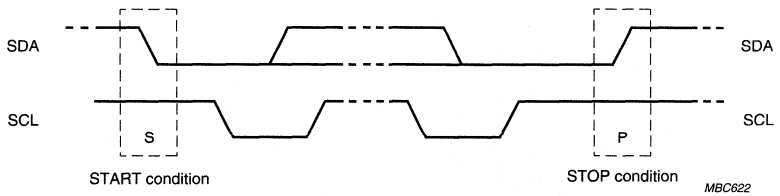


Fig.17 Definition of START and STOP conditions.

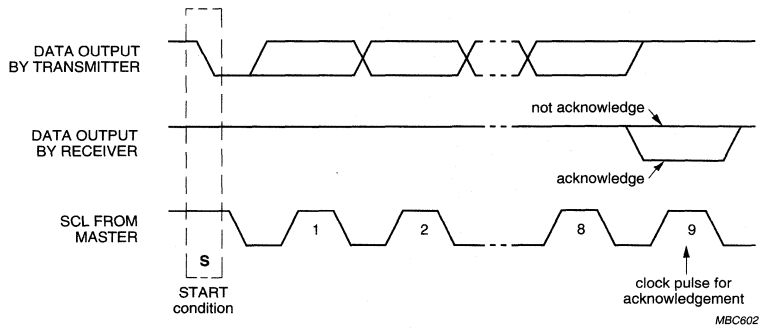


Fig.18 Acknowledgement on the I²C-bus.

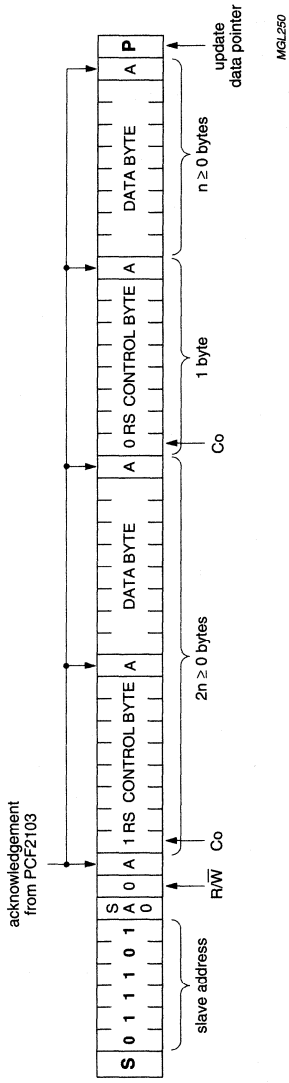
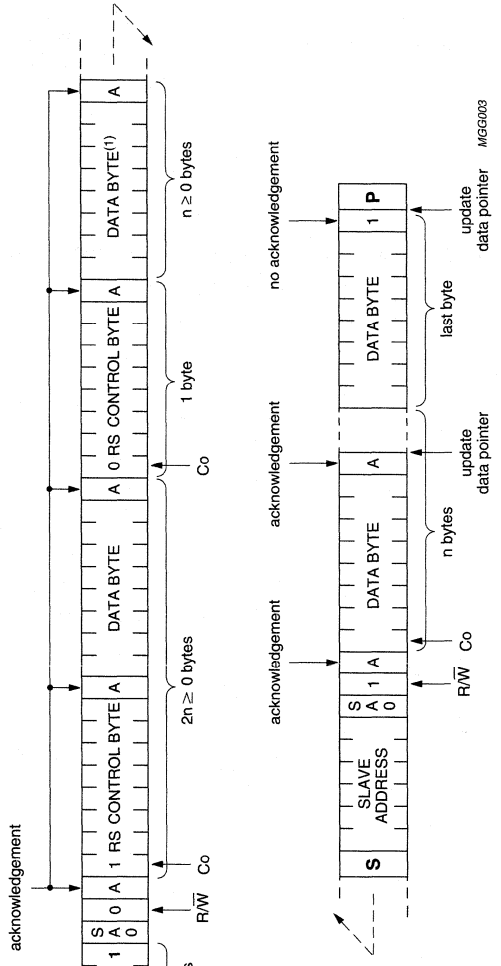


Fig.19 Master transmits to slave receiver; write mode.



(1) Last data byte is a dummy byte (may be omitted).

Fig.20 Master reads after setting word address; write word address, set RS; 'read data'.

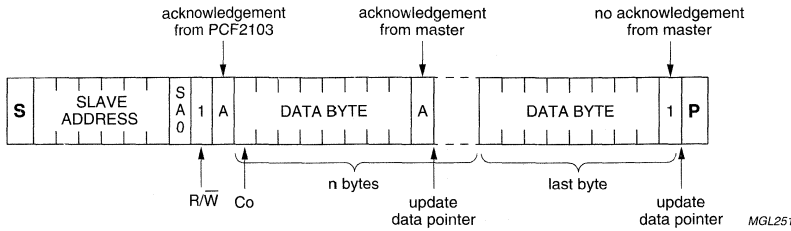


Fig.21 Master reads slave immediately after first byte; read mode (RS previously defined).

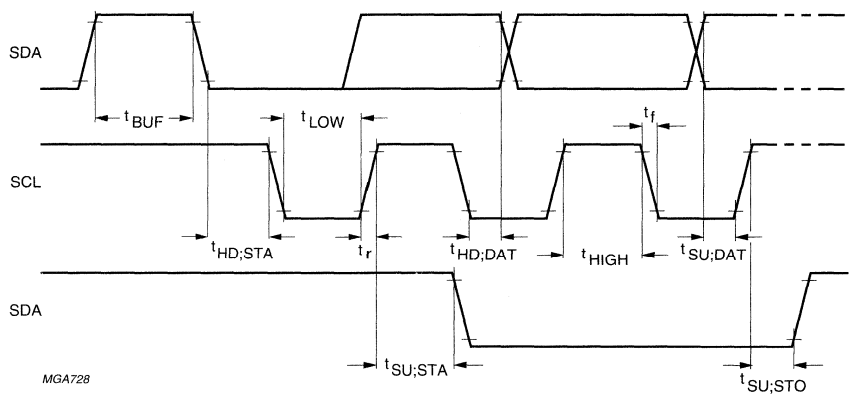


Fig.22 I²C-bus timing diagram.

10 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.5	+6.5	V
V_{LCD}	LCD supply voltage	−0.5	+7.5	V
$V_{I(1)}$	input voltage on pins OSC, RS, R/$\overline{W}$, E and DB7 to DB0	−0.5	V_{DD} + 0.5	V
$V_{I(2)}$	input voltage on pins SCL and SDA	−0.5	+6.5	V
V_O	output voltage on pins R1 to R18, C1 to C60 and V_{LCD}	−0.5	V_{LCD} + 0.5	V
I_I	DC input current	−10	+10	mA
I_O	DC output current	−10	+10	mA
I_{DD}, I_{SS} and I_{LCD}	V_{DD}, V_{SS} or V_{LCD} current	−50	+50	mA
P_{tot}	total power dissipation	−	400	mW
P/out	power dissipation per output	−	100	mW
T_{stg}	storage temperature	−65	+150	°C

11 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see *"Handling MOS Devices"*).

12 DC CHARACTERISTICS

V_{DD} = 1.8 to 5.5 V; V_{SS} = 0 V; V_{LCD} = 2.2 to 6.5 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage		1.8	–	5.5	V
V_{LCD}	LCD supply voltage		2.2	–	6.5	V
I_{SS}	supply current	note 1	–	60	120	μA
		V_{DD} = 3 V; V_{LCD} = 5 V; notes 1 and 2	–	45	80	μA
		icon mode; V_{DD} = 3 V; V_{LCD} = 2.5 V; notes 1 and 2	–	25	45	μA
		power-down mode; V_{DD} = 3 V; V_{LCD} = 2.5 V; DB7 to DB0, RS and R/$\overline{W}$ = 1; OSC = 0; PD = 1; note 1	–	2	6	μA
V_{POR}	power-on reset voltage	note 3	–	1.3	1.6	V
Logic						
V_{IL}	LOW-level input voltage on pins T1, E, RS, R/$\overline{W}$, DB7 to DB0 and SA0		0	–	0.3V_{DD}	V
V_{IH}	HIGH-level input voltage on pins T1, E, RS, R/$\overline{W}$, DB7 to DB0 and SA0		0.7V_{DD}	–	V_{DD}	V
$V_{IL(PD)}$	LOW-level input voltage on pin PD		0	–	0.2V_{DD}	V
$V_{IH(PD)}$	HIGH-level input voltage on pin PD		0.8V_{DD}	–	V_{DD}	V
$V_{IL(OSC)}$	LOW-level input voltage on pin OSC		0	–	V_{DD} − 1.5	V
$V_{IH(OSC)}$	HIGH-input voltage on pin OSC		V_{DD} − 0.1	–	V_{DD}	V
$I_{OL(DB)}$	LOW-level output current on pins DB7 to DB0	V_{OL} = 0.4 V; V_{DD} = 5 V	1.6	4	–	mA
$I_{OH(DB)}$	HIGH-level output current on pins DB7 to DB0	V_{OH} = 4 V; V_{DD} = 5 V	−1	−8	–	mA
I_{pu}	pull-up current on pins DB7 to DB0	V_I = V_{SS}	0.04	0.12	1	μA
I_L	leakage current on pins OSC, E, RS, R/$\overline{W}$, DB7 to DB0 and SA0	V_I = V_{DD} or V_{SS}	−1	–	+1	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I²C-bus						
SDA AND SCL						
V_{IL}	LOW-level input voltage		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	–	5.5	V
I_L	input leakage current	$V_I = V_{DD}$ or V_{SS}	−1	–	+1	μA
C_i	input capacitance	note 4	–	–	10	pF
I_{OL}	LOW-level output current pin SDA	V_{OL} = 0.4 V; V_{DD} = 5 V	3	–	–	mA
LCD outputs						
$R_{o(ROW)}$	row output resistance on pins R1 to R18	note 5	–	10	30	kΩ
$R_{o(COL)}$	column output resistance on pins C1 to C60	note 5	–	15	40	kΩ
$V_{bias(tol)}$	bias tolerance on pins R1 to R18 and C1 to C60	note 6	–	20	130	mV

Notes

1. LCD outputs are open-circuit; inputs at V_{DD} or V_{SS}; bus inactive.
2. T_{amb} = 25 °C; f_{osc} = 200 kHz.
3. Resets all logic when $V_{DD} < V_{POR}$; 3 oscillator clock cycles required.
4. Tested on sample basis.
5. Resistance of output terminals (R1 to R18 and C1 to C60) with a load current of 20 μA; outputs measured one at a time.
6. LCD outputs open-circuit.

13 AC CHARACTERISTICS

V_{DD} = 1.8 to 5.5 V; V_{SS} = 0 V; V_{LCD} = 2.2 – 6.5 V; T_{amb} = –40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$f_{fr(LCD)}$	LCD frame frequency (internal clock)	V_{DD} = 5.0 V	45	81	147	Hz
f_{osc}	oscillator frequency (not available at any pin)		140	250	450	kHz
$f_{osc(ext)}$	external clock frequency		140	–	450	kHz
t_{OSCST}	oscillator start-up time after PD going from logic 1 to logic 0		–	200	300	µs
Bus timing characteristics: parallel interface; note 1						
WRITE OPERATION (WRITING DATA FROM MICROCONTROLLER TO PCF2103); see Fig.23						
$T_{en(cy)}$	enable cycle time		500	–	–	ns
$t_{W(en)}$	enable pulse width		220	–	–	ns
$t_{su(A)}$	address set-up time		50	–	–	ns
$t_{h(A)}$	address hold time		25	–	–	ns
$t_{su(D)}$	data set-up time		60	–	–	ns
$t_{h(D)}$	data hold time		25	–	–	ns
READ OPERATION (READING DATA FROM PCF2103 TO MICROCONTROLLER); see Fig.24						
$T_{en(cy)}$	enable cycle time		500	–	–	ns
$t_{W(en)}$	enable pulse width		220	–	–	ns
$t_{su(A)}$	address set-up time		50	–	–	ns
$t_{h(A)}$	address hold time		25	–	–	ns
$t_{d(D)}$	data delay time		–	–	150	ns
$t_{h(D)}$	data hold time		20	–	100	ns
Timing characteristics: I^2C-bus interface; note 1						
f_{SCL}	SCL clock frequency		–	–	400	kHz
t_{LOW}	SCL clock LOW period		1.3	–	–	µs
t_{HIGH}	SCL clock HIGH period		0.6	–	–	µs
$t_{SU;DAT}$	data set-up time		100	–	–	ns
$t_{HD;DAT}$	data hold time		0	–	–	ns
t_r	SCL and SDA rise time		–	–	300	ns
t_f	SCL and SDA fall time		–	–	300	ns
C_B	capacitive bus line load		–	–	400	pF
$t_{SU;STA}$	set-up time for a repeated START condition		0.6	–	–	µs
$t_{HD;STA}$	START condition hold time		0.6	–	–	µs
$t_{SU;STO}$	set-up time for STOP condition		0.6	–	–	µs
t_{SW}	tolerable spike width on bus		–	–	50	ns

Note

1. All timing values are valid within the operating supply voltage and ambient temperature range and are referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

14 TIMING CHARACTERISTICS

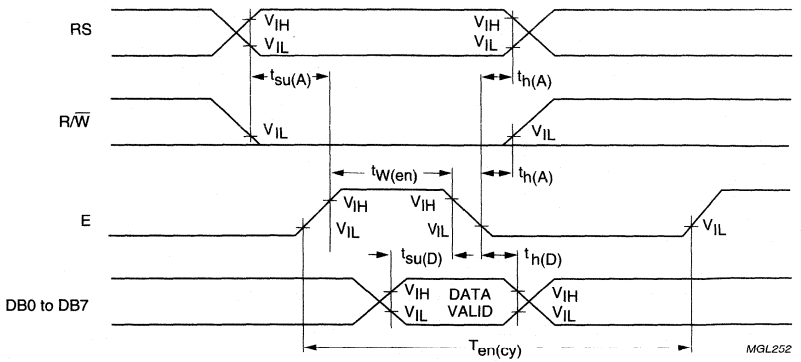


Fig.23 Parallel bus write operation sequence; writing data from microcontroller to PCF2103.

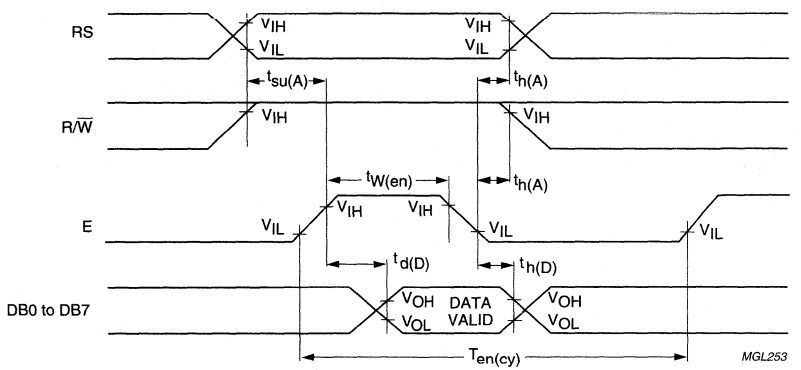


Fig.24 Parallel bus read operation sequence; reading data from PCF2103 to microcontroller.

15 APPLICATION INFORMATION

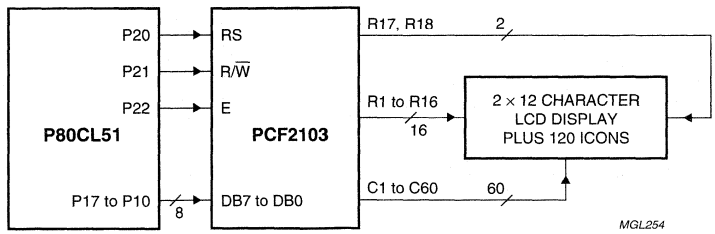


Fig.25 Direct connection to 8-bit microcontroller; 8-bit bus.

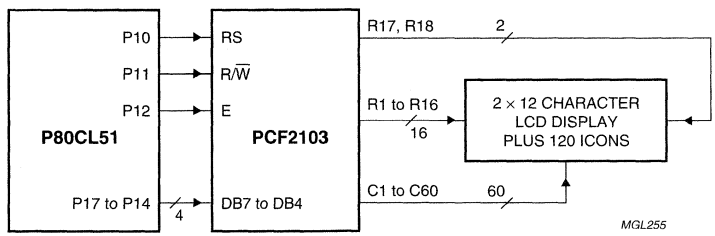


Fig.26 Direct connection to 8-bit microcontroller; 4-bit bus.

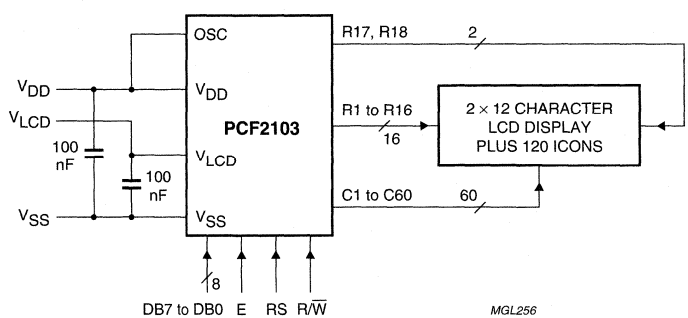


Fig.27 Application example using parallel interface.

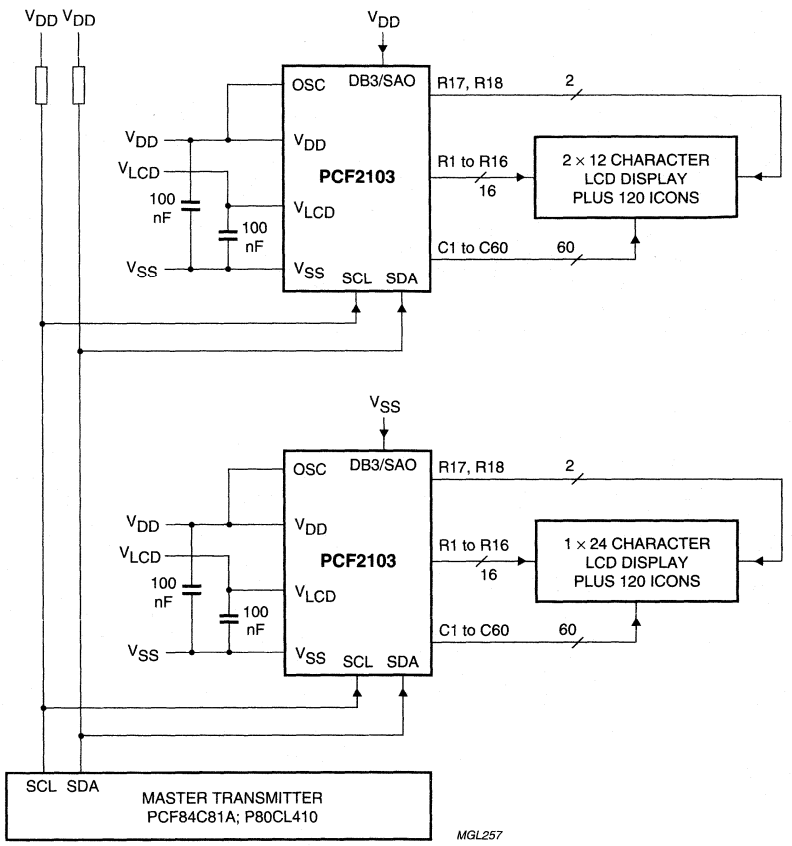


Fig.28 Application using I²C-bus interface.

15.1 4-bit operation, 1-line display using internal reset

The program must set functions prior to 4-bit operation; Table 11 shows an example. When power is turned on, 8-bit operation is automatically selected and the PCF2103 attempts to perform the first write as an 8-bit operation. Since nothing is connected to DB0 to DB3, a rewrite is then required. However, since one operation is completed in two accesses of 4-bit operation, a rewrite is required to set the functions (see Table 11 step 3). Thus, DB4 to DB7 of the 'function set' are written twice.

15.2 8-bit operation, 1-line display using internal reset

Table 12 shows an example of a 1-line display in 8-bit operation. The PCF2103 functions must be set by the 'function set' instruction prior to display. Since the DDRAM can store data for 80 characters, the RAM can be used for advertising displays when combined with display shift operation.

Since the display shift operation changes display position only and DDRAM contents remain unchanged, display data entered first can be displayed when the 'return home' operation is performed.

15.3 8-bit operation, 2-line display

For a 2-line display, the cursor automatically moves from the first to the second line after the 40th digit of the first line has been written. Thus, if there are only 8 characters in the first line, the DDRAM address must be set after the eighth character is completed (see Table 6). It should be noted that both lines of the display are always shifted together; data does not shift from one line to the other.

15.4 I²C-bus operation, 1-line display

A control byte is required with most commands (see Table 15).

Table 11 4-bit operation, 1-line display example; using internal reset

STEP	INSTRUCTION						DISPLAY	OPERATION
1	power supply on (PCF2103 is initialized by the internal reset circuit)							initialized; no display appears
2	function set							
	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4		sets to 4-bit operation; in this instance operation is handled as 8-bit by initialization and only this instruction completes with one write
	0	0	0	0	1	0		
3	function set							
	0	0	0	0	1	0		sets to 4-bit operation, selects 1-line display and $V_{LCD} = V_0$; 4-bit operation starts from this point and resetting is needed
	0	0	0	0	0	0		
4	display on/off control							
	0	0	0	0	0	0	_	turns on display and cursor; entire display is blank after initialization
	0	0	1	1	1	0		
5	entry mode set							
	0	0	0	0	0	0	_	sets mode to increment the address by 1 and to shift the cursor to the right at the time of write to the DD/CGRAM; display is not shifted
	0	0	0	1	1	0		
6	'write data' to CGRAM/DDRAM							
	1	0	0	1	0	1	P_	writes 'P'; the DDRAM has already been selected by initialization at power-on; the cursor is incremented by 1 and shifted to the right
	1	0	0	0	0	0		

Table 12 8-bit operation, 1-line display example; using internal reset (character set 'A')

STEP	INSTRUCTION	DISPLAY	OPERATION
1	power supply on (PCF2103 is initialized by the internal reset function)		initialized; no display appears
2	function set RS R/$\overline{W}$ DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 1 1 0 0 0 0		sets to 8-bit operation, selects 1-line display
3	display mode on/off control 0 0 0 0 0 0 1 1 1 0	_	turns on display and cursor; entire display is blank after initialization
4	entry mode set 0 0 0 0 0 0 0 1 1 0	_	sets mode to increment the address by 1 and to shift the cursor to the right at the time of the write to the DD/CGRAM; display is not shifted
5	'write data' to CGRAM/DDRAM 1 0 0 1 0 1 0 0 0 0	**P**_	writes 'P'; the DDRAM has already been selected by initialization at power-on; the cursor is incremented by 1 and shifted to the right
6	'write data' to CGRAM/DDRAM 1 0 0 1 0 0 1 0 0 0	**PH**_	writes 'H'
7 to 11			
12	'write data' to CGRAM/DDRAM 1 0 0 1 0 1 0 0 1 1	**PHILIPS**_	writes 'S'
13	entry mode set 0 0 0 0 0 0 0 1 1 1	**PHILIPS**_	sets mode for display shift at the time of write
14	'write data' to CGRAM/DDRAM 1 0 0 0 1 0 0 0 0 0	**HILIPS** _	writes space
15	'write data' to CGRAM/DDRAM 1 0 0 1 0 0 1 1 0 1	**ILIPS M**_	writes 'M'
16			

STEP	INSTRUCTION	DISPLAY	OPERATION
17	'write data' to CGRAM/DDRAM 1 0 0 1 0 0 1 1 1 1	**MICROKO_**	writes 'O'
18	cursor/display shift 0 0 0 0 0 1 0 0 0 0	**MICROKO**	shifts only the cursor position to the left
19	cursor/display shift 0 0 0 0 0 1 0 0 0 0	**MICROKO**	shifts only the cursor position to the left
20	'write data' to CGRAM/DDRAM 1 0 0 1 0 0 0 0 1 1	**ICROKO**	writes 'C' correction; the display moves to the left
21	cursor/display shift 0 0 0 0 0 1 1 1 0 0	**MICROKO**	shifts the display and cursor to the right
22	cursor/display shift 0 0 0 0 0 1 0 1 0 0	**MICROCO_**	shifts only the cursor to the right
23	'write data' to CGRAM/DDRAM 1 0 0 1 0 0 1 1 0 1	**ICROCOM_**	writes 'M'
24			
25	return home 0 0 0 0 0 0 0 0 1 0	**PHILIPS M**	returns both display and cursor to the original position (address 0)

Table 13 8-bit operation, 1-line display and icon example; using internal reset (character set 'A')

STEP	INSTRUCTION	DISPLAY	OPERATION
1	power supply on (PCF2103 is initialized by the internal reset function)		initialized; no display appears
2	function set RS R/$\overline{W}$ DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 1 1 0 0 0 0		sets to 8-bit operation, selects 1-line display
3	display mode on/off control 0 0 0 0 0 0 1 1 1 0	_	turns on display and cursor; entire display is blank after initialization
4	entry mode set 0 0 0 0 0 0 0 1 1 0	_	sets mode to increment the address by 1 and to shift the cursor to the right at the time of the write to the DD/CGRAM; display is not shifted
5	set CGRAM address 0 0 0 1 0 0 0 0 0 0	_	sets the CGRAM address to position of character 0; the CGRAM is selected
6	'write data' to CGRAM/DDRAM 1 0 0 0 0 0 1 0 1 0	_	writes data to CGRAM for icon even phase; icons appear
7			
8	set CGRAM address 0 0 0 1 1 1 0 0 0 0	_	sets the CGRAM address to position of character 4; the CGRAM is selected
9	'write data' to CGRAM/DDRAM 1 0 0 0 0 0 1 0 1 0	_	writes data to CGRAM for icon odd phase
10			
11	function set 0 0 0 0 1 1 0 0 0 1	_	sets H = 1
12	icon control 0 0 0 0 0 0 1 0 1 0	_	icons blink
13	function set 0 0 0 0 1 1 0 0 0 1	_	sets H = 0

STEP	INSTRUCTION										DISPLAY	OPERATION
14	set DDRAM address											
	0	0	1	0	0	0	0	0	0	0		sets the DDRAM address to the first position; DDRAM is selected
15	'write data' to CGRAM/DDRAM											
	1	0	0	1	0	1	0	0	0	0	**P_**	writes 'P'; the cursor is incremented by 1 and shifted to the right
16	'write data' to CGRAM/DDRAM											
	1	0	0	1	0	0	1	0	0	0	**PH_**	writes 'H'
17 to 20												
21	return home											
	0	0	0	0	0	0	0	0	1	0	**PHILIPS**	returns both display and cursor to the original position (address 0)

Table 14 8-bit operation, 2-line display example; using internal reset

STEP	INSTRUCTION	DISPLAY	OPERATION
1	power supply on (PCF2103 is initialized by the internal reset function)		initialized; no display appears
2	function set RS R/$\overline{W}$ DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 1 1 1 0 0 0		sets to 8-bit operation; selects 2-line display and voltage generator off
3	display on/off control 0 0 0 0 0 0 1 1 1 0	_	turns on display and cursor; entire display is blank after initialization
4	entry mode set 0 0 0 0 0 0 0 1 1 0	_	sets mode to increment the address by 1 and to shift the cursor to the right at the time of write to the CG/DDRAM; display is not shifted
5	'write data' to CGRAM/DDRAM 1 0 0 1 0 1 0 0 0 0	**P**_	writes 'P'; the DDRAM has already been selected by initialization at power-on; the cursor is incremented by 1 and shifted to the right
6 to 10			
11	'write data' to CGRAM/DDRAM 1 0 0 1 0 1 0 0 1 1	**PHILIPS_**	writes 'S'
12	set DDRAM address 0 0 1 1 0 0 0 0 0 0	**PHILIPS** _	sets DDRAM address to position the cursor at the head of the 2nd line
13	'write data' to CGRAM/ DDRAM 1 0 0 1 0 0 1 1 0 1	**PHILIPS** **M**_	writes 'M'
14 to 19			

STEP	INSTRUCTION	DISPLAY	OPERATION
20	'write data' to CGRAM/DDRAM 1 0 0 1 0 0 1 1 1 1	PHILIPS MICROCO_	writes 'O'
21	'write data' to CGRAM/DDRAM 0 0 0 0 0 0 0 1 1 1	PHILIPS MICROCO_	sets mode for display shift at the time of write
22	'write data' to CGRAM/DDRAM 1 0 0 1 0 0 1 1 0 1	HILIPS ICROCOM_	writes 'M'; display is shifted to the left; the first and second lines shift together
23			
24	return home 0 0 0 0 0 0 0 0 1 0	PHILIPS MICROCOM	returns both display and cursor to the original position (address 0)

Table 15 Example of I²C-bus operation; 1-line display (using internal reset, assuming SA0 = V_{SS}; note 1)

STEP	INSTRUCTION	DISPLAY	OPERATION
1	I²C-bus start		initialized; no display appears
2	slave address for write SA6 SA5 SA4 SA3 SA2 SA1 SA0 R/$\overline{W}$ Ack 0 1 1 1 0 1 0 0 1		during the acknowledge cycle SDA will be pulled-down by the PCF2103
3	send a control byte for 'function set' Co RS 0 0 0 0 0 0 Ack 0 0 0 0 0 0 0 0 1		control byte sets RS for following data bytes
4	function set DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 0 1 X 0 0 0 0 1		selects 1-line display; SCL pulse during acknowledge cycle starts execution of instruction
5	display on/off control DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 0 0 0 1 1 1 0 1	_	turns on display and cursor; entire display shows character 20H (blank in ASCII-like character sets)
6	entry mode set DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 0 0 0 0 1 1 0 1	_	sets mode to increment the address by 1 and to shift the cursor to the right at the time of write to the DDRAM or CGRAM; display is not shifted
7	I²C-bus start	_	for writing data to DDRAM, RS must be set to 1; therefore a control byte is needed
8	slave address for write SA6 SA5 SA4 SA3 SA2 SA1 SA0 R/$\overline{W}$ Ack 0 1 1 1 0 1 0 0 1	_	
9	send a control byte for 'write data' Co RS 0 0 0 0 0 0 Ack 0 1 0 0 0 0 0 0 1	_	
10	'write data' to DDRAM DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 1 0 1 0 0 0 0 1	 **P**_	writes 'P'; the DDRAM has been selected at power-up; the cursor is incremented by 1 and shifted to the right

STEP	INSTRUCTION	DISPLAY	OPERATION
11	'write data' to DDRAM DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 1 0 0 1 0 0 0 1	**PH_**	writes 'H'
12 to 15			
16	'write data' to DDRAM DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 1 0 1 0 0 1 1 1	**PHILIPS_**	writes 'S'
17	(optional I^2C-bus stop) I^2C-bus start + slave address for write (as step 8)	**PHILIPS_**	
18	control byte Co RS 0 0 0 0 0 0 Ack 1 0 0 0 0 0 0 0 1	**PHILIPS_**	
19	return home DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 0 0 0 0 0 1 0 1	**PHILIPS**	sets DDRAM address 0 in address counter (also returns shifted display to original position; DDRAM contents unchanged); this instruction does not update the Data Register (DR)
20	I^2C-bus start	**PHILIPS**	
21	slave address for read SA6 SA5 SA4 SA3 SA2 SA1 SA0 R/$\overline{W}$ Ack 0 1 1 1 0 1 0 1 1	**PHILIPS**	during the acknowledge cycle the content of the DR is loaded into the internal I^2C-bus interface to be shifted out; in the previous instruction neither a 'set address' nor a 'read data' has been performed; therefore the content of the DR was unknown; R/$\overline{W}$ has to be set to logic 1 while still in I^2C-bus write mode
22	control byte for read Co RS 0 0 0 0 0 0 Ack 0 1 1 0 0 0 0 0 1	**PHILIPS**	DDRAM content will be read from following instructions

STEP	INSTRUCTION	DISPLAY	OPERATION
23	'read data': 8 × SCL + master acknowledge; note 2 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack X X X X X X X X 0	PHILIPS	8 × SCL; content loaded into interface during previous acknowledge cycle is shifted out over SDA; MSB is DB7; during master acknowledge content of DDRAM address 01 is loaded into the I²C-bus interface
24	'read data': 8 × SCL + master acknowledge; note 2 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 1 0 0 1 0 0 0 0	PHILIPS	8 × SCL; code of letter 'H' is read first; during master acknowledge code of 'I' is loaded into the I²C-bus interface
25	'read data': 8 × SCL + no master acknowledge; note 2 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 1 0 0 1 0 0 1 1	PHILIPS	no master acknowledge; after the content of the I²C-bus interface register is shifted out no internal action is performed; no new data is loaded to the interface register, Data Register (DR) is not updated, Address Counter (AC) is not incremented and cursor is not shifted
26	I²C-bus stop	PHILIPS	

Notes

1. X = don't care.
2. SDA is left at high-impedance by the microcontroller during the read acknowledge.

Table 16 Initialization by instruction, 8-bit interface (note 1)

STEP										DESCRIPTION
power-on or unknown state										
					↓					
wait 2 ms after V_{DD} rises above V_{POR}										
					↓					
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	BF cannot be checked before this instruction
0	0	0	0	1	1	X	X	X	X	function set (interface is 8 bits long)
					↓					
wait 2 ms										
					↓					
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	BF cannot be checked before this instruction
0	0	0	0	1	1	X	X	X	X	function set (interface is 8 bits long)
					↓					
wait more than 40 µs										
					↓					
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	BF cannot be checked before this instruction
0	0	0	0	1	1	X	X	X	X	function set (interface is 8 bits long)
					↓					BF can be checked after the following instructions; when BF is not checked, the waiting time between instructions is the specified instruction time (see Table 4)
					↓					
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	function set (interface is 8 bits long); specify the number of display lines
0	0	0	0	1	1	0	M	0	H	
0	0	0	0	0	0	1	0	0	0	display off
0	0	0	0	0	0	0	0	0	1	clear display
0	0	0	0	0	0	0	1	I/D	S	entry mode set
					↓					
Initialization ends										

Note

1. X = don't care.

Table 17 Initialization by instruction, 4-bit interface; not applicable for I²C-bus operation

STEP						DESCRIPTION
Power-on or unknown state						
			↓			
Wait 2 ms after V_{DD} rises above V_{POR}						
			↓			
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	BF cannot be checked before this instruction
0	0	0	0	1	1	function set (interface is 8 bits long)
			↓			
Wait 2 ms						
			↓			
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	BF cannot be checked before this instruction
0	0	0	0	1	1	function set (interface is 8 bits long)
			↓			
Wait 40 μs						
			↓			
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	BF cannot be checked before this instruction
0	0	0	0	1	1	function set (interface is 8 bits long)
			↓			BF can be checked after the following instructions; when BF is not checked, the waiting time between instructions is the specified instruction time (see Table 4)
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	function set (set interface to 4 bits long)
0	0	0	0	1	0	interface is 8 bits long
0	0	0	0	1	0	function set (interface is 4 bits long)
0	0	0	M	0	H	specify number of display lines
0	0	0	0	0	0	
0	0	1	0	0	0	display off
0	0	0	0	0	0	clear display
0	0	0	0	0	1	
0	0	0	0	0	0	entry mode set
0	0	0	1	I/D	S	
			↓			
Initialization ends						

16 BONDING PAD LOCATIONS

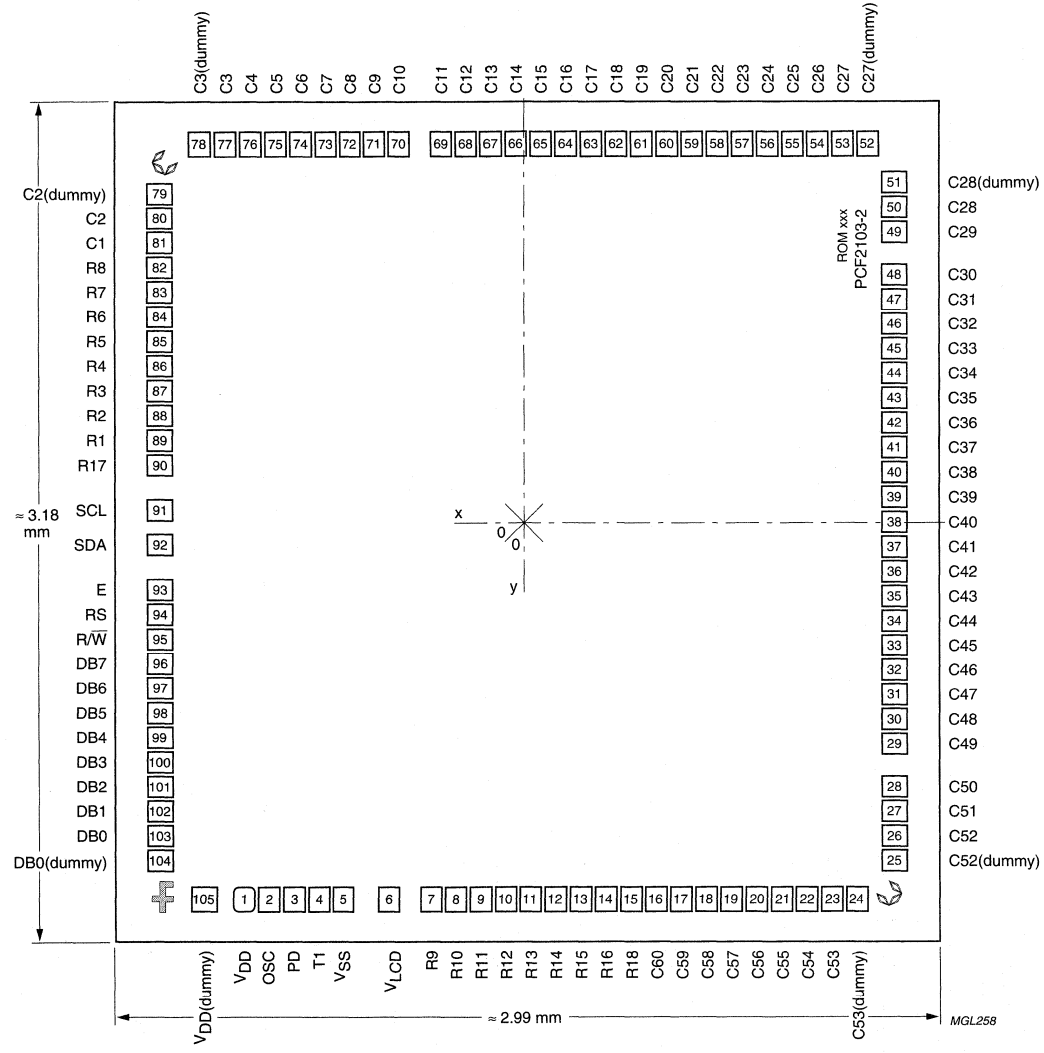


Fig.29 Bonding pad locations.

Table 18 Bonding pad locations (dimensions in μm). All x/y coordinates are referenced to centre of chip (see Fig.29)

SYMBOL	PAD	X	Y
V_{DD} (dummy)	105	−1228	−1414
V_{DD}	1	−1048	−1414
OSC	2	−958	−1414
PD	3	−868	−1414
T1	4	−778	−1414
V_{SS}	5	−688	−1414
V_{LCD}	6	−516	−1414
R9	7	−349	−1414
R10	8	−259	−1414
R11	9	−169	−1414
R12	10	−79	−1414
R13	11	11	−1414
R14	12	101	−1414
R15	13	191	−1414
R16	14	281	−1414
R18	15	371	−1414
C60	16	461	−1414
C59	17	551	−1414
C58	18	641	−1414
C57	19	731	−1414
C56	20	821	−1414
C55	21	911	−1414
C54	22	1001	−1414
C53	23	1091	−1414
C53 (dummy)	24	1181	−1414
C52 (dummy)	25	1344	−1254
C52	26	1344	−1164
C51	27	1344	−1074
C50	28	1344	−948
C49	29	1344	−812
C48	30	1344	−722
C47	31	1344	−632
C46	32	1344	−542
C45	33	1344	−452
C44	34	1344	−362
C43	35	1344	−272
C42	36	1344	−182
C41	37	1344	−92

SYMBOL	PAD	X	Y
C40	38	1344	−2
C39	39	1344	88
C38	40	1344	178
C37	41	1344	268
C36	42	1344	358
C35	43	1344	448
C34	44	1344	538
C33	45	1344	628
C32	46	1344	718
C31	47	1344	808
C30	48	1344	898
C29	49	1344	1070
C28	50	1344	1160
C28 (dummy)	51	1344	1250
C27 (dummy)	52	1262	1414
C27	53	1172	1414
C26	54	1082	1414
C25	55	992	1414
C24	56	902	1414
C23	57	805	1414
C22	58	715	1414
C21	59	625	1414
C20	60	535	1414
C19	61	445	1414
C18	62	355	1414
C17	63	265	1414
C16	64	175	1414
C15	65	85	1414
C14	66	−5	1414
C13	67	−95	1414
C12	68	−185	1414
C11	69	−275	1414
C10	70	−446	1414
C9	71	−536	1414
C8	72	−626	1414
C7	73	−716	1414
C6	74	−806	1414
C5	75	−896	1414

SYMBOL	PAD	X	Y
C4	76	−986	1414
C3	77	−1076	1414
C3 (dummy)	78	−1166	1414
C2 (dummy)	79	−1344	1303
C2	80	−1344	1213
C1	81	−1344	1123
R8	82	−1344	1033
R7	83	−1344	943
R6	84	−1344	853
R5	85	−1344	763
R4	86	−1344	673
R3	87	−1344	583
R2	88	−1344	493
R1	89	−1344	403
R17	90	−1344	313
SCL	91	−1344	131
SDA	92	−1344	−9
E	93	−1344	−195
RS	94	−1344	−289
RW	95	−1344	−382
DB7	96	−1344	−476
DB6	97	−1344	−572
DB5	98	−1344	−668
DB4	99	−1344	−765
DB3	100	−1344	−861
DB2	101	−1344	−957
DB1	102	−1344	−1054
DB0	103	−1344	−1150
DB0 (dummy)	104	−1344	−1240
Rec. Pat. C1		1335	−1405
Rec. Pat. C2		−1335	1405
Rec. Pat. F		−1340	−1397

Table 19 Bump specifications

PARAMETER	SPECIFICATION	UNIT
Bump variant	N	–
Type	galvanic; pure aurum	–
Bump width	60 ±6	μm
Bump length	90 ±6	μm
Bump height	17.5 ±5	μm
Height difference in one die	<2	μm
Convex deformation	<5	μm
Pad size; aluminium	80 × 100	μm
Passivation opening CBB	46 × 76	μm
Wafer thickness	380 ±25	μm
Minimum pitch	90	μm

CONTENTS

1 FEATURES

- Single chip LCD controller/driver
- 1 or 2-line display of up to 24 characters per line, or 2 or 4 lines of up to 12 characters per line
- 5 × 7 character format plus cursor; 5 × 8 for kana (Japanese syllabary) and user-defined symbols
- On-chip:
  - generation of intermediate LCD bias voltages
  - oscillator requires no external components (external clock also possible)
- Display data RAM: 80 characters
- Character generator ROM: 240 characters
- Character generator RAM: 16 characters
- 4 or 8-bit parallel bus or 2-wire I²C-bus interface
- CMOS/TTL compatible
- 32 row, 60 column outputs
- MUX rates 1 : 32 and 1 : 16
- Uses common 11 code instruction set
- Logic supply voltage range, $V_{DD} - V_{SS}$: 2.5 to 6 V
- Display supply voltage range, $V_{DD} - V_{LCD}$: 3.5 to 9 V
- Low power consumption.
- I²C-bus address: 011101 SA0.

2 APPLICATIONS

- Telecom equipment
- Portable instruments
- Point-of-sale terminals.

3 GENERAL DESCRIPTION

The PCF2104x integrated circuit is similar to the PCF2114x (described in the *"PCF2116 family"* data sheet) but does not contain the high voltage generator of that device.

The PCF2104x is optimized for chip-on-glass applications. The 'x' in 'PCF2104x' represents a specific letter code for a character set in the character generator ROM (CGROM).

Two standard character sets are currently available, specified by the letters 'C' and 'L' (see Figs 5 and 6). Other character sets are available on request.

The PCF2104x is a low-power CMOS LCD controller and driver, designed to drive a split screen dot matrix LCD display of 1 or 2 lines by 24 characters or 2 or 4 lines by 12 characters with a 5 × 8 dot format. All necessary functions for the display are provided in a single chip, including on-chip generation of LCD bias voltages which results in a minimum of external components and lower system power consumption. To allow partial V_{DD} shutdown the ESD protection system of the SCL and SDA pins does not use a diode connected to V_{DD}.

The chip contains a character generator and displays alphanumeric and kana characters. The PCF2104x interfaces to most microcontrollers via a 4 or 8-bit bus, or via the 2-wire I²C-bus.

3.1 Packages

- PCF2104xU/2; chip with bumps in tray
- PCF2104xU/7; chip with bumps on tape.

For further details see Chapter 18.

3.2 Available types

- PCF2104CU/x: character set 'C' in CGROM
- PCF2104LU/x: character set 'L' in CGROM
- PCF2104NU/x: character set 'N' in CGROM.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF2104CU/2	–	chip with bumps in tray	–
PCF2104CU/7	–	chip with bumps on tape	–
PCF2104LU/2	–	chip with bumps in tray	–
PCF2104LU/7	–	chip with bumps on tape	–
PCF2104NU/2	–	chip with bumps in tray	–
PCF2104NU/7	–	chip with bumps on tape	–

5 BLOCK DIAGRAM

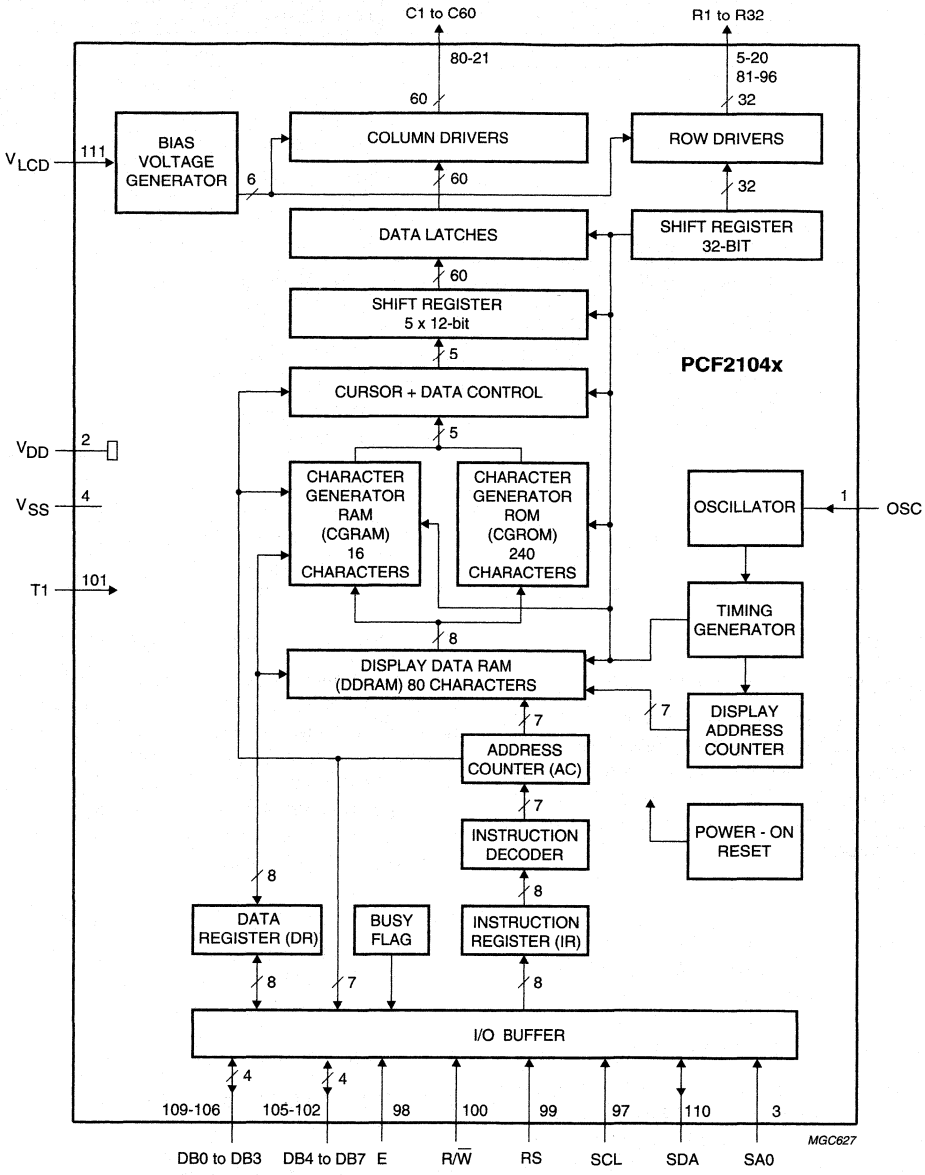


Fig.1 Block diagram.

6 PINNING

SYMBOL	FFC PAD	TYPE	DESCRIPTION
OSC	1	I	oscillator/external clock input
V_{DD}	2	P	logic supply voltage
SA0	3	I	I²C-bus address pin input
V_{SS}	4	P	ground
R8 to R5	5 to 8	O	LCD row driver outputs
R32 to R29	9 to12	O	LCD row driver outputs
R24 to R17	13 to 20	O	LCD row driver outputs
C60 to C1	21 to 80	O	LCD column driver outputs
R9 to R16	81 to 88	O	LCD row driver outputs
R25 to R28	89 to 92	O	LCD row driver outputs
R1 to R4	93 to 96	O	LCD row driver outputs
SCL	97	I	I²C-bus serial clock input
E	98	I	data bus clock input
RS	99	I	register select input
R/$\overline{W}$	100	I	read/write input
T1	101	I	test pad input
DB7 to DB0	102 to 109	I/O	8-bit bidirectional data bus input/output
SDA	110	I/O	I²C-bus serial data input/output
V_{LCD}	111	I	LCD supply voltage input

7 PIN FUNCTIONS

7.1 RS: register select (parallel control)

RS selects the register to be accessed for read and write when the device is controlled by the parallel interface. RS = logic 0 selects the instruction register for write and the Busy Flag and Address Counter for read. RS = logic 1 selects the data register for both read and write. There is an internal pull-up on pin RS.

7.2 R/$\overline{W}$: read/write (parallel control)

R/$\overline{W}$ selects either the read (R/$\overline{W}$ = logic 1) or write (R/$\overline{W}$ = logic 0) operation when control is by the parallel interface. There is an internal pull-up on this pin.

7.3 E: data bus clock (parallel control)

The E pin is set HIGH to signal the start of a read or write operation when the device is controlled by the parallel interface. Data is clocked in or out of the chip on the negative edge of the clock. Note that this pin must be tied to logic 0 (V_{SS}) when I²C-bus control is used.

7.4 DB0 to DB7: data bus (parallel control)

The bidirectional, 3-state data bus transfers data between the system controller and the PCF2104x. DB7 may be used as the Busy Flag, signalling that internal operations are not yet completed. In 4-bit operations the 4 higher order lines DB4 to DB7 are used; DB0 to DB3 must be left open circuit. There is an internal pull-up on each of the data lines. Note that these pins must be left open circuit when I²C-bus control is used.

7.5 C1 to C60: column driver outputs

These pins output the data for pairs of columns. This arrangement permits optimized chip-on-glass (COG) layout for 4-line by 12 characters.

7.6 R1 to R32: row driver outputs

These pins output the row select waveforms to the left and right halves of the display.

7.7 V_{LCD}: LCD power supply

Negative power supply for the liquid crystal display.

7.8 OSC: oscillator

When the on-chip oscillator is used, this pin must be connected to V_{DD}. An external clock signal, if used, is input at this pin.

7.9 SCL: serial clock line

Input for the I^2C-bus clock signal.

7.10 SDA: serial data line

Input/output for the I^2C-bus data line.

7.11 SA0: address pin

The hardware sub-address line is used to program the device sub-address for 2 different PCF2104xs on the same I^2C-bus.

7.12 T1: test pad

Must be connected to V_{SS}. Not user accessible.

8 FUNCTIONAL DESCRIPTION (see Fig.1)

8.1 LCD bias voltage generator

The intermediate bias voltages for the LCD display are also generated on-chip. This removes the need for an external resistive bias chain and significantly reduces the system power consumption. The optimum levels depend on the multiplex rate and are selected automatically when the number of lines in the display is defined.

The optimum value of V_{OP} depends on the multiplex rate, the LCD threshold voltage (V_{th}) and the number of bias levels. The relationships are given in Table 1.

Using a 5-level bias scheme for 1 : 16 MUX rate allows $V_{OP} < 5$ V for most LCD liquids. The effect on the display contrast is negligible.

Table 1 Optimum values for V_{OP}

MUX RATE	NUMBER OF BIAS LEVELS	V_{OP}/V_{th}	DISCRIMINATION V_{on}/V_{off}
1 : 16	5	3.67	1.277
1 : 32	6	5.19	1.196

8.2 Oscillator

The on-chip oscillator provides the clock signal for the display system. No external components are required. Pin OSC must be connected to V_{DD}.

8.3 External clock

If an external clock is to be used, it must be input at pin OSC. The resulting display frame frequency is given by $f_{frame} = {}^1/_{2304} f_{osc}$. A clock signal must always be present, otherwise the LCD may be frozen in a DC state.

8.4 Power-on reset

The Power-on reset block initializes the chip after power-on or power failure.

8.5 Registers

The PCF2104x has two 8-bit registers, an instruction register (IR) and a data register (DR). The register select signal (RS) determines which register will be accessed.

The instruction register stores instruction codes such as display clear and cursor shift, and address information for the Display Data RAM (DDRAM) and Character Generator RAM (CGRAM). The instruction register can be written to, but not read from, by the system controller.

The data register temporarily stores data to be read from the DDRAM and CGRAM. When reading, data from the DDRAM or CGRAM (corresponding to the address in the Address Counter) is written to the data register prior to being read by the 'Read data' instruction.

8.6 Busy Flag

The Busy Flag indicates the free/busy status of the PCF2104x. Logic 1 indicates that the chip is busy and further instructions will not be accepted. The Busy Flag is output at pin DB7 when RS = logic 0 and R/$\overline{W}$ = logic 1. Instructions should only be written after checking that the Busy Flag is at logic 0 or waiting for the required number of clock cycles.

8.7 Address Counter (AC)

The Address Counter assigns addresses to the DDRAM and CGRAM for reading and writing and is set by the instructions 'Set CGRAM address' and 'Set DDRAM address'. After a read/write operation the Address Counter is automatically incremented or decremented by 1. The Address Counter contents are output to the bus (DB0 to DB6) when RS = logic 0 and R/$\overline{W}$ = logic 1.

8.8 Display data RAM (DDRAM)

The DDRAM stores up to 80 characters of display data, represented by 8-bit character codes. DDRAM locations not used for storing display data can be used as general purpose RAM. The basic DDRAM-to-display mapping scheme is shown in Fig.2. With no display shift, the characters represented by the codes in the first 12 or 24 RAM locations, starting at address 00 in line 1, are displayed. Subsequent lines display data starting at addresses 20, 40, or 60 Hex. Figures 3 and 4 show the DDRAM-to-display mapping scheme when the display is shifted.

The address range for a 1-line display is 00 to 4F; for a 2-line display from 00 to 27 (line 1) and 40 to 67 (line 2); for a 4-line display from 00 to 13, 20 to 33, 40 to 53 and 60 to 73 for lines 1, 2, 3 and 4 respectively. For 2 and 4-line displays the end address of one line and the start address of the next line are not consecutive. When the display is shifted each line wraps around independently of the others (see Figs 3 and 4).

When data is written to the DDRAM wrap-around occurs from 4F to 00 in 1-line mode and from 27 to 40 and 67 to 00 in 2-line mode; from 13 to 20, 33 to 40, 53 to 60 and 73 to 00 in 4-line mode.

8.9 Character generator ROM (CGROM)

The character generator ROM generates 240 character patterns in 5 × 8 dot format from 8-bit character codes. Figures 5 and 6 show the character sets currently available.

8.10 Character generator RAM (CGRAM)

Up to 16 user-defined characters may be stored in the character generator RAM. The CGROM and CGRAM use a common address space, of which the first column is reserved for the CGRAM (see Fig.5). Figure 8 shows the addressing principle for the CGRAM.

8.11 Cursor control circuit

The cursor control circuit generates the cursor (underline and/or character blink as shown in Fig.9) at the DDRAM address contained in the Address Counter. When the Address Counter contains the CGRAM address the cursor will be inhibited.

8.12 Timing generator

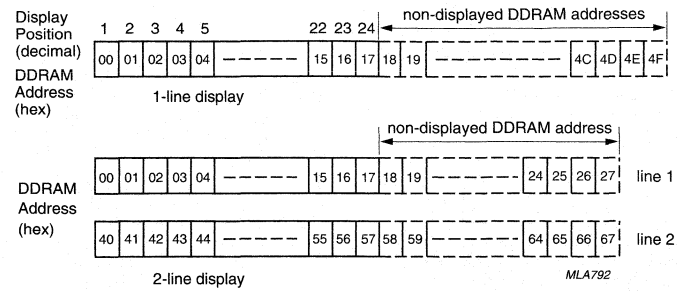
The timing generator produces the various signals required to drive the internal circuitry. Internal chip operation is not disturbed by operations on the data buses.

8.13 LCD row and column drivers

The PCF2104x contains 32 row and 60 column drivers, which connect the appropriate LCD bias voltages in sequence to the display, in accordance with the data to be displayed. The bias voltages and the timing are selected automatically when the number of lines in the display is selected. Figures 10 and 11 show typical waveforms.

In the 1-line mode (1 : 16) the row outputs are driven in pairs: R1/R17, R2/R18 for example. This allows the output pairs to be connected in parallel, thereby providing greater drive capability.

Unused outputs should be left unconnected.



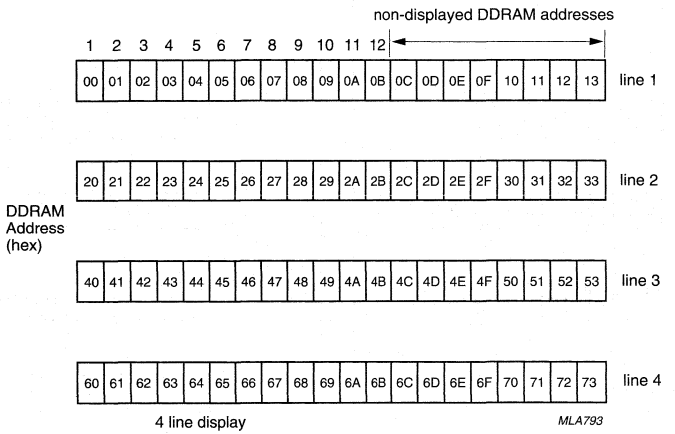
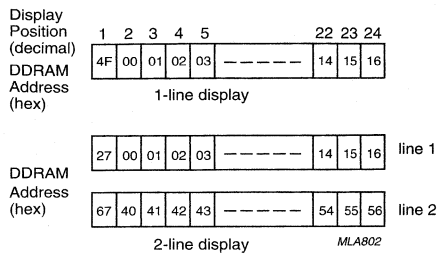


Fig.2 DDRAM-to-display mapping; no shift (PCF2104x).



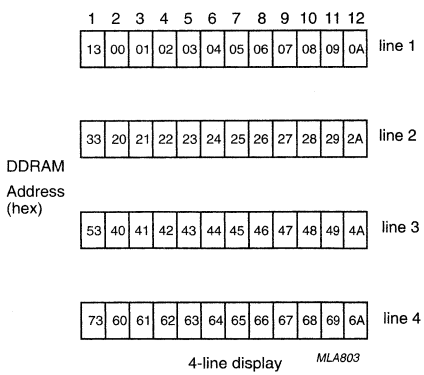
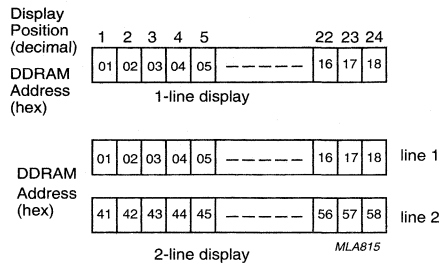


Fig.3 DDRAM-to-display mapping; right shift (PCF2104x).



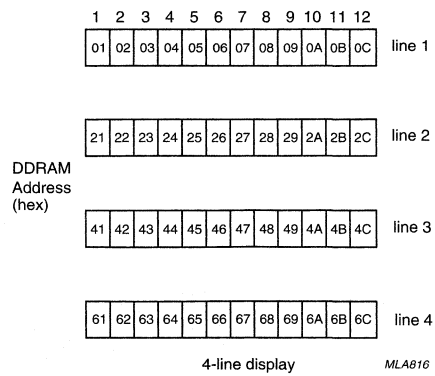


Fig.4 DDRAM-to-display mapping; left shift (PCF2104x).

lower 4 bits \ upper 4 bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
xxxx 0000	CG RAM 1															
xxxx 0001	2															
xxxx 0010	3															
xxxx 0011	4															
xxxx 0100	5															
xxxx 0101	6															
xxxx 0110	7															
xxxx 0111	8															
xxxx 1000	9															
xxxx 1001	10															
xxxx 1010	11															
xxxx 1011	12															
xxxx 1100	13															
xxxx 1101	14															
xxxx 1110	15															
xxxx 1111	16															

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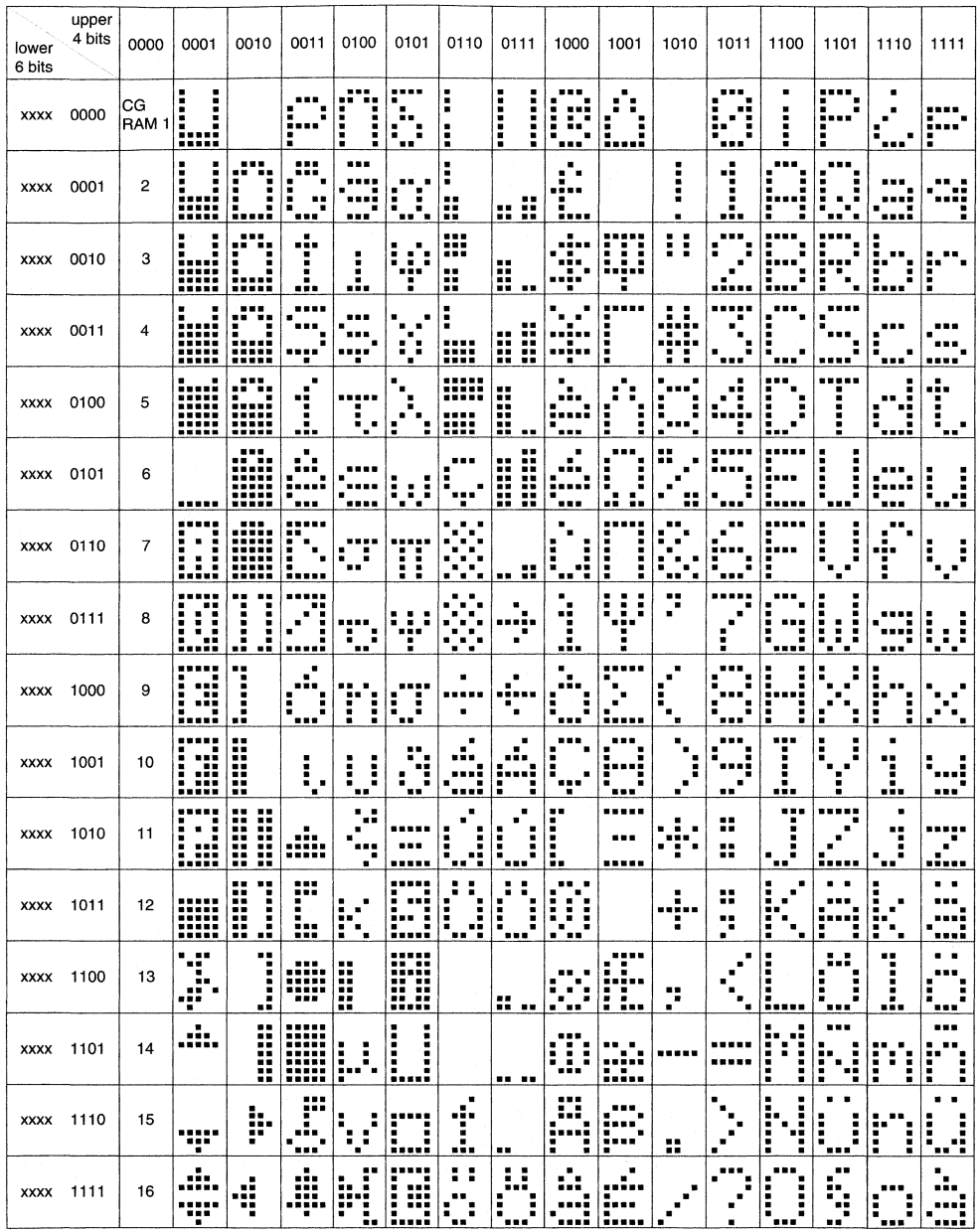
Fig.5 Character set 'C' in CGROM; **PCF2104C**.

lower 6 bits / upper 4 bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
xxxx 0000	CG RAM 1															
xxxx 0001	2															
xxxx 0010	3															
xxxx 0011	4															
xxxx 0100	5															
xxxx 0101	6															
xxxx 0110	7															
xxxx 0111	8															
xxxx 1000	9															
xxxx 1001	10															
xxxx 1010	11															
xxxx 1011	12															
xxxx 1100	13															
xxxx 1101	14															
xxxx 1110	15															
xxxx 1111	16															



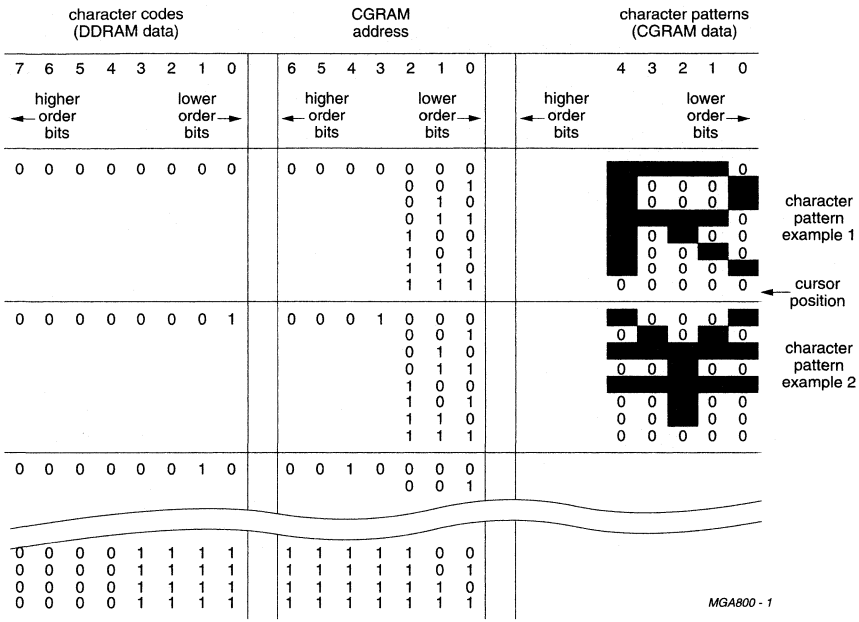
MGC629

Fig.6 Character set 'L' in CGROM; **PCF2104L**.

lower 4 bits \ upper 4 bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
xxxx 0000	CG RAM 1															
xxxx 0001	2															
xxxx 0010	3															
xxxx 0011	4															
xxxx 0100	5															
xxxx 0101	6															
xxxx 0110	7															
xxxx 0111	8															
xxxx 1000	9															
xxxx 1001	10															
xxxx 1010	11															
xxxx 1011	12															
xxxx 1100	13															
xxxx 1101	14															
xxxx 1110	15															
xxxx 1111	16															

MGM134

Fig.7 Character set 'N' in CGROM; **PCF2104N**.



Character code bits 0 to 3 correspond to CGRAM address bits 3 to 6.

CGRAM address bits 0 to 2 designate character pattern line position. The 8th line is the cursor position and display is performed by logical OR with the cursor. Data in the 8th line will appear in the cursor position.

Character pattern column positions correspond to CGRAM data bits 0 to 4; bit 4 being at the left end, as shown in the figure.

CGRAM character patterns are selected when character code bits 4 to 7 are all logic 0. CGRAM data = logic 1 corresponds to selection for display.

Only bits 0 to 5 of the CGRAM address are set by the 'Set CGRAM address' instruction. Bit 6 can be set using the 'Set DDRAM address' instruction or by using the auto-increment feature during CGRAM write. All bits 0 to 6 can be read using the 'Read Busy Flag and address' instruction.

Fig.8 Relationship between CGRAM addresses, data and display patterns.

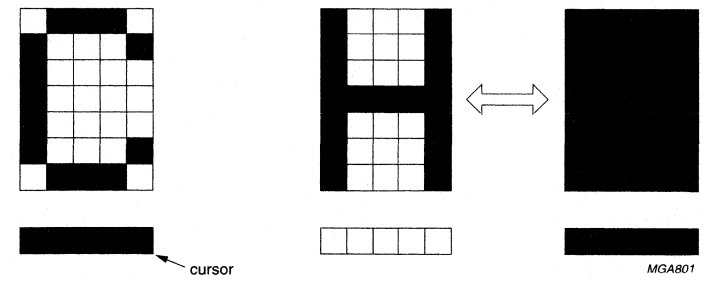


Fig.9 Cursor and blink display examples.

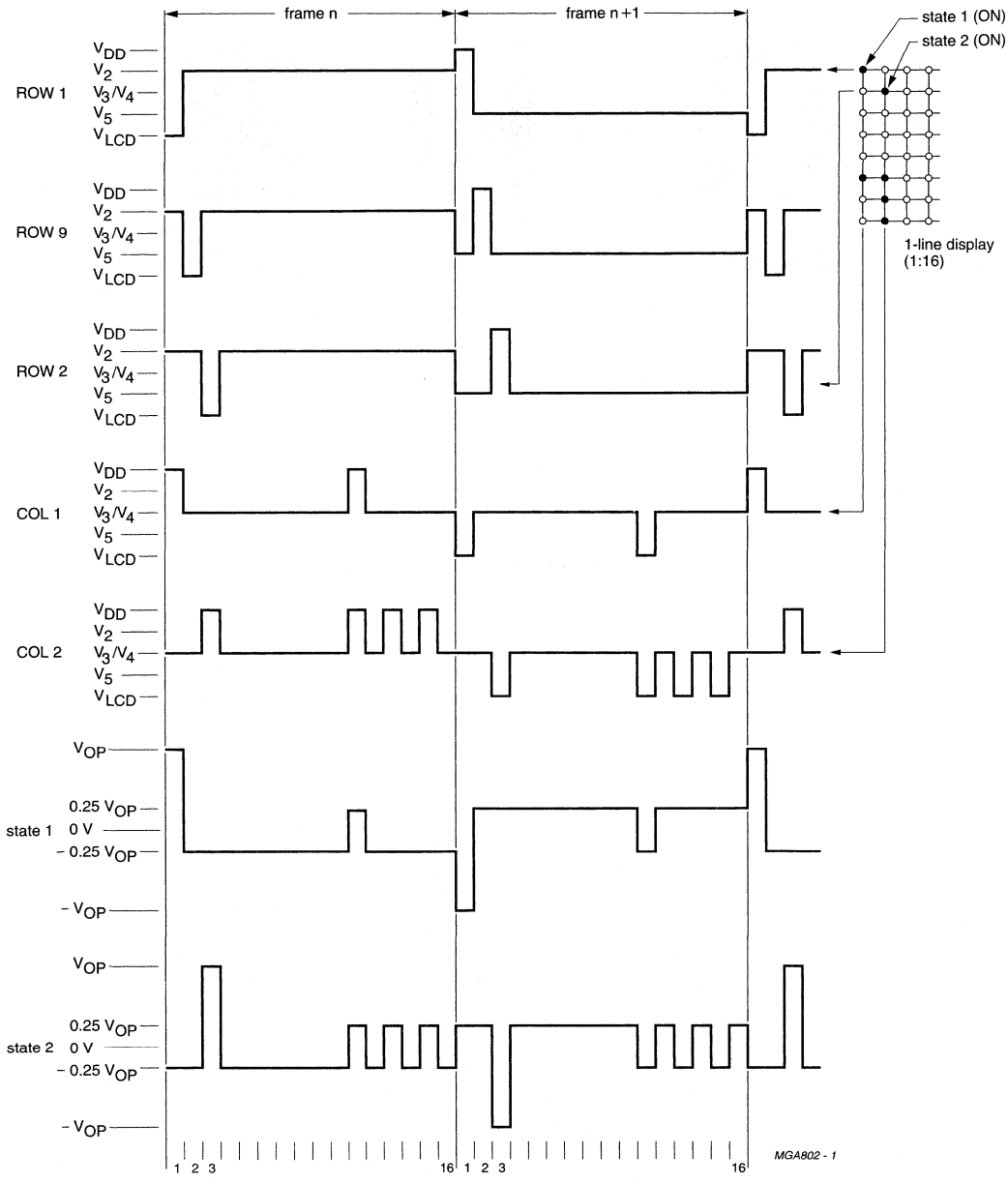


Fig.10 Typical LCD waveforms; 1-line mode.

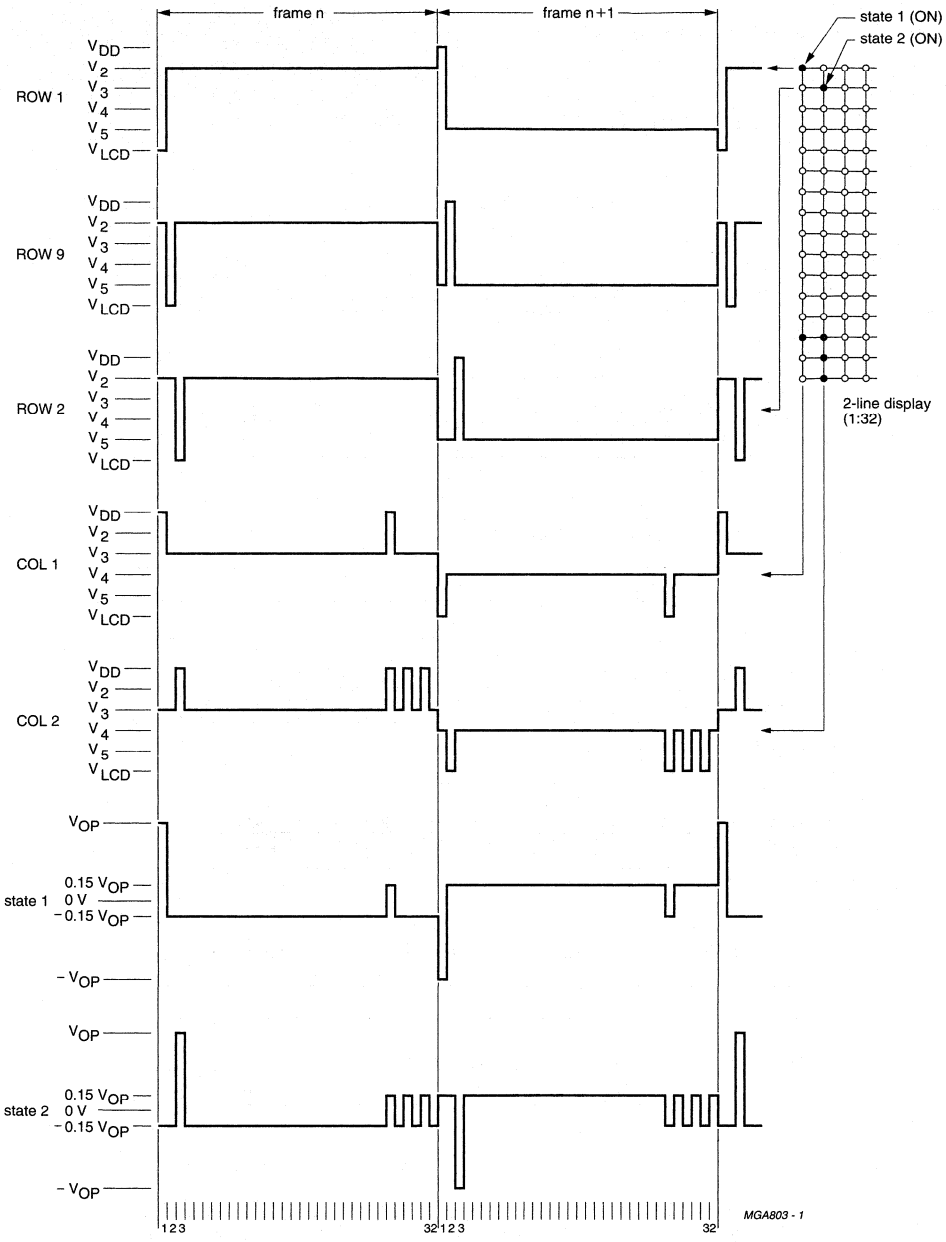


Fig.11 Typical LCD waveforms; 2-line mode.

8.14 Programming of MUX 1 : 16 displays with PCF2104x

The PCF2104x can be used in the following ways:

- 1-line mode to drive a 2-line display
- 2 × 12 characters with MUX rate 1 : 16, resulting in better contrast. The internal data flow of the chip is optimized for this purpose.

Using the 'Function set' instruction, M and N are set to 0, 0 (respectively). Figures 12, 13 and 14 show the DDRAM addresses of the display characters. The second row of each table corresponds to either the right half of a 1-line display or to the second line of a 2-line display. Wrap around of data during display shift or when writing data is non-standard.

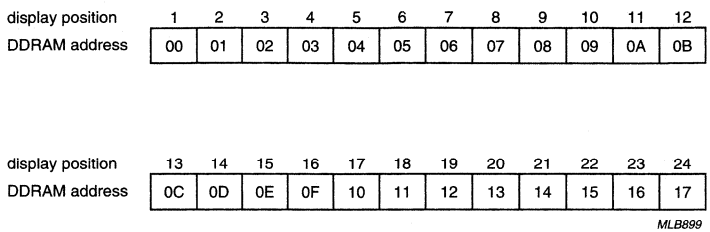


Fig.12 DDRAM-to-display mapping; no shift (PCF2104x).

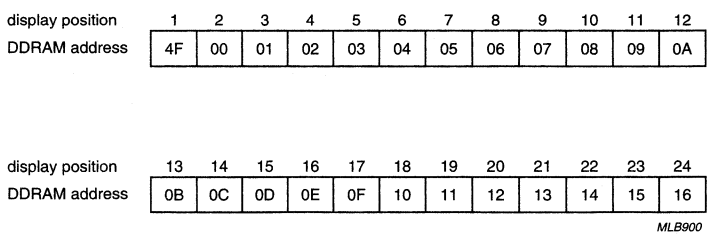


Fig.13 DDRAM-to-display mapping; right shift (PCF2104x).

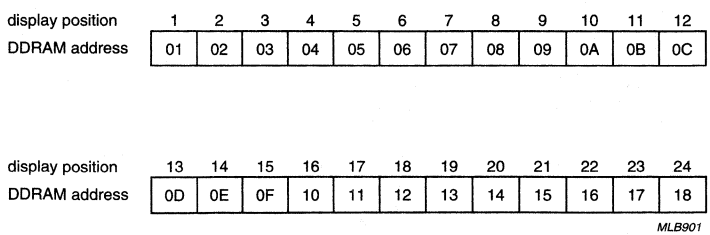


Fig.14 DDRAM-to-display mapping; left shift (PCF2104x).

8.15 Programming of MUX 1 : 32 displays with PCF2104x

To drive a 2-line by 24 characters MUX 1 : 32 display, use instruction 'Function set' to set M, N to 0, 1 (respectively).

To drive a 4-line by 12 characters MUX 1:32 display, use instruction 'Function set' to set M, N to 1, 1 (respectively).

8.16 Reset function

The PCF2104 automatically initializes (resets) when power is turned on. The state after reset is given in Table 2.

Table 2 State after reset

STEP	DESCRIPTION
1	Display clear.
2	Function set: DL = 1: 8-bit interface M, N = 0 1-line display G = 0: not used
3	Display on/off control: D = 0: display off C = 0: cursor off; B = 0: blink off;
4	Entry mode set: I/D = 1: +1 (increment) G = 0: not used
5	Default address pointer to DDRAM. The Busy Flag (BF) indicates the busy state (BF = logic 1) until initialization ends. The busy state lasts 2 ms. The chip may also be initialized by software. See Tables 10 and 11.
6	I^2C-bus interface reset.

9 INSTRUCTIONS

Only two PCF2104x registers, the instruction register (IR) and the data register (DR) can be directly controlled by the microcontroller. Before internal operation, control information is stored temporarily in these registers to allow interface to various types of microcontrollers which operate at different speeds or to allow interfacing to peripheral control ICs.
The PCF2104x operation is controlled by the instructions shown in Table 3 together with their execution time. Details are explained in subsequent sections.

Instructions are of 4 categories, those that:

1. Designate PCF2104x functions such as display format, data length, etc.
2. Set internal RAM addresses
3. Perform data transfer with internal RAM
4. Others.

In normal use, category 3 instructions are used most frequently. However, automatic incrementing by 1 (or decrementing by 1) of internal RAM addresses after each data write lessens the microcontroller program load. The display shift in particular can be performed concurrently with display data write, thus enabling the designer to develop systems in minimum time with maximum programming efficiency.

During internal operation, no instruction other than the Busy Flag/address read instruction will be executed.

Because the Busy Flag is set to logic 1 while an instruction is being executed, it is advisable to ensure that the flag it is at logic 0 before sending the next instruction or wait for the maximum instruction execution time, as given in Table 3. An instruction sent while the Busy Flag is HIGH will not be executed.

Table 3 Instructions (note 1)

INSTRUCTION	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DESCRIPTION	REQUIRED CLOCK CYCLES(2)
NOP	0	0	0	0	0	0	0	0	0	0	No operation.	0
Clear display	0	0	0	0	0	0	0	0	0	1	Clears entire display and sets DDRAM address 0 in Address Counter.	165
Return home	0	0	0	0	0	0	0	0	1	0	Sets DDRAM address 0 in Address Counter Also returns shifted display to original position DDRAM contents remain unchanged.	3
Entry mode set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies shift of display. These operations are performed during data write and read.	3
Display control	0	0	0	0	0	0	1	D	C	B	Sets entire display on/off (D), cursor on/off (C) and blink of cursor position character (B).	3
Cursor/display shift	0	0	0	0	0	1	S/C	R/L	0	0	Moves cursor and shifts display without changing DDRAM contents.	3
Function set	0	0	0	0	1	DL	N	M	G	0	Sets interface data length (DL), number of display lines (N, M) and voltage generator control (G).	3
Set CGRAM address	0	0	0	1	A_{CG}						Sets CGRAM address.	3
Set DDRAM address	0	0	1	A_{DD}							Sets DDRAM address.	3
Read busy flag and address	0	1	BF	A_C							Reads Busy Flag (BF) indicating internal operation is being performed and reads Address Counter contents.	0
Read data	1	1	read data								Reads data from CGRAM or DDRAM.	3
Write data	1	0	write data								Writes data to CGRAM or DDRAM.	3

Notes

1. In the I²C-bus mode the DL bit is don't care. 8-bit mode is assumed.
   In the I²C-bus mode a control byte is required when RS or R/$\overline{W}$ is changed; control byte: Co, RS, R/$\overline{W}$, 0, 0, 0, 0, 0; command byte: DB7 to DB0.
2. Example: f_{osc} = 150 kHz, $T_{cy} = \frac{1}{f_{osc}}$ = 6.67 µs ; 3 cycles = 20 µs, 165 cycles = 1.1 ms.

Table 4 Command bit identities

BIT	LOGIC 0	LOGIC 1
I/D	decrement	increment
S	display freeze	display shift
D	display off	display on
C	cursor off	cursor on
B	character at cursor position does not blink	character at cursor position blinks
S/C	cursor move	display shift
R/L	left shift	right shift
DL	4 bits	8 bits
N (M = 0)	2 line × 12 characters; MUX 1 : 16	2 lines × 24 characters; MUX 1 : 32
N (M = 1)	reserved	4 lines × 12 characters; MUX 1 : 32
BF	end of internal operation	internal operation in progress
Co	last control byte, only data bytes to follow	next two bytes are a data byte and another control byte

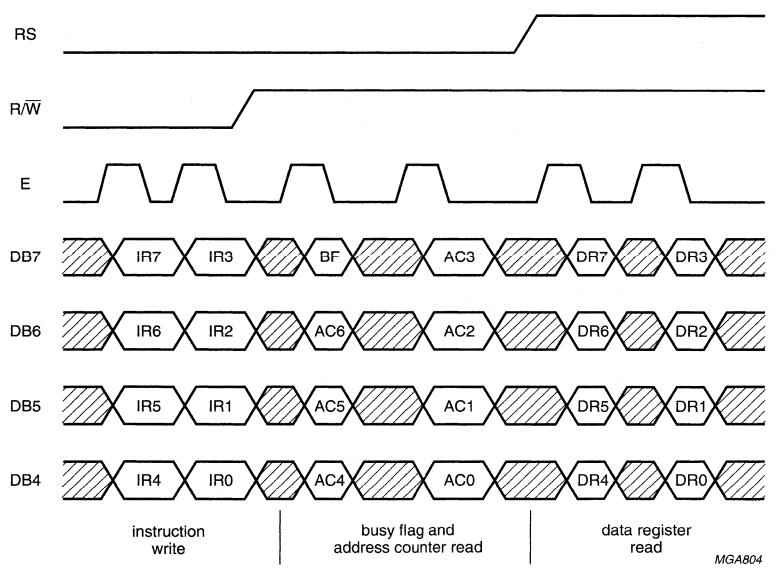
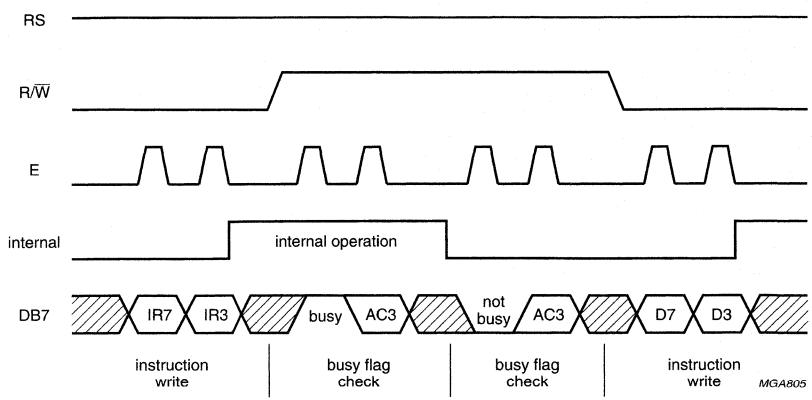


Fig.15 4-bit transfer example.



IR7, IR3: instruction 7th bit, 3rd bit.
AC3: Address Counter 3rd bit.

Fig.16 An example of 4-bit data transfer timing sequence.

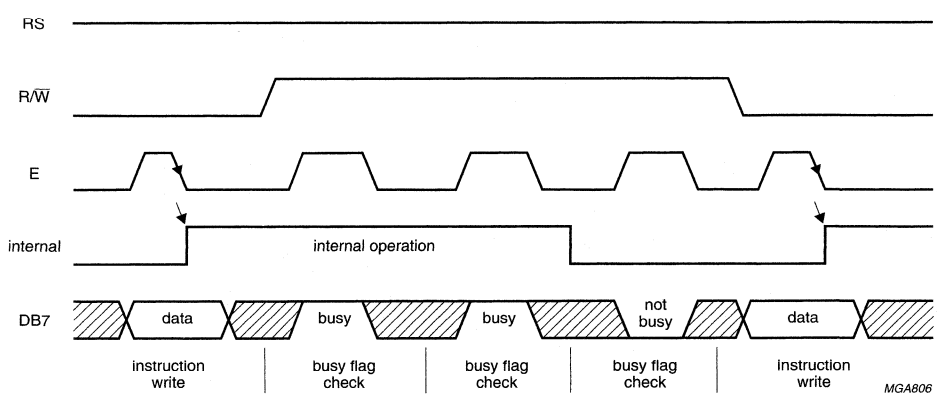


Fig.17 Example of Busy Flag check timing sequence.

9.1 Clear display

'Clear display' writes space code 20 (hexadecimal) into all DDRAM addresses (the character pattern for character code 20 must be a blank pattern), sets the DDRAM Address Counter to logic 0 and returns the display to its original position if it was shifted. Consequently, the display disappears and the cursor or blink position goes to the left edge of the display (the first line if 2 or 4 lines are displayed) and sets the entry mode to I/D = logic 1 (increment mode). S of entry mode does not change.

The instruction 'Clear display' requires extra execution time. This may be allowed for by checking the Busy Flag (BF) or by waiting until 2 ms has elapsed. The latter must be applied where no read-back options are foreseen, as in some chip-on-glass (COG) applications.

9.2 Return home

'Return home' sets the DDRAM Address Counter to logic 0 and returns the display to its original position if it was shifted. DDRAM contents do not change. The cursor or blink position goes to the left of the display (the first line if 2 or 4 lines are displayed). I/D and S of entry mode do not change.

9.3 Entry mode set

9.3.1 I/D

When I/D = logic 1 (0) the DDRAM or CGRAM address increments (decrements) by 1 when data is written to or read from the DDRAM or CGRAM. The cursor or blink position moves to the right when incremented and to the left when decremented. The cursor and blink are inhibited when the CGRAM is accessed.

9.3.2 S

When S = logic 1, the entire display shifts either to the right (I/D = logic 0) or to the left (I/D = logic 1) during a DDRAM write. Consequently, it looks as if the cursor stands still and the display moves. The display does not shift when reading from the DDRAM, or when writing to or reading from the CGRAM. When S = logic 0 the display does not shift.

9.4 Display on/off control

9.4.1 D

The display is on when D = logic 1 and off when D = logic 0. Display data in the DDRAM is not affected and can be displayed immediately by setting D to logic 1.

9.4.2 C

The cursor is displayed when C = logic 1 and inhibited when C = logic 0. Even if the cursor disappears, the display functions I/D, etc. remain in operation during display data write. The cursor is displayed using 5 dots in the 8th line (see Fig.9).

9.4.3 B

The character indicated by the cursor blinks when B = logic 1. The blink is displayed by switching between display characters and all dots on with a period of 1 second when f_{osc} = 150 kHz (see Fig.9). At other clock frequencies the blink period is equal to 150 kHz/f_{osc}. The cursor and the blink can be set to display simultaneously.

9.5 Cursor/display shift

'Cursor/display shift' moves the cursor position or the display to the right or left without writing or reading display data. This function is used to correct a character or move the cursor through the display. In 2 or 4-line displays, the cursor moves to the next line when it passes the last position of the line (40 or 20 decimal). When the displayed data is shifted repeatedly all lines shift at the same time; displayed characters do not shift into the next line. The Address Counter (AC) content does not change if the only action performed is shift display, but increments or decrements with the cursor shift.

9.6 Function set

9.6.1 DL (PARALLEL MODE ONLY)

Sets interface data width. Data is sent or received in bytes (DB7 to DB0) when DL = logic 1 or in two nibbles (DB7 to DB4) when DL = logic 0. When 4-bit width is selected, data is transmitted in two cycles using the parallel bus(1).

Function set from I²C-bus interface: DL bit can not bet set to logic 0 from the I²C-bus interface. If bit DL has been set to logic 0 via the parallel bus, programming via the I²C-bus interface is complicated.

9.6.2 N, M

Sets number of display lines.

(1) In a 4-bit application DB3 to DB0 are left open (internal pull-ups). Hence in the first function set instruction after power-on G and H are set to 1. A second function set must then be sent (2 nibbles) to set G and H to their required values.

9.7 Set CGRAM address

'Set CGRAM address' sets bits 0 to 5 of the CGRAM address (A_{CG} in Table 3) into the Address Counter (binary A[5] to A[0]). Data can then be written to or read from the CGRAM.

Only bits 0 to 5 of the CGRAM address are set by the 'Set CGRAM address' instruction. Bit 6 can be set using the 'Set DDRAM address' instruction or by using the auto-increment feature during CGRAM write. All bits 0 to 6 can be read using the 'Read busy flag and address' instruction.

9.8 Set DDRAM address

Set DDRAM address sets the DDRAM address (A_{DD} in Table 3) into the Address Counter (binary A[6] to A[0]). Data can then be written to or read from the DDRAM.

Table 5 Hexadecimal address ranges

ADDRESS	FUNCTION
00 to 4F	1-line by 24
00 to 0B and 0C to 4F	2-line by 12
00 to 27 and 40 to 67	2-line by 24
00 to 13, 20 to 33, 40 to 53 and 60 to 73	4-line by 12

9.9 Read busy flag and address

'Read busy flag and address' reads the Busy Flag (BF). When BF = logic 1 it indicates that an internal operation is in progress. The next instruction will not be executed until BF = logic 0, so BF should be checked before sending another instruction.

At the same time, the value of the Address Counter expressed in binary A[6] to A[0] is read out. The Address Counter is used by both CGRAM and DDRAM and its value is determined by the previous instruction.

9.10 Write data to CGRAM or DDRAM

Writes binary 8-bit data D[7] to D[0] to the CGRAM or the DDRAM.

Whether the CGRAM or DDRAM is to be written to is determined by the previous specification of CGRAM or DDRAM address setting. After writing, the address automatically increments or decrements by 1, in accordance with the entry mode. Only bits D0 to D4 of CGRAM data are valid, bits D5 to D7 are 'don't care'.

9.11 Read data from CGRAM or DDRAM

Reads binary 8-bit data D[7] to D[0] from the CGRAM or DDRAM.

The most recent 'Set address' instruction determines whether the CGRAM or DDRAM is to be read.

The 'Read data' instruction gates the content of the data register (DR) to the bus while E = HIGH. After E goes LOW again, internal operation increments (or decrements) the AC and stores RAM data corresponding to the new AC into the DR.

Remark: the only three instructions that update the data register (DR) are:

- 'Set CGRAM address'
- 'Set DDRAM address'
- 'Read data' from CGRAM or DDRAM.

Other instructions (e.g. 'Write data, 'Cursor/display shift', 'Clear display', 'Return home') will not modify the data register content.

10 INTERFACE TO MICROCONTROLLER (PARALLEL INTERFACE)

The PCF2104x can send data in either two 4-bit operations or one 8-bit operation and can thus interface to 4-bit or 8-bit microcontrollers.

In the 8-bit mode data is transferred as 8-bit bytes using the 8 data lines DB0 to DB7. Three further control lines E, RS, and R/$\overline{W}$ are required.

In the 4-bit mode data is transferred in two cycles of 4-bits each. The higher order bits (corresponding to DB4 to DB7 in 8-bit mode) are sent in the first cycle and the lower order bits (DB0 to DB3 in 8-bit mode) in the second cycle. Data transfer is complete after two 4-bit data transfers. It should be noted that two cycles are also required for the Busy Flag check. 4-bit operation is selected by instruction. See Figs 15, 16 and 17 for examples of bus protocol.

In the 4-bit mode pins DB3 to DB0 must be left open-circuit. They are pulled up to V_{DD} internally.

11 INTERFACE TO MICROCONTROLLER (I²C-BUS INTERFACE)

11.1 Characteristics of the I²C-bus

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

11.2 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

11.3 Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P).

11.4 System configuration

A device generating a message is a 'transmitter', a device receiving a message is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves'.

11.5 Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

11.6 I²C-bus protocol

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always carried out with the first byte transmitted after the start procedure. The I²C-bus configuration for the different PCF2104x READ and WRITE cycles is illustrated in Figs 22, 23 and 24.

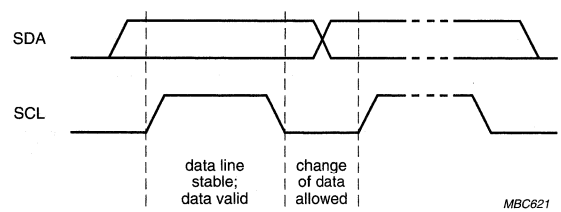


Fig.18 Bit transfer.

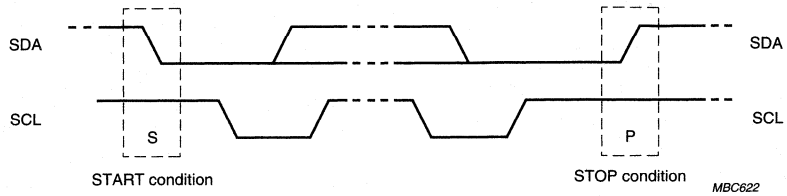


Fig.19 Definition of START and STOP conditions.

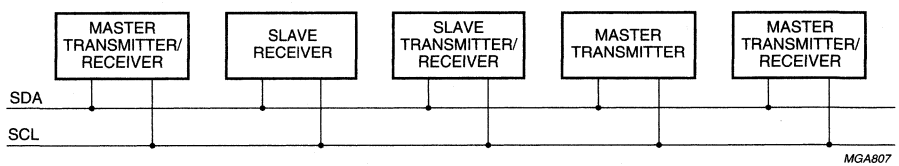


Fig.20 System configuration.

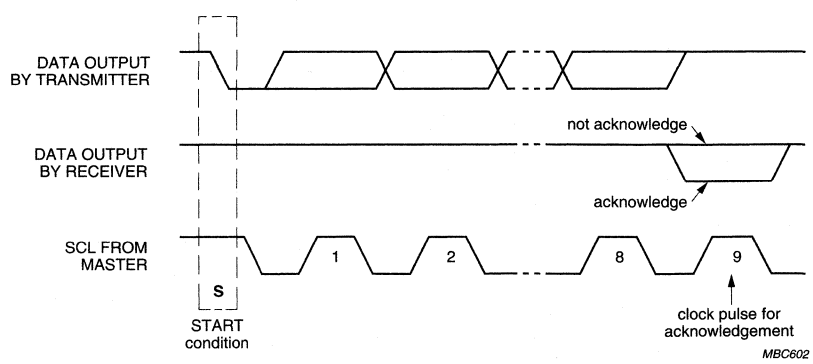


Fig.21 Acknowledgement on the I²C-bus.

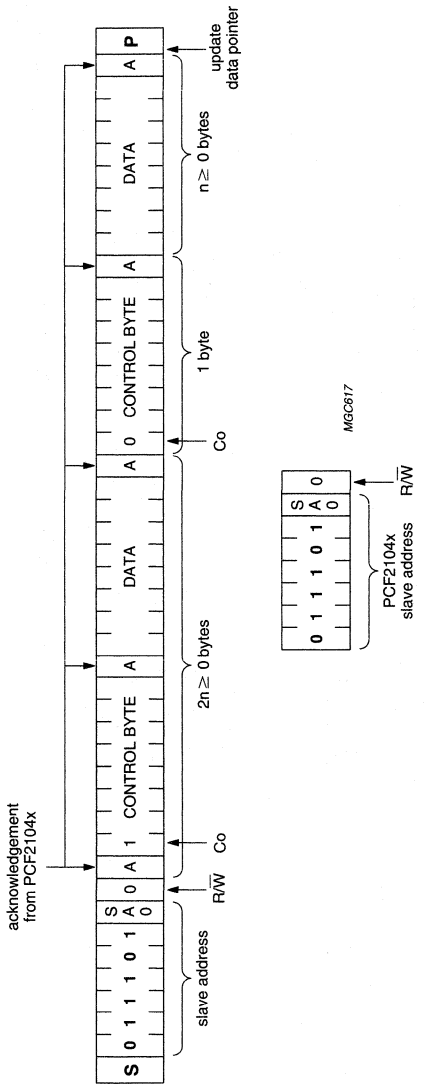


Fig.22 Master transmits to slave receiver; WRITE mode.

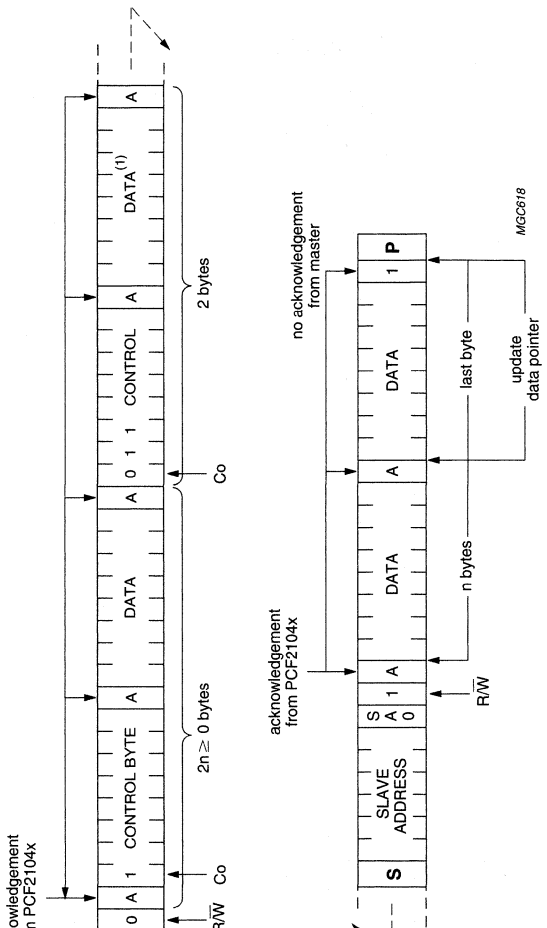


Fig.23 Master reads after setting word address; write word address, set RS/$\overline{RW}$; READ data.

(1) Last data byte is a dummy byte (may be omitted).

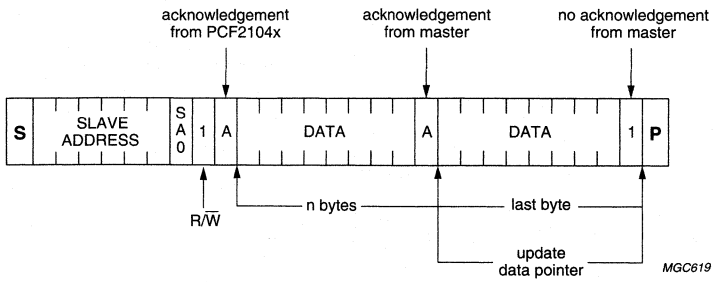


Fig.24 Master reads slave immediately after first byte; READ mode (RS previously defined).

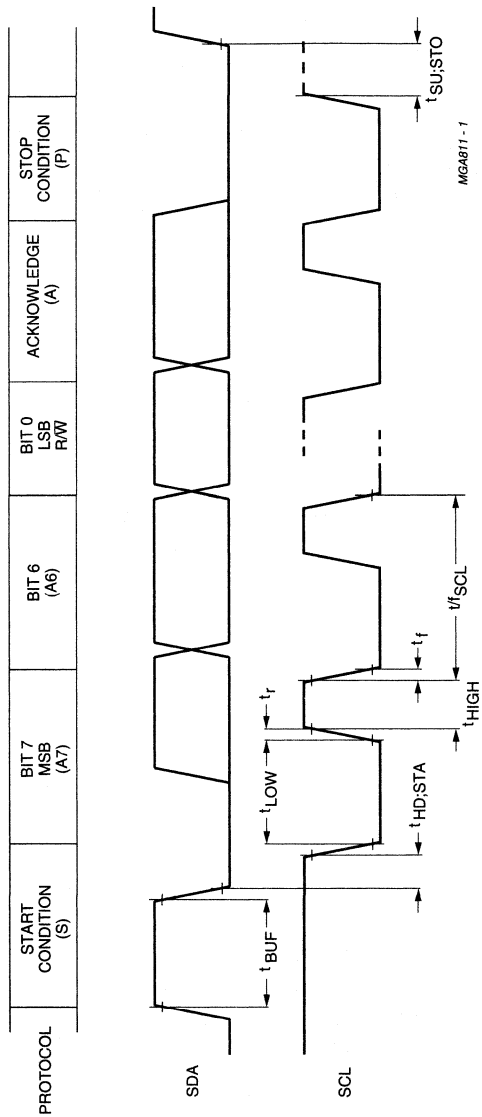


Fig.25 I²C-bus timing diagram; rise and fall times refer to V_{IL} and V_{IH}.

12 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.5	+8.0	V
V_{LCD}	LCD supply voltage	V_{DD} − 11	V_{DD}	V
V_I	input voltage OSC, RS, R/$\overline{W}$, E and DB0 to DB7	V_{SS} − 0.5	V_{DD} + 0.5	V
V_O	output voltage R1 to R32, C1 to C60 and V_{LCD}	V_{LCD} − 0.5	V_{DD} + 0.5	V
I_I	DC input current	−10	+10	mA
I_O	DC output current	−10	+10	mA
I_{DD}, I_{SS}, I_{LCD}	V_{DD}, V_{SS} or V_{LCD} current	−50	+50	mA
P_{tot}	total power dissipation	−	400	mW
P_O	power dissipation per output	−	100	mW
T_{stg}	storage temperature	−65	+150	°C

13 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see *"Handling MOS Devices"*).

14 DC CHARACTERISTICS

V_{DD} = 2.5 to 6 V; V_{SS} = 0 V; V_{LCD} = V_{DD} − 3.5 to V_{DD} − 9 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage		2.5	−	6.0	V
V_{LCD}	LCD supply voltage		V_{DD} − 9	−	V_{DD} − 3.5	V
I_{DD}	supply current external V_{LCD}	note 1	−	−	−	
I_{DD1}	supply current 1		−	200	500	µA
I_{DD2}	supply current 2	V_{DD} = 5 V; V_{OP} = 9 V; f_{osc} = 150 kHz; T_{amb} = 25 °C	−	200	300	µA
I_{DD3}	supply current 3	V_{DD} = 3 V; V_{OP} = 5 V; f_{osc} = 150 kHz; T_{amb} = 25 °C	−	150	200	µA
I_{LCD}	V_{LCD} input current	notes 1 and 6	−	50	100	µA
V_{POR}	Power-on reset voltage level	note 2	−	1.3	1.8	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Logic						
V_{IL1}	LOW level input voltage pins E, RS, R/$\overline{W}$, DB0 to DB7 and SA0		V_{SS}	–	$0.3V_{DD}$	V
V_{IH1}	HIGH level input voltage pins E, RS, R/$\overline{W}$, DB0 to DB7 and SA0		$0.7V_{DD}$	–	V_{DD}	V
$V_{IL(osc)}$	LOW level input voltage pin OSC		V_{SS}	–	$V_{DD} - 1.5$	V
$V_{IH(osc)}$	HIGH level input voltage pin OSC		$V_{DD} - 0.1$	–	V_{DD}	V
I_{pu}	pull-up current at pins DB0 to DB7, RS and R/$\overline{W}$	$V_I = V_{SS}$	0.04	0.15	1.00	µA
$I_{OL(DB)}$	LOW level output current pins DB0 to DB7	V_{OL} = 0.4 V; V_{DD} = 5 V	1.6	–	–	mA
$I_{OH(DB)}$	HIGH level output current pins DB0 to DB7	V_{OH} = 4 V; V_{DD} = 5 V	−1.0	–	–	mA
I_{L1}	leakage current pins OSC, E, RS, R/$\overline{W}$, DB0 to DB7 and SA0	$V_I = V_{DD}$ or V_{SS}	−1	–	+1	µA
I²C-bus						
SDA, SCL						
V_{IL2}	LOW level input voltage	note 3	V_{SS}	–	$0.3V_{DD}$	V
V_{IH2}	HIGH level input voltage	note 3	$0.7V_{DD}$	–	V_{DD}	V
I_{L2}	leakage current	$V_I = V_{DD}$ or V_{SS}	−1	–	+1	µA
C_i	input capacitance	note 4	–	–	7	pF
$I_{OL(SDA)}$	LOW level output current (SDA)	V_{OL} = 0.4 V; V_{DD} = 5 V	3	–	–	mA
LCD outputs						
R_{ROW}	row output resistance pins R1 to R32	note 5	–	1.5	3	kΩ
R_{COL}	column output resistance pins C1 to C60	note 5	–	3	6	kΩ
V_{tol1}	bias voltage tolerance pins R1 to R32 and C1 to C60	note 6	–	±20	±130	mV

Notes

1. LCD outputs are open-circuit; inputs at V_{DD} or V_{SS}; $V_0 = V_{DD}$; bus inactive; internal or external clock with duty cycle 50% (I_{DD1} only).
2. Resets all logic when $V_{DD} < V_{POR}$.
3. When the voltages are above or below the supply voltages V_{DD} or V_{SS}, an input current may flow; this current must not exceed ±0.5 mA.
4. Tested on sample basis.
5. Resistance of output terminals (R1 to R32 and C1 to C60) with load current I_{load} = 150 µA; $V_{OP} = V_{DD} - V_{LCD}$ = 9 V; outputs measured one at a time.
6. LCD outputs open-circuit.

15 AC CHARACTERISTICS

V_{DD} = 2.5 to 6.0 V; V_{SS} = 0 V; V_{LCD} = V_{DD} − 3.5 V to V_{DD} − 9 V; T_{amb} = −40 °C to + 85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{FR}	LCD frame frequency (internal clock)	note 1	40	65	100	Hz
f_{osc}	external clock frequency		90	150	225	kHz
Bus timing characteristics: Parallel Interface; notes 1 and 2						
WRITE OPERATION (WRITING DATA FROM MICROCONTROLLER TO PCF2104x)						
T_{cy}	enable cycle time		500	–	–	ns
PW_{EH}	enable pulse width		220	–	–	ns
t_{ASU}	address set-up time		50	–	–	ns
t_{AH}	address hold time		25	–	–	ns
t_{DSW}	data set-up time		60	–	–	ns
t_{HD}	data hold time		25	–	–	ns
READ OPERATION (READING DATA FROM PCF2104x TO MICROCONTROLLER)						
T_{cy}	enable cycle time		500	–	–	ns
PW_{EH}	enable pulse width		220	–	–	ns
t_{ASU}	address set-up time		50	–	–	ns
t_{AH}	address hold time		25	–	–	ns
t_{DHD}	data delay time		–	–	150	ns
t_{HD}	data hold time		20	–	100	ns
Timing characteristics: I^2C-bus interface; note 2						
f_{SCL}	SCL clock frequency		–	–	100	kHz
t_{SW}	tolerable spike width on bus		–	–	100	ns
t_{BUF}	bus free time		4.7	–	–	µs
$t_{SU;STA}$	set-up time for a repeated START condition		4.7	–	–	µs
$t_{HD;STA}$	start condition hold time		4	–	–	µs
t_{LOW}	SCL LOW time		4.7	–	–	µs
t_{HIGH}	SCL HIGH time		4	–	–	µs
t_r	SCL and SDA rise time		–	–	1	µs
t_f	SCL and SDA fall time		–	–	0.3	µs
$t_{SU;DAT}$	data set-up time		250	–	–	ns
$t_{HD;DAT}$	data hold time		0	–	–	ns
$t_{SU;STO}$	set-up time for STOP condition		4	–	–	µs

Notes

1. V_{DD} = 5.0 V.
2. All timing values are valid within the operating supply voltage and ambient temperature range and are referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

16 TIMING DIAGRAMS

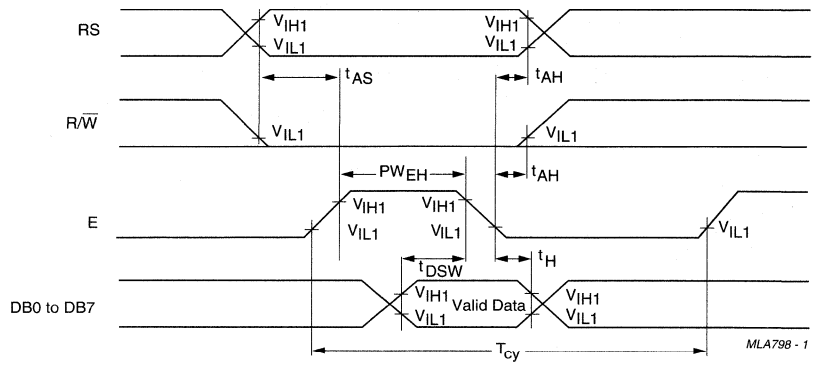


Fig.26 Parallel bus write operation sequence; writing data from microcontroller to PCF2104x.

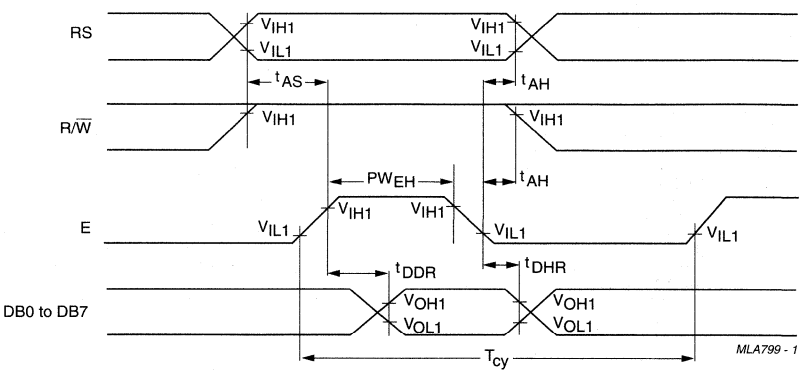


Fig.27 Parallel bus read operation sequence; reading data from PCF2104x to microcontroller.

17 APPLICATION INFORMATION

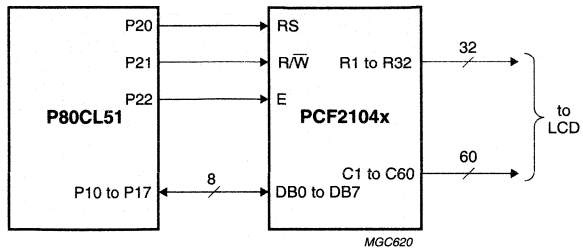


Fig.28 Direct connection to 8-bit microcontroller; 8-bit bus.

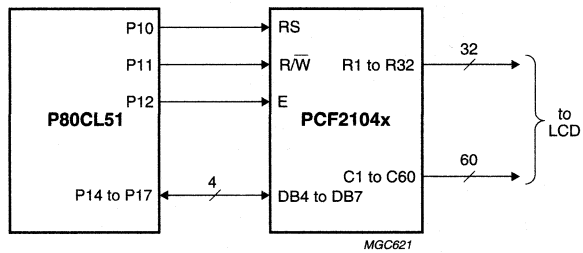


Fig.29 Direct connection to 8-bit microcontroller; 4-bit bus.

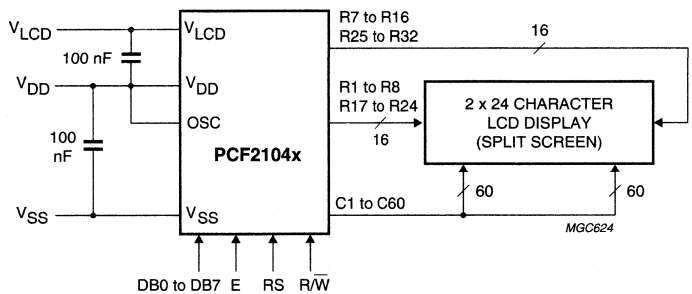


Fig.30 Typical application using parallel interface.

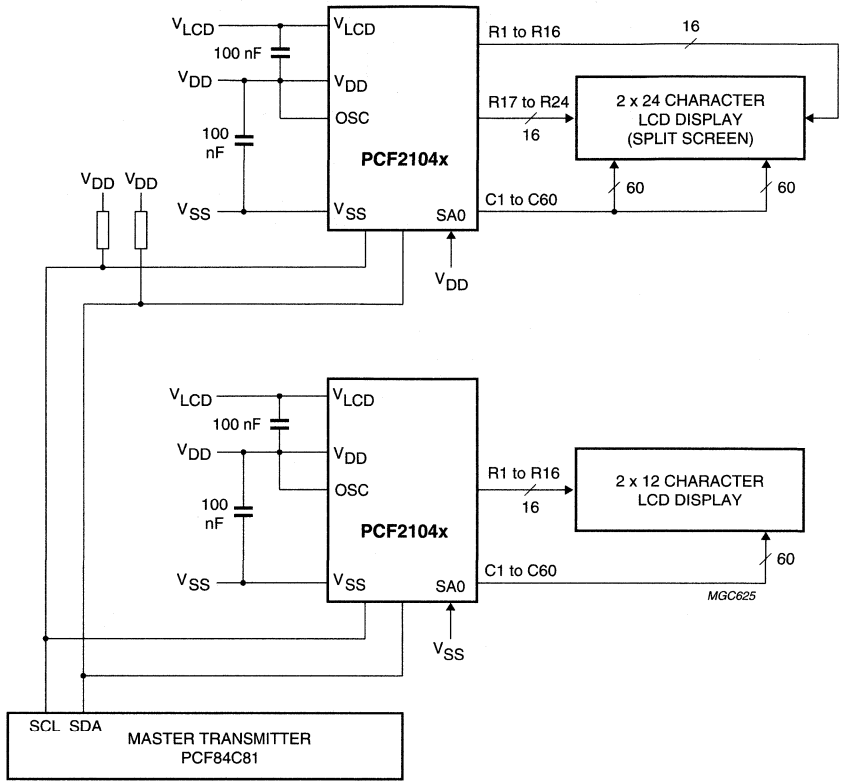


Fig.31 Application using I²C-bus interface.

17.1 8-bit operation, 2 × 12 display using internal reset

Table 7 shows an example of a 1-line display in 8-bit operation. The PCF2104x functions must be set by the function set instruction prior to display. Since the display data RAM can store data for 80 characters, the RAM can be used for advertising displays when combined with display shift operation. Since the display shift operation changes the display position only and DDRAM contents remain unchanged. Display data entered first can be displayed when the 'Return home' instruction is performed.

17.2 4-bit operation, 2 × 12 display using internal reset

The program must set functions prior to 4-bit operation. Table 6 shows an example. When power is turned on, 8-bit operation is automatically selected and the PCF2104x attempts to perform the first write as an 8-bit operation. Since nothing is connected to DB0 to DB3, a rewrite is then required. However, since one operation is completed in two accesses of 4-bit operation, a rewrite is required to set the functions (see Table 6 step 3).

Thus, DB4 to DB7 of the function set are written twice.

17.3 8-bit operation, 2 × 24 display

For a 2-line display, the cursor automatically moves from the first to the second line after the 40th digit of the first line has been written. Thus, if there are only 8 characters in the first line, the DDRAM address must be set after the eighth character is completed (see Table 8). It should be noted that both lines of the display are always shifted together, data does not shift from one line to the other.

17.4 I²C operation, 2 × 12 display

A control byte is required with most instructions (see Table 9).

17.5 Initializing by instruction

If the power supply conditions for correctly operating the internal reset circuit are not met, the PCF2104x must be initialized by instruction. Tables 10 and 11 show how this may be performed for 8-bit and 4-bit operation.

Table 6 4-bit operation, 1-line display example; using internal reset

STEP	INSTRUCTION	DISPLAY	OPERATION
1	Power supply on (PCF2104x is initialized by the internal reset circuit).		Initialized. No display appears.
2	Function set: RS = 0; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 0; DB5 = 1; DB4 = 0		Sets to 4-bit operation. In this instance operation is handled as 8-bits by initialization and only this instruction completes with one write.
3	Function set: RS = 0; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 0; DB5 = 1; DB4 = 0 RS = 0; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 0; DB5 = 0; DB4 = 0		Sets to 4-bit operation, selects 2 × 12 display. 4-bit operation starts from this point and resetting is needed.
4	Display on/off control: RS = 0; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 0; DB5 = 0; DB4 = 0 RS = 0; R/$\overline{W}$ = 0; DB7 = 1; DB6 = 1; DB5 = 1; DB4 = 0		Turns on display and cursor. Entire display is blank after initialization.
5	Entry mode set: RS = 0; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 0; DB5 = 0; DB4 = 0 RS = 0; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 1; DB5 = 1; DB4 = 0	_	Sets mode to increment the address by 1 and to shift the cursor to the right at the time of write to the DD/CGRAM. Display is not shifted.
6	Write data to CGRAM/DDRAM: RS = 1; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 1; DB5 = 0; DB4 = 1 RS = 1; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 1; DB5 = 1; DB4 = 0	**P**_	Writes 'P'. The DDRAM has already been selected by initialization at power-on. The cursor is incremented by 1 and shifted to the right.

Table 7 8-bit operation, 1-line display example; using internal reset (character set 'A')

STEP	INSTRUCTION	DISPLAY	OPERATION
1	Power supply on (PCF2104x is initialized by the internal reset function).		Initialized. No display appears.
2	Function set: RS = 0; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 0; DB5 = 1; DB4 = 1; DB3 = 0; DB2 = 0; DB1 = 0; DB0 = 0		Sets to 8-bit operation, selects 2 × 12 display.
3	Display mode on/off control: RS = 0; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 0; DB5 = 0; DB4 = 0; DB3 = 1; DB2 = 1; DB1 = 1; DB0 = 0	_	Turns on display and cursor. Entire display is blank after initialization.
4	Entry mode set: RS = 0; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 0; DB5 = 0; DB4 = 0; DB3 = 0; DB2 = 1; DB1 = 1; DB0 = 0	_	Sets mode to increment the address by 1 and to shift the cursor to the right at the time of the write to the DD/CGRAM. Display is not shifted.
5	Write data to CGRAM/DDRAM: RS = 1; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 1; DB5 = 0; DB4 = 1; DB3 = 0; DB2 = 0; DB1 = 0; DB0 = 0	**P_**	Writes 'P'. The DDRAM has already been selected by initialization at power-on. The cursor is incremented by 1 and shifted to the right.
6	Write data to CGRAM/DDRAM: RS = 1; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 1; DB5 = 1; DB4 = 1; DB3 = 1; DB2 = 0; DB1 = 0; DB0 = 0	**PH_**	Writes 'H'.
7			
8	Write data to CGRAM/DDRAM: RS = 1; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 1; DB5 = 0; DB4 = 1; DB3 = 0; DB2 = 0; DB1 = 1; DB0 = 1	**PHILIPS_**	Writes 'S'.
9	Entry mode set: RS = 0; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 0; DB5 = 0; DB4 = 0; DB3 = 0; DB2 = 1; DB1 = 1; DB0 = 1	**PHILIPS_**	Sets mode for display shift at the time of write.
10	Write data to CGRAM/DDRAM: RS = 1; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 0; DB5 = 1; DB4 = 0; DB3 = 0; DB2 = 0; DB1 = 0; DB0 = 0	**HILIPS _**	Writes space.
11	Write data to CGRAM/DDRAM: RS = 1; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 1; DB5 = 0; DB4 = 0; DB3 = 1; DB2 = 1; DB1 = 0; DB0 = 1	**ILIPS M_**	Writes 'M'.
12			

STEP	INSTRUCTION	DISPLAY	OPERATION
13	Write data to CGRAM/DDRAM: RS = 1; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 1; DB5 = 0; DB4 = 0; DB3 = 1; DB2 = 1; DB1 = 1; DB0 = 1	**MICROKO_**	Writes 'O'.
14	Cursor or display shift: RS = 0; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 0; DB5 = 0; DB4 = 1; DB3 = 0; DB2 = 0; DB1 = 0; DB0 = 0	**MICROKO**	Shifts only the cursor position to the left.
15	Cursor or display shift: RS = 0; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 0; DB5 = 0; DB4 = 1; DB3 = 0; DB2 = 0; DB1 = 0; DB0 = 0	**MICROKO**	Shifts only the cursor position to the left.
16	Write data to CGRAM/DDRAM: RS = 1; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 1; DB5 = 0; DB4 = 0; DB3 = 0; DB2 = 0; DB1 = 1; DB0 = 1	**ICROCO**	Writes 'C' correction. The display moves to the left.
17	Cursor or display shift: RS = 0; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 0; DB5 = 0; DB4 = 1; DB3 = 1; DB2 = 1; DB1 = 0; DB0 = 0	**MICROCO**	Shifts the display and cursor to the right.
18	Cursor or display shift: RS = 0; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 0; DB5 = 0; DB4 = 1; DB3 = 0; DB2 = 1; DB1 = 0; DB0 = 0	**MICROCO_**	Shifts only the cursor to the right.
19	Write data to CGRAM/DDRAM: RS = 1; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 1; DB5 = 0; DB4 = 0; DB3 = 1; DB2 = 1; DB1 = 0; DB0 = 1	**ICROCOM_**	Writes 'M'.
20			
21	Return home: RS = 0; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 0; DB5 = 0; DB4 = 0; DB3 = 0; DB2 = 0; DB1 = 1; DB0 = 0	**PHILIPS M**	Returns both display and cursor to the original position (address 0).

Table 8 8-bit operation, 2-line display example; using internal reset

STEP	INSTRUCTION	DISPLAY	OPERATION
1	Power supply on (PCF2104x is initialized by the internal reset function).		Initialized. No display appears.
2	Function set: RS = 0; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 0; DB5 = 1; DB4 = 1; DB3 = 1; DB2 = 0; DB1 = 0; DB0 = 0		Sets to 8-bit operation, selects 2 × 24 display
3	Display on/off control: RS = 0; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 0; DB5 = 0; DB4 = 0; DB3 = 1; DB2 = 1; DB1 = 1; DB0 = 0	_	Turns on display and cursor. Entire display is blank after initialization.
4	Entry mode set: RS = 0; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 0; DB5 = 0; DB4 = 0; DB3 = 0; DB2 = 1; DB1 = 1; DB0 = 0	_	Sets mode to increment the address by 1 and to shift the cursor to the right at the time of write to the CG/DDRAM. Display is not shifted.
5	Write data to CGRAM/DDRAM: RS = 1; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 1; DB5 = 0; DB4 = 1; DB3 = 0; DB2 = 0; DB1 = 0; DB0 = 0	**P**_	Writes 'P'. The DDRAM has already been selected by initialization at power-on. The cursor is incremented by 1 and shifted to the right.
6			
7	Write data to CGRAM/DDRAM: RS = 1; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 1; DB5 = 0; DB4 = 1; DB3 = 0; DB2 = 0; DB1 = 1; DB0 = 1	**PHILIPS**_	Writes 'S'.
8	Set DDRAM address: RS = 0; R/$\overline{W}$ = 0; DB7 = 1; DB6 = 1; DB5 = 0; DB4 = 0; DB3 = 0; DB2 = 0; DB1 = 0; DB0 = 0	**PHILIPS** _	Sets DDRAM address to position the cursor at the head of the 2nd line.
9	Write data to CGRAM/ DDRAM: RS = 1; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 1; DB5 = 0; DB4 = 0; DB3 = 1; DB2 = 1; DB1 = 0; DB0 = 1	**PHILIPS** **M**_	Writes 'M'.
10			
11	Write data to CGRAM/ DDRAM: RS = 1; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 1; DB5 = 0; DB4 = 0; DB3 = 1; DB2 = 1; DB1 = 1; DB0 = 1	**PHILIPS** **MICROCO**_	Writes 'O'.
12	Write data to CGRAM/ DDRAM: RS = 0; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 0; DB5 = 0; DB4 = 0; DB3 = 0; DB2 = 1; DB1 = 1; DB0 = 1	**PHILIPS** **MICROCO**_	Sets mode for display shift at the time of write.

STEP	INSTRUCTION	DISPLAY	OPERATION
13	Write data to CGRAM/ DDRAM: RS = 1; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 1; DB5 = 0; DB4 = 0; DB3 = 1; DB2 = 1; DB1 = 0; DB0 = 1	**HILIPS** **ICROCOM_**	Writes 'M'. Display is shifted to the left. The first and second lines shift together.
14			
15	Return home: RS = 0; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 0; DB5 = 0; DB4 = 0; DB3 = 0; DB2 = 0; DB1 = 1; DB0 = 0	**PHILIPS** **MICROCOM**	Returns both display and cursor to the original position (address 0).

Table 9 Example of I²C-bus operation; 1-line display (using internal reset, assuming SA0 = V_{SS}; note 1)

STEP	I²C-BUS BYTE	DISPLAY	OPERATION
1	I²C-bus start		Initialized. No display appears.
2	Slave address for write: SA6 = 0; SA5 = 1; SA4 = 1; SA3 = 1; SA2 = 0; SA1 = 1; SA0 = 0; R/$\overline{W}$ = 0; Ack = 1		During the acknowledge cycle SDA will be pulled-down by the PCF2104x.
3	Send a control byte for function set: Co = 0; RS = 0; R/$\overline{W}$ = 0; Ack = 1		Control byte sets RS and R/$\overline{W}$ for following data bytes.
4	Function set: DB7 = 0; DB6 = 0; DB5 = 1; DB4 = X; DB3 = 0; DB2 = 0; DB1 = 0; DB0 = 0; Ack = 1		Selects 1-line display; SCL pulse during acknowledge cycle starts execution of instruction.
5	Display on/off control: DB7 = 0; DB6 = 0; DB5 = 0; DB4 = 0; DB3 = 1; DB2 = 1; DB1 = 1; DB0 = 0; Ack = 1	_	Turns on display and cursor. Entire display shows character Hex 20 (blank in ASCII-like character sets).
6	Entry mode set: DB7 = 0; DB6 = 0; DB5 = 0; DB4 = 0; DB3 = 0; DB2 = 1; DB1 = 1; DB0 = 0; Ack = 1	_	Sets mode to increment the address by 1 and to shift the cursor to the right at the time of write to the DDRAM or CGRAM. Display is not shifted.
7	I²C-bus start	_	For writing data to DDRAM, RS must be set to 1. Therefore a control byte is needed.
8	Slave address for write: SA6 = 0; SA5 = 1; SA4 = 1; SA3 = 1; SA2 = 0; SA1 = 1; SA0 = 0; R/$\overline{W}$ = 0; Ack = 1	_	
9	Send a control byte for write data: Co = 0; RS = 1; R/$\overline{W}$ = 0; Ack = 1	_	
10	Write data to DDRAM: DB7 = 0; DB6 = 1; DB5 = 0; DB4 = 1; DB3 = 0; DB2 = 0; DB1 = 0; DB0 = 0; Ack = 1	**P**_	Writes 'P'. The DDRAM has been selected at power-up. The cursor is incremented by 1 and shifted to the right.
11	Write data to DDRAM: DB7 = 0; DB6 = 1; DB5 = 0; DB4 = 0; DB3 = 1; DB2 = 0; DB1 = 0; DB0 = 0; Ack = 1	**PH**_	Writes 'H'.
12 to 15			
16	Write data to DDRAM: DB7 = 0; DB6 = 1; DB5 = 0; DB4 = 1; DB3 = 0; DB2 = 0; DB1 = 1; DB0 = 1; Ack = 1	**PHILIPS**_	Writes 'S'.

STEP	I²C-BUS BYTE	DISPLAY	OPERATION
17	(optional I²C-bus stop) I²C-bus start + slave address for write (as step 8)	PHILIPS_	
18	Control byte: Co = 1; RS = 0; R/$\overline{W}$ = 0; Ack = 1	PHILIPS_	
19	Return home: DB7 = 0; DB6 = 0; DB5 = 0; DB4 = 0; DB3 = 0; DB2 = 0; DB1 = 1; DB0 = 0; Ack = 1	PHILIPS	Sets DDRAM address 0 in Address Counter. (Also returns shifted display to original position. DDRAM contents unchanged). This instruction does not update the Data Register (DR).
20	Control byte for read: Co = 0; RS = 1; R/$\overline{W}$ = 1; Ack = 1	PHILIPS	DDRAM content will be read from following instructions. The R/$\overline{W}$ has to be set to 1 while still in I²C-bus write mode.
21	I²C-bus start	PHILIPS	
22	Slave address for read: SA6 = 0; SA5 = 1; SA4 = 1; SA3 = 1; SA2 = 0; SA1 = 1; SA0 = 0; R/$\overline{W}$ = 1; Ack = 1	PHILIPS	During the acknowledge cycle the content of the DR is loaded into the internal I²C-bus interface to be shifted out. In the previous instruction neither a 'Set address' nor a 'Read data' has been performed. Therefore the content of the DR was unknown.
23	Read data: 8 × SCL + master acknowledge; note 2: DB7 = X; DB6 = X; DB5 = X; DB4 = X; DB3 = X; DB2 = X; DB1 = X; DB0 = X; Ack = 1	PHILIPS	8 × SCL; content loaded into interface during previous acknowledge cycle is shifted out over SDA. MSB is DB7. During master acknowledge content of DDRAM address 01 is loaded into the I²C-bus interface.
24	Read data: 8 × SCL + master acknowledge; note 2: DB7 = 0; DB6 = 1; DB5 = 0; DB4 = 0; DB3 = 1; DB2 = 0; DB1 = 0; DB0 = 0; Ack = 0	PHILIPS	8 × SCL; code of letter 'H' is read first. During master acknowledge code of 'I' is loaded into the I²C-bus interface.
25	Read data: 8 × SCL + no master acknowledge; note 2: DB7 = 0; DB6 = 1; DB5 = 0; DB4 = 0; DB3 = 1; DB2 = 0; DB1 = 0; DB0 = 1; Ack = 1	PHILIPS	No master acknowledge; After the content of the I²C-bus interface register is shifted out no internal action is performed. No new data is loaded to the interface register, Data Register (DR) is not updated, Address Counter (AC) is not incremented and cursor is not shifted.
26	I²C stop	PHILIPS	

Notes

1. X = don't care.
2. SDA is left at high-impedance by the microcontroller during the READ acknowledge.

Table 10 Initialization by instruction, 8-bit interface (note 1)

STEP	DESCRIPTION
Power-on or unknown state	
|	
Wait 2 ms after V_{DD} rises above V_{POR}	
|	
RS = 0; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 0; DB5 = 1; DB4 = 1; DB3 = X; DB2 = X; DB1 = X; DB0 = X	BF cannot be checked before this instruction. 'Function set' (interface is 8-bits long).
|	
Wait 2 ms	
|	
RS = 0; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 0; DB5 = 1; DB4 = 1; DB3 = X; DB2 = X; DB1 = X; DB0 = X	BF cannot be checked before this instruction.'Function set' (interface is 8-bits long).
|	
Wait more than 40 μs	
|	
RS = 0; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 0; DB5 = 1; DB4 = 1; DB3 = X; DB2 = X; DB1 = X; DB0 = X	BF cannot be checked before this instruction. 'Function set' (interface is 8-bits long).
|	BF can be checked after the following instructions. When BF is not checked, the waiting time between instructions is the specified instruction time (see Table 3).
RS = 0; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 0; DB5 = 1; DB4 = 1; DB3 = N; DB2 = M; DB1 = X; DB0 = 0	'Function set' (interface is 8-bits long). Specify the number of display lines.
RS = 0; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 0; DB5 = 0; DB4 = 0; DB3 = 1; DB2 = 0; DB1 = 0; DB0 = 0	'Display off'.
RS = 0; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 0; DB5 = 0; DB4 = 0; DB3 = 0; DB2 = 0; DB1 = 0; DB0 = 1	'Clear display'.
RS = 0; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 0; DB5 = 0; DB4 = 0; DB3 = 0; DB2 = 1; DB1 = I/D; DB0 = S	'Entry mode set'.
|	
Initialization ends	

Note

1. X = don't care.

Table 11 Initialization by instruction, 4-bit interface. Not applicable for I²C-bus operation

STEP	DESCRIPTION
Power-on or unknown state	
|	
Wait 2 ms after V_{DD} rises above V_{POR}	
|	
RS = 0; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 0; DB5 = 1; DB4 = 1	BF cannot be checked before this instruction. 'Function set' (interface is 8-bits long).
|	
Wait 2 µs	
|	
RS = 0; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 0; DB5 = 1; DB4 = 1	BF cannot be checked before this instruction. 'Function set' (interface is 8-bits long).
|	
Wait 40 µs	
|	
RS = 0; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 0; DB5 = 1; DB4 = 1	BF cannot be checked before this instruction. 'Function set' (interface is 8-bits long).
|	BF can be checked after the following instructions. When BF is not checked, the waiting time between instructions is the specified instruction time (see Table 3).
RS = 0; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 0; DB5 = 1; DB4 = 0	'Function set' (set interface to 4-bits long). Interface is 8-bits long.
RS = 0; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 0; DB5 = 1; DB4 = 0	'Function set' (interface is 4-bits long).
RS = 0; R/$\overline{W}$ = 0; DB7 = N; DB6 = M; DB5 = 0; DB4 = 0	Specify number of display lines and voltage generator characteristic.
RS = 0; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 0; DB5 = 0; DB4 = 0	'Display off'.
RS = 0; R/$\overline{W}$ = 0; DB7 = 1; DB6 = 0; DB5 = 0; DB4 = 0	
RS = 0; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 0; DB5 = 0; DB4 = 0	'Clear display'.
RS = 0; R/$\overline{W}$ = 0; DB7 = 1; DB6 = 0; DB5 = 0; DB4 = 0	
RS = 0; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 0; DB5 = 0; DB4 = 0	'Entry mode set'.
RS = 0; R/$\overline{W}$ = 0; DB7 = 0; DB6 = 1; DB5 = I/D; DB4 = S	
|	
Initialization ends	

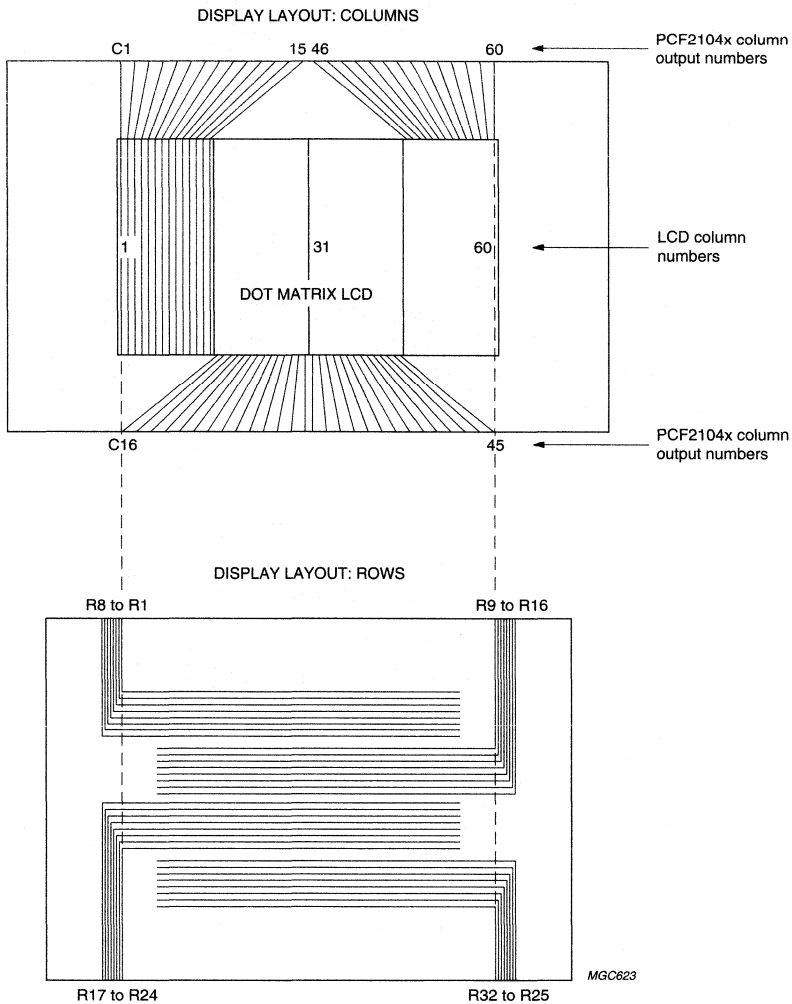


Fig.32 Example of 4 × 12 display layout (PCF2104x).

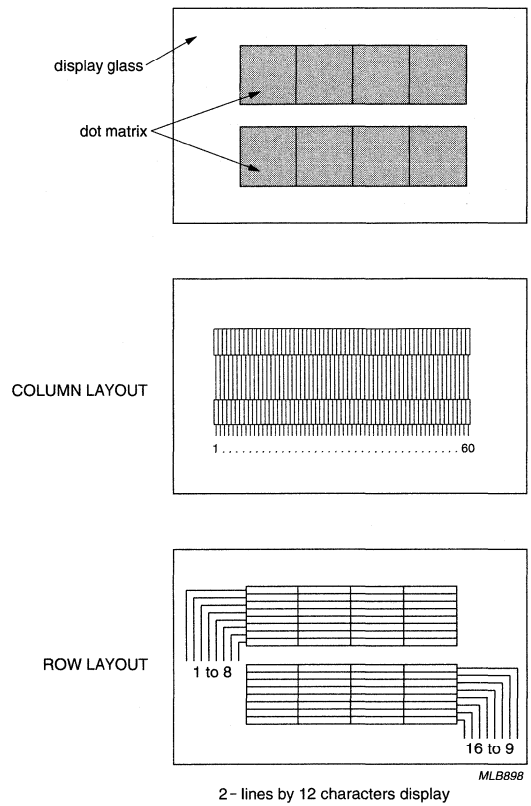


Fig.33 Display example (PCF2104x); 2 lines by 12 characters.

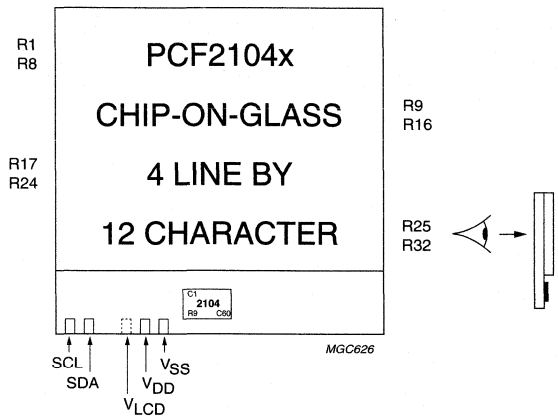
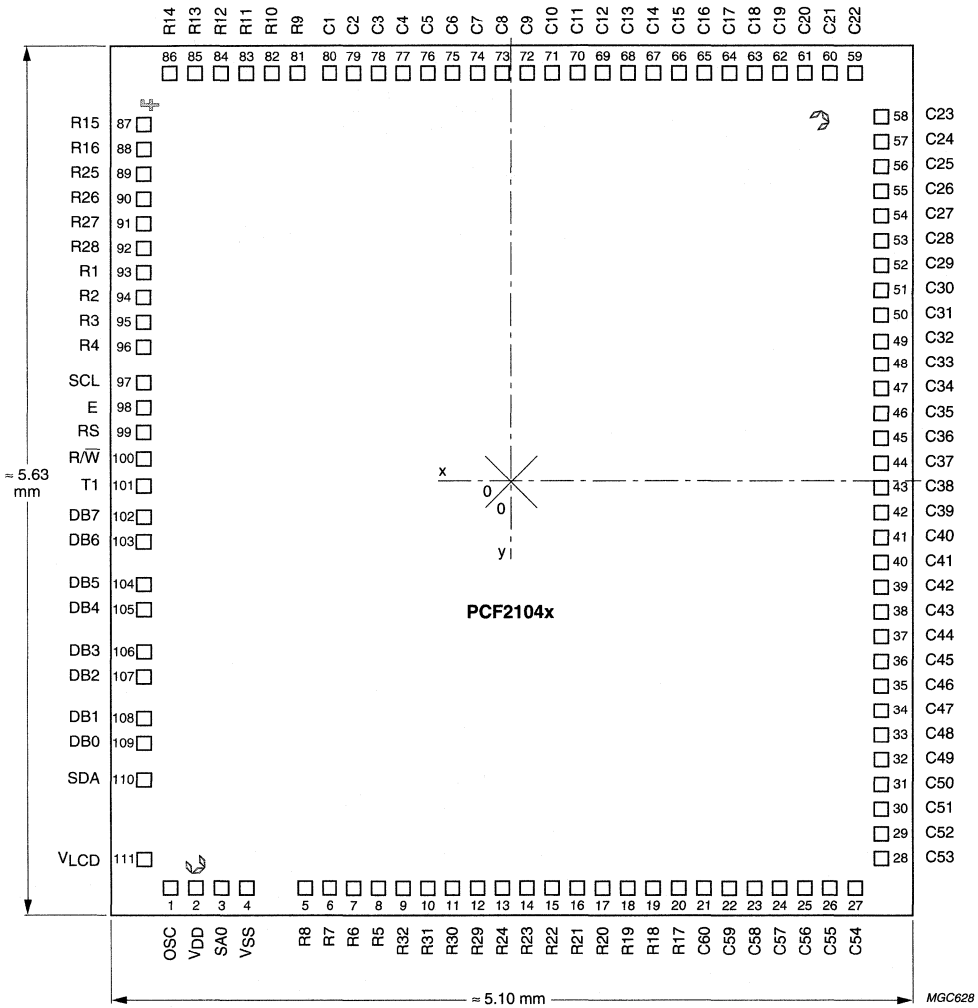


Fig.34 Chip-on-glass application.

18 BONDING PAD LOCATIONS



Chip dimensions: approximately 5.10 × 5.63 mm.
Gold bump dimensions: approximately 89 × 89 × 25 µm.

Fig.35 Bonding pad locations.

Table 12 Bonding pad locations (dimensions in μm); all x/y coordinates are referenced to centre of chip, see Fig.35

SYMBOL	PAD	x	y
OSC	1	−2184.5	−2637
V_{DD}	2	−2024.5	−2637
SA0	3	−1864.5	−2637
V_{SS}	4	−1704.5	−2637
R8	5	−1339	−2637
R7	6	−1179	−2637
R6	7	−1019	−2637
R5	8	−859	−2637
R32	9	−699	−2637
R31	10	−539	−2637
R30	11	−379	−2637
R29	12	−219	−2637
R24	13	−59	−2637
R23	14	101	−2637
R22	15	261	−2637
R21	16	421	−2637
R20	17	581	−2637
R19	18	741	−2637
R18	19	901	−2637
R17	20	1061	−2637
C60	21	1221	−2637
C59	22	1381	−2637
C58	23	1541	−2637
C57	24	1701	−2637
C56	25	1861	−2637
C55	26	2021	−2637
C54	27	2181	−2637
C53	28	2350	−2445
C52	29	2350	−2285
C51	30	2350	−2125
C50	31	2350	−1965
C49	32	2350	−1805
C48	33	2350	−1645
C47	34	2350	−1485
C46	35	2350	−1325
C45	36	2350	−1165
C44	37	2350	−1005
C43	38	2350	−845
C42	39	2350	−685
C41	40	2350	−525
C40	41	2350	−365
C39	42	2350	−205
C38	43	2350	−45
C37	44	2350	115
C36	45	2350	275
C35	46	2350	435
C34	47	2350	595
C33	48	2350	755
C32	49	2350	915
C31	50	2350	1075
C30	51	2350	1235
C29	52	2350	1395
C28	53	2350	1555
C27	54	2350	1715
C26	55	2350	1875
C25	56	2350	2035
C24	57	2350	2195
C23	58	2350	2355
C22	59	2185	2637.5
C21	60	2025	2637.5
C20	61	1865	2637.5
C19	62	1705	2637.5
C18	63	1545	2637.5
C17	64	1385	2637.5
C16	65	1225	2637.5
C15	66	1065	2637.5
C14	67	905	2637.5
C13	68	745	2637.5
C12	69	585	2637.5
C11	70	425	2637.5
C10	71	265	2637.5
C9	72	105	2637.5
C8	73	−55	2637.5
C7	74	−215	2637.5
C6	75	−375	2637.5
C5	76	−535	2637.5

SYMBOL	PAD	x	y
C4	77	−695	2637.5
C3	78	−855	2637.5
C2	79	−1015	2637.5
C1	80	−1175	2637.5
R9	81	−1385	2637.5
R10	82	−1545	2637.5
R11	83	−1705	2637.5
R12	84	−1865	2637.5
R13	85	−2025	2637.5
R14	86	−2185	2637.5
R15	87	−2349	2308
R16	88	−2349	2148
R25	89	−2349	1988
R26	90	−2349	1828
R27	91	−2349	1668
R28	92	−2349	1508
R1	93	−2349	1348
R2	94	−2349	1188
R3	95	−2349	1028
R4	96	−2349	868
SCL	97	−2349	632
E	98	−2349	472
RS	99	−2349	312
R/$\overline{W}$	100	−2349	142
T1	101	−2349	−34
DB7	102	−2349	−233
DB6	103	−2349	−393
DB5	104	−2349	−668
DB4	105	−2349	−828
DB3	106	−2349	−1103
DB2	107	−2349	−1263
DB1	108	−2349	−1538
DB0	109	−2349	−1698
SDA	110	−2349	−1933
V_{LCD}	111	−2349	−2453
RECPAT 'F'		−2327.5	2427.5
RECPAT 'C'		−2027.5	−2512.5
RECPAT 'C'		1982.5	2297.5

CONTENTS

LCD controller/driver PCF2105

1 FEATURES

- Single chip Liquid Crystal Display (LCD) controller/driver
- 1 or 2-line display of up to 24 characters per line, or 2 or 4-line display of up to 12 characters per line
- 5 × 7 character format plus cursor; 5 × 8 for kana (Japanese syllabary) and user-defined symbols
- On-chip generation of intermediate LCD bias voltages
- On-chip oscillator requires no external components (external clock also possible)
- Display data RAM: 80 characters
- Character generator ROM: 240 characters
- Character generator RAM: 16 characters
- 4 or 8-bit parallel bus or 2-wire I²C-bus interface (400 kHz)
- CMOS and TTL compatible
- 32 row, 60 column outputs
- Multiplex (MUX) rates 1 : 32 and 1 : 16
- Uses common 11-code instruction set
- Logic supply voltage range: $V_{DD} - V_{SS}$ = 2.5 to 6 V
- Display supply voltage range: $V_{DD} - V_{LCD}$ = 3.5 to 9 V
- Low power consumption
- I²C-bus address selection (SA0): 011101.

2 APPLICATIONS

- Telecom equipment
- Portable instruments
- Point-of-sale terminals.

3 GENERAL DESCRIPTION

The PCF2105 integrated circuit is similar to the PCF2114x (described in the *"PCF2116 family"* data sheet) but does not contain the high voltage generator of that device.

Furthermore, a fast I²C-bus interface (400 kHz) is provided.

The PCF2105 is optimized for chip-on-glass applications.

A specific letter code 'M' for a character set is programmed in the Character Generator ROM (CGROM) (see Fig.5).

The PCF2105 is a low power CMOS LCD controller/driver, designed to drive a split screen dot matrix LCD of 1 or 2 lines by 24 characters or 2 or 4 lines by 12 characters with a 5 × 8 dot format. All necessary functions for the display are provided in a single chip, including on-chip generation of LCD bias voltages which results in a minimum of external components and lower system power consumption. To allow partial V_{DD} shutdown the ESD protection system of the SCL and SDA pads does not use a diode connected to V_{DD}.

The chip contains a character generator and displays alphanumeric and kana characters. The PCF2105 interfaces to most microcontrollers via a 4 or 8-bit parallel bus, or via the 2-wire I²C-bus.

3.1 Packages

- PCF2105MU/2: chip with bumps in tray.

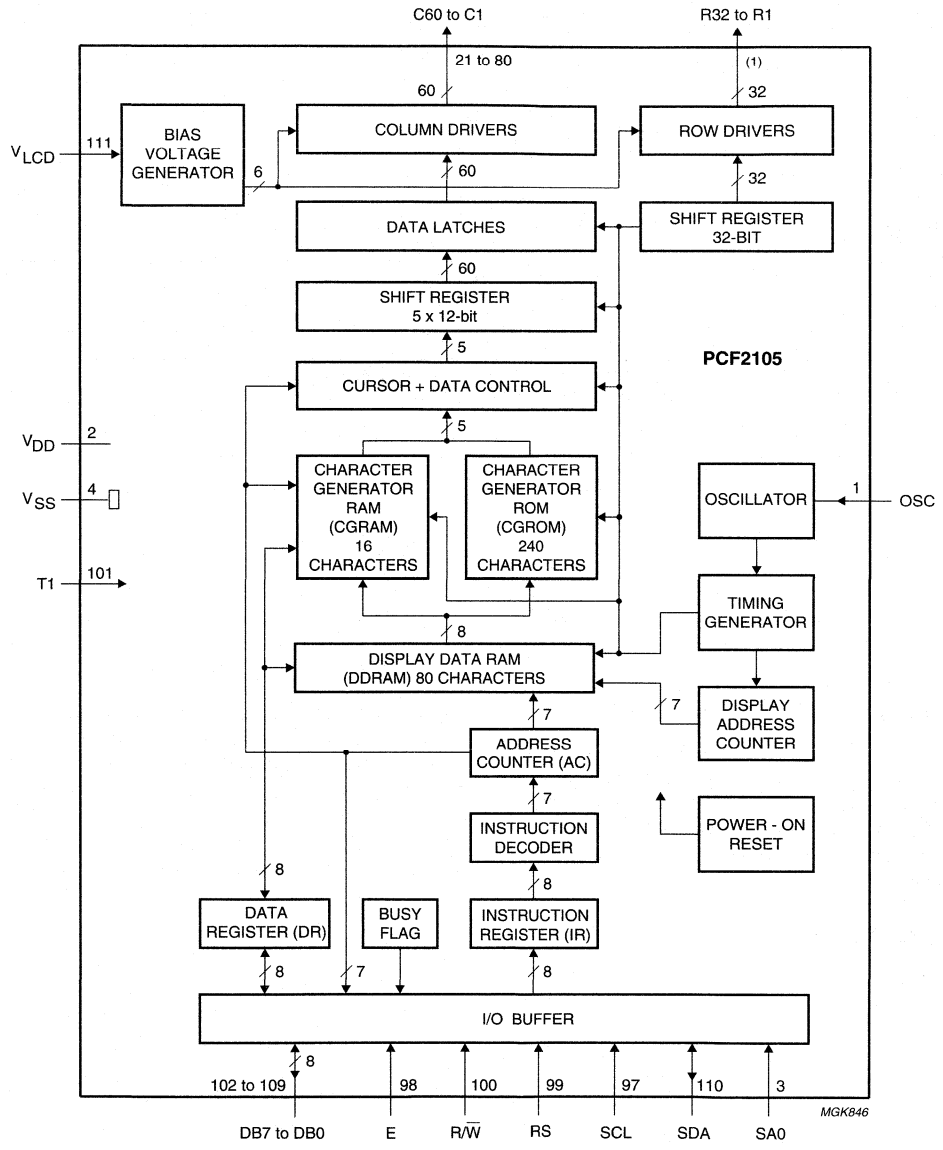
3.2 Available types

- PCF2105MU/2: character set 'M' in CGROM.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF2105MU/2	–	chip with bumps in tray	–

5 BLOCK DIAGRAM



(1) Pads 5 to 8 and 9 to 12 correspond with symbols R8 to R5 and R32 to R29.
Pads 13 to 20 and 81 to 88 correspond with symbols R24 to R17 and R9 to R16.
Pads 89 to 92 and 93 to 96 correspond with symbols R25 to R28 and R1 to R4.

Fig.1 Block diagram.

6 PINNING

SYMBOL	PAD	I/O	DESCRIPTION
OSC	1	I	oscillator/external clock input
V_{DD}	2	–	logic supply voltage
SA0	3	I	I²C-bus address selection input
V_{SS}	4	–	logic ground
R8 to R5	5 to 8	O	LCD row driver outputs
R32 to R29	9 to 12	O	LCD row driver outputs
R24 to R17	13 to 20	O	LCD row driver outputs
C60 to C1	21 to 80	O	LCD column driver outputs
R9 to R16	81 to 88	O	LCD row driver outputs
R25 to R28	89 to 92	O	LCD row driver outputs
R1 to R4	93 to 96	O	LCD row driver outputs
SCL	97	I	I²C-bus serial clock input
E	98	I	data bus clock input
RS	99	I	register select input
R/$\overline{W}$	100	I	read/write input
T1	101	I	test input
DB7 to DB0	102 to 109	I/O	8-bit bidirectional data bus input/output
SDA	110	I/O	I²C-bus serial data input/output
V_{LCD}	111	I	LCD supply voltage input

7 PAD FUNCTIONS

7.1 RS: Register Select (parallel control)

Bit RS selects the register to be accessed for read and write when the device is controlled by the parallel interface. RS = 0 selects the instruction register for write and the busy flag and address counter for read. RS = 1 selects the data register for both read and write. There is an internal pull-up resistor on pad RS.

7.2 R/$\overline{W}$: read/write (parallel control)

R/$\overline{W}$ selects either the read (R/$\overline{W}$ = 1) or write (R/$\overline{W}$ = 0) operation when control is by the parallel interface. There is an internal pull-up resistor on pad R/$\overline{W}$.

7.3 E: data bus clock (parallel control)

Pad E should be HIGH to signal the start of a read or write operation when the device is controlled by the parallel interface. Data is clocked in or out of the chip on the falling edge of the clock. Note that pad E must be connected to V_{SS} (logic 0) when I²C-bus control is used.

7.4 DB7 to DB0: data bus (parallel control)

The bidirectional, 3-state data bus transfers data between the system controller and the PCF2105. DB7 acts as the busy flag, signalling that internal operations are not yet completed. In 4-bit operations, DB7 to DB4 are used and DB3 to DB0 must be left open-circuit. There is an internal pull-up resistor on each of the data lines. Note that pads DB7 to DB0 must be left open-circuit when I²C-bus control is used.

7.5 C60 to C1: column driver outputs

Pads C60 to C1 output the data for pairs of columns. This arrangement permits optimized Chip-On-Glass (COG) layout for 4-line by 12 characters.

7.6 R32 to R1: row driver outputs

Pads R32 to R1 output the row select waveforms to the left and right halves of the display.

7.7 V_{LCD}: LCD power supply

Negative power supply for the liquid crystal display.

7.8 OSC: oscillator

When the on-chip oscillator is used, pad OSC must be connected to V_{DD}. An external clock signal, if used, is input at pad OSC.

7.9 SCL: serial clock line

Pad SCL is input for the I²C-bus clock signal.

7.10 SDA: serial data line

Pad SDA is input/output for the I²C-bus data line.

7.11 SA0: address input

The hardware subaddress line is used to program the device subaddress for 2 different PCF2105s on the same I²C-bus.

7.12 T1: test input

Pad T1 must be connected to V_{SS}. Not user accessible.

8 FUNCTIONAL DESCRIPTION

Figure 1 shows the block diagram for the PCF2105. Details are explained in subsequent sections.

8.1 LCD bias voltage generator

The intermediate bias voltages for the LCD are generated on-chip. This removes the need for an external resistive bias chain and significantly reduces the system power consumption. The optimum levels depend on the multiplex (MUX) rate and are selected automatically when the number of lines in the display is defined.

The optimum value of the LCD operating voltage V_{OP} depends on the MUX rate, the LCD threshold voltage V_{th} and the number of bias levels. The relationships, together with the discrimination ratio (D) are given in Table 1.

Using a 5-level bias scheme for MUX rate 1 : 16 allows $V_{OP} < 5$ V for most LCDs. The effect on the display contrast is negligible.

Table 1 Optimum values for V_{OP}

MUX RATE	NUMBER OF BIAS LEVELS	$\frac{V_{OP}}{V_{th}}$	$D = \frac{V_{on}}{V_{off}}$
1 : 16	5	3.67	1.277
1 : 32	6	5.19	1.196

8.2 Oscillator

The on-chip oscillator provides the clock signal for the display system. No external components are required. Pad OSC must be connected to V_{DD}.

8.3 External clock

If an external clock is to be used, it must be input at pad OSC. The resulting display frame frequency is given by $f_{frame} = \frac{f_{osc}}{2304}$

A clock signal must always be present, otherwise the LCD may be frozen in a DC state.

8.4 Power-on reset

The Power-on reset block initializes the chip after power-on or power failure.

8.5 Registers

The PCF2105 has two 8-bit registers, an Instruction Register (IR) and a Data Register (DR). The Register Select (RS) signal determines which register will be accessed.

The IR stores instruction codes such as 'clear display' and 'cursor shift', and address information for the DDRAM and CGRAM. The system controller can write data to but can not read data from the instruction register.

The DR temporarily stores data to be read from the DDRAM and CGRAM. When reading, data from the DDRAM or CGRAM (corresponding to the address in the address counter) is written to the DR prior to being read by the 'read data' instruction.

8.6 Busy flag

The Busy Flag (BF) indicates the free or busy status of the PCF2105. Bit BF = 1 indicates that the chip is busy and further instructions will not be accepted. The BF is output at pad DB7 when bit RS = 0 and bit R/$\overline{W}$ = 1. Instructions should only be written after checking that BF = 0 or waiting for the required number of clock cycles.

8.7 Address Counter (AC)

The AC assigns addresses to the DDRAM and CGRAM for reading and writing and is set by the instructions 'set CGRAM address' and 'set DDRAM address'. After a read/write operation the AC is automatically incremented or decremented by 1. The AC contents are output to the bus (pads DB6 to DB0) when bit RS = 0 and bit R/$\overline{W}$ =1.

8.8 Display Data RAM (DDRAM)

The DDRAM stores up to 80 characters of display data, represented by 8-bit character codes. DDRAM locations not used for storing display data can be used as general purpose RAM. The basic DDRAM-to-display mapping scheme is shown in Fig.2. With no display shift, the characters represented by the codes in the first 12 or 24 DDRAM locations, starting at address 00 in line 1, are displayed. Subsequent lines display data starting at addresses 20, 40, or 60 hexadecimal (hex). Figures 3 and 4 show the DDRAM-to-display mapping scheme when the display is shifted.

The address range for a 1-line display is 00 to 4F; for a 2-line display from 00 to 27 (line 1) and 40 to 67 (line 2); for a 4-line display from 00 to 13, 20 to 33, 40 to 53 and 60 to 73 for lines 1, 2, 3 and 4 respectively. For 2 and 4-line displays the end address of one line and the start address of the next line are not successive. When the display is shifted each line wraps around independently of the others (see Figs 3 and 4).

When data is written to the DDRAM, wrap-around occurs from 4F to 00 in 1-line display and from 27 to 40 and 67 to 00 in 2-line display; from 13 to 20, 33 to 40, 53 to 60 and 73 to 00 in 4-line display.

8.9 Character Generator ROM (CGROM)

The CGROM generates 240 character patterns in 5×8 dot format from 8-bit character codes. Figure 5 shows the character set currently available.

8.10 Character Generator RAM (CGRAM)

Up to 16 user-defined characters may be stored in the CGRAM. The CGROM and CGRAM use a common address space, of which the first column is reserved for the CGRAM (see Fig.5). Figure 6 shows the addressing principle for the CGRAM.

8.11 Cursor control circuit

The cursor control circuit generates the cursor (underline and/or character blink as shown in Fig.7) at the DDRAM address contained in the address counter. When the address counter contains the CGRAM address the cursor will be inhibited.

8.12 Timing generator

The timing generator produces the various signals required to drive the internal circuitry. Internal chip operation is not disturbed by operations on the data buses.

8.13 LCD row and column drivers

The PCF2105 contains 32 row drivers and 60 column drivers. They connect the appropriate LCD bias voltages in sequence to the display, in accordance with the data to be displayed. The bias voltages and the timing are selected automatically when the number of lines in the display is selected. Figures 8 and 9 show typical waveforms.

In the 1-line display (MUX rate 1 : 16), the row outputs are driven in pairs, for example R1/R17 and R2/R18. This allows the output pairs to be connected in parallel, thereby providing greater drive capability.

Unused outputs should be left unconnected.

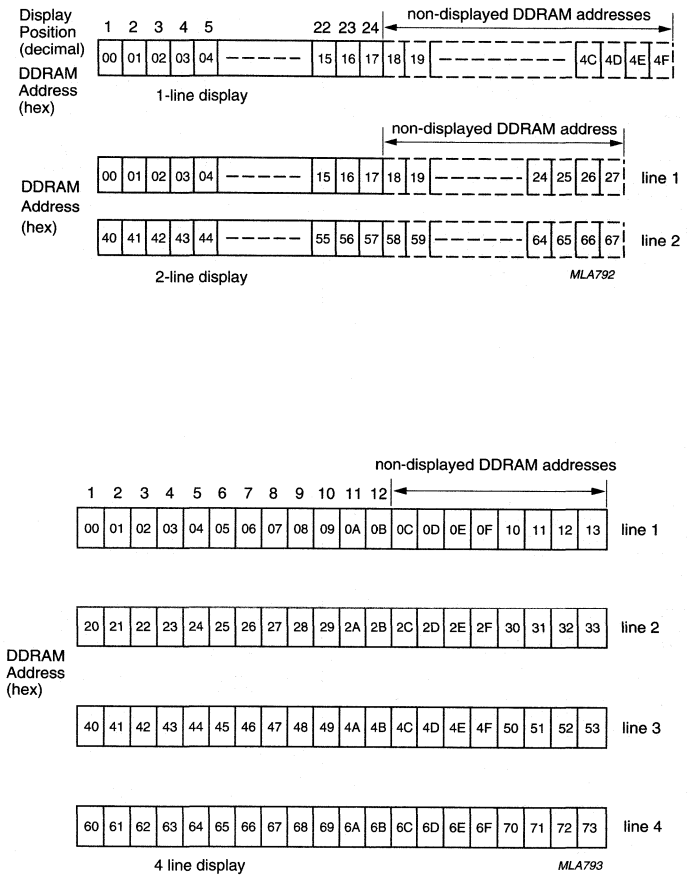


Fig.2 DDRAM-to-display mapping; no shift.

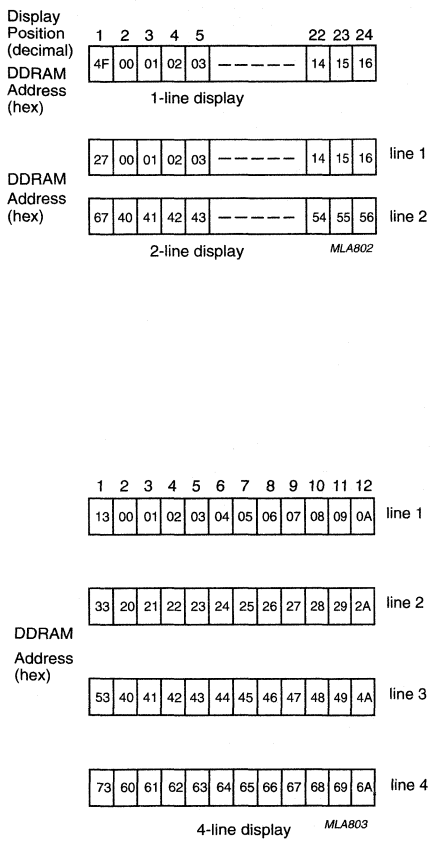


Fig.3 DDRAM-to-display mapping; right shift.

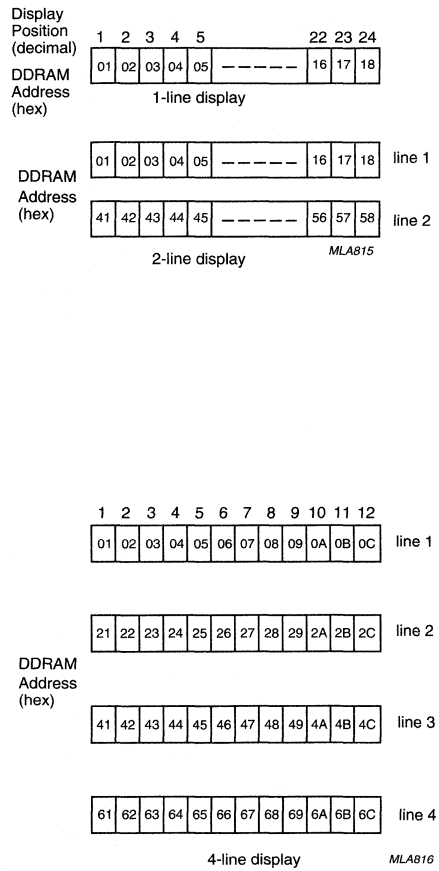
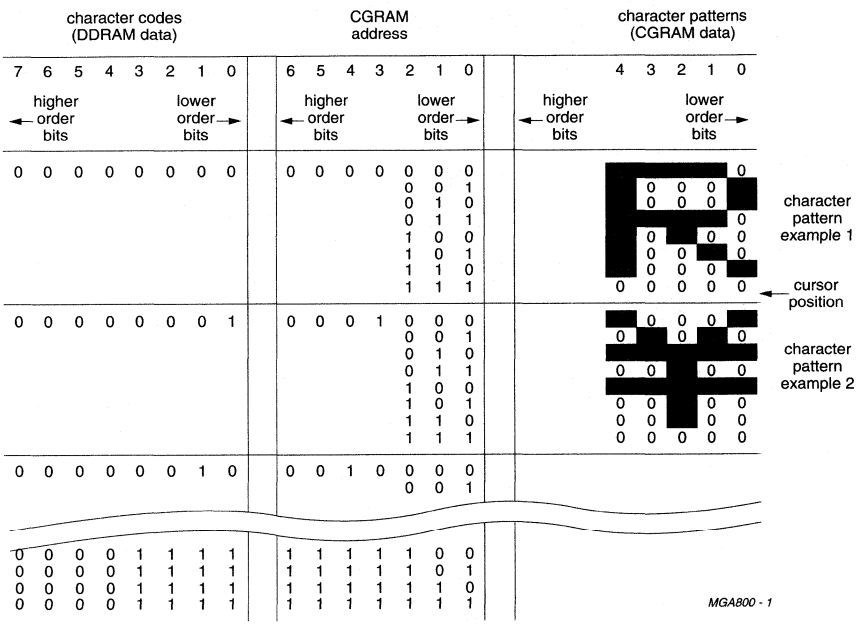


Fig.4 DDRAM-to-display mapping; left shift.

lower 4 bits \ upper 4 bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
xxxx 0000	CG RAM 1															
xxxx 0001	2															
xxxx 0010	3															
xxxx 0011	4															
xxxx 0100	5															
xxxx 0101	6															
xxxx 0110	7															
xxxx 0111	8															
xxxx 1000	9															
xxxx 1001	10															
xxxx 1010	11															
xxxx 1011	12															
xxxx 1100	13															
xxxx 1101	14															
xxxx 1110	15															
xxxx 1111	16															

MGK847

Fig.5 Character set 'M' in CGROM.



Character code bits 0 to 3 correspond to CGRAM address bits 3 to 6.

CGRAM address bits 0 to 2 designate character pattern line position. The 8th line is the cursor position and display is performed by logical OR with the cursor. Data in the 8th line will appear in the cursor position.

Character pattern column positions correspond to CGRAM data bits 0 to 4; bit 4 being at the left end, as shown in this figure.

CGRAM character patterns are selected when character code bits 4 to 7 are all logic 0. CGRAM data is logic 1 corresponds to selection for display.

Only bits 0 to 5 of the CGRAM address are set by the 'set CGRAM address' instruction. Bit 6 can be set using the 'set DDRAM address' instruction or by using the auto-increment feature during CGRAM write. All bits 0 to 6 can be read using the 'read busy flag and address' instruction.

Fig.6 Relationship between CGRAM addresses, data and display patterns.

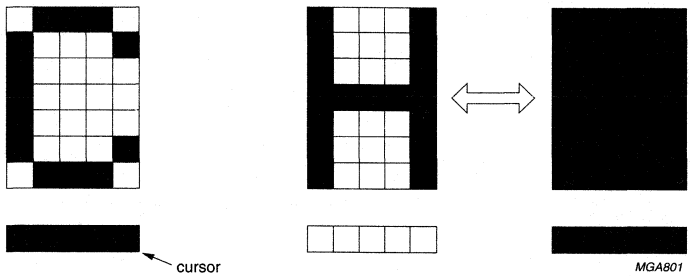


Fig.7 Cursor and blink display examples.

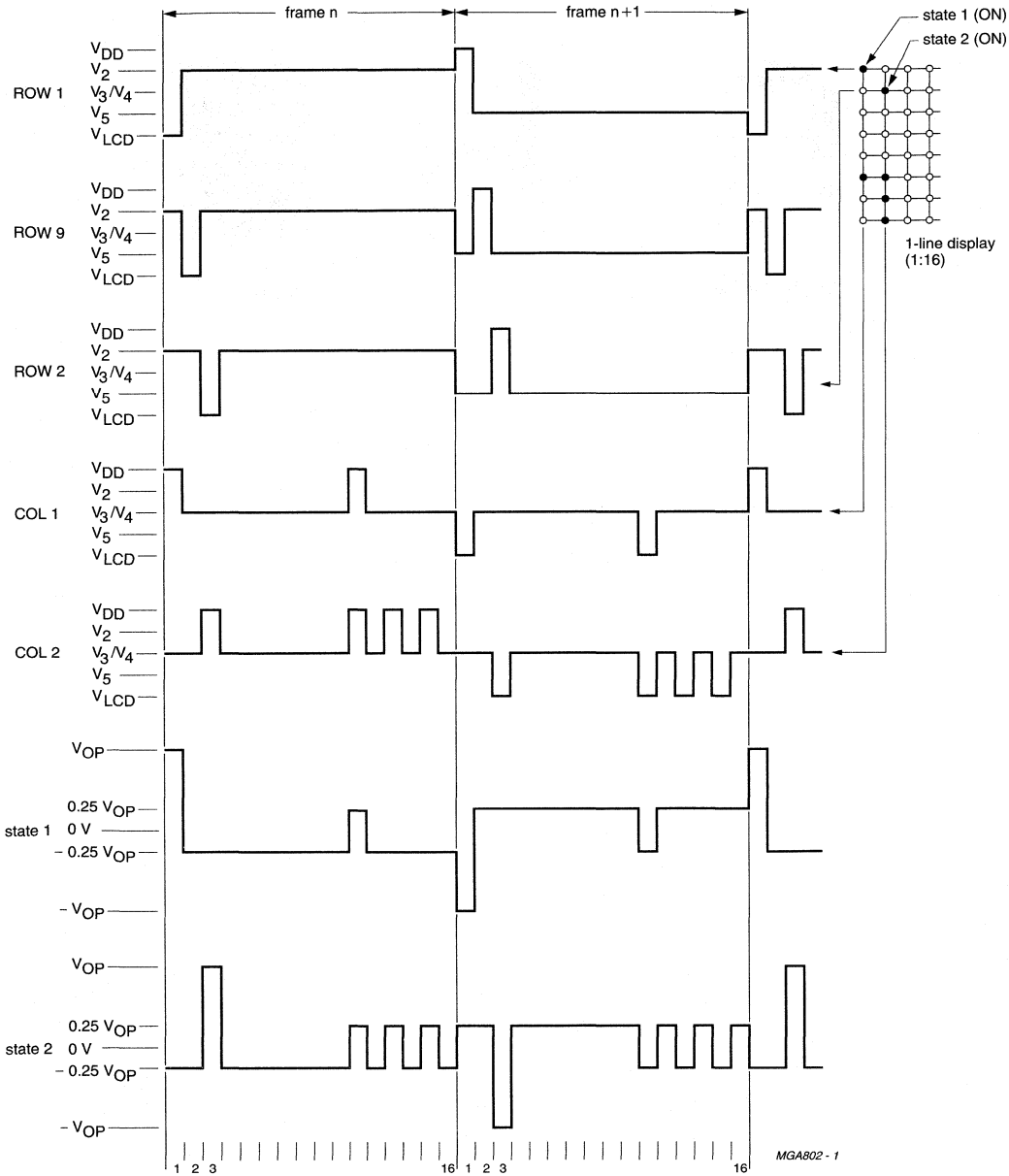


Fig.8 Typical LCD waveforms; 1-line display.

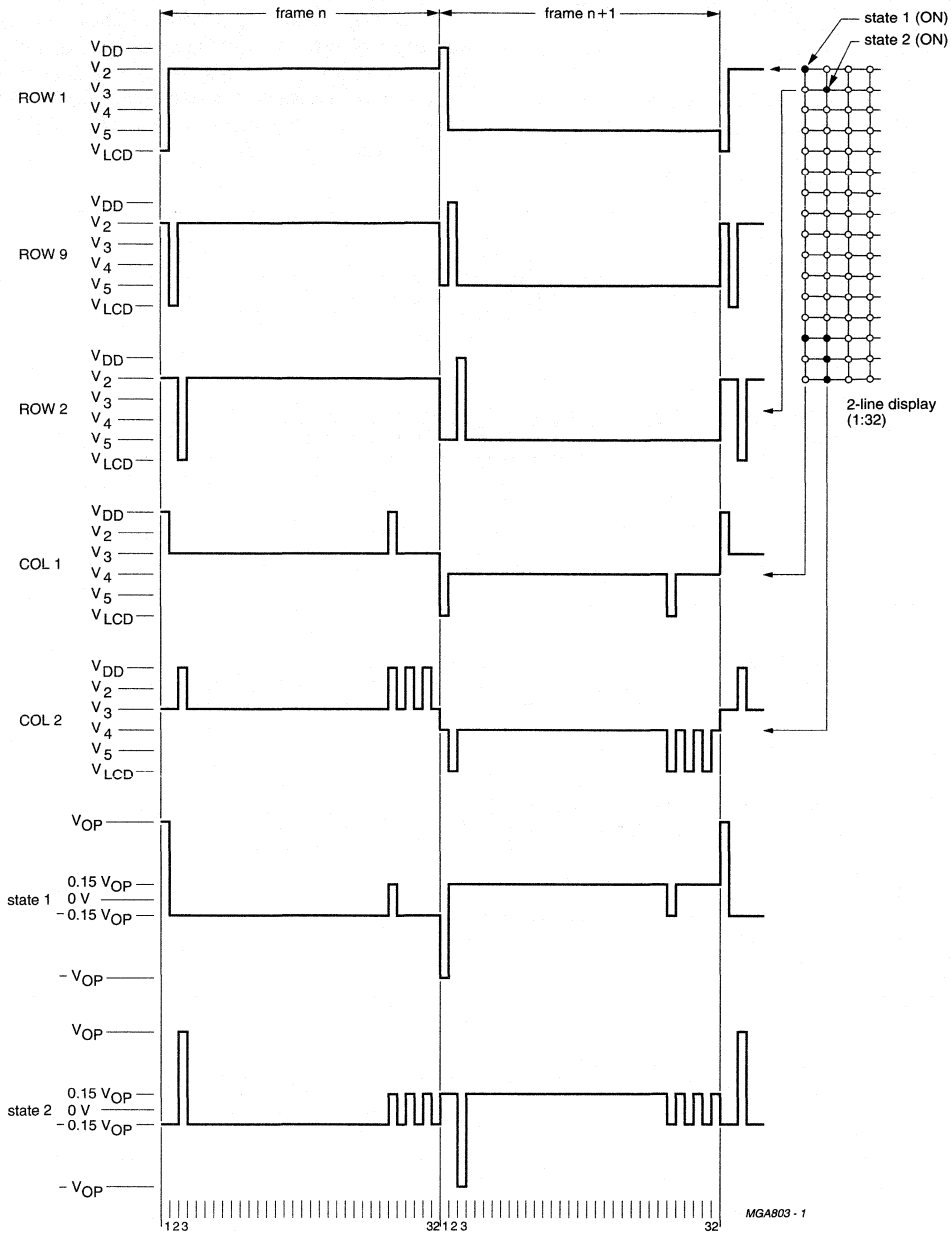


Fig.9 Typical LCD waveforms; 2-line display.

8.14 Programming of the MUX rate 1 : 16

With the MUX rate 1 : 16 the PCF2105 can be used in the following ways:

- To drive a 1-line display of 24 characters
- To drive a 2-line display of 12 characters, resulting in better contrast. The internal data flow of the chip is optimized for this purpose.

To program the MUX rate 1 : 16, bits M and N of the 'function set' instruction must be set to logic 0 (see Table 3). Figures 10, 11 and 12 show the DDRAM addresses of the display characters. The second row of each figure corresponds to either the right half of a 1-line display or to the second line of a 2-line display. Wrap around of data during display shift or when writing data is non-standard.

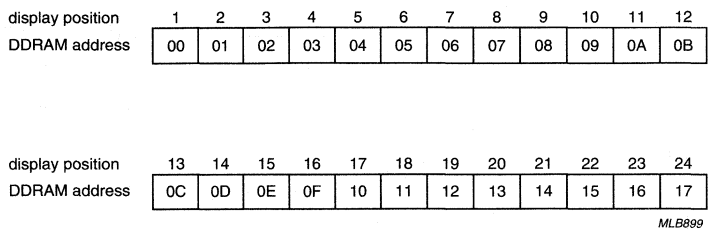


Fig.10 DDRAM-to-display mapping; no shift.

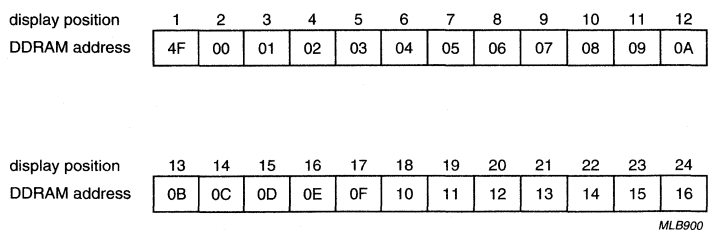


Fig.11 DDRAM-to-display mapping; right shift.

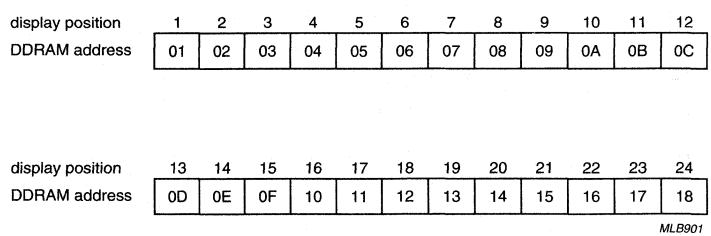


Fig.12 DDRAM-to-display mapping; left shift.

8.15 Programming of the MUX rate 1 : 32

With the MUX rate 1 : 32 the PCF2105 can be used in the following ways:

- To drive a 2-line display of 24 characters, use instruction 'function set' to set bit M to logic 0 and bit N to logic 1
- To drive a 4-line display of 12 characters, use instruction 'function set' to set both bits M and N to logic 1.

8.16 Reset function

The PCF2105 automatically initializes (resets) when power is turned on. The state after reset is given in Table 2 (see Tables 3 and 4 for the description of the bits).

Table 2 State after reset

STEP	DESCRIPTION
1	clear display
2	function set: bit DL = 1: 8-bit interface bits M and N = 0: 1-line display bit G = 0: not used
3	display control: bit D = 0: display off bit C = 0: cursor off bit B = 0: blink off
4	entry mode set: bit I/D = 1: +1(increment) bit G = 0: not used
5	default address pointer to DDRAM; the busy flag indicates the busy state (BF = 1) until initialization ends; the busy state lasts 2 ms; the chip may also be initialized by software; see Tables 10 and 11.
6	I^2C-bus interface reset

9 INSTRUCTIONS

Only two PCF2105 registers, the Instruction Register (IR) and the Data Register (DR) can be directly controlled by the microcontroller. Before internal operation, control information is stored temporarily in these registers to allow interface to various types of microcontrollers which operate at different speeds or to allow interfacing to peripheral control ICs. The PCF2105 operation is controlled by the instructions shown in Table 3 together with their execution time. Details are explained in subsequent sections.

Instructions are of 4 categories, those that:

1. Designate PCF2105 functions such as display format, data length, etc.
2. Set internal RAM addresses
3. Perform data transfer with internal RAM
4. Others.

In normal use, category 3 instructions are used most frequently. However, automatic incrementing by 1 (or decrementing by 1) of internal RAM addresses after each data write lessens the microcontroller program load. The display shift in particular can be performed concurrently with display data write, thus enabling the designer to develop systems in minimum time with maximum programming efficiency.

During internal operation, no instruction other than the 'read busy flag and address' will be executed.

Because the busy flag is set to logic 1 while an instruction is being executed, it is advisable to ensure that the flag is set to logic 0 before sending the next instruction or wait for the maximum instruction execution time, as given in Table 3. An instruction sent while the busy flag is HIGH will not be executed.

9.1 Clear display

'Clear display' writes space code 20 (hexadecimal) into all DDRAM addresses (the character pattern for character code 20 must be a blank pattern), sets the DDRAM address counter to logic 0 and returns the display to its original position if it was shifted. Consequently, the display disappears and the cursor or blink position goes to the left edge of the display (the first line if 2 or 4 lines are displayed) and sets bit I/D of 'entry mode set' to logic 1 (increment mode). Bit S of 'entry mode set' does not change.

The instruction 'clear display' requires extra execution time. This may be allowed for checking the Busy Flag (BF) or by waiting until 2 ms has elapsed. The latter must be applied where no read-back options are available, as in some Chip-On-Glass (COG) applications.

9.2 Return home

'Return home' sets the DDRAM address counter to logic 0 and returns the display to its original position if it was shifted. DDRAM contents do not change. The cursor or blink position goes to the left of the display (the first line if 2 or 4 lines are displayed). Bits I/D and S of 'entry mode set' do not change.

Table 3 Instructions (note 1)

INSTRUCTION	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DESCRIPTION	REQUIRED CLOCK CYCLES(2)
NOP	0	0	0	0	0	0	0	0	0	0	no operation	0
Clear display	0	0	0	0	0	0	0	0	0	1	clears entire display and sets DDRAM address 00 in Address Counter (AC)	165
Return home	0	0	0	0	0	0	0	0	1	0	sets DDRAM address 00 in the AC; also returns shifted display to original position; DDRAM contents remain unchanged	3
Entry mode set	0	0	0	0	0	0	0	1	I/D	S	sets cursor move direction and specifies shift of display; these operations are performed during data write and read	3
Display control	0	0	0	0	0	0	1	D	C	B	sets entire display on/off (D), cursor on/off (C) and blink of cursor position character (B)	3
Cursor/display shift	0	0	0	0	0	1	S/C	R/L	0	0	moves cursor and shifts display without changing DDRAM contents	3
Function set	0	0	0	0	1	DL	N	M	G	0	sets interface data length (DL), number of display lines (N, M) and voltage generator control (G); bit G is not used	3
Set CGRAM address	0	0	0	1	A_{CG}						sets CGRAM address	3
Set DDRAM address	0	0	1	A_{DD}							sets DDRAM address	3
Read busy flag and address	0	1	BF	A_C							reads BF indicating internal operation is being performed and reads AC contents	0
Read data	1	1	read data								reads data from CGRAM or DDRAM	3
Write data	1	0	write data								writes data to CGRAM or DDRAM	3

Notes

1. In the I²C-bus mode the DL bit is don't care. 8-bit mode is assumed. In the I²C-bus mode a control byte is required when bit RS or R/$\overline{W}$ is changed; control byte: Co, RS, R/$\overline{W}$, 0, 0, 0, 0, 0; command byte: DB7 to DB0.
2. Example: f_{osc} = 150 kHz, $T_{cy} = \frac{1}{f_{osc}}$ = 6.67 µs ; 3 cycles = 20 µs; 165 cycles = 1.1 ms.

Table 4 Command bit identities, used in Table 3

BIT	LOGIC 0	LOGIC 1
I/D	decrement	increment
S	display freeze	display shift
D	display off	display on
C	cursor off	cursor on
B	character at cursor position does not blink	character at cursor position blinks
S/C	cursor move	display shift
R/L	left shift	right shift
DL	4 bits	8 bits
N (M = 0)	2 lines × 12 characters; MUX rate 1 : 16	2 lines × 24 characters; MUX rate 1 : 32
N (M = 1)	reserved	4 lines × 12 characters; MUX rate 1 : 32
BF	end of internal operation	internal operation in progress
Co	last control byte, only data bytes to follow	next two bytes are a data byte and another control byte

9.3 Entry mode set

9.3.1 I/D

When bit I/D = 1 (0), the DDRAM or CGRAM address increments (decrements) by 1 when data is written to or read from the DDRAM or CGRAM. The cursor or blink position moves to the right when incremented and to the left when decremented. The cursor and blink are inhibited when the CGRAM is accessed.

9.3.2 S

When bit S = 1, the entire display shifts either to the right (bit I/D = 0) or to the left (I/D = 1) during a DDRAM write. Consequently, it looks as if the cursor stands still and the display moves. The display does not shift when reading from the DDRAM, or when writing to or reading from the CGRAM. When S = 0 the display does not shift.

9.4 Display control

9.4.1 D

The display is on when bit D = 1 and off when D = 0. Display data in the DDRAM is not affected and can be displayed immediately by setting D to logic 1.

9.4.2 C

The cursor is displayed when bit C = 1 and inhibited when C = 0. Even if the cursor disappears, the display functions, I/D, etc. remain in operation during display data write. The cursor is displayed using 5 dots in the 8th line (see Fig.7).

9.4.3 B

The character indicated by the cursor blinks when bit B = 1. The blink is displayed by switching between display characters and all dots on with a period of 1 second when f_{osc} = 150 kHz (see Fig.7).
At other clock frequencies the blink period is equal to

$$\frac{150\ \text{kHz}}{f_{osc}}$$

The cursor and the blink can be set to display simultaneously.

9.5 Cursor/display shift

'Cursor/display shift' moves the cursor position or the display to the right or left without writing or reading display data. This function is used to correct a character or move the cursor through the display. In the 2 or 4-line display, the cursor moves to the next line when it passes the last position of the line (40 or 20 decimal). When the displayed data is shifted repeatedly all lines shift at the same time; displayed characters do not shift into the next line.
The Address Counter (AC) content does not change if the only action performed is shift display, but increments or decrements with the cursor shift.

9.6 Function set

9.6.1 DL (PARALLEL MODE ONLY)

Bit DL sets the interface data length. Data is sent or received in bytes (DB7 to DB0) when DL = 1 or in two nibbles (DB7 to DB4) when DL = 0. When 4-bit length is selected, data is transmitted in two cycles using the parallel bus. In a 4-bit application DB3 to DB0 are left open (internal pull-ups).

DL can not be set to logic 0 from the I^2C-bus interface. If DL has been set to logic 0 via the parallel bus, programming via the I^2C-bus interface is complicated.

9.6.2 N AND M

Bits N and M set the number of display lines.

9.7 Set CGRAM address

'Set CGRAM address' sets bits 0 to 5 of the CGRAM address (A_{CG} in Table 3) into the AC (binary A[5] to A[0]). Data can then be written to or read from the CGRAM.

Only bits 0 to 5 of the CGRAM address are set by the 'set CGRAM address' instruction. Bit 6 can be set using the 'set DDRAM address' instruction or by using the auto-increment feature during CGRAM write. All bits 0 to 6 can be read using the 'read busy flag and address' instruction.

9.8 Set DDRAM address

'Set DDRAM address' sets the DDRAM address (A_{DD} in Table 3) into the AC (binary A[6] to A[0]). Data can then be written to or read from the DDRAM.

Table 5 Hexadecimal address ranges

ADDRESS	FUNCTION
00 to 4F	1 line of 24 characters
00 to 0B and 0C to 4F	2 lines of 12 characters
00 to 27 and 40 to 67	2 lines of 24 characters
00 to 13, 20 to 33, 40 to 53 and 60 to 73	4 lines of 12 characters

9.9 Read busy flag and address

'Read busy flag and address' reads the Busy Fag (BF). When bit BF = 1 it indicates that an internal operation is in progress. The next instruction will not be executed until BF = 0, so BF should be checked before sending another instruction.

At the same time, the value of the AC expressed in binary A[6] to A[0] is read out. The address counter is used by both CGRAM and DDRAM and its value is determined by the previous instruction.

9.10 Write data to CGRAM or DDRAM

'Write data' writes binary 8-bit data (D[7] to D[0]) to the CGRAM or the DDRAM.

Whether the CGRAM or DDRAM is to be written to is determined by the previous specification of CGRAM or DDRAM address setting. After writing, the address automatically increments or decrements by 1, in accordance with the 'entry mode set'.
Only bits D[4] to D[0] of CGRAM data are valid, bits D[7] to D[5] are 'don't care'.

9.11 Read data from CGRAM or DDRAM

'Read data' reads binary 8-bit data D[7] to D[0] from the CGRAM or DDRAM.

The most recent 'set address' instruction determines whether the CGRAM or DDRAM is to be read.

The 'read data' instruction gates the content of the Data Register (DR) to the bus while pad E = HIGH. After E goes LOW again, internal operation increments (or decrements) the AC and stores RAM data corresponding to the new AC into the DR.

Remark: the only three instructions that update the DR are:

- 'Set CGRAM address'
- 'Set DDRAM address'
- 'Read data' from CGRAM or DDRAM.

Other instructions (e.g. 'write data', 'cursor/display shift', 'clear display', 'return home') will not change the data register content.

10 INTERFACE TO MICROCONTROLLER (PARALLEL INTERFACE)

The PCF2105 can send data in either two 4-bit modes or one 8-bit mode and can thus interface to 4 or 8-bit microcontrollers.

In the 8-bit mode data is transferred as 8-bit bytes using the 8 data lines DB7 to DB0. The control lines E, RS, and R/$\overline{W}$ are required.

In the 4-bit mode data is transferred in two cycles of 4-bits each. The higher order bits (corresponding to DB7 to DB4 in 8-bit mode) are sent in the first cycle and the lower order bits (DB3 to DB0 in 8-bit mode) in the second cycle. Data transfer is complete after two 4-bit data transfers. It should be noted that two cycles are also required for the busy flag check. The 4-bit mode is selected by instruction.
See Figs 13, 14 and 15 for examples of bus protocol.

In the 4-bit mode, the pads DB3 to DB0 must be left open-circuit. They are pulled up to V_{DD} internally.

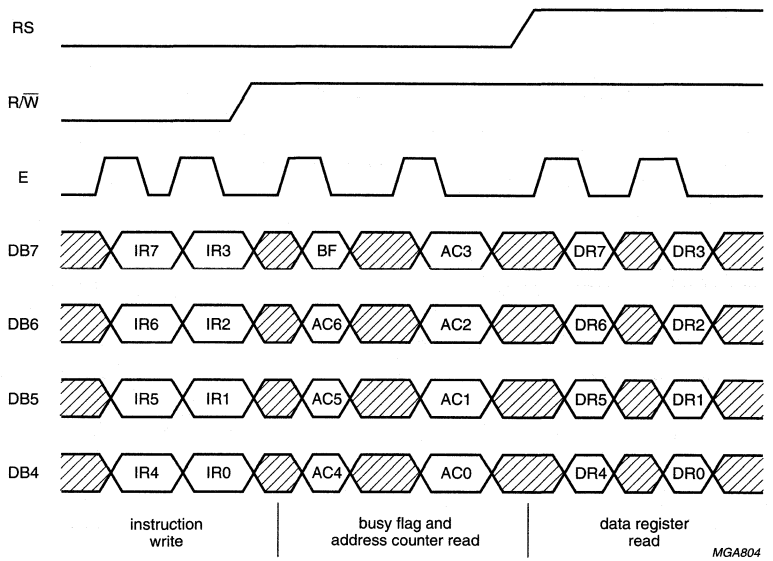
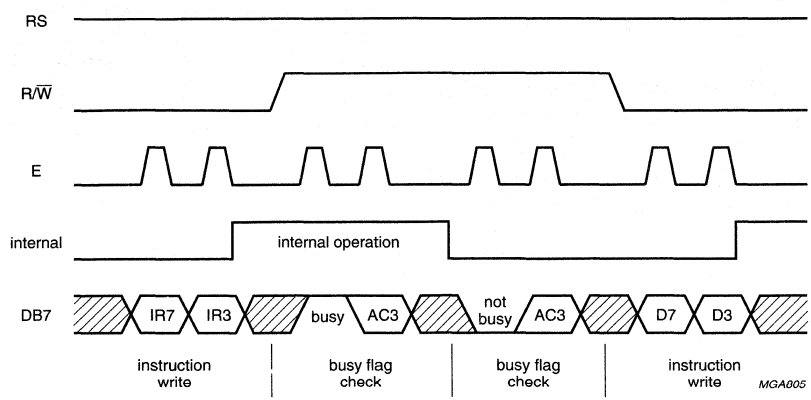


Fig.13 4-bit transfer example.



IR7 and IR3: instruction 7th bit and 3rd bit.
AC3: address counter 3rd bit.

Fig.14 An example of 4-bit data transfer timing sequence.

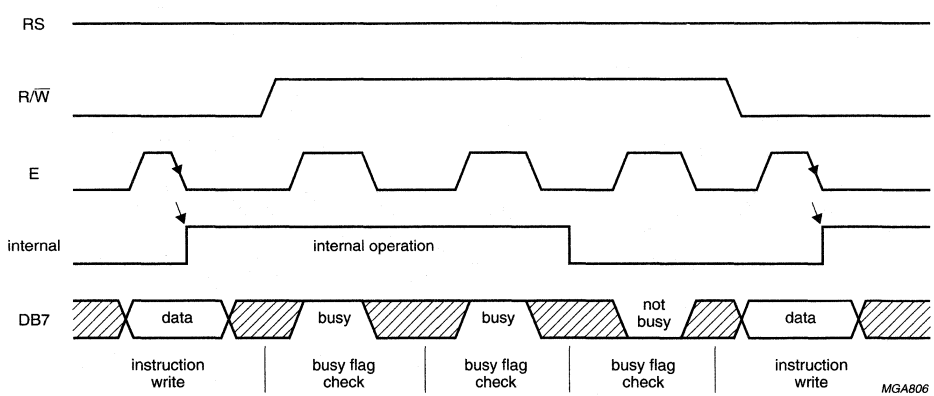


Fig.15 Example of busy flag check timing sequence.

11 INTERFACE TO MICROCONTROLLER (I²C-BUS INTERFACE)

11.1 Characteristics of the I²C-bus

The I²C-bus is for bidirectional, 2-line communication between different ICs or modules. The 2 lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

11.2 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH-level period of the clock pulse as changes in the data line at this time will be interpreted as a control signal (see Fig.16).

11.3 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P) (see Fig.17).

11.4 System configuration

A device generating a message is a transmitter, a device receiving a message is the receiver. The device that controls the message is the master and the devices which are controlled by the master are the slaves (see Fig.18).

11.5 Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of 8 bits is followed by an acknowledge bit. The acknowledge bit is a HIGH signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition (see Fig.19).

11.6 I²C-bus protocol

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always carried out with the first byte transmitted after the start procedure. The I²C-bus configuration for the different PCF2105 read and write cycles is illustrated in Figs 20, 21 and 22.

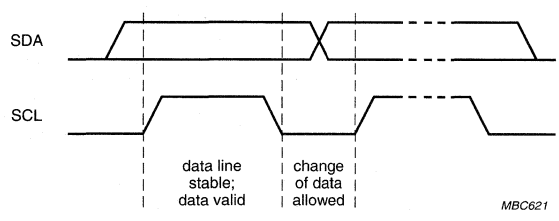


Fig.16 Bit transfer.

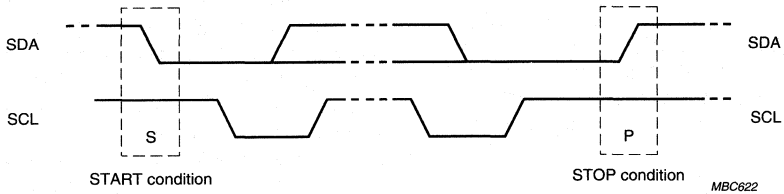


Fig.17 Definition of START and STOP conditions.

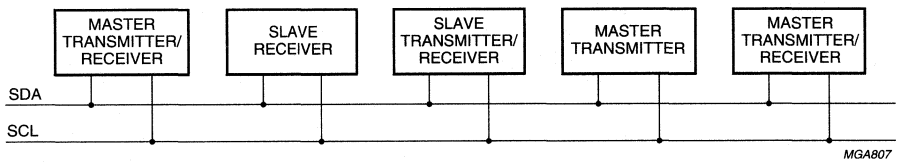


Fig.18 System configuration.

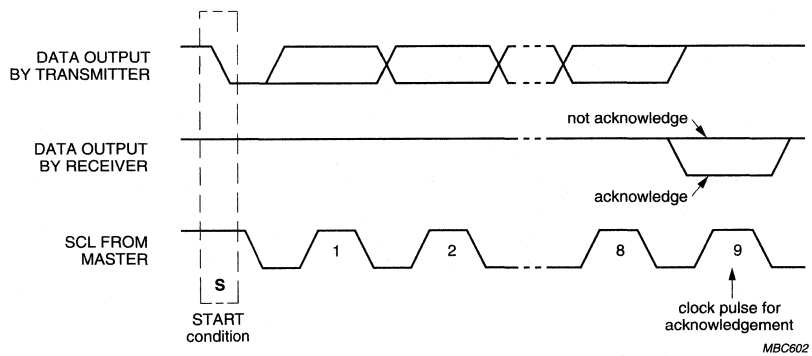


Fig.19 Acknowledgement on the I²C-bus.

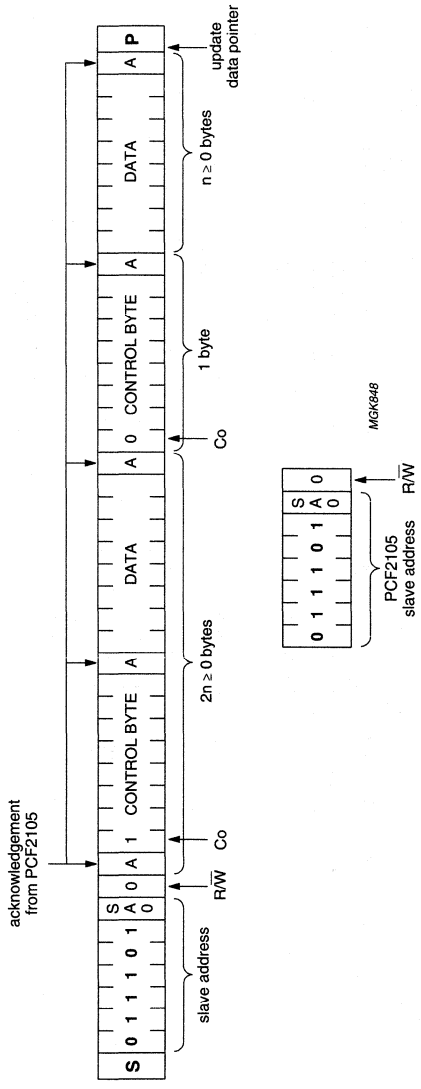
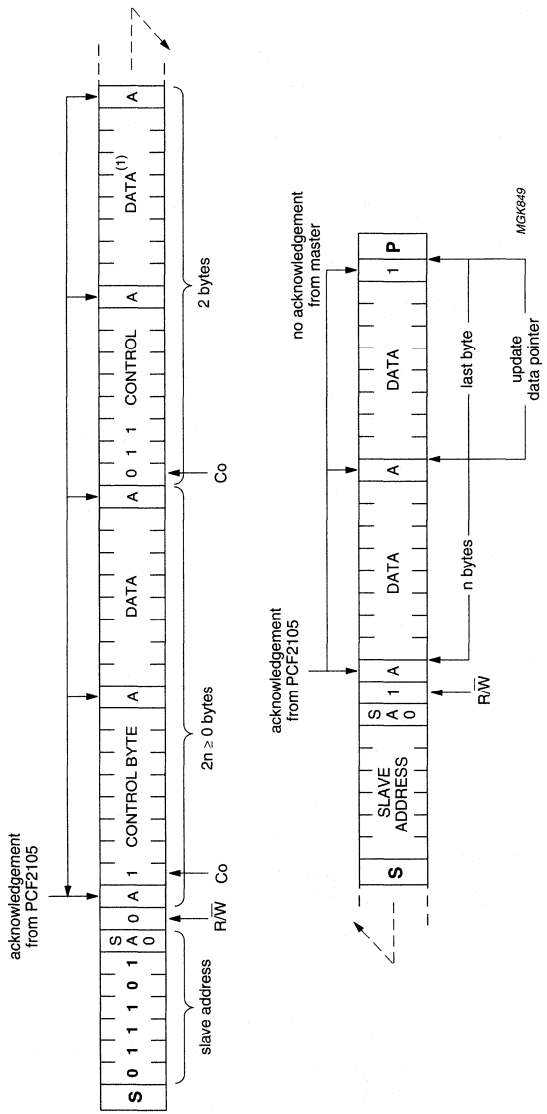


Fig.20 Master transmits to slave receiver; write mode.



(1) Last data byte is a dummy byte (may be omitted).

Fig.21 Master reads after setting word address; write word address, set RS and R/$\overline{W}$; read data.

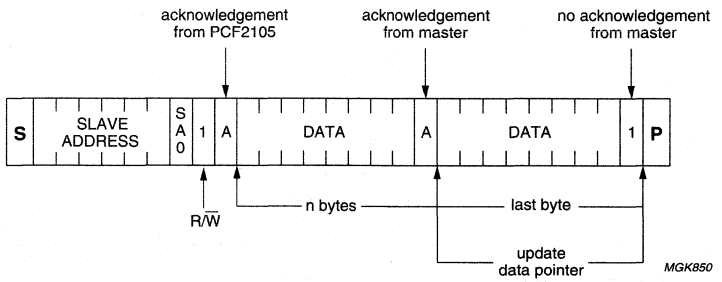


Fig.22 Master reads slave immediately after first byte; read mode (RS previously defined).

12 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	logic supply voltage	−0.5	+8.0	V
V_{LCD}	LCD supply voltage	V_{DD} − 11	V_{DD}	V
$V_{I(n)}$	input voltage on pads OSC, RS, R/$\overline{W}$, E and DB0 to DB7	V_{SS} − 0.5	V_{DD} + 0.5	V
$V_{O(n)}$	output voltage on pads R1 to R32, C1 to C60 and V_{LCD}	V_{LCD} − 0.5	V_{DD} + 0.5	V
$I_{I(n)}$	DC input current on every pad	−10	+10	mA
$I_{O(n)}$	DC output current on every pad	−10	+10	mA
I_n	current on V_{DD}, V_{SS} and V_{LCD}	−50	+50	mA
P_{tot}	total power dissipation	−	400	mW
P/out	power dissipation per output	−	100	mW
T_{stg}	storage temperature	−65	+150	°C

13 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see *"Handling MOS Devices"*).

14 DC CHARACTERISTICS

V_{DD} = 2.5 to 6 V; V_{SS} = 0 V; V_{LCD} = V_{DD} − 3.5 to V_{DD} − 9 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	logic supply voltage		2.5	–	6.0	V
V_{LCD}	LCD supply voltage		V_{DD} − 9	–	V_{DD} − 3.5	V
$I_{DD(ext)}$	external supply current	note 1	–	200	500	μA
		V_{DD} = 5 V; V_{OP} = 9 V; f_{osc} = 150 kHz; T_{amb} = 25 °C	–	200	300	μA
		V_{DD} = 3 V; V_{OP} = 5 V; f_{osc} = 150 kHz; T_{amb} = 25 °C	–	150	200	μA
$I_{I(LCD)}$	input current on V_{LCD}	note 1	–	50	100	μA
V_{POR}	Power-on reset voltage level	note 2	–	1.3	1.8	V
Logic						
V_{IL}	LOW-level input voltage on pads E, RS, R/$\overline{W}$, DB7 to DB0 and SA0		V_{SS}	–	0.3V_{DD}	V
V_{IH}	HIGH-level input voltage on pads E, RS, R/$\overline{W}$, DB7 to DB0 and SA0		0.7V_{DD}	–	V_{DD}	V
$V_{IL(OSC)}$	LOW-level input voltage on pad OSC		V_{SS}	–	V_{DD} − 1.5	V
$V_{IH(OSC)}$	HIGH-level input voltage on pad OSC		V_{DD} − 0.1	–	V_{DD}	V
I_{pu}	pull-up current on pads DB7 to DB0, RS and R/$\overline{W}$	pads set to logic 0 (V_{SS})	0.04	0.15	1.00	μA
$I_{OL(DB)}$	LOW-level output current on pads DB7 to DB0	V_{OL} = 0.4 V; V_{DD} = 5 V	1.6	–	–	mA
$I_{OH(DB)}$	HIGH-level output current on pads DB7 to DB0	V_{OH} = 4 V; V_{DD} = 5 V	−1.0	–	–	mA
I_L	leakage current on pads DB7 to DB0, OSC, E, RS, R/$\overline{W}$ and SA0	pads set to logic 0 (V_{SS}) or logic 1 (V_{DD})	−1	–	+1	μA
I²C-bus						
SDA and SCL						
V_{IL}	LOW-level input voltage	note 3	V_{SS}	–	0.3V_{DD}	V
V_{IH}	HIGH-level input voltage	note 3	0.7V_{DD}	–	V_{DD}	V
I_L	leakage current	pads set to logic 0 (V_{SS}) or logic 1 (V_{DD})	−1	–	+1	μA
C_i	input capacitance	note 4	–	–	7	pF
$I_{OL(SDA)}$	LOW-level output current on SDA	V_{OL} = 0.4 V; V_{DD} = 5 V	3	–	–	mA
LCD outputs						
$R_{o(ROW)}$	row output resistance on pads R32 to R1	note 5	–	1.5	3	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{o(COL)}$	column output resistance on pads C60 to C1	note 5	–	3	6	kΩ
$V_{bias(tol)}$	bias voltage tolerance on pads R32 to R1 and C60 to C1	note 6	–	±20	±130	mV

Notes

1. LCD outputs are open-circuit; inputs at V_{DD} or V_{SS}; bus inactive; internal or external clock with duty factor 50%.
2. Resets all logic when $V_{DD} < V_{POR}$.
3. When the voltages are above V_{DD} or below V_{SS}, an input current may flow; this current must not exceed ±0.5 mA.
4. Tested on sample basis.
5. Resistance of output terminals (R32 to R1 and C60 to C1) with load current I_L = 150 μA; $V_{OP} = V_{DD} - V_{LCD}$ = 9 V; outputs measured one at a time.
6. LCD outputs open-circuit.

15 AC CHARACTERISTICS

V_{DD} = 2.5 to 6.0 V; V_{SS} = 0 V; $V_{LCD} = V_{DD}$ – 3.5 V to V_{DD} – 9 V; T_{amb} = –40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$f_{fr(LCD)}$	LCD frame frequency (internal clock)	note 1	40	65	100	Hz
f_{osc}	oscillator frequency (external clock)		90	150	225	kHz
Bus timing characteristics: Parallel Interface; notes 1 and 2						
WRITE OPERATION (WRITING DATA FROM MICROCONTROLLER TO PCF2105); see Fig.23						
$T_{cy(en)}$	enable cycle time		500	–	–	ns
$t_{W(en)}$	enable pulse width		220	–	–	ns
$t_{su(A)}$	address set-up time		50	–	–	ns
$t_{h(A)}$	address hold time		25	–	–	ns
$t_{su(D)}$	data set-up time		60	–	–	ns
$t_{h(D)}$	data hold time		25	–	–	ns
READ OPERATION (READING DATA FROM PCF2105 TO MICROCONTROLLER); see Fig.24						
$T_{cy(en)}$	enable cycle time		500	–	–	ns
$t_{W(en)}$	enable pulse width		220	–	–	ns
$t_{su(A)}$	address set-up time		50	–	–	ns
$t_{h(A)}$	address hold time		25	–	–	ns
$t_{d(D)}$	data delay time		–	–	150	ns
$t_{h(D)}$	data hold time		20	–	100	ns
Timing characteristics: I^2C-bus interface; note 2; see Fig.25						
f_{SCL}	SCL clock frequency		–	–	400	kHz
t_{SW}	tolerable spike width on bus		–	–	50	ns
t_{BUF}	bus free time		1.3	–	–	μs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{SU;STA}$	set-up time for a repeated START condition		0.6	–	–	µs
$t_{HD;STA}$	START condition hold time		0.6	–	–	µs
t_{LOW}	SCL LOW time		1.3	–	–	µs
t_{HIGH}	SCL HIGH time		0.6	–	–	µs
t_r	SCL and SDA rise time	note 3	–	$20 + RC_L$	300	ns
t_f	SCL and SDA fall time	note 3	–	$20 + RC_L$	300	ns
$t_{SU;DAT}$	data set-up time	note 4	100	–	–	ns
$t_{HD;DAT}$	data hold time	notes 5 and 6	0	–	0.9	µs
$t_{SU;STO}$	set-up time for STOP condition		0.6	–	–	µs
C_L	load capacitance for each bus line		–	–	400	pF

Notes

1. V_{DD} = 5.0 V.
2. All timing values are valid within the operating supply voltage and ambient temperature range and are referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.
3. C_L = total capacitance of one bus line in pF and R = 100 Ω.
4. A fast mode I^2C-bus device can be used in a standard-mode I^2C-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)} + t_{SU;DAT} = 1000 + 250 = 1250$ ns (according to the standard-mode I^2C-bus specification) before the SCL line is released.
5. A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the $V_{IH(min)}$ of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.
6. The maximum $t_{HD;DAT}$ has only to be met if the device does not stretch t_{LOW} of the SCL signal.

16 TIMING DIAGRAMS

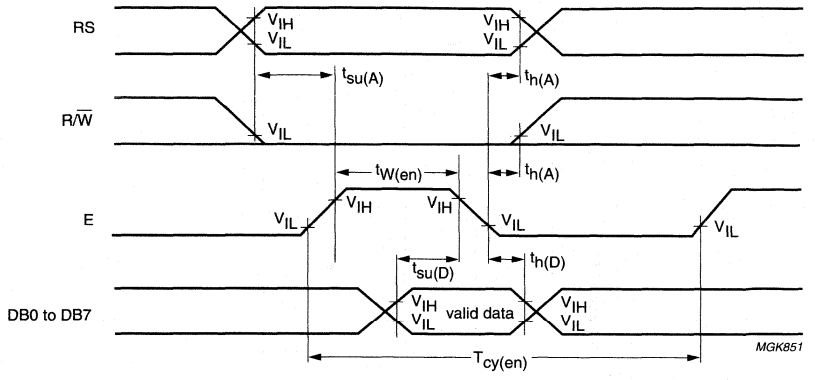


Fig.23 Parallel bus write operation sequence; writing data from microcontroller to PCF2105.

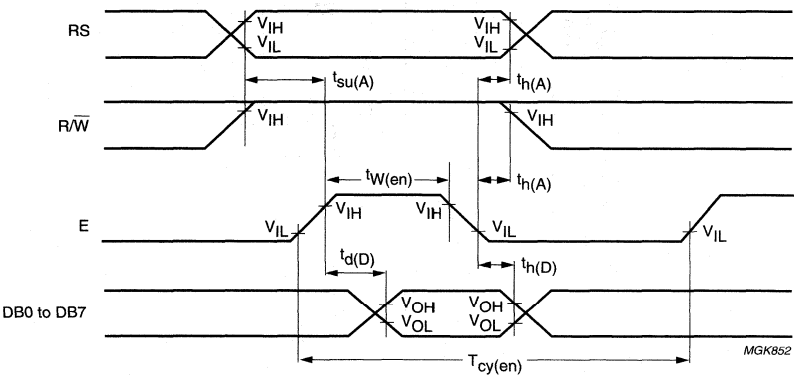


Fig.24 Parallel bus read operation sequence; reading data from PCF2105 to microcontroller.

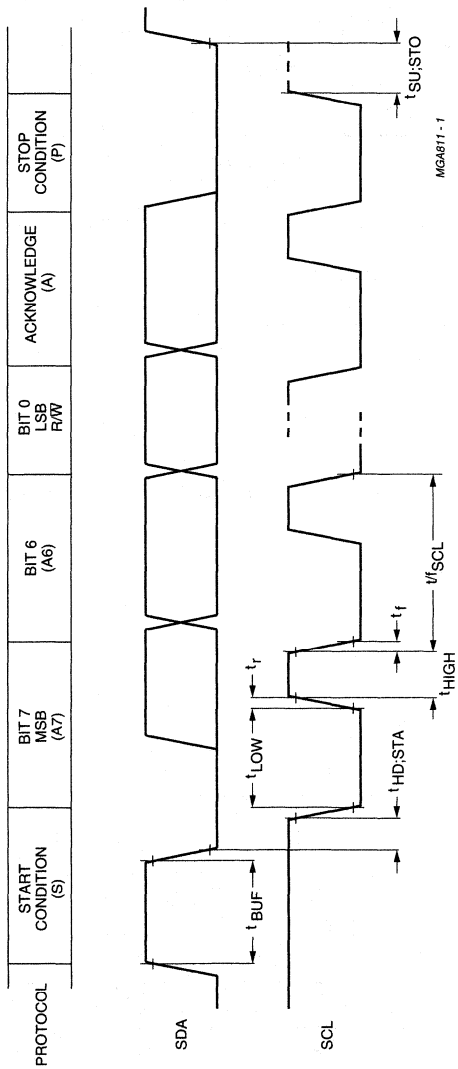


Fig.25 I²C-bus timing diagram; rise and fall times refer to V_{IL} and V_{IH}.

17 APPLICATION INFORMATION

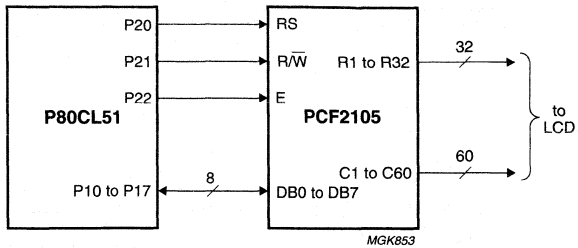


Fig.26 Direct connection to 8-bit microcontroller; 8-bit bus.

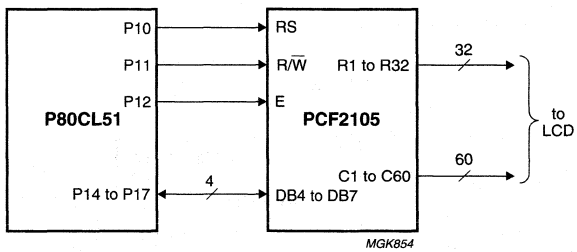


Fig.27 Direct connection to 8-bit microcontroller; 4-bit bus.

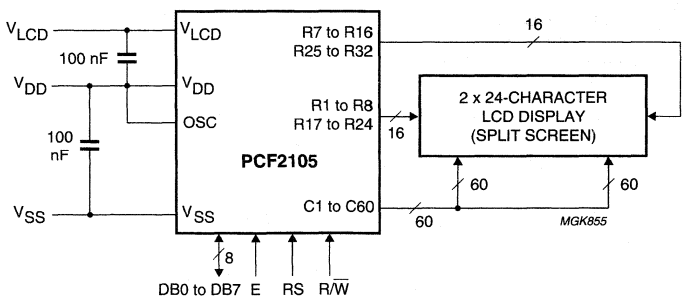


Fig.28 Typical application using parallel interface.

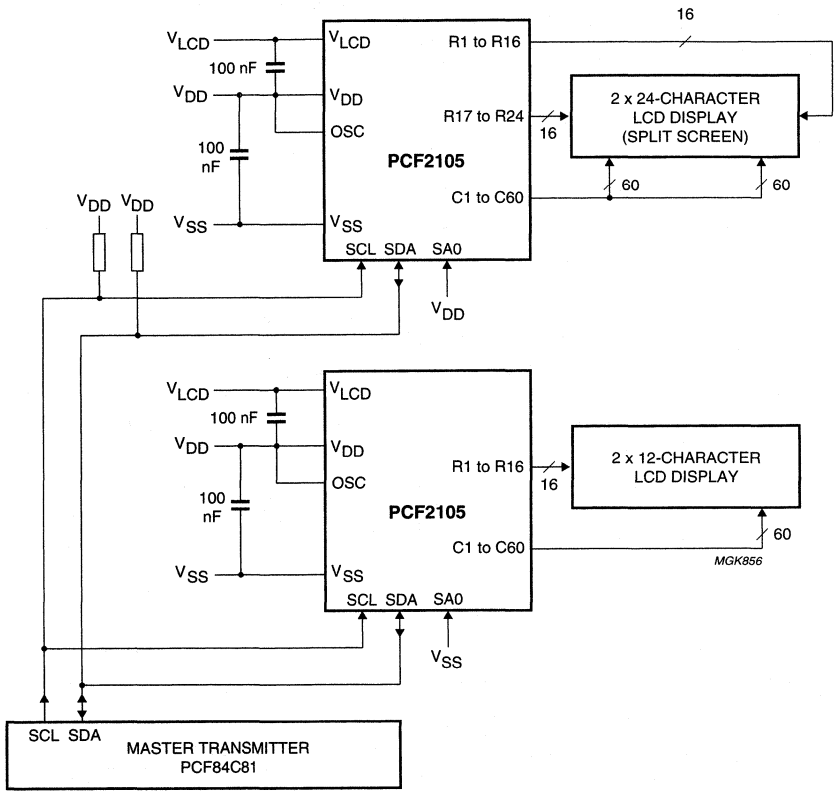


Fig.29 Application using I²C-bus interface.

17.1 4-bit operation, 2 × 12 display using internal reset

The program must set functions prior to 4-bit operation. Table 6 shows an example. When power is turned on, 8-bit operation is automatically selected and the PCF2105 attempts to perform the first write as an 8-bit operation. Since nothing is connected to DB3 to DB0, a rewrite is then required. However, since one operation is completed in two accesses of 4-bit operation, a rewrite is required to set the functions (see Table 6 step 3).

Thus, DB7 to DB4 of the 'function set' are written twice.

17.2 8-bit operation, 2 × 12 display using internal reset

Table 7 shows an example of a 1-line display in 8-bit operation. The PCF2105 functions must be set by the 'function set' instruction prior to display. Since the DDRAM can store data for 80 characters, the RAM can be used for advertising displays when combined with display shift operation. Since the display shift operation changes the display position only DDRAM contents remain unchanged. Display data entered first can be displayed when the 'return home' instruction is performed.

17.3 8-bit operation, 2 × 24 display

For a 2-line display, the cursor automatically moves from the first to the second line after the 40th digit of the first line has been written. Thus, if there are only 8 characters in the first line, the DDRAM address must be set after the 8th character is completed (see Table 8). It should be noted that both lines of the display are always shifted together, data does not shift from one line to the other.

17.4 I^2C-bus operation, 2 × 12 display

A control byte is required with most instructions (see Table 9).

17.5 Initializing by instruction

If the power supply conditions for correctly operating the internal reset circuit are not met, the PCF2105 must be initialized by instruction. Tables 10 and 11 show how this may be performed for 8-bit and 4-bit operation.

Table 6 Example of 4-bit operation; 1-line display; using internal reset

STEP	INSTRUCTION	DISPLAY	OPERATION
1	power supply on (PCF2105 is initialized by the internal reset circuit)		initialized; no display appears
2	function set RS R/$\overline{W}$ DB7 DB6 DB5 DB4 0 0 0 0 1 0		sets to 4-bit operation; in this instance operation is handled as 8-bits by initialization and only this instruction completes with one write
3	function set RS R/$\overline{W}$ DB7 DB6 DB5 DB4 0 0 0 0 1 0		sets to 4-bit operation; selects 2 × 12 display
	0 0 0 0 0 0		4-bit operation starts from this point and resetting is needed
4	display control RS R/$\overline{W}$ DB7 DB6 DB5 DB4 0 0 0 0 0 0	_	turns display and cursor on
	0 0 1 1 1 0		entire display is blank after initialization
5	entry mode set RS R/$\overline{W}$ DB7 DB6 DB5 DB4 0 0 0 0 0 0	_	sets mode to increment the address by 1 and to shift the cursor to the right at the time of write to the DDRAM or CGRAM
	0 0 0 1 1 0		display is not shifted
6	write data to CGRAM or DDRAM RS R/$\overline{W}$ DB7 DB6 DB5 DB4 1 0 1 1 0 1	P_	writes 'P'; the DDRAM has already been selected by initialization at power-on
	1 0 0 1 1 0		the cursor is incremented by 1 and shifted to the right

Table 7 Example of 8-bit operation; 1-line display; using internal reset (character set 'M')

STEP	INSTRUCTION	DISPLAY	OPERATION
1	power supply on (PCF2105 is initialized by the internal reset function)		initialized; no display appears
2	function set RS R/$\overline{W}$ DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 1 1 0 0 0 0		sets to 8-bit operation; selects 2 × 12 display
3	display control RS R/$\overline{W}$ DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 0 0 1 1 1 0	_	turns display and cursor on; entire display is blank after initialization
4	entry mode set RS R/$\overline{W}$ DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 0 0 0 1 1 0	_	sets mode to increment the address by 1 and to shift the cursor to the right at the time of the write to the DDRAM or CGRAM; display is not shifted
5	write data to CGRAM or DDRAM RS R/$\overline{W}$ DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 1 1 0 1 0 0 0 0	**P**_	writes 'P'; the DDRAM has already been selected by initialization at power-on; the cursor is incremented by 1 and shifted to the right
6	write data to CGRAM or DDRAM RS R/$\overline{W}$ DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 1 1 0 0 1 0 0 0	**PH**_	writes 'H'
7			
8	write data to CGRAM or DDRAM RS R/$\overline{W}$ DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 1 1 0 1 0 0 1 1	**PHILIPS**_	writes 'S'
9	entry mode set RS R/$\overline{W}$ DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 0 0 0 1 1 1	**PHILIPS**_	sets mode for display shift at the time of write
10	write data to CGRAM or DDRAM RS R/$\overline{W}$ DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 0 0 1 0 0 0 0 0	**HILIPS**_	writes space
11	write data to CGRAM or DDRAM RS R/$\overline{W}$ DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 1 1 0 0 1 1 0 1	**ILIPS M**_	writes 'M'

STEP	INSTRUCTION	DISPLAY	OPERATION
12		⋮	
13	write data to CGRAM or DDRAM RS R/$\overline{W}$ DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 1 1 0 0 1 1 1 1	**MICROKO_**	writes 'O'
14	cursor or display shift RS R/$\overline{W}$ DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 0 1 0 0 0 0	**MICROKO**	shifts only the cursor position to the left
15	cursor or display shift RS R/$\overline{W}$ DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 0 1 0 0 0 0	**MICROKO**	shifts only the cursor position to the left
16	write data to CGRAM or DDRAM RS R/$\overline{W}$ DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 0 1 0 0 0 0 1 1	**ICROCO**	writes 'C' (correction); the display moves to the left
17	cursor or display shift RS R/$\overline{W}$ DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 0 1 1 1 0 0	**MICROCO**	shifts the display and cursor to the right
18	cursor or display shift RS R/$\overline{W}$ DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 0 1 0 1 0 0	**MICROCO_**	shifts only the cursor to the right
19	write data to CGRAM or DDRAM RS R/$\overline{W}$ DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 1 1 0 0 1 1 0 1	**ICROCOM_**	writes 'M'
20		⋮	
21	return home RS R/$\overline{W}$ DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 0 0 0 0 1 0	**PHILIPS M**	returns both display and cursor to the original position (address 0)

Table 8 Example of 8-bit operation; 2-line display; using internal reset

STEP	INSTRUCTION	DISPLAY	OPERATION
1	power supply on (PCF2105 is initialized by the internal reset function)		initialized; no display appears
2	function set RS R/$\overline{W}$ DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 1 1 1 0 0 0		sets to 8-bit operation; selects 2 × 24 display
3	display control RS R/$\overline{W}$ DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 0 0 1 1 1 0		turns display and cursor on; entire display is blank after initialization
4	entry mode set RS R/$\overline{W}$ DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 0 0 0 1 1 0	_	sets mode to increment the address by 1 and to shift the cursor to the right at the time of write to the CGRAM or DDRAM; display is not shifted
5	write data to CGRAM or DDRAM RS R/$\overline{W}$ DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 1 1 0 1 0 0 0 0	**P**_	writes 'P'; the DDRAM has already been selected by initialization at power-on; the cursor is incremented by 1 and shifted to the right
6			
7	write data to CGRAM or DDRAM RS R/$\overline{W}$ DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 1 1 0 1 0 0 1 1	**PHILIPS**_	writes 'S'
8	set DDRAM address RS R/$\overline{W}$ DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 1 1 0 0 0 0 0 0	**PHILIPS** _	sets DDRAM address to position the cursor at the head of the 2nd line
9	write data to CGRAM or DDRAM RS R/$\overline{W}$ DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 1 1 0 0 1 1 0 1	**PHILIPS** **M**_	writes 'M'
10			
11	write data to CGRAM or DDRAM RS R/$\overline{W}$ DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 1 1 0 0 1 1 1 1	**PHILIPS** **MICROCO**_	writes 'O'

STEP	INSTRUCTION	DISPLAY	OPERATION
12	write data to CGRAM or DDRAM RS R/$\overline{W}$ DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 0 0 0 1 1 1	**PHILIPS** **MICROCO_**	sets mode for display shift at the time of write
13	write data to CGRAM or DDRAM RS R/$\overline{W}$ DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 1 1 0 0 1 1 0 1	**HILIPS** **ICROCOM_**	writes 'M'; display is shifted to the left; the first and second lines shift together
14			
15	return home RS R/$\overline{W}$ DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 0 0 0 0 1 0	**PHILIPS** **MICROCOM**	returns both display and cursor to the original position (address 0)

Table 9 Example of I²C-bus operation; 1-line display; using internal reset (assuming SA0 = V_{SS}); note 1

STEP	INSTRUCTION	DISPLAY	OPERATION
1	I²C-bus start		initialized; no display appears
2	slave address for write SA6 SA5 SA4 SA3 SA2 SA1 SA0 R/$\overline{W}$ Ack 0 1 1 1 0 1 0 0 1		during the acknowledge cycle SDA will be pulled-down by the PCF2105
3	send a control byte for function set Co RS R/$\overline{W}$ Ack 0 0 0 1		control byte sets RS and R/$\overline{W}$ for following data bytes
4	function set DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 0 1 X 0 0 0 0 1		selects 1-line display; SCL pulse during acknowledge cycle starts execution of instruction
5	display control DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 0 0 0 1 1 1 0 1	_	turns display and cursor on; entire display shows character hexadecimal 20 (blank in ASCII-like character sets)
6	entry mode set DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 0 0 0 0 1 1 0 1	_	sets mode to increment the address by 1 and to shift the cursor to the right at the time of write to the DDRAM or CGRAM; display is not shifted

STEP	INSTRUCTION	DISPLAY	OPERATION
7	I^2C-bus start	_	for writing data to DDRAM, RS must be set to logic 1; therefore a control byte is needed
8	slave address for write SA6 SA5 SA4 SA3 SA2 SA1 SA0 R/$\overline{W}$ Ack 0 1 1 1 0 1 0 0 1	_	
9	send a control byte for write data Co RS R/$\overline{W}$ Ack 0 1 0 1	_	
10	write data to DDRAM DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 1 1 0 1 0 0 0 0 1	**P**_	writes 'P'; the DDRAM has been selected at power-up; the cursor is incremented by 1 and shifted to the right
11	write data to DDRAM DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 1 1 0 0 1 0 0 0 1	**PH**_	writes 'H'
12 to 15		| | | |	
16	write data to DDRAM DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 1 1 0 1 0 0 1 1 1	**PHILIPS**_	writes 'S'
17	(optional I^2C-bus stop) I^2C-bus start + slave address for write (as step 8)	**PHILIPS**_	
18	control byte Co RS R/$\overline{W}$ Ack 1 0 0 1	**PHILIPS**_	
19	return home DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 0 0 0 0 0 1 0 1	**PHILIPS**	sets DDRAM address 0 in AC; also returns shifted display to original position; DDRAM contents unchanged; this instruction does not update the DR
20	control byte for read Co RS R/$\overline{W}$ Ack 0 1 1 1	**PHILIPS**	DDRAM content will be read from following instructions; the R/$\overline{W}$ has to be set to logic 1 while still in I^2C-bus write mode
21	I^2C-bus start	**PHILIPS**	

STEP	INSTRUCTION	DISPLAY	OPERATION
22	slave address for read SA6 SA5 SA4 SA3 SA2 SA1 SA0 R/$\overline{W}$ Ack 0 1 1 1 0 1 0 1 1	**PHILIPS**	during the acknowledge cycle the content of the DR is loaded into the internal I²C-bus interface and to be shifted out; in the previous instruction neither a 'set address' nor a 'read data' has been performed; therefore the content of the DR was unknown
23	read data: 8 × SCL + master acknowledge; note 2 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack X X X X X X X X 1	**PHILIPS**	8 × SCL; content loaded into interface during previous acknowledge cycle and shifted out over SDA; MSB is DB7; during master acknowledge content of DDRAM address 01 is loaded into the I²C-bus interface
24	read data: 8 × SCL + master acknowledge; note 2 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 1 0 0 1 0 0 0 0	**PHILIPS**	8 × SCL; code of letter 'H' is read first; during master acknowledge code of letter 'I' is loaded into the I²C-bus interface
25	read data: 8 × SCL + no master acknowledge; note 2 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 1 0 0 1 0 0 1 1	**PHILIPS**	no master acknowledge; after the content of the I²C-bus interface register is shifted out no internal action is performed; no new data is loaded to the interface register; DR is not updated; AC is not incremented and cursor is not shifted
26	I²C-bus stop	**PHILIPS**	

Notes

1. X = don't care.
2. SDA is left at high-impedance by the microcontroller during the READ acknowledge.

Table 10 Initialization by instruction; 8-bit interface (note 1)

STEP										DESCRIPTION
Power-on or unknown state										
|										
Wait 2 ms after V_{DD} rises above V_{POR}										
|										
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	BF cannot be checked before this instruction; function set (interface is 8-bits long)
0	0	0	0	1	1	X	X	X	X	
|										
Wait 2 ms										
|										
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	BF cannot be checked before this instruction; function set (interface is 8-bits long)
0	0	0	0	1	1	X	X	X	X	
|										
Wait more than 40 µs										
|										
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	BF cannot be checked before this instruction; function set (interface is 8-bits long)
0	0	0	0	1	1	X	X	X	X	
|										BF can be checked after the following instructions; when BF is not checked, the waiting time between instructions is the specified instruction time (see Table 3)
|										
|										
|										
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	function set (interface is 8-bits long); specify the number of display lines
0	0	0	0	1	1	N	M	X	0	
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	display off
0	0	0	0	0	0	1	0	0	0	
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	clear display
0	0	0	0	0	0	0	0	0	1	
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	entry mode set
0	0	0	0	0	0	0	1	I/D	S	
|										
Initialization ends										

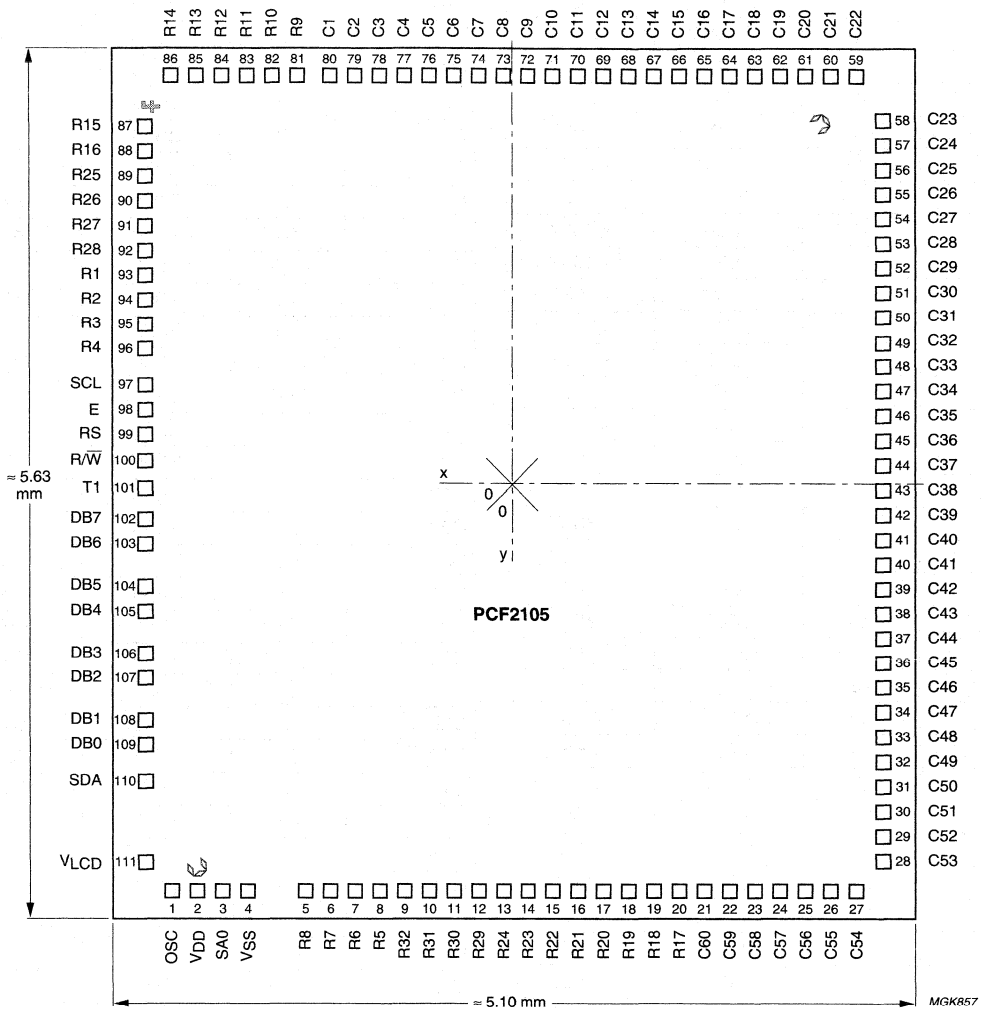
Note

1. X = don't care.

Table 11 Initialization by instruction; 4-bit interface; not applicable for I²C-bus operation

STEP						DESCRIPTION
Power-on or unknown state						
Wait 2 ms after V_{DD} rises above V_{POR}						
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	BF cannot be checked before this instruction; function set (interface is 8-bits long)
0	0	0	0	1	1	
Wait 2 ms						
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	BF cannot be checked before this instruction; function set (interface is 8-bits long)
0	0	0	0	1	1	
Wait 40 µs						
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	BF cannot be checked before this instruction; function set (interface is 8-bits long)
0	0	0	0	1	1	
						BF can be checked after the following instructions; when BF is not checked, the waiting time between instructions is the specified instruction time (see Table 3)
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	function set (set interface to 4-bits long); interface is 8-bits long
0	0	0	0	1	0	
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	function set (interface is 4-bits long)
0	0	0	0	1	0	
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	specify number of display lines and voltage generator characteristic
0	0	N	M	0	0	
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	display off
0	0	0	0	0	0	
0	0	1	0	0	0	
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	clear display
0	0	0	0	0	0	
0	0	1	0	0	0	
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	entry mode set
0	0	0	0	0	0	
0	0	0	1	I/D	S	
Initialization ends						

18 BONDING PAD LOCATIONS



Chip dimensions: approximately 5.10 × 5.63 mm.
Gold bump dimensions: approximately 89 × 89 × 25 µm.

Fig.30 Bonding pad locations.

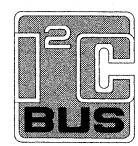
Table 12 Bonding pad locations (dimensions in μm); all x/y coordinates are referenced to centre of chip, see Fig.30

SYMBOL	PAD	x	y
OSC	1	−2184.5	−2637
V_{DD}	2	−2024.5	−2637
SA0	3	−1864.5	−2637
V_{SS}	4	−1704.5	−2637
R8	5	−1339	−2637
R7	6	−1179	−2637
R6	7	−1019	−2637
R5	8	−859	−2637
R32	9	−699	−2637
R31	10	−539	−2637
R30	11	−379	−2637
R29	12	−219	−2637
R24	13	−59	−2637
R23	14	101	−2637
R22	15	261	−2637
R21	16	421	−2637
R20	17	581	−2637
R19	18	741	−2637
R18	19	901	−2637
R17	20	1061	−2637
C60	21	1221	−2637
C59	22	1381	−2637
C58	23	1541	−2637
C57	24	1701	−2637
C56	25	1861	−2637
C55	26	2021	−2637
C54	27	2181	−2637
C53	28	2350	−2445
C52	29	2350	−2285
C51	30	2350	−2125
C50	31	2350	−1965
C49	32	2350	−1805
C48	33	2350	−1645
C47	34	2350	−1485
C46	35	2350	−1325
C45	36	2350	−1165
C44	37	2350	−1005
C43	38	2350	−845

SYMBOL	PAD	x	y
C42	39	2350	−685
C41	40	2350	−525
C40	41	2350	−365
C39	42	2350	−205
C38	43	2350	−45
C37	44	2350	115
C36	45	2350	275
C35	46	2350	435
C34	47	2350	595
C33	48	2350	755
C32	49	2350	915
C31	50	2350	1075
C30	51	2350	1235
C29	52	2350	1395
C28	53	2350	1555
C27	54	2350	1715
C26	55	2350	1875
C25	56	2350	2035
C24	57	2350	2195
C23	58	2350	2355
C22	59	2185	2637.5
C21	60	2025	2637.5
C20	61	1865	2637.5
C19	62	1705	2637.5
C18	63	1545	2637.5
C17	64	1385	2637.5
C16	65	1225	2637.5
C15	66	1065	2637.5
C14	67	905	2637.5
C13	68	745	2637.5
C12	69	585	2637.5
C11	70	425	2637.5
C10	71	265	2637.5
C9	72	105	2637.5
C8	73	−55	2637.5
C7	74	−215	2637.5
C6	75	−375	2637.5
C5	76	−535	2637.5

SYMBOL	PAD	x	y
C4	77	−695	2637.5
C3	78	−855	2637.5
C2	79	−1015	2637.5
C1	80	−1175	2637.5
R9	81	−1385	2637.5
R10	82	−1545	2637.5
R11	83	−1705	2637.5
R12	84	−1865	2637.5
R13	85	−2025	2637.5
R14	86	−2185	2637.5
R15	87	−2349	2308
R16	88	−2349	2148
R25	89	−2349	1988
R26	90	−2349	1828
R27	91	−2349	1668
R28	92	−2349	1508
R1	93	−2349	1348
R2	94	−2349	1188
R3	95	−2349	1028
R4	96	−2349	868
SCL	97	−2349	632
E	98	−2349	472
RS	99	−2349	312
R/$\overline{W}$	100	−2349	142
T1	101	−2349	−34
DB7	102	−2349	−233
DB6	103	−2349	−393
DB5	104	−2349	−668
DB4	105	−2349	−828
DB3	106	−2349	−1103
DB2	107	−2349	−1263
DB1	108	−2349	−1538
DB0	109	−2349	−1698
SDA	110	−2349	−1933
V_{LCD}	111	−2349	−2453
RECPAT 'F'	–	−2327.5	2427.5
RECPAT 'C'	–	−2027.5	−2512.5
RECPAT 'C'	–	1982.5	2297.5

CONTENTS



1 FEATURES

- Single-chip LCD controller/driver
- 2-line display of up to 12 characters + 120 icons, or 1-line display of up to 24 characters + 120 icons
- 5 × 7 character format plus cursor; 5 × 8 for kana (Japanese syllabary) and user defined symbols
- Icon mode: reduced current consumption while displaying icons only(1)
- Icon blink function
- On-chip:
  - generation of LCD supply voltage, programmable by instruction (external supply also possible)
  - temperature compensation of on-chip generated V_{LCD}: −8 to −12 mV/K at 5.0 V (programmable by instruction)
  - generation of intermediate LCD bias voltages
  - oscillator requires no external components (external clock also possible)
- Display data RAM: 80 characters
- Character generator ROM: 240, 5 × 8 characters
- Character generator RAM: 16, 5 × 8 characters; 3 characters used to drive 120 icons, 6 characters used if icon-blink feature is used in application
- 4 or 8-bit parallel bus and 2-wire I²C-bus interface
- CMOS compatible
- 18 row, 60 column outputs
- MUX rates 1 : 18 (for normal operation) and 1 : 2 (for icon-only mode)
- Uses common 11 code instruction set (extended)
- Logic supply voltage range, $V_{DD} - V_{SS}$ = 1.8 to 4.0 V (up to 5.5 V if external V_{LCD} is used); chip may be driven with two battery cells
- Display supply voltage range, $V_{LCD} - V_{SS}$ = 2.2 to 6.5 V
- Very low current consumption (20 to 200 μA):
  - icon mode: <25 μA
  - power-down mode: <2.5 μA.

(1) Icon mode is used to save current. When only icons are displayed, a much lower operating voltage V_{LCD} can be used and the switching frequency of the LCD outputs is reduced. In most applications it is possible to use V_{DD} as V_{LCD}. Never use the voltage generator in icon mode.

2 APPLICATIONS

- Telecom equipment
- Portable instruments
- Point-of-sale terminals.

3 GENERAL DESCRIPTION

The PCF2113x is a low power CMOS LCD controller and driver, designed to drive a dot matrix LCD display of 2 line by 12 and 1 line by 24 characters with 5 × 8 dot format. All necessary functions for the display are provided in a single chip, including on-chip generation of LCD bias voltages, resulting in a minimum of external components and lower system current consumption. The PCF2113x interfaces to most microcontrollers via a 4 or 8-bit bus or via the 2-wire I²C-bus. The chip contains a character generator and displays alphanumeric and kana (Japanese) characters. Three character sets (A, D and E) are currently available (see Figs 7, 8 and 9). Various other character sets can be manufactured on request.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF2113AU/10/F2	–	chip on flexible film carrier	–
PCF2113DU/10/F2	–	chip on flexible film carrier	–
PCF2113DU/F2	–	chip in tray	–
PCF2113DH/F2	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
PCF2113EU/2/F2	–	chip with bumps in tray	–

5 BLOCK DIAGRAM

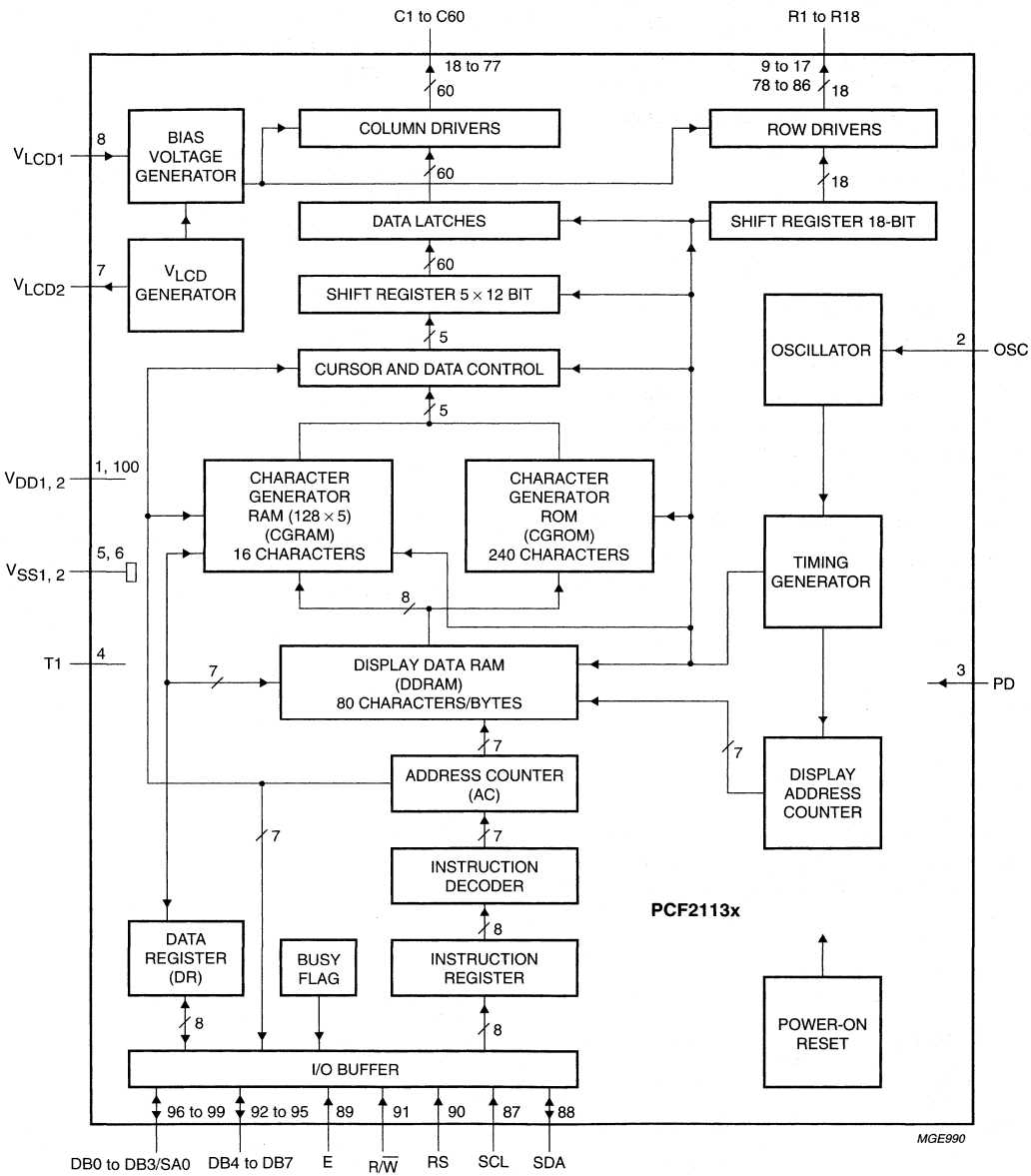


Fig.1 Block diagram.

6 PINNING

SYMBOL	PIN	TYPE	DESCRIPTION
V_{DD1}	1	P	supply voltage for all except high voltage generator
OSC	2	I	oscillator/external clock input
PD	3	I	power-down pad input
T1	4	I	test pad (connected to V_{SS})
V_{SS1}	5	P	ground for all except high voltage generator
V_{SS2}	6	P	ground for high voltage generator
V_{LCD2}	7	O	V_{LCD} output; note 1
V_{LCD1}	8	I	V_{LCD} input; note 2
R9 to R16	9 to 16	O	LCD row driver outputs 9 to 16
R18	17	O	LCD row driver output 18
C60 to C1	18 to 77	O	LCD column driver outputs 60 to 1
R8 to R1	78 to 85	O	LCD row driver outputs 8 to 1
R17	86	O	LCD row driver output 17
SCL	87	I	I^2C serial clock input
SDA	88	I/O	I^2C serial data input/output
E	89	I	data bus clock input
RS	90	I	register select input
R/$\overline{W}$	91	I	read/write input
DB7	92	I/O	1 bit of 8-bit bidirectional data bus
DB6	93	I/O	1 bit of 8-bit bidirectional data bus
DB5	94	I/O	1 bit of 8-bit bidirectional data bus
DB4	95	I/O	1 bit of 8-bit bidirectional data bus
DB3/SA0	96	I/O	1 bit of 8-bit bi-directional data bus/I^2C address pin
DB2	97	I/O	1 bit of 8-bit bidirectional data bus
DB1	98	I/O	1 bit of 8-bit bidirectional data bus
DB0	99	I/O	1 bit of 8-bit bidirectional data bus
V_{DD2}	100	P	supply voltage for high voltage generator; note 3

Notes

1. This is the V_{LCD} output pin, if V_{LCD} is generated internally and has to be connected to V_{LCD1}. If V_{LCD1} is generated externally, V_{LCD2} has to be left open or connected to ground.
2. This is the voltage used for the generation of LCD bias levels.
3. This is the supply for the high voltage generator. If V_{LCD} is generated externally, connect V_{DD2} to V_{SS}.

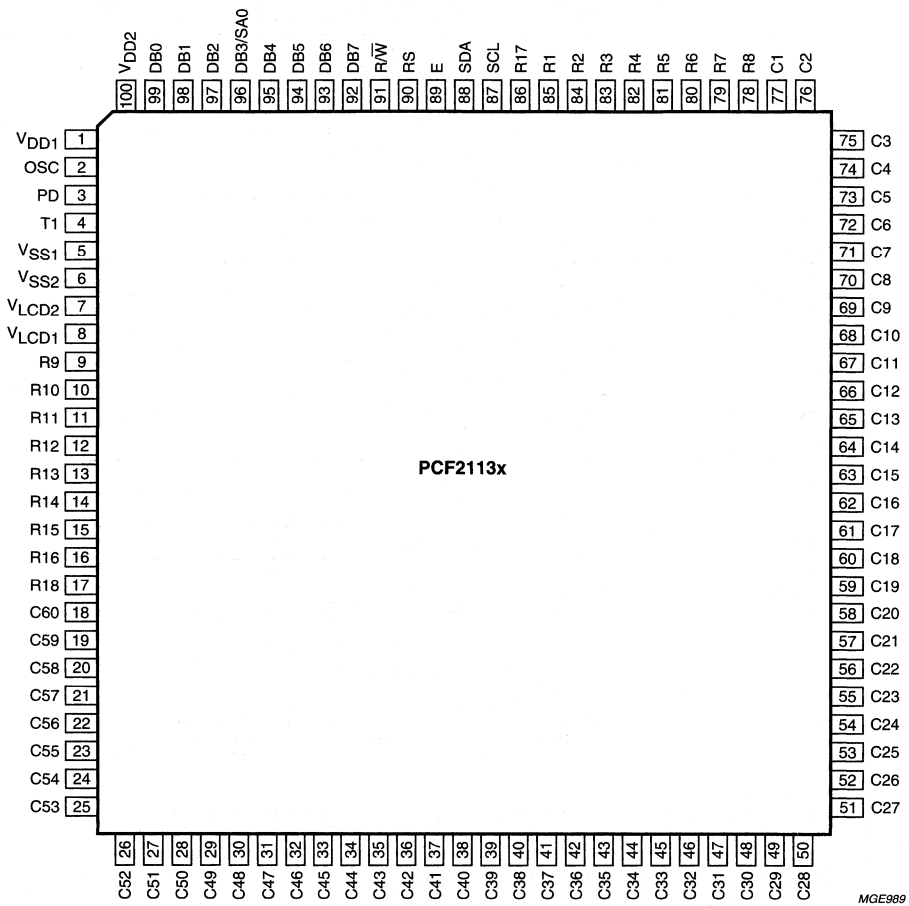


Fig.2 Pin configuration (LQFP100).

7 PIN FUNCTIONS

NAME	FUNCTION	DESCRIPTION
RS	register select	RS selects the register to be accessed for read and write when the device is controlled by the parallel interface. There is an internal pull-up on this pin. RS = logic 0 selects the instruction register for write and the Busy Flag and Address Counter for read. RS = logic 1 selects the data register for both read and write.
R/$\overline{W}$	read/write	R/$\overline{W}$ selects either the read (R/$\overline{W}$ = logic 1) or write (R/$\overline{W}$ = logic 0) operation when the device is controlled by the parallel interface. There is an internal pull-up on this pin.
E	data bus clock	The E pin is set HIGH to signal the start of a read or write operation when the device is controlled by the parallel interface. Data is clocked in or out of the chip on the negative edge of the clock. Note that this pin must be tied to logic 0 (V_{SS}) when I^2C-bus control is used.
DB7 to DB0	data bus	The parallel interface of the device. This bi-directional, 3-state data bus transfers data between the system controller and the PCF2113x. There is an internal pull-up on each of the data lines. DB7 to DB0 must be connected to V_{DD} or left open circuit when I^2C-bus control is used. Note that DB3 shares the same pin as SA0. In 4-bit operations only DB7 to DB4 are used, and DB3 to DB0 must be left open circuit. See note 1. DB7 may be used as the Busy Flag, signalling that internal operations are not yet completed.
C1 to C60	column driver outputs	These pins output the data for columns.
R1 to R18	row driver outputs	These pins output the row select waveforms to the display. R17 and R18 drive the icons.
V_{LCD}	LCD power supply	Positive power supply for the liquid crystal display. This may be generated on-chip or supplied externally.
OSC	oscillator	When the on-chip oscillator is used this pin must be connected to V_{DD}. An external clock signal, if used, is input at this pin.
SCL	serial clock line	Input for the I^2C-bus clock signal. SCL must be connected to V_{SS} or V_{DD} when the parallel interface is used.
SDA	serial data line	I/O for the I^2C-bus data line. SDA must be connected to V_{SS} or V_{DD} when the parallel interface is used.
SA0	address pin	The hardware sub-address line is used to program the device sub-address for two different PCF2113xs on the same I^2C bus. Note that SA0 shares the same pin as DB3.
T1	test pad	T1 must be connected to V_{SS} and is not user accessible.
PD	power-down pad	PD selects chip power-down mode. For normal operation PD = logic 0.

Note

1. If the 4-bit interface is used without reading out from the PCF2113x (i.e. R/$\overline{W}$ is set permanently to logic 0), the unused ports DB0 to DB3 can either be set to V_{SS} or V_{DD} instead of leaving them open.

8 FUNCTIONAL DESCRIPTION (see Fig.1)

8.1 LCD supply voltage generator

The LCD supply voltage may be generated on-chip. The voltage generator is controlled by two internal 6-bit registers, V_A and V_B. The nominal LCD operating voltage at room temperature is given by the relationships:

$V_{OP(nom)}$ = [(integer value of register) × 0.08 + 1.9] V

8.2 Programming ranges (T_{ref} = 27 °C)

Programmed value range: 1 to 63.
Voltage range: 1.90 to 6.84 V.

Values producing more than 6.5 V at operating temperature are not allowed. Operation above this voltage may damage the device. When programming the operating voltage the V_{LCD} temperature coefficient must be taken into account.

Values below 2.2 V are below the specified operating range of the chip and are therefore not allowed.

Value 0 for V_A and V_B switches the generator off.

Usually register V_A is programmed with the voltage for character mode and register V_B with the voltage for icon mode. V_B must be programmed to FF in character mode and V_A must be programmed to 00 in icon mode.

When V_{LCD} is generated on-chip the V_{LCD} pins should be decoupled to V_{SS} with a suitable capacitor. The generated V_{LCD} is independent of V_{DD} and is temperature compensated. When the generator is switched off an external voltage may be supplied at connected pins $V_{LCD1,2}$. $V_{LCD1,2}$ may be higher or lower than V_{DD} if external V_{LCD} is used. **If internally generated it must not be lower than V_{DD}** and $V_{DD} \leq 4$ V.

8.3 LCD bias voltage generator

The intermediate bias voltages for the LCD display are also generated on-chip. This removes the need for an external resistive bias chain and significantly reduces the system current consumption. The optimum value of V_{LCD} depends on the multiplex rate, the LCD threshold voltage (V_{th}) and the number of bias levels and is given by the relationships given in Tables 1 and 2. Using a 5-level bias scheme for 1 : 18 maximum rate allows V_{LCD} < 5 V for most LCD liquids.

Table 1 Optimum/maximum values for V_{OP} (off pixels start darkening; $V_{off} = V_{th}$)

MUX RATE	NUMBER OF LEVELS	V_{on}/V_{th}	V_{OP}/V_{th}	V_{OP} (typical; for V_{th} = 1.4 V)
1 : 18	5	1.272	3.7	5.2 V
1 : 2	3	2.236	2.283	3.9 V

Table 2 Minimum values for V_{OP} (on pixels clearly visible; $V_{on} > V_{th}$)

MUX RATE	NUMBER OF LEVELS	V_{on}/V_{th}	V_{OP}/V_{th}	V_{OP} (typical; for V_{th} = 1.4 V)
1 : 18	5	1.12	3.2	4.6 V
1 : 2	3	1.2	1.5	2.1 V

8.4 Oscillator

The on-chip oscillator provides the clock signal for the display system. No external components are required and the OSC pin must be connected to V_{DD}.

8.5 External clock

If an external clock is to be used this is input at the OSC pin. The resulting display frame frequency is given by

$$f_{frame} = \frac{f_{OSC}}{3072}$$

Only in the power-down state is the clock allowed to be stopped (OSC connected to V_{ss}), otherwise the LCD is frozen in a DC state.

8.6 Power-on reset

The on-chip power-on reset block initializes the chip after power-on or power failure. This is a synchronous reset and requires 3 OSC cycles to be executed.

8.7 Power-down mode

The chip can be put into power-down mode where all static currents are switched off (no internal oscillator, no bias level generation, all LCD-outputs are internally connected to V_{SS}) when PD = logic 1.

During power-down, the whole chip is reset and will restart with a clear display after power-down. Therefore, the whole chip has to be initialized after a power-down as after initial power- up.

The device should be put into 'display off' mode (instruction 'Display control') before putting the chip in power-down mode, otherwise the LCD output voltages are not defined.

8.8 Registers

The PCF2113x has two 8-bit registers, an Instruction Register (IR) and a Data Register (DR). The Register Select signal (RS) determines which register will be accessed. The instruction register stores instruction codes such as 'Display clear' and 'Cursor shift', and address information for the Display Data RAM (DDRAM) and Character Generator RAM (CGRAM). The instruction register can be written from but not read by the system controller. The data register temporarily stores data to be read from the DDRAM and CGRAM. When reading, data from the DDRAM or CGRAM corresponding to the address in the instruction register is written to the data register prior to being read by the 'Read data' instruction.

8.9 Busy Flag

The Busy Flag indicates the free/busy status of the PCF2113x. Logic 1 indicates that the chip is busy and further instructions will not be accepted. The Busy Flag is output to pin DB7 when RS = logic 0 and R/$\overline{W}$ = logic 1. Instructions should only be written after checking that the Busy Flag is logic 0 or waiting for the required number of cycles.

8.10 Address Counter (AC)

The Address Counter assigns addresses to the DDRAM and CGRAM for reading and writing and is set by the instructions 'Set CGRAM address' and 'Set DDRAM address'. After a read/write operation the Address Counter is automatically incremented or decremented by 1. The Address Counter contents are output to the bus (DB6 to DB0) when RS = logic 0 and R/$\overline{W}$ = logic 1.

8.11 Display Data RAM (DDRAM)

The DDRAM stores up to 80 characters of display data represented by 8-bit character codes. RAM locations which are not used for storing display data can be used as general purpose RAM. The basic DDRAM-to-display mapping is shown in Fig.3. With no display shift the characters represented by the codes in the first 24 RAM locations starting at address 00 in line 1 are displayed. Figures 4 and 5 show the display mapping for right and left shift respectively.

When data is written to or read from the DDRAM wrap-around occurs from the end of one line to the start of the next line. When the display is shifted each line wraps around within itself, independently of the others. Thus all lines are shifted and wrapped around together.
The address ranges and wrap- around operations for the various modes are shown in Table 3.

Table 3 Address space and wrap-around operation

MODE	1 × 24	2 × 12
address space	00 to 4F	00 to 27; 40 to 67
read/write wrap-around (moves to next line)	4F to 00	27 to 40; 67 to 00
display shift wrap-around (stays within line)	4F to 00	27 to 00; 67 to 40

8.12 Character Generator ROM (CGROM)

The Character Generator ROM (CGROM) generates 240 character patterns in 5 × 8 dot format from 8-bit character codes. Figures 7, 8 and 9 show the character sets that are currently implemented.

8.13 Character Generator RAM (CGRAM)

Up to 16 user defined characters may be stored in the Character Generator RAM (CGRAM). Some CGRAM characters (see Fig.17) are also used to drive icons (6 if icons blink and both icon rows are used in application; 3 if no blink but both icon rows are used in application; 0 if no icons are driven by the icon rows). The CGROM and CGRAM use a common address space, of which the first column is reserved for the CGRAM (see Fig.7). Figure 10 shows the addressing principle for the CGRAM.

8.14 Cursor control circuit

The cursor control circuit generates the cursor (underline and/or cursor blink as shown in Fig.6) at the DDRAM address contained in the Address Counter. When the Address Counter contains the CGRAM address the cursor will be inhibited.

8.15 Timing generator

The timing generator produces the various signals required to drive the internal circuitry. Internal chip operation is not disturbed by operations on the data buses.

8.16 LCD row and column drivers

The PCF2113x contains 18 row and 60 column drivers, which connect the appropriate LCD bias voltages in sequence to the display in accordance with the data to be displayed. R17 and R18 drive the icon rows.

The bias voltages and the timing are selected automatically when the number of lines in the display is selected. Figures 11, 12 and 13 show typical waveforms. Unused outputs should be left unconnected.

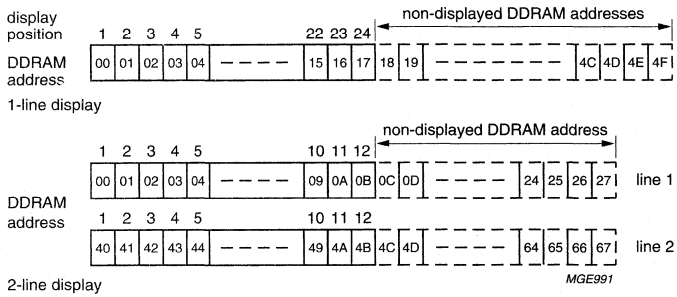


Fig.3 DDRAM-to-display mapping: no shift.

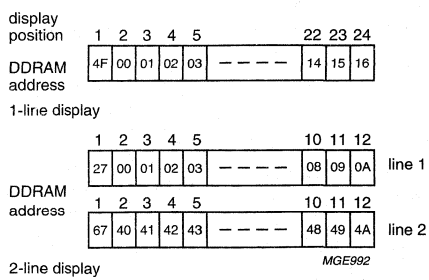


Fig.4 DDRAM-to-display mapping: right shift.

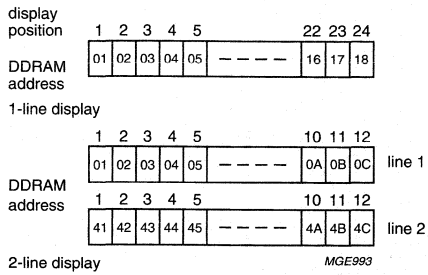
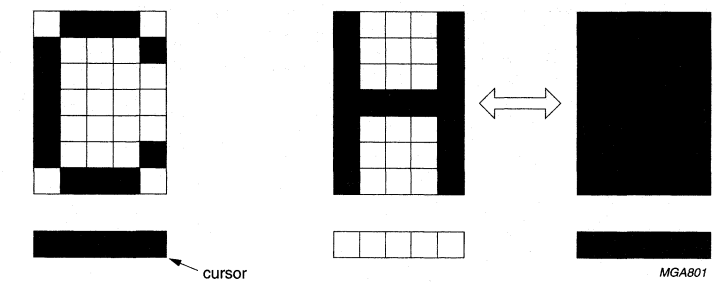


Fig.5 DDRAM-to-display mapping: left shift.



cursor display example

blink display example

Fig.6 Cursor and blink display examples.

lower 4 bits \ upper 4 bits		0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
xxxx	0000	1															
xxxx	0001	2															
xxxx	0010	3															
xxxx	0011	4															
xxxx	0100	5															
xxxx	0101	6															
xxxx	0110	7															
xxxx	0111	8															
xxxx	1000	9															
xxxx	1001	10															
xxxx	1010	11															
xxxx	1011	12															
xxxx	1100	13															
xxxx	1101	14															
xxxx	1110	15															
xxxx	1111	16															

MGE994

Fig.7 Character set 'A' in CGROM: **PCF2113A**.

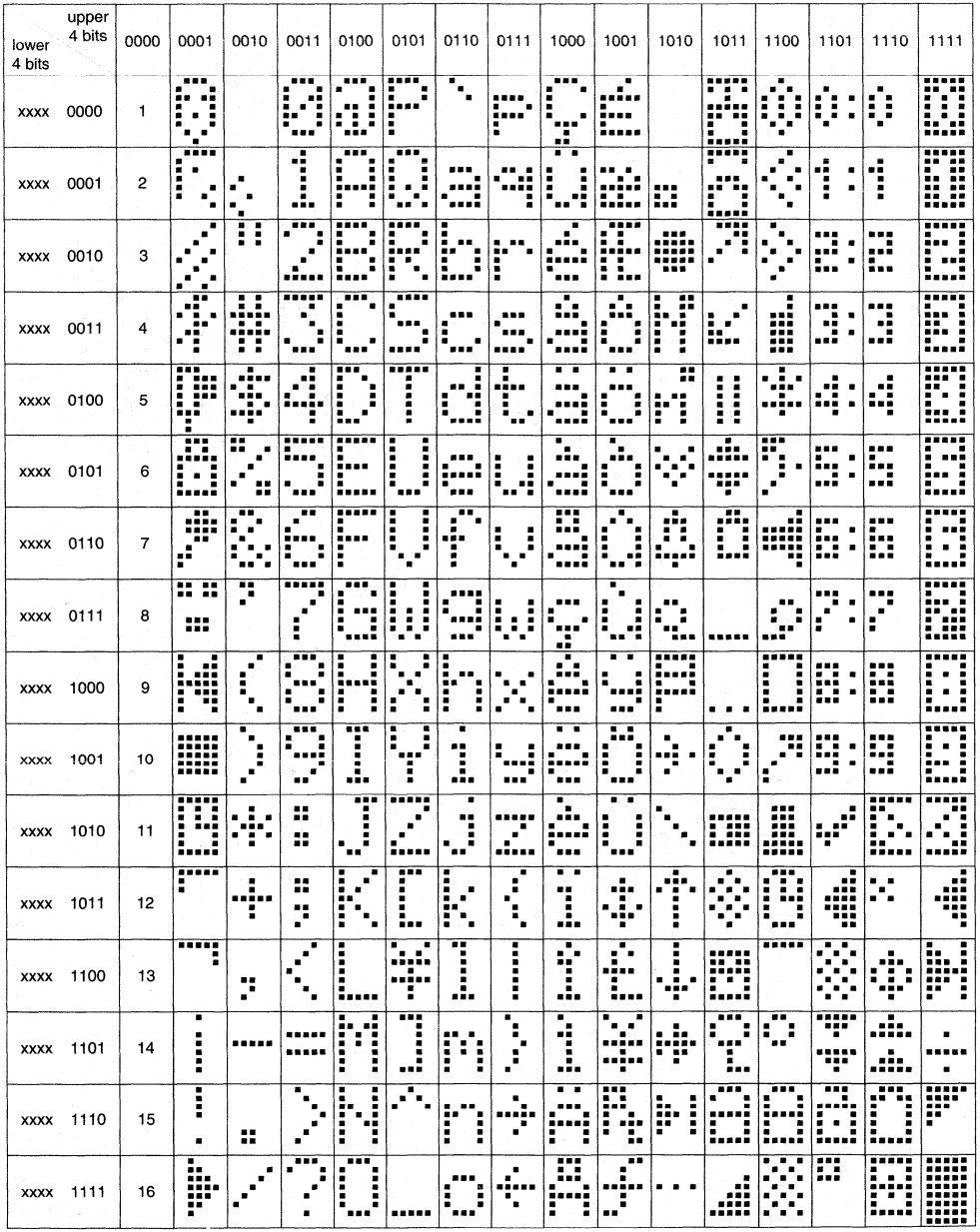
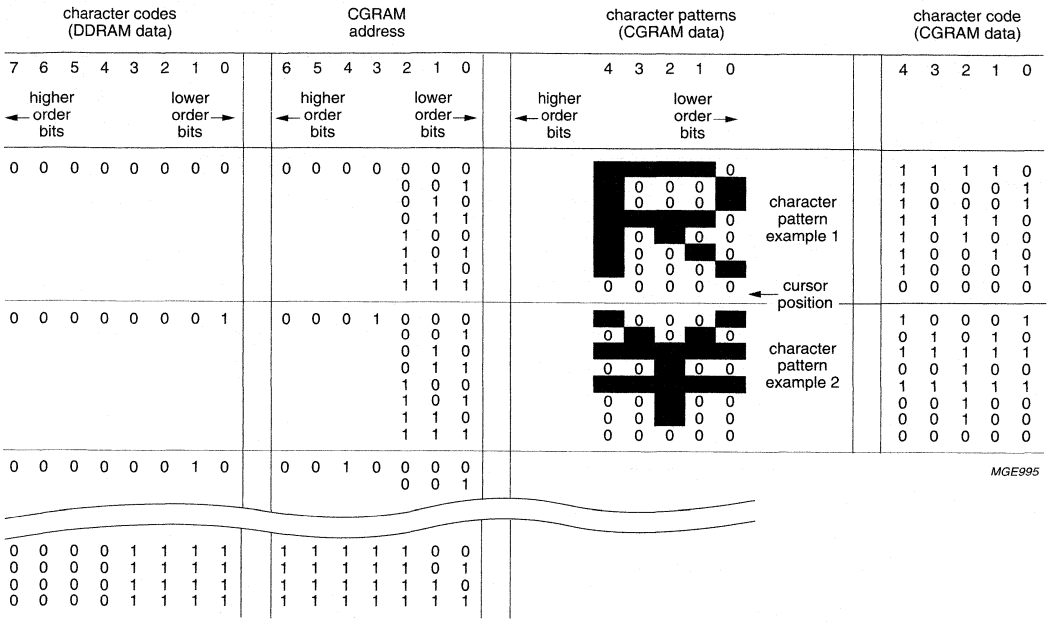


Fig.8 Character set 'D' in CGROM: **PCF2113D**.

lower 4 bits	upper 4 bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
xxxx	0000	1															
xxxx	0001	2															
xxxx	0010	3															
xxxx	0011	4															
xxxx	0100	5															
xxxx	0101	6															
xxxx	0110	7															
xxxx	0111	8															
xxxx	1000	9															
xxxx	1001	10															
xxxx	1010	11															
xxxx	1011	12															
xxxx	1100	13															
xxxx	1101	14															
xxxx	1110	15															
xxxx	1111	16															

MGD689

Fig.9 Character set 'E' in CGROM: **PCF2113E**.



Character code bits 0 to 3 correspond to CGRAM address bits 3 to 6.

CGRAM address bits 0 to 2 designate the character pattern line position. The 8th line is the cursor position and display is performed by logical OR with the cursor. Data in the 8th position will appear in the cursor position.

Character pattern column positions correspond to CGRAM data bits 0 to 4, as shown in this figure.

CGRAM character patterns are selected when character code bits 4 to 7 are all logic 0. CGRAM data = logic 1 corresponds to selection for display.

Only bits 0 to 5 of the CGRAM address are set by the 'set CGRAM address' instruction. Bit 6 can be set using the 'set DDRAM address' instruction in the valid address range or by using the auto-increment feature during CGRAM write. All bits 0 to 6 can be read using the 'Read busy flag and address' instruction.

Fig.10 Relationship between CGRAM addresses and data and display patterns.

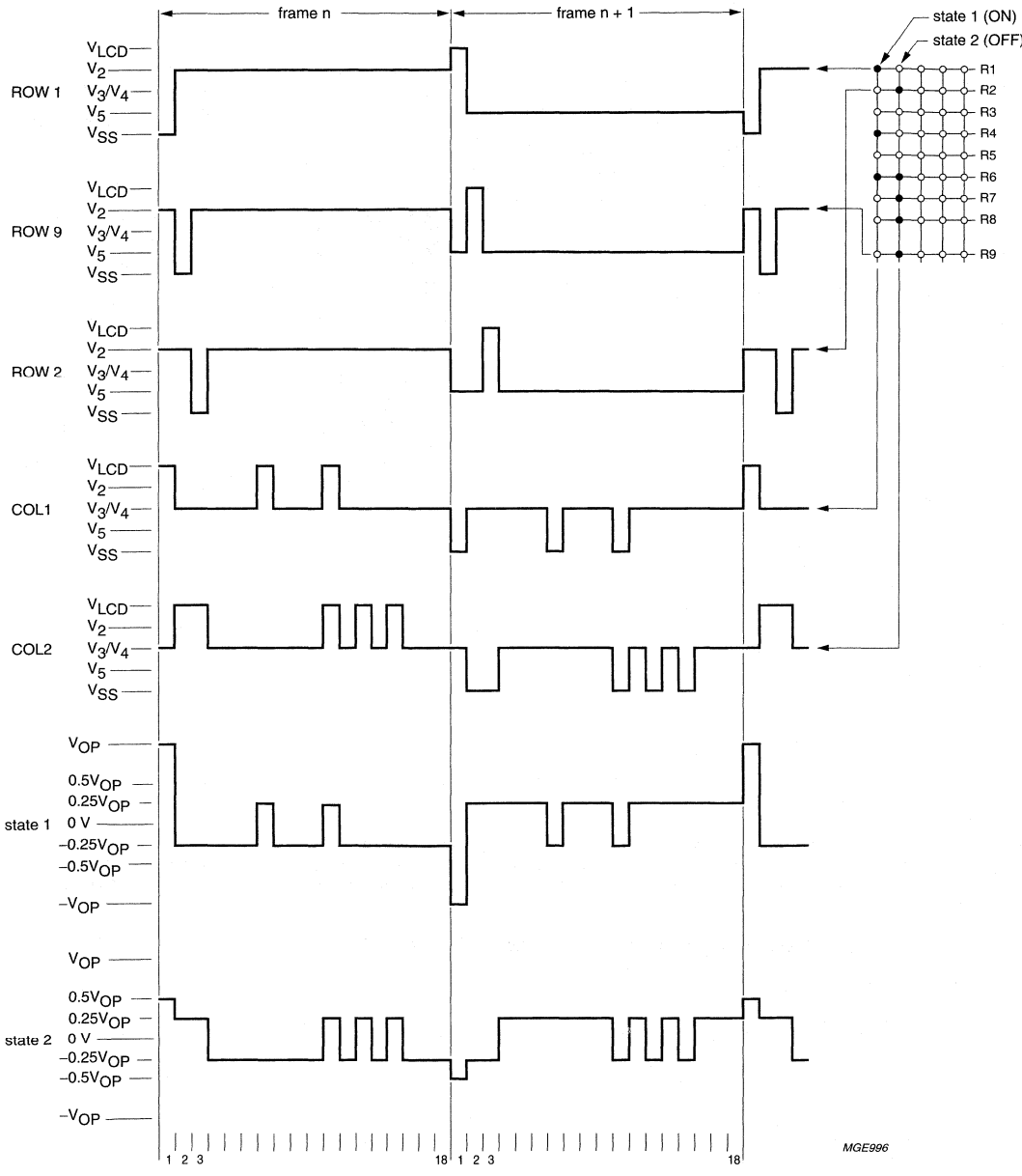


Fig.11 Typical LCD waveforms; character mode.

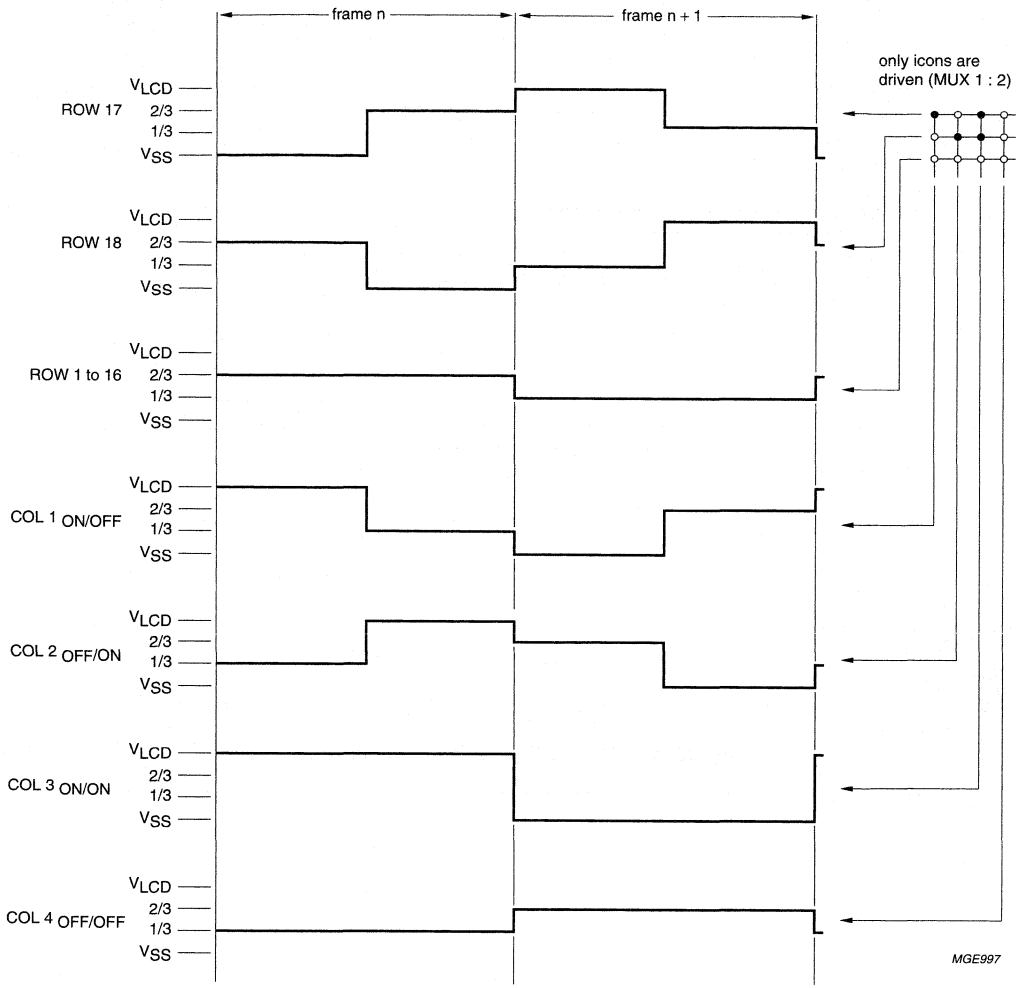
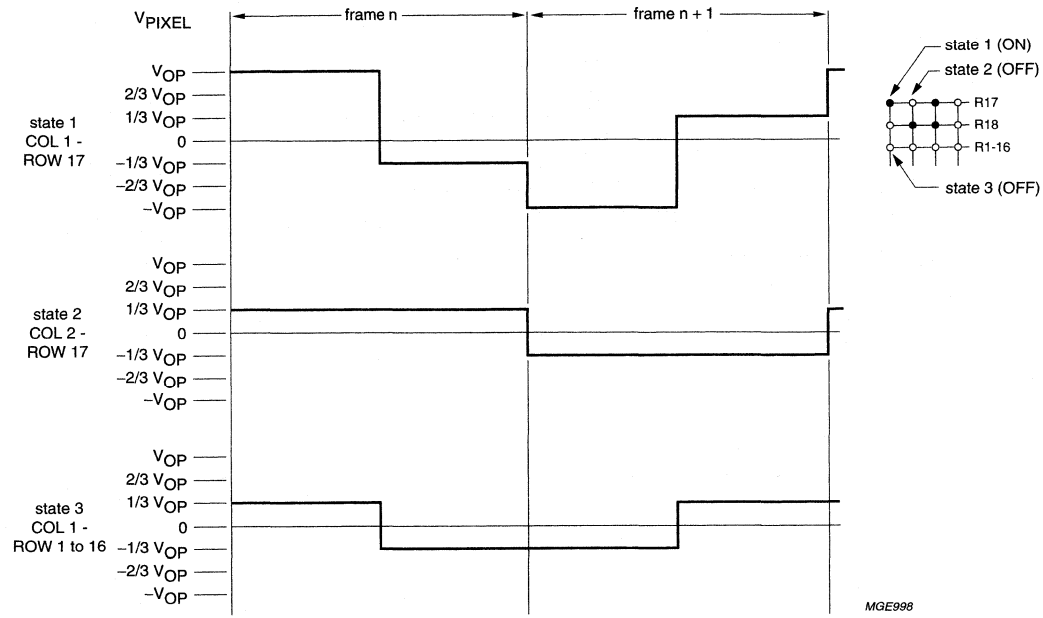


Fig.12 MUX 1 : 2 LCD waveforms; icon-mode.



$V_{ON(rms)} = 0.745V_{OP}$.

$V_{OFF(rms)} = 0.333V_{OP}$.

$$D = \frac{V_{ON}}{V_{OFF}} = 2.23$$

Fig.13 MUX 1 : 2 LCD waveforms; icon-mode.

8.17 Reset function

The PCF2113x automatically initializes (resets) when power is turned on. The chip executes a reset sequence, requiring 165 OSC cycles. After the reset the chip's functions are in the states shown in Table 4.

Table 4 State after reset

STEP	FUNCTION	RESET STATE (BIT/REGISTER)	RESET STATE (DESCRIPTION)
1	clear display		
2	entry mode set	I/D = 1	+1 (increment)
		S = 0	no shift
3	display control	D = 0	display off
		C = 0	cursor off
		B = 0	cursor character blink off
4	function set	DL = 1	8-bit interface
		M = 0	1-line display
		H = 0	normal instruction set
5	default address pointer to DDRAM; the Busy Flag (BF) indicates the busy state (BF = logic 1) until initialization ends; the busy state lasts 2 ms; the chip may also be initialized by software; see Tables 17 and 18		
6	icon control	IM, IB = 00	icons/icon blink disabled
7	display/screen configuration	L, P, Q = 000	default configurations
8	V_{LCD} temperature coefficient	TC1, TC2 = 00	default temperature coefficient
9	set V_{LCD}	V_A, V_B = 0	V_{LCD} generator off
10	I^2C-bus interface reset		

9 INSTRUCTIONS

Only two PCF2113x registers, the Instruction Register (IR) and the Data Register (DR) can be directly controlled by the microcontroller. Before internal operation, control information is stored temporarily in these registers, to allow interface to various types of microcontrollers which operate at different speeds or to allow interface to peripheral control ICs.
The format for instructions when I²C-bus control is used is shown in Table 5. The PCF2113x operation is controlled by the instructions shown in Table 6, which also gives execution times in clock cycles. Details are explained in subsequent sections.

Instructions are of 4 types, those that:

1. Designate PCF2113x functions such as display format, data length, etc.
2. Set internal RAM addresses
3. Perform data transfer with internal RAM
4. Others.

In normal use, category 3 instructions are used most frequently. However, automatic incrementing by 1 (or decrementing by 1) of internal RAM addresses after each data write lessens the microcontroller program load. The display shift in particular can be performed concurrently with display data write, enabling the designer to develop systems in minimum time with maximum programming efficiency.

During internal operation, no instruction other than the 'Read busy flag and address' instruction will be executed. Because the Busy Flag is set to logic 1 while an instruction is being executed, check to make sure it is on logic 0 before sending the next instruction or wait for the maximum instruction execution time, as given in Table 6. An instruction sent while the Busy Flag is logic 1 will not be executed.

Table 5 Instruction format for I²C-bus instructions

CONTROL BYTE[1]								COMMAND BYTE							
Co	RS	0	0	0	0	0	0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

Note

1. R/$\overline{W}$ is set together with the slave address.

Table 6 Instructions

INSTRUCTION	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DESCRIPTION	REQUIRED CLOCK CYCLES
H = 0 or 1												
NOP	0	0	0	0	0	0	0	0	0	0	no operation	3
Function set	0	0	0	0	1	DL	0	M	0	H	sets interface Data Length (DL) and number of display lines (M); extended instruction set control (H)	3
Read busy flag and address	0	1	BF	A_C							reads the Busy Flag (BF) indicating internal operating is being performed and reads Address Counter contents	0
Read data	1	1	read data								reads data from CGRAM or DDRAM	3
Write data	1	0	write data								writes data from CGRAM or DDRAM	3
H = 0												
Clear display	0	0	0	0	0	0	0	0	0	1	clears entire display and sets DDRAM address 0 in Address Counter	165
Return home	0	0	0	0	0	0	0	0	1	0	sets DDRAM address 0 in Address Counter; also returns shifted display to original position; DDRAM contents remain unchanged	3
Entry mode set	0	0	0	0	0	0	0	1	I/D	S	sets cursor move direction and specifies shift of display; these operations are performed during data write and read	3
Display control	0	0	0	0	0	0	1	D	C	B	sets entire display on/off (D), cursor on/off (C) and blink of cursor position character (B); D = 0 (display off) puts chip into power-down mode	3
Cursor/display shift	0	0	0	0	0	1	S/C	R/L	0	0	moves cursor and shifts display without changing DDRAM contents	3
Set CGRAM address	0	0	0	1	A_{CG}						sets CGRAM address; bit 6 is to be set by the instruction 'Set DDRAM address'; look at the description of the instructions	3
Set DDRAM address	0	0	1	A_{DD}							sets DDRAM address	3

INSTRUCTION	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DESCRIPTION	REQUIRED CLOCK CYCLES
H = 1												
Reserved	0	0	0	0	0	0	0	0	0	1	do not use	–
Screen configuration	0	0	0	0	0	0	0	0	1	L	set screen configuration	3
Display configuration	0	0	0	0	0	0	0	1	P	Q	set display configuration	3
Icon control	0	0	0	0	0	0	1	IM	IB	0	set icon mode (IM), icon blink (IB)	3
Temperature control	0	0	0	0	0	1	0	0	TC1	TC2	set temperature coefficient (TCx)	3
Reserved	0	0	0	1	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	do not use	–
Set V_{LCD}	0	0	1	V	voltage						store V_{LCD} in register V_A or V_B (V)	3

Note

1. X = don't care.

Table 7 Explanations of symbols used in Table 6

BIT	0	1
I/D	decrement	increment
S	display freeze	display shift
D	display off	display on
C	cursor off	cursor on
B	cursor character blink off: character at cursor position does not blink	cursor character blink on: character at cursor position blinks
S/C	cursor move	display shift
R/L	left shift	right shift
DL	4 bits	8 bits
H	use basic instruction set	use extended instruction set
L (no impact, if M = 1)	left/right screen: standard connection (as in PCF2114); 1st 12 characters of 24: columns are from 1 to 60 2nd 12 characters of 24: columns are from 1 to 60	left/right screen: mirrored connection (as in PCF2116); 1st 12 characters of 24: columns are from 1 to 60 2nd 12 characters of 24: columns are from 60 to 1
P	column data: left to right (as in PCF2116); column data is displayed from 1 to 60	column data: right to left; column data is displayed from 60 to 1
Q	row data: top to bottom (as in PCF2116); row data is displayed from 1 to 16 and icon row data is in 17 and 18	row data: bottom to top; row data is displayed from 16 to 1 and icon row data is in 18 and 17
IM	character mode; full display	icon mode; only icons displayed
IB	icon blink disabled	icon blink enabled
V	set V_A	set V_B
M	1-line by 24 display	2-line by 12 display
C_0	last control byte; see Table 5	another control byte follows after data/instruction

Table 8 Explanation of TC1 and TC2 used in Table 6

TC1	TC2	DESCRIPTION
0	0	V_{LCD} temperature coefficient 0
1	0	V_{LCD} temperature coefficient 1
0	1	V_{LCD} temperature coefficient 2
1	1	V_{LCD} temperature coefficient 3; for ranges for TC see Chapter 15

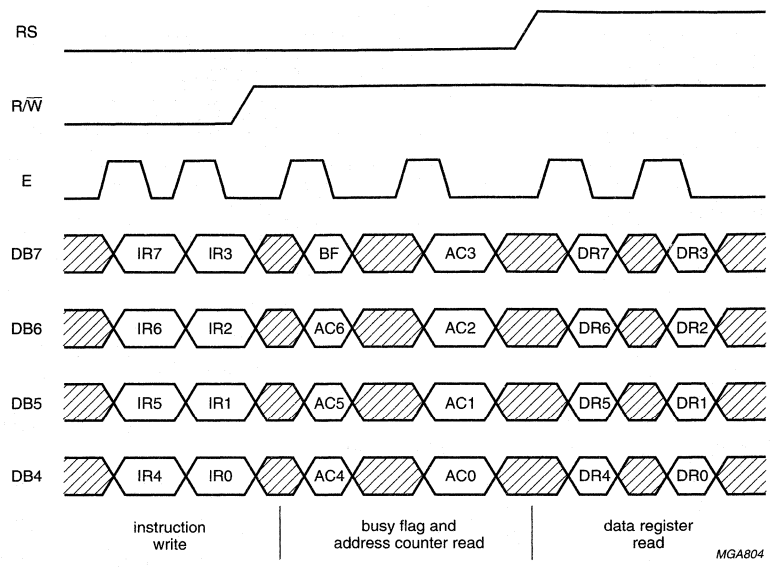
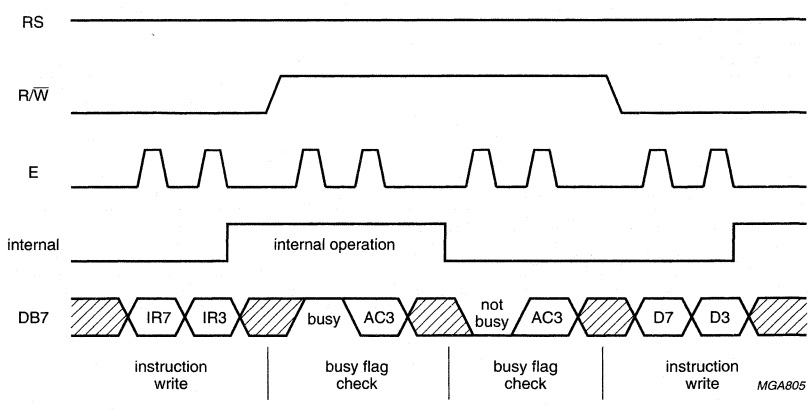


Fig.14 4-bit transfer example.



IR7, IR3: instruction 7th, 3rd bit.
AC3: Address Counter 3rd bit.
D7, D3: data 7th, 3rd bit.

Fig.15 An example of 4-bit data transfer timing sequence.

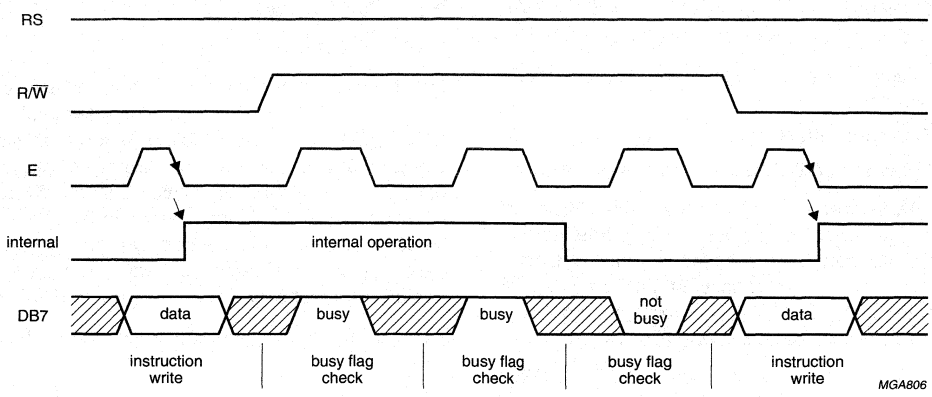


Fig.16 Example of Busy Flag checking timing sequence.

9.1 Clear display

'Clear display' writes character code 20 (hexadecimal) into all DDRAM addresses (the character pattern for character code 20 must be blank pattern), sets the DDRAM Address Counter to logic 0 and returns display to its original position if it was shifted. Thus, the display disappears and the cursor or blink position goes to the left edge of the display. Sets entry mode I/D = logic 1 (increment mode). S of entry mode does not change.

The instruction 'Clear display' requires extra execution time. This may be allowed by checking the Busy Flag (BF) or by waiting until the 165 clock cycles have elapsed. The latter must be applied where no read-back options are foreseen, as in some Chip-On-Glass (COG) applications.

9.2 Return home

'Return home' sets the DDRAM Address Counter to logic 0 and returns display to its original position if it was shifted. DDRAM contents do not change. The cursor or blink position goes to the left of the first display line. I/D and S of entry mode do not change.

9.3 Entry mode set

9.3.1 I/D

When I/D = logic 1 (0) the DDRAM or CGRAM address increments (decrements) by 1 when data is written into or read from the DDRAM or CGRAM. The cursor or blink position moves to the right when incremented and to the left when decremented. The cursor underline and cursor character blink are inhibited when the CGRAM is accessed.

9.3.2 S

When S = logic 1, the entire display shifts either to the right (I/D = logic 0) or to the left (I/D = logic 1) during a DDRAM write. Thus it looks as if the cursor stands still and the display moves. The display does not shift when reading from the DDRAM, or when writing into or reading out of the CGRAM. When S = logic 0 the display does not shift.

9.4 Display control (and partial power-down mode)

9.4.1 D

The display is on when D = logic 1 and off when D = logic 0. Display data in the DDRAM are not affected and can be displayed immediately by setting D to logic 1.

When the display is off (D = logic 0) the chip is in partial power-down mode:

- The LCD-outputs are connected to V_{SS}
- The LCD generator and bias generator are turned off.

3 OSC cycles are required after sending the 'Display off' instruction to ensure all outputs are at V_{SS}, afterwards OSC can be stopped. If the oscillator is running during partial power-down mode ('Display off') the chip can still execute instructions. Even lower current consumption is obtained by inhibiting the oscillator (OSC = V_{SS}).

To ensure $I_{DD} < 1$ µA the parallel bus pins DB7 to DB0 should be connected to V_{DD}; RS, R/$\overline{W}$, to V_{DD} or left open and PD to V_{DD}. Recovery from power-down mode: PD back to logic 0, if necessary OSC back to V_{DD}, send a 'Display control' instruction with D = logic 1.

9.4.2 C

The cursor is displayed when C = logic 1 and inhibited when C = logic 0. Even if the cursor disappears, the display functions I/D, etc. remain in operation during display data write. The cursor is displayed using 5 dots in the 8th line (see Fig.6).

9.4.3 B

The character indicated by the cursor blinks when B = logic 1. The cursor character blink is displayed by switching between display characters and all dots on with a period of approximately 1 s, with $f_{BLINK} = \frac{f_{OSC}}{52\,224}$

The cursor underline and the cursor character blink can be set to display simultaneously.

9.5 Cursor/display shift

'Cursor/display shift' moves the cursor position or the display to the right or left without writing or reading display data. This function is used to correct a character or move the cursor through the display. In 2-line displays, the cursor moves to the next line when it passes the last position (40) of the line. When the displayed data is shifted repeatedly all lines shift at the same time; displayed characters do not shift into the next line.

The Address Counter (AC) content does not change if the only action performed is shift display, but increments or decrements with the 'cursor shift'.

9.6 Function set

9.6.1 DL (PARALLEL MODE ONLY)

Sets interface data width. Data is sent or received in bytes (DB7 to DB0) when DL = logic 1 or in two nibbles (DB7 to DB4) when DL = logic 0. When 4-bit width is selected, data is transmitted in two cycles using the parallel bus. In a 4-bit application DB3 to DB0 should be left open (internal pull-ups). Hence in the first 'Function set' instruction after power-on N and H are set to logic 1. A second 'Function set' must then be sent (2 nibbles) to set N and H to their required values.

'Function set' from I^2C-interface sets the DL bit to logic 1.

9.6.2 M

Chooses either 1-line by 24 display (M = 0) or 2-line by 12 display (M = 1).

9.6.3 H

When H = logic 0 the chip can be programmed via the standard 11 instruction codes used in the PCF2116 and other LCD controllers.

When H = logic 1 the extended range of instructions will be used. These are mainly for controlling the display configuration and the icons.

9.7 Set CGRAM address

'Set CGRAM address' sets bits 5 to 0 of the CGRAM address (A_{CG} in Table 6) into the Address Counter (binary A[5] to A[0]).
Data can then be written to or read from the CGRAM.

Attention: the CGRAM address uses the same address register as the DDRAM address and consists of 7 bits (binary A[6] to A[0]). With the 'Set CGRAM address' instruction, only bits 5 down to 0 are set. Bit 6 can be set using the 'Set DDRAM address' instruction first, or by using the auto-increment feature during CGRAM write. All of bits 6 to 0 can be read using the 'Read busy flag and address' instruction.

When writing to the lower part of the CGRAM, make sure that bit 6 of the address is not set (e.g. by an earlier DDRAM write or read action).

9.8 Set DDRAM address

'Set DDRAM address' sets the DDRAM address (A_{DD} in Table 6) into the Address Counter (binary A[6] to A[0]). Data can then be written to or read from the DDRAM.

9.9 Read busy flag and address

'Read busy flag and address' reads the Busy Flag (BF) and Address Counter (AC). BF = logic 1 indicates that an internal operation is in progress. The next instruction will not be executed until BF = logic 0, so BF should be checked before sending another instruction.

At the same time, the value of the Address Counter expressed in binary A[6] to A[0] is read out. The Address Counter is used by both CGRAM and DDRAM, and its value is determined by the previous instruction.

9.10 Write data to CGRAM or DDRAM

'Write data' writes binary 8-bit data D[7] to D[0] to the CGRAM or the DDRAM.

Whether the CGRAM or DDRAM is to be written into is determined by the previous 'Set CGRAM address' or 'Set DDRAM address' instruction. After writing, the address automatically increments or decrements by 1, in accordance with the entry mode. Only bits D[4] to D[0] of CGRAM data are valid, bits D[7] to D[5] are 'don't care'.

9.11 Read data from CGRAM or DDRAM

'Read data' reads binary 8-bit data D[7] to D[0] from the CGRAM or DDRAM.

The most recent 'Set address' instruction determines whether the CGRAM or DDRAM is to be read.

The 'Read data' instruction gates the content of the Data Register (DR) to the bus while E is high. After E goes low again, internal operation increments (or decrements) the AC and stores RAM data corresponding to the new AC into the DR.

Note: the only three instructions that update the Data Register (DR) are:

- 'Set CGRAM address'
- 'Set DDRAM address'
- 'Read data' from CGRAM or DDRAM.

Other instructions (e.g. 'Write data', 'Cursor/display shift', 'Clear display', 'Return home') do not modify the data register content.

10 EXTENDED FUNCTION SET INSTRUCTIONS AND FEATURES

10.1 New instructions

H = logic 1 sets the chip into alternate instruction set mode.

10.2 Icon control

The PCF2113x can drive up to 120 icons. See Fig.17 for CGRAM to icon mapping.

10.3 IM

When IM = logic 0 the chip is in character mode. In character mode characters and icons are driven (MUX 1 : 18). The V_{LCD} generator, if used, produces the V_{LCD} voltage programmed in register V_A.

When IM = logic 1 the chip is in icon mode. In icon mode only the icons are driven (MUX 1 : 2) and the V_{LCD} voltage generator, if used, produces the V_{LCD} voltage programmed in register V_B.

Remark: If internally generated V_{LCD} must not be lower than V_{DD} ($V_{DD} \leq 4$ V)

10.4 IB

Icon blink control is independent of the cursor/character blink function.

When IB = logic 0 icon blink is disabled. Icon data is stored in CGRAM character 0 to 2 ($3 \times 8 \times 5 = 120$ bits for 120 icons).

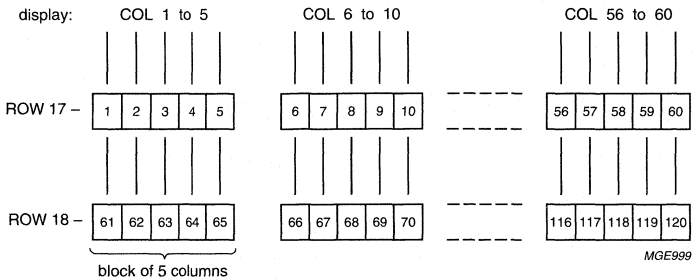
When IB = logic 1 icon blink is enabled. In this case each icon is controlled by two bits. Blink consists of two half phases (corresponding to the cursor on and off phases called even and odd phases hereafter).

Icon states for the even phase are stored in CGRAM characters 0 to 2 ($3 \times 8 \times 5 = 120$ bits for 120 icons). These bits also define icon state when icon blink is not used.

Icon states for the odd phase are stored in CGRAM character 4 to 6 (another 120 bits for the 120 icons). When icon blink is disabled CGRAM characters 4 to 6 may be used as normal CGRAM characters.

Table 9 Blink effect for icons and cursor character blink

PARAMETER	EVEN PHASE	ODD PHASE
Cursor underline	on	off
Cursor character blink	block (all on)	normal (display character)
Icons	state 1: CGRAM character 0 to 2	state 2: CGRAM character 4 to 6



icon no.	phase	ROW/COL	character codes	CGRAM address	CGRAM data	icon view
			7 6 5 4 3 2 1 0 MSB LSB	6 5 4 3 2 1 0 MSB LSB	4 3 2 1 0 MSB LSB	
1-5	even	17/1-5	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0	1 0 1 0 1	
6-10	even	17/6-10	0 0 0 0 0 0 0 0	0 0 0 0 0 0 1	0 1 0 1 0	
11-15	even	17/11-15	0 0 0 0 0 0 0 0	0 0 0 0 0 1 0	0 1 1 1 0	
⋮	⋮	⋮	⋮	⋮	⋮	⋮
56-60	even	17/56-60	0 0 0 0 0 0 0 1	0 0 0 1 0 1 1	1 1 1 1 1	
61-65	even	18/1-5	0 0 0 0 0 0 0 1	0 0 0 1 1 0 0	1 1 0 0 0	
⋮	⋮	⋮	⋮	⋮	⋮	⋮
116-120	even	18/56-60	0 0 0 0 0 0 1 0	0 0 1 0 1 1 1	1 1 1 0 1	
1-5	odd (blink)	17/1-5	0 0 0 0 0 1 0 0	0 1 0 0 0 0 0	0 0 0 0 0	
⋮	⋮	⋮	⋮	⋮	⋮	⋮
116-120	odd (blink)	18/56-60	0 0 0 0 0 1 1 0	0 1 1 0 0 1 1	0 0 1 1 0	

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CGRAM data bit = logic 1 turns the icon on, data bit = logic 0 turns the icon off.
Data in character codes 0 to 2 define the icon-states when icon blink is disabled or during the even phase when icon blink is enabled.
Data in character codes 4 to 6 define the icon-state during the odd phase when icon blink is enabled (not used for icons when icon blink is disabled).

Fig.17 CGRAM to icon mapping.

10.5 Normal/Icon mode operation

IM	CONDITION	V_{LCD}
0	character mode	generates V_A
1	icon mode	generates V_B

10.6 Screen configuration

L: default is L = logic 0.

L = logic 0: the two halves of a split screen are connected in a standard way i.e. column 1/61, 2/62 to 60/120.

L = logic 1: the two halves of a split screen are connected in a mirrored way i.e. column 1/120, 2/119 to 60/61. This allows single layer PCB or glass layout.

10.7 Display configuration

P, Q: default is P, Q = logic 0.

P = logic 1 mirrors the column data.

Q = logic 1 mirrors the row data.

10.8 TC1, TC2

Default is TC1, TC2 = logic 0. This selects the default temperature coefficient for the internally generated V_{LCD}. TC1,TC2 = 10,01 and 11 selects alternative temperature coefficients 1, 2 and 3 respectively.

10.9 Set V_{LCD}

V_{LCD} value is programmed by instruction. Two on-chip registers hold V_{LCD} values for character mode and icon mode respectively (V_A and V_B). The generated V_{LCD} value is independent of V_{DD}, allowing battery operation of the chip. V_B must be programmed to FF in character mode (i.e. using V_A) and V_A must be programmed to 00 in icon mode.

Note: **If internally generated V_{LCD} must not be lower than V_{DD}.**

Note: $V_{DD} \leq 4V$

V_{LCD} programming:

1. send 'Function set' instruction with H = 1
2. send 'Set V_{LCD}' instruction to write to voltage register:
   a) DB7, DB6 = 10: DB5 to DB0 are V_{LCD} of character mode (V_A)
   b) DB7, DB6 = 11: DB5 to DB0 are V_{LCD} of icon mode (V_B)
   c) DB5 to DB0 = 000000 switches V_{LCD} generator off (when selected)
   d) During 'display off' and power-down V_{LCD} generator is also disabled
3. send 'Function set' instruction with H = 0 to resume normal programming.

10.10 Reducing current consumption

Reducing current consumption can be achieved by one of the options mentioned in Table 10.

Table 10 Reducing current consumption

ORIGINAL MODE	ALTERNATIVE MODE
Character mode	icon mode (control bit IM)
Display on	display off (control bit D)

When V_{LCD} lies outside the V_{DD} range and must be generated, it is usually more efficient to use the on-chip generator than an external regulator.

Table 11 Use of the V_A and V_B registers

MODE	V_A	V_B
Normal operation	V_{LCD} character mode	V_{LCD} icon mode

11 INTERFACE TO MICROCONTROLLER (PARALLEL INTERFACE)

The PCF2113x can send data in either two 4-bit operations or one 8-bit operation and can thus interface to 4-bit or 8-bit microcontrollers.

In 8-bit mode data is transferred as 8-bit bytes using the 8 data lines DB7 to DB0. Three further control lines E, RS, and R/$\overline{W}$ are required. See Chapter 7.

In 4-bit mode data is transferred in two cycles of 4 bits each using pins DB7 to DB4 for transaction. The higher order bits (corresponding to DB7 to DB4 in 8-bit mode) are sent in the first cycle and the lower order bits (DB3 to DB0 in 8-bit mode) in the second. Data transfer is complete after two 4-bit data transfers. Note that two cycles are also required for the Busy Flag check. 4-bit operation is selected by instruction. See Figs 14 to 17 for examples of bus protocol.

In 4-bit mode pins DB3 to DB0 must be left open-circuit. They are pulled up to V_{DD} internally.

12 INTERFACE TO MICROCONTROLLER (I²C-BUS INTERFACE)

12.1 Characteristics of the I²C-bus

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a Serial Clock Line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

12.2 I²C-bus protocol

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always carried out with the first byte transmitted after the start procedure. The I²C-bus configuration for the different PCF2113x read and write cycles is shown in Figs 23 and 24. The slow down feature of the I²C-bus protocol (receiver holds SCL low during internal operations) is not used in the PCF2113x.

12.3 Definitions

- Transmitter: the device which sends the data to the bus
- Receiver: the device which receives the data from the bus
- Master: the device which initiates a transfer, generates clock signals and terminates a transfer
- Slave: the device addressed by a master
- Multi-Master: more than one master can attempt to control the bus at the same time without corrupting the message
- Arbitration: procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted
- Synchronization: procedure to synchronize the clock signals of two or more devices.

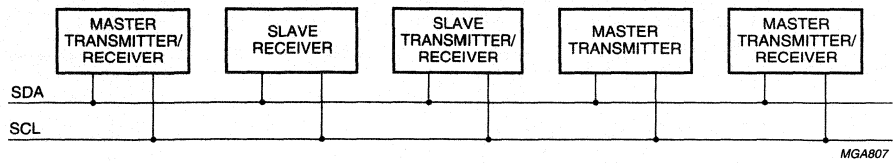


Fig.18 System configuration.

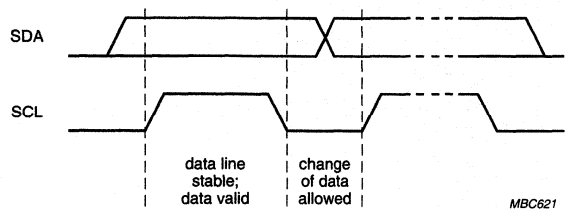


Fig.19 Bit transfer.

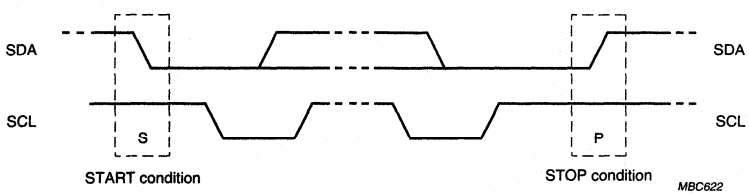


Fig.20 Definition of START and STOP conditions.

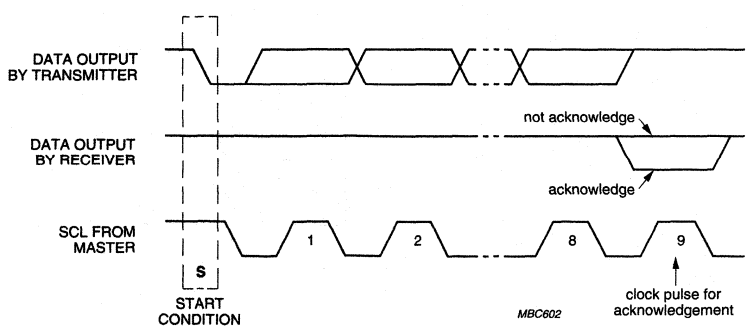


Fig.21 Acknowledgement on the I^2C-bus.

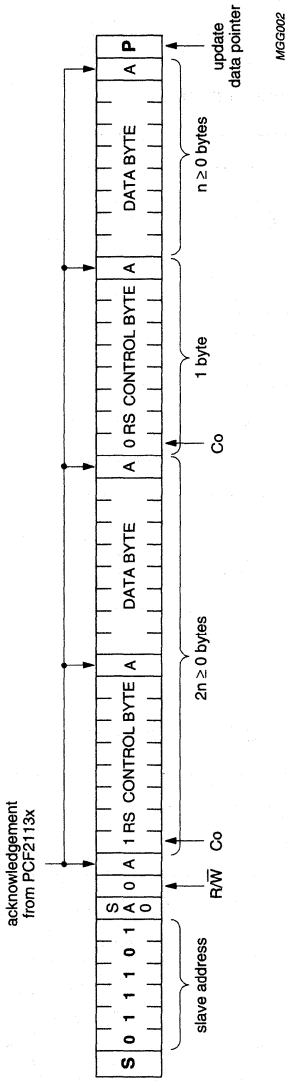
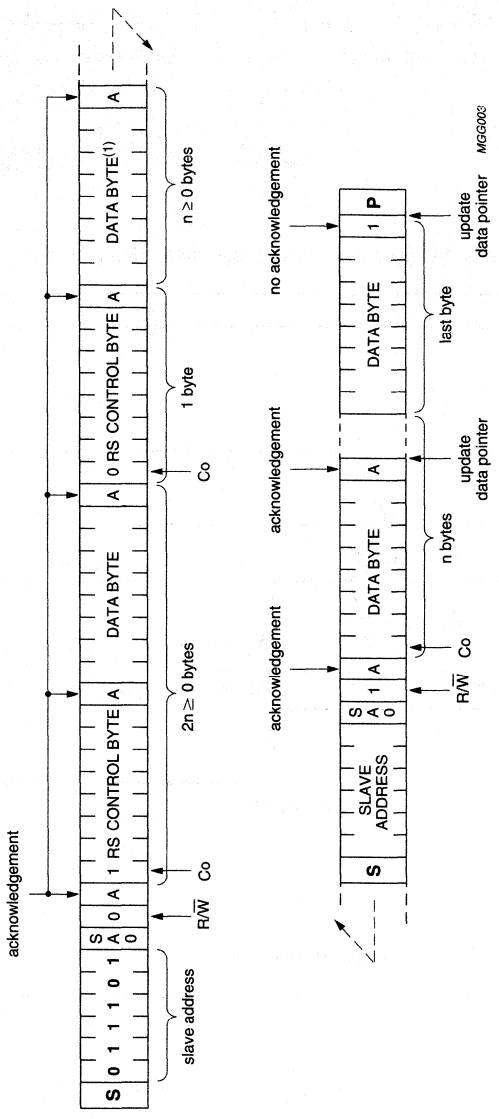


Fig.22 Master transmits to slave receiver; write mode.



(1) Last data byte is a dummy byte (may be omitted).

Fig.23 Master reads after setting word address; write word address, set RS; 'read data'.

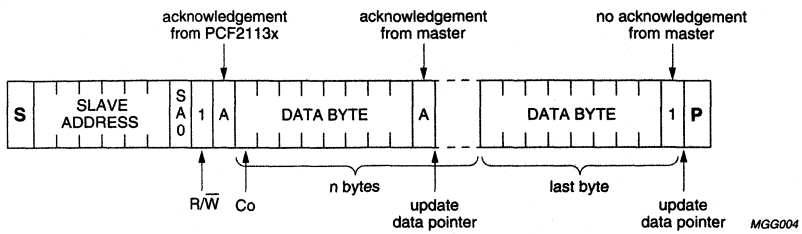


Fig.24 Master reads slave immediately after first byte; read mode (RS previously defined).

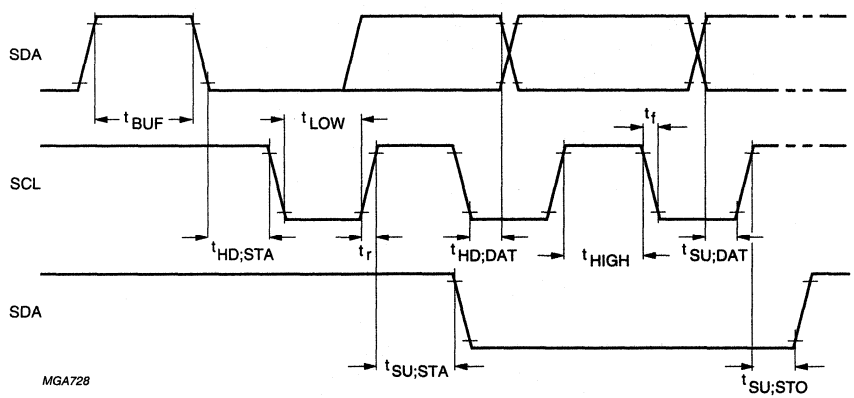


Fig.25 I²C-bus timing diagram.

13 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.5	+6.5	V
V_{LCD}	LCD supply voltage	−0.5	+7.5	V
V_I	input voltage OSC, RS, R/$\overline{W}$, E and DB7 to DB0	−0.5	V_{DD} + 0.5	V
V_O	output voltage R1 to R18, C1 to C60 and V_{LCD}	−0.5	V_{LCD} + 0.5	V
I_I	DC input current	−10	+10	mA
I_O	DC output current	−10	+10	mA
I_{DD}, I_{SS}, I_{LCD}	V_{DD}, V_{SS} or V_{LCD} current	−50	+50	mA
P_{tot}	total power dissipation	−	400	mW
P_O	power dissipation per output	−	100	mW
T_{stg}	storage temperature	−65	+150	°C

14 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see *"Handling MOS Devices"*).

15 DC CHARACTERISTICS

V_{DD} = 1.8 to 4.0 V (external V_{LCD}: V_{DD} = 1.8 to 5.5 V); V_{SS} = 0 V; V_{LCD} = 2.2 to 6.5 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage	internal V_{LCD} generation	1.8	–	4.0	V
V_{DD}	supply voltage	external V_{LCD}	1.8	–	5.5	V
V_{LCD}	LCD supply voltage		2.2	–	6.5	V
I_{SS}	supply current, external V_{LCD}	note 1				
I_{SS1}	supply current 1		–	60	120	µA
I_{SS3}	supply current 3	V_{DD} = 3 V; V_{LCD} = 5 V; note 2	–	45	80	µA
I_{SS4}	supply current 4 (icon mode)	V_{DD} = 3 V; V_{LCD} = 2.5 V; note 2	–	25	45	µA
I_{SS5}	supply current 5 (power-down mode)	V_{DD} = 3 V; V_{LCD} = 2.5 V; DB7 to DB0, RS, R/$\overline{W}$ = 1; OSC = 0; PD = 1	–	0.5	5	µA
I_{SS}	supply current, internal V_{LCD}	notes 1, 3				
I_{SS6}	supply current 6		–	200	400	µA
I_{SS8}	supply current 8	V_{DD} = 3 V; V_{LCD} = 5 V; note 2	–	200	400	µA
I_{SS9}	supply current 9 (icon mode)	V_{DD} = 3 V; V_{LCD} = 2.5 V; note 2	–	100	–	µA
V_{POR}	Power-on reset voltage level	note 4	–	1.3	1.6	V
Logic						
V_{IL1}	LOW level input voltage T1, E, RS, R/$\overline{W}$, DB[7..0] and SA0		0	–	$0.3V_{DD}$	V
V_{IH1}	HIGH level input voltage T1, E, RS, R/$\overline{W}$, DB[7..0] and SA0		$0.7V_{DD}$	–	V_{DD}	V
$V_{IL(PD)}$	LOW level input voltage PD		0	–	$0.2V_{DD}$	V
$V_{IH(PD)}$	HIGH level input voltage PD		$0.8V_{DD}$	–	V_{DD}	V
$V_{IL(osc)}$	LOW level input voltage OSC		0	–	V_{DD} − 1.5	V
$V_{IH(osc)}$	HIGH input voltage OSC		V_{DD} − 0.1	–	V_{DD}	V
$I_{OL(DB)}$	LOW level output current DB[7..0]	V_{OL} = 0.4 V; V_{DD} = 5 V	1.6	4	–	mA
$I_{OH(DB)}$	HIGH level output current DB[7..0]	V_{OH} = 4 V; V_{DD} = 5 V	−1.0	–	–	mA
I_{pu}	pull-up current DB[7..0]	V_I = V_{SS}	0.04	0.15	1	µA
I_{L1}	leakage current OSC, E, RS, R/$\overline{W}$, DB[7..0] and SA0	V_I = V_{DD} or V_{SS}	−1.0	–	+1.0	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I²C-bus						
SDA AND SCL						
V_{IL2}	LOW level input voltage		0	–	$0.3V_{DD}$	V
V_{IH2}	HIGH level input voltage		$0.7V_{DD}$	–	5.5	V
I_{L2}	input leakage current	$V_I = V_{DD}$ or V_{SS}	−1	–	+1	μA
C_i	input capacitance	note 5	–	–	10	pF
$I_{OL(SDA)}$	LOW level output current (SDA)	V_{OL} = 0.4 V; V_{DD} = 5 V	3	–	–	mA
LCD outputs						
R_{ROW}	row output resistance R1 to R18	note 6	–	10	30	kΩ
R_{COL}	column output resistance C1 to C60	note 6	–	15	40	kΩ
V_{tol1}	bias voltage tolerance R1 to R18 and C1 to C60	note 7	–	20	130	mV
V_{tol2a}	V_{LCD} tolerance	T_{amb} = 25 °C; V_{LCD} < 3 V; note 3	–	–	200	mV
V_{tol2b}	V_{LCD} tolerance	T_{amb} = 25 °C; V_{LCD} < 4 V; note 3	–	–	350	mV
V_{tol2c}	V_{LCD} tolerance	T_{amb} = 25 °C; V_{LCD} < 5 V; note 3	–	–	400	mV
TC0	V_{LCD} temperature coefficient 0	note 8	–	−7.6	–	mV/K
TC1	V_{LCD} temperature coefficient 1	note 8	–	−8.4	–	mV/K
TC2	V_{LCD} temperature coefficient 2	note 8	–	−10.4	–	mV/K
TC3	V_{LCD} temperature coefficient 3	note 8	–	−12.4	–	mV/K

Notes

1. LCD outputs are open-circuit; inputs at V_{DD} or V_{SS}; bus inactive.
2. T_{amb} = 25 °C; f_{OSC} = 200 kHz.
3. LCD outputs are open-circuit; HV generator is on; load current I_{VLCD} (at V_{LCD}) = 5 μA.
4. Resets all logic when $V_{DD} < V_{POR}$; 3 OSC clock cycles required.
5. Tested on sample basis.
6. Resistance of output terminals (R1 to R18 and C1 to C60) with a load current of 20 μA; outputs measured one at a time; external V_{LCD}.
7. LCD outputs open-circuit; external V_{LCD}.
8. Temperature coefficient at V_{OP} = 5.0 V. Typical range ±2 mV/K.

16 AC CHARACTERISTICS

V_{DD} = 1.8 to 5.5 V; V_{SS} = 0 V; V_{LCD} = 2.2 – 6.5 V; T_{amb} = –40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{FR}	LCD frame frequency (internal clock)	V_{DD} = 5.0 V	45	81	147	Hz
f_{OSC}	oscillator frequency (not available at any pin)		140	250	450	kHz
f_{OSC}	external clock frequency		140	–	450	kHz
t_{OSCST}	oscillator start-up time after power-down		–	200	300	µs
Bus timing characteristics: parallel interface; note 1						
WRITE OPERATION (WRITING DATA FROM MICROCONTROLLER TO PCF2113X)						
T_{cy}	enable cycle time		500	–	–	ns
PW_{EH}	enable pulse width		220	–	–	ns
t_{ASU}	address set-up time		50	–	–	ns
t_{AHD}	address hold time		25	–	–	ns
t_{DSW}	data set-up time		60	–	–	ns
t_{HD}	data hold time		25	–	–	ns
READ OPERATION (READING DATA FROM PCF2113X TO MICROCONTROLLER)						
T_{cy}	enable cycle time		500	–	–	ns
PW_{EH}	enable pulse width		220	–	–	ns
t_{ASU}	address set-up time		50	–	–	ns
t_{AH}	address hold time		25	–	–	ns
t_{DHD}	data delay time		–	–	150	ns
t_{HD}	data hold time		20	–	100	ns
Timing characteristics: I^2C-bus interface; note 1						
f_{SCL}	SCL clock frequency		–	–	400	kHz
t_{LOW}	SCL clock low period		1.3	–	–	µs
t_{HIGH}	SCL clock high period		0.6	–	–	µs
$t_{SU;DAT}$	data set-up time		100	–	–	ns
$t_{HD;DAT}$	data hold time		0	–	–	ns
t_r	SCL, SDA rise time		–	–	300	ns
t_f	SCL, SDA fall time		–	–	300	ns
C_B	capacitive bus line load		–	–	400	pF
$t_{SU;STA}$	set-up time for a repeated START condition		0.6	–	–	µs
$t_{HD;STA}$	START condition hold time		0.6	–	–	µs
$t_{SU;STO}$	set-up time for STOP condition		0.6	–	–	µs
t_{SW}	tolerable spike width on bus		–	–	50	ns

Note

1. All timing values are valid within the operating supply voltage and ambient temperature range and are referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

17 TIMING CHARACTERISTICS

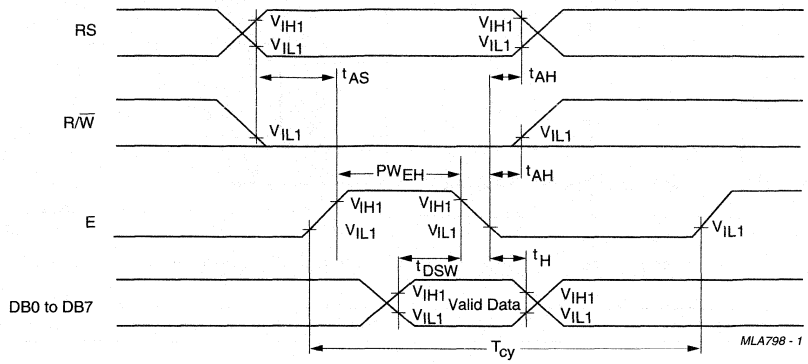


Fig.26 Parallel bus write operation sequence; writing data from microcontroller to PCF2113x.

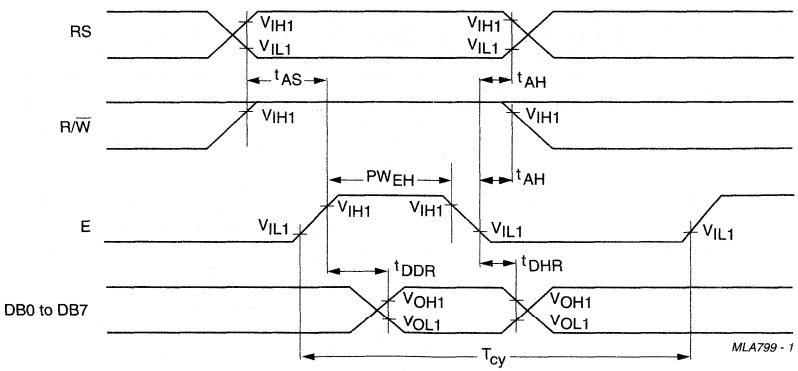


Fig.27 Parallel bus read operation sequence; reading data from PCF2113x to microcontroller.

18 APPLICATION INFORMATION

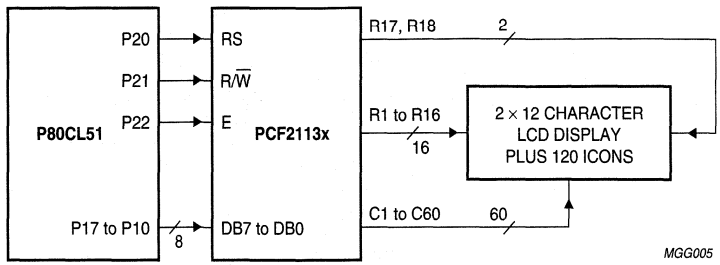


Fig.28 Direct connection to 8-bit microcontroller; 8-bit bus.

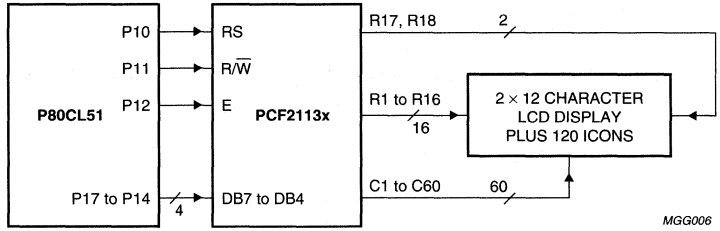


Fig.29 Direct connection to 8-bit microcontroller; 4-bit bus.

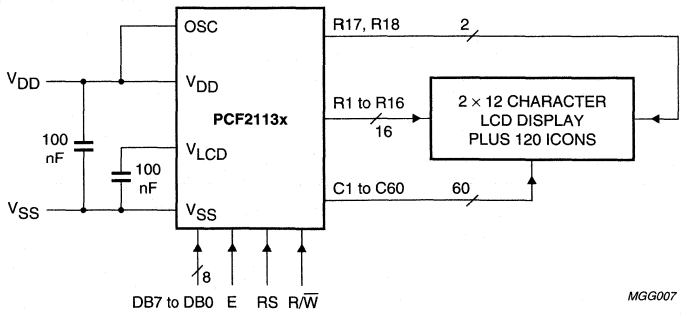


Fig.30 Typical application using parallel interface.

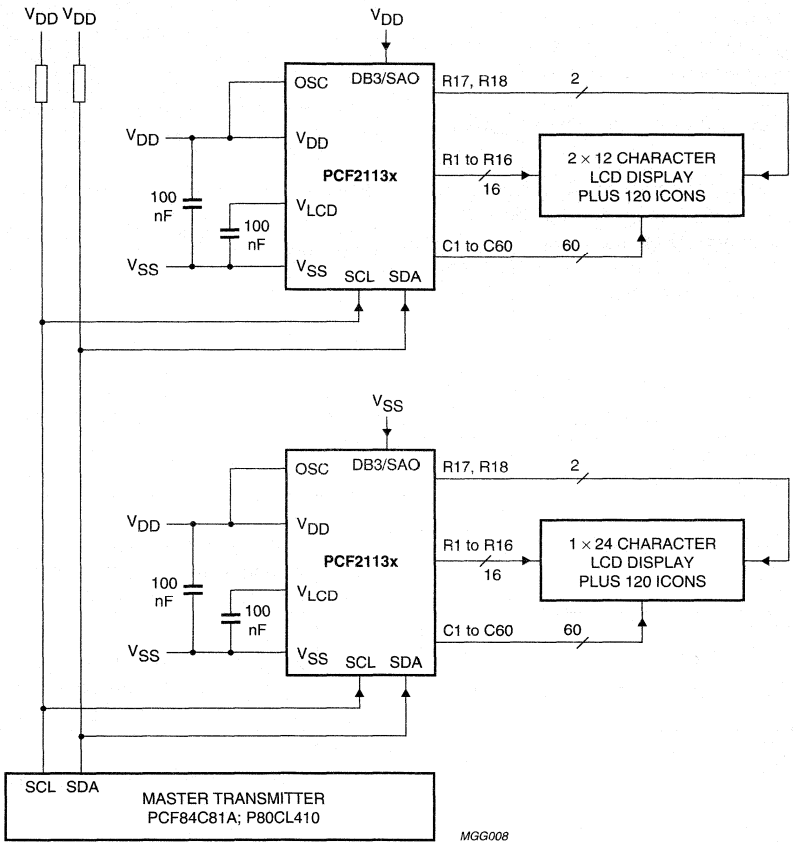


Fig.31 Application using I²C-bus interface.

18.1 8-bit operation, 1-line display using internal reset

Table 13 shows an example of a 1-line display in 8-bit operation. The PCF2113x functions must be set by the 'function set' instruction prior to display. Since the DDRAM can store data for 80 characters, the RAM can be used for advertising displays when combined with display shift operation. Since the display shift operation changes display position only and DDRAM contents remain unchanged, display data entered first can be displayed when the 'return home' operation is performed.

18.2 4-bit operation, 1-line display using internal reset

The program must set functions prior to 4-bit operation. Table 12 shows an example. When power is turned on, 8-bit operation is automatically selected and the PCF2113x attempts to perform the first write as an 8-bit operation. Since nothing is connected to DB0 to DB3, a rewrite is then required.

However, since one operation is completed in two accesses of 4-bit operation, a rewrite is required to set the functions (see Table 12 step 3).

Thus, DB4 to DB7 of the 'function set' are written twice.

18.3 8-bit operation, 2-line display

For a 2-line display, the cursor automatically moves from the first to the second line after the 40th digit of the first line has been written. Thus, if there are only 8 characters in the first line, the DDRAM address must be set after the eighth character is completed (see Table 5). Note that both lines of the display are always shifted together; data does not shift from one line to the other.

18.4 I²C operation, 1-line display

A control byte is required with most instructions (see Table 16).

Table 12 4-bit operation, 1-line display example; using internal reset

STEP	INSTRUCTION						DISPLAY	OPERATION
1	power supply on (PCF2113x is initialized by the internal reset circuit)							initialized; no display appears
2	function set							
	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4		sets to 4-bit operation; in this instance operation is handled as 8-bits by initialization and only this instruction completes with one write
	0	0	0	0	1	0		
3	function set							
	0	0	0	0	1	0		sets to 4-bit operation, selects 1-line display and $V_{LCD} = V_0$; 4-bit operation starts from this point and resetting is needed
	0	0	0	0	0	0		
4	display on/off control							
	0	0	0	0	0	0	_	turns on display and cursor; entire display is blank after initialization
	0	0	1	1	1	0		
5	entry mode set							
	0	0	0	0	0	0	_	sets mode to increment the address by 1 and to shift the cursor to the right at the time of write to the DD/CGRAM; display is not shifted
	0	0	0	1	1	0		
6	'write data' to CGRAM/DDRAM							
	1	0	0	1	0	1	P_	writes 'P'; the DDRAM has already been selected by initialization at power-on; the cursor is incremented by 1 and shifted to the right
	1	0	0	0	0	0		

Table 13 8-bit operation, 1-line display example; using internal reset (character set 'A')

STEP	INSTRUCTION	DISPLAY	OPERATION
1	power supply on (PCF2113x is initialized by the internal reset function)		initialized; no display appears
2	function set RS R/$\overline{W}$ DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 1 1 0 0 0 0		sets to 8-bit operation, selects 1-line display and $V_{LCD} = V_0$
3	display mode on/off control 0 0 0 0 0 0 1 1 1 0	_	turns on display and cursor; entire display is blank after initialization
4	entry mode set 0 0 0 0 0 0 0 1 1 0	_	sets mode to increment the address by 1 and to shift the cursor to the right at the time of the write to the DD/CGRAM; display is not shifted
5	'write data' to CGRAM/DDRAM 1 0 0 1 0 1 0 0 0 0	**P**_	writes 'P'; the DDRAM has already been selected by initialization at power-on; the cursor is incremented by 1 and shifted to the right
6	'write data' to CGRAM/DDRAM 1 0 0 1 0 0 1 0 0 0	**PH**_	writes 'H'
7 to 11			
12	'write data' to CGRAM/DDRAM 1 0 0 1 0 1 0 0 1 1	**PHILIPS**_	writes 'S'
13	entry mode set 0 0 0 0 0 0 0 1 1 1	**PHILIPS**_	sets mode for display shift at the time of write
14	'write data' to CGRAM/DDRAM 1 0 0 0 1 0 0 0 0 0	**HILIPS** _	writes space
15	'write data' to CGRAM/DDRAM 1 0 0 1 0 0 1 1 0 1	**ILIPS M**_	writes 'M'
16			

STEP	INSTRUCTION	DISPLAY	OPERATION
17	'write data' to CGRAM/DDRAM 1 0 0 1 0 0 1 1 1 1	**MICROKO_**	writes 'O'
18	cursor/display shift 0 0 0 0 0 1 0 0 0 0	**MICROKO**	shifts only the cursor position to the left
19	cursor/display shift 0 0 0 0 0 1 0 0 0 0	**MICROKO**	shifts only the cursor position to the left
20	'write data' to CGRAM/DDRAM 1 0 0 1 0 0 0 0 1 1	**ICROCO**	writes 'C' correction; the display moves to the left
21	cursor/display shift 0 0 0 0 0 1 1 1 0 0	**MICROCO**	shifts the display and cursor to the right
22	cursor/display shift 0 0 0 0 0 1 0 1 0 0	**MICROCO_**	shifts only the cursor to the right
23	'write data' to CGRAM/DDRAM 1 0 0 1 0 0 1 1 0 1	**ICROCOM_**	writes 'M'
24			
25	return home 0 0 0 0 0 0 0 0 1 0	**PHILIPS M**	returns both display and cursor to the original position (address 0)

Table 14 8-bit operation, 1-line display and icon example; using internal reset (character set 'A')

STEP	INSTRUCTION	DISPLAY	OPERATION
1	power supply on (PCF2113x is initialized by the internal reset function)		initialized; no display appears
2	function set RS R/$\overline{W}$ DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 1 1 0 0 0 0		sets to 8-bit operation, selects 1-line display and $V_{LCD} = V_0$
3	display mode on/off control 0 0 0 0 0 0 1 1 1 0	_	turns on display and cursor; entire display is blank after initialization
4	entry mode set 0 0 0 0 0 0 0 1 1 0	_	sets mode to increment the address by 1 and to shift the cursor to the right at the time of the write to the DD/CGRAM; display is not shifted
5	set CGRAM address 0 0 0 1 0 0 0 0 0 0	_	sets the CGRAM address to position of character 0; the CGRAM is selected
6	'write data' to CGRAM/DDRAM 1 0 0 0 0 0 1 0 1 0	_	writes data to CGRAM for icon even phase; icons appears
7			
8	set CGRAM address 0 0 0 1 1 1 0 0 0 0	_	sets the CGRAM address to position of character 4; the CGRAM is selected
9	'write data' to CGRAM/DDRAM 1 0 0 0 0 0 1 0 1 0	_	writes data to CGRAM for icon odd phase
10			
11	function set 0 0 0 0 1 1 0 0 0 1	_	sets H = 1
12	icon control 0 0 0 0 0 0 1 0 1 0	_	icons blink
13	function set 0 0 0 0 1 1 0 0 0 1	_	sets H = 0

STEP	INSTRUCTION	DISPLAY	OPERATION
14	set DDRAM address 0 0 1 0 0 0 0 0 0 0		sets the DDRAM address to the first position; DDRAM is selected
15	'write data' to CGRAM/DDRAM 1 0 0 1 0 1 0 0 0 0	**P_**	writes 'P'; the cursor is incremented by 1 and shifted to the right
16	'write data' to CGRAM/DDRAM 1 0 0 1 0 0 1 0 0 0	**PH_**	writes 'H'
17 to 20		|	
21	return home 0 0 0 0 0 0 0 0 1 0	**PHILIPS**	returns both display and cursor to the original position (address 0)

Table 15 8-bit operation, 2-line display example; using internal reset

STEP	INSTRUCTION	DISPLAY	OPERATION
1	power supply on (PCF2113x is initialized by the internal reset function)		initialized; no display appears
2	function set RS R/$\overline{W}$ DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 1 1 1 0 0 0		sets to 8-bit operation; selects 2-line display and voltage generator off
3	display on/off control 0 0 0 0 0 0 1 1 1 0	_	turns on display and cursor; entire display is blank after initialization
4	entry mode set 0 0 0 0 0 0 0 1 1 0	_	sets mode to increment the address by 1 and to shift the cursor to the right at the time of write to the CG/DDRAM; display is not shifted
5	'write data' to CGRAM/DDRAM 1 0 0 1 0 1 0 0 0 0	**P**_	writes 'P'; the DDRAM has already been selected by initialization at power-on; the cursor is incremented by 1 and shifted to the right
6 to 10			
11	'write data' to CGRAM/DDRAM 1 0 0 1 0 1 0 0 1 1	**PHILIPS_**	writes 'S'
12	set DDRAM address 0 0 1 1 0 0 0 0 0 0	**PHILIPS** _	sets DDRAM address to position the cursor at the head of the 2nd line
13	'write data' to CGRAM/ DDRAM 1 0 0 1 0 0 1 1 0 1	**PHILIPS** **M**_	writes 'M'
14 to 19			

STEP	INSTRUCTION	DISPLAY	OPERATION
20	'write data' to CGRAM/DDRAM 1 0 0 1 0 0 1 1 1 1	PHILIPS MICROCO_	writes 'O'
21	'write data' to CGRAM/DDRAM 0 0 0 0 0 0 0 1 1 1	PHILIPS MICROCO_	sets mode for display shift at the time of write
22	'write data' to CGRAM/DDRAM 1 0 0 1 0 0 1 1 0 1	HILIPS ICROCOM_	writes 'M'; display is shifted to the left; the first and second lines shift together
23			
24	return home 0 0 0 0 0 0 0 0 1 0	PHILIPS MICROCOM	returns both display and cursor to the original position (address 0)

Table 16 Example of I²C operation; 1-line display (using internal reset, assuming SA0 = V_{SS}; note 1)

STEP	I²C BYTE									DISPLAY	OPERATION
1	I²C start										initialized; no display appears
2	slave address for write										during the acknowledge cycle SDA will be pulled-down by the PCF2113x
	SA6	SA5	SA4	SA3	SA2	SA1	SA0	R/$\overline{W}$	Ack		
	0	1	1	1	0	1	0	0	1		
3	send a control byte for 'function set'										control byte sets RS for following data bytes
	Co	RS	0	0	0	0	0	0	Ack		
	0	0	0	0	0	0	0	0	1		
4	function set										selects 1-line display and $V_{LCD} = V_0$; SCL pulse during acknowledge cycle starts execution of instruction
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Ack		
	0	0	1	X	0	0	0	0	1		
5	display on/off control									–	turns on display and cursor; entire display shows character 20H (blank in ASCII-like character sets)
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Ack		
	0	0	0	0	1	1	1	0	1		
6	entry mode set									–	sets mode to increment the address by 1 and to shift the cursor to the right at the time of write to the DDRAM or CGRAM; display is not shifted
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Ack		
	0	0	0	0	0	1	1	0	1		
7	I²C start									–	for writing data to DDRAM, RS must be set to 1; therefore a control byte is needed
8	slave address for write									–	
	SA6	SA5	SA4	SA3	SA2	SA1	SA0	R/$\overline{W}$	Ack		
	0	1	1	1	0	1	0	0	1		
9	send a control byte for 'write data'									–	
	Co	RS	0	0	0	0	0	0	Ack		
	0	1	0	0	0	0	0	0	1		
10	'write data' to DDRAM										writes 'P'; the DDRAM has been selected at power-up; the cursor is incremented by 1 and shifted to the right
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Ack		
	0	1	0	1	0	0	0	0	1	**P**_	

STEP	I²C BYTE	DISPLAY	OPERATION
11	'write data' to DDRAM DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 1 0 0 1 0 0 0 1	**PH_**	writes 'H'
12 to 15			
16	'write data' to DDRAM DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 1 0 1 0 0 1 1 1	**PHILIPS_**	writes 'S'
17	(optional I²C stop) I²C start + slave address for write (as step 8)	**PHILIPS_**	
18	control byte Co RS 0 0 0 0 0 0 Ack 1 0 0 0 0 0 0 0 1	**PHILIPS_**	
19	return home DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 0 0 0 0 0 1 0 1	**PHILIPS**	sets DDRAM address 0 in Address Counter (also returns shifted display to original position; DDRAM contents unchanged); this instruction does not update the Data Register (DR)
20	I²C start	**PHILIPS**	
21	slave address for read SA6 SA5 SA4 SA3 SA2 SA1 SA0 R/$\overline{W}$ Ack 0 1 1 1 0 1 0 1 1	**PHILIPS**	during the acknowledge cycle the content of the DR is loaded into the internal I²C interface to be shifted out; in the previous instruction neither a 'set address' nor a 'read data' has been performed; therefore the content of the DR was unknown. The R/W has to be set to 1 while still in I²C-write mode.
22	control byte for read Co RS 0 0 0 0 0 0 Ack 0 1 1 0 0 0 0 0 1	**PHILIPS**	DDRAM content will be read from following instructions

STEP	I²C BYTE	DISPLAY	OPERATION
23	'read data': 8 × SCL + master acknowledge; note 2 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack X X X X X X X X 0	PHILIPS	8 × SCL; content loaded into interface during previous acknowledge cycle is shifted out over SDA; MSB is DB7; during master acknowledge content of DDRAM address 01 is loaded into the I²C interface
24	'read data': 8 × SCL + master acknowledge; note 2 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 1 0 0 1 0 0 0 0	PHILIPS	8 × SCL; code of letter 'H' is read first; during master acknowledge code of 'I' is loaded into the I²C interface
25	'read data': 8 × SCL + no master acknowledge; note 2 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 1 0 0 1 0 0 1 1	PHILIPS	no master acknowledge; after the content of the I²C interface register is shifted out no internal action is performed; no new data is loaded to the interface register, Data Register (DR) is not updated, Address Counter (AC) is not incremented and cursor is not shifted
26	I²C stop	PHILIPS	

Notes

1. X = don't care.
2. SDA is left at high-impedance by the microcontroller during the read acknowledge.

Table 17 Initialization by instruction, 8-bit interface (note 1)

STEP										DESCRIPTION
power-on or unknown state										
					|					
wait 2 ms after V_{DD} rises above V_{POR}										
					|					
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	BF cannot be checked before this instruction
0	0	0	0	1	1	X	X	X	X	function set (interface is 8 bits long)
					|					
wait 2 ms										
					|					
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	BF cannot be checked before this instruction
0	0	0	0	1	1	X	X	X	X	function set (interface is 8 bits long)
					|					
wait more than 40 μs										
					|					
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	BF cannot be checked before this instruction
0	0	0	0	1	1	X	X	X	X	function set (interface is 8 bits long)
					|				BF can be checked after the following instructions; when BF is not checked, the waiting time between instructions is the specified instruction time (see Table 3)
					|					
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	function set (interface is 8 bits long); specify the number of display lines.
0	0	0	0	1	1	0	M	0	H	
0	0	0	0	0	0	1	0	0	0	display off
0	0	0	0	0	0	0	0	0	1	clear display
0	0	0	0	0	0	0	1	I/D	S	entry mode set
					|					
Initialization ends										

Note

1. X = don't care.

Table 18 Initialization by instruction, 4-bit interface; not applicable for I²C-bus operation

STEP						DESCRIPTION
Power-on or unknown state						
Wait 2 ms after V_{DD} rises above V_{POR}						
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	BF cannot be checked before this instruction
0	0	0	0	1	1	function set (interface is 8 bits long)
Wait 2 ms						
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	BF cannot be checked before this instruction
0	0	0	0	1	1	function set (interface is 8 bits long)
Wait 40 µs						
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	BF cannot be checked before this instruction
0	0	0	0	1	1	function set (interface is 8 bits long)
						BF can be checked after the following instructions; when BF is not checked, the waiting time between instructions is the specified instruction time (see Table 3)
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	function set (set interface to 4 bits long)
0	0	0	0	1	0	interface is 8 bits long
0	0	0	0	1	0	function set (interface is 4 bits long)
0	0	0	M	0	H	specify number of display lines
0	0	0	0	0	0	
0	0	1	0	0	0	display off
0	0	0	0	0	0	clear display
0	0	0	0	0	1	
0	0	0	0	0	0	entry mode set
0	0	0	1	I/D	S	
Initialization ends						

19 BONDING PAD LOCATIONS

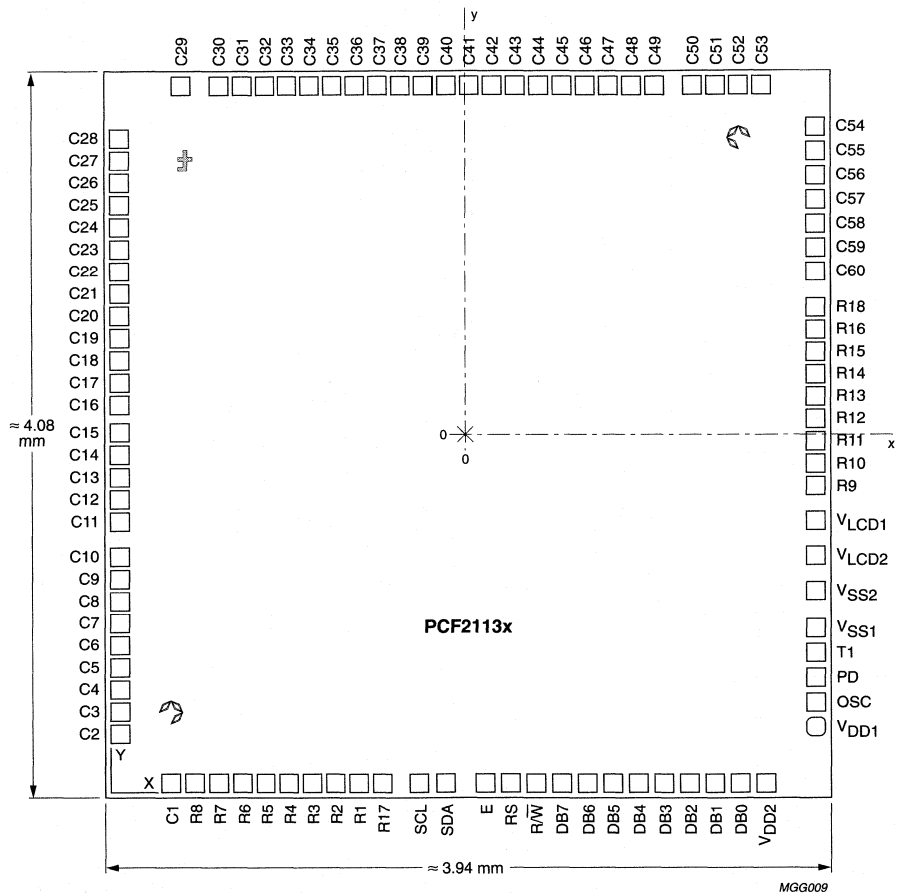


Fig.32 Bonding pad locations.

Table 19 Bonding pad locations (dimensions in μm) All x/y coordinates are referenced to centre of chip (see Fig.32).

SYMBOL	PAD	X	Y
V_{DD1}	1	1811.3	−1547.1
OSC	2	1811.3	−1416.5
PD	3	1811.3	−1285.9
T1	4	1811.3	−1155.3
V_{SS1}	5	1811.3	−1024.7
V_{SS2}	6	1811.3	−822.1
V_{LCD2}	7	1811.3	−633.9
V_{LCD1}	8	1811.3	−446.3
R9	9	1811.3	−264.0
R10	10	1811.3	−144.0
R11	11	1811.3	−24.0
R12	12	1811.3	96.0
R13	13	1811.3	216.0
R14	14	1811.3	336.0
R15	15	1811.3	456.0
R16	16	1811.3	576.0
R18	17	1811.3	696.0
C60	18	1811.3	889.4
C59	19	1811.3	1009.4
C58	20	1811.3	1129.4
C57	21	1811.3	1249.4
C56	22	1811.3	1369.4
C55	23	1811.3	1489.4
C54	24	1811.3	1609.4
C53	25	1536.5	1877.7
C52	26	1416.5	1877.7
C51	27	1296.5	1877.7
C50	28	1176.5	1877.7
C49	29	983.9	1877.7
C48	30	863.9	1877.7
C47	31	743.9	1877.7
C46	32	623.9	1877.7
C45	33	503.9	1877.7
C44	34	383.9	1877.7
C43	35	263.9	1877.7
C42	36	143.9	1877.7
C41	37	23.9	1877.7
C40	38	−96.1	1877.7L

SYMBOL	PAD	X	Y
C39	39	−216.1	1877.7
C38	40	−336.1	1877.7
C37	41	−456.1	1877.7
C36	42	−576.1	1877.7
C35	43	−696.1	1877.7
C34	44	−816.1	1877.7
C33	45	−936.1	1877.7
C32	46	−1056.1	1877.7
C31	47	−1176.1	1877.7
C30	48	−1296.1	1877.7
C29	49	−1488.7	1877.7
C28	50	−1811.3	1609.4
C27	51	−1811.3	1489.4
C26	52	−1811.3	1369.4
C25	53	−1811.3	1249.4
C24	54	−1811.3	1129.4
C23	55	−1811.3	1009.4
C22	56	−1811.3	889.4
C21	57	−1811.3	769.4
C20	58	−1811.3	649.4
C19	59	−1811.3	529.4
C18	60	−1811.3	409.4
C17	61	−1811.3	289.4
C16	62	−1811.3	169.4
C15	63	−1811.3	23.2
C14	64	−1811.3	−96.8
C13	65	−1811.3	−216.8
C12	66	−1811.3	−336.8
C11	67	−1811.3	−456.8
C10	68	−1811.3	−649.4
C9	69	−1811.3	−769.4
C8	70	−1811.3	−889.4
C7	71	−1811.3	−1009.4
C6	72	−1811.3	−1129.4
C5	73	−1811.3	−1249.4
C4	74	−1811.3	−1369.4
C3	75	−1811.3	−1489.4
C2	76	−1811.3	−1609.4

SYMBOL	PAD	X	Y
C1	77	−1542.7	−1877.7
R8	78	−1422.4	−1877.7
R7	79	−1302.4	−1877.7
R6	80	−1182.4	−1877.7
R5	81	−1062.4	−1877.7
R4	82	−942.4	−1877.7
R3	83	−822.4	−1877.7
R2	84	−702.4	−1877.7
R1	85	−582.4	−1877.7
R17	86	−462.4	−1877.7
SCL	87	−271.2	−1877.7
SDA	88	−130.2	−1877.7
E	89	74.4	−1877.7
RS	90	205.1	−1877.7
RW	91	335.7	−1877.7
DB7	92	468.8	−1877.7
DB6	93	603.8	−1877.7
DB5	94	738.8	−1877.7
DB4	95	873.8	−1877.7
DB3	96	1008.8	−1877.7
DB2	97	1143.8	−1877.7
DB1	98	1278.8	−1877.7
DB0	99	1413.8	−1877.7
V_{DD2}	100	1546.0	−1877.7
Sign C1		−1518.0	−1387.7
Sign C2		1405.0	1671.3
Sign f		−1491.0	1602.3

CONTENTS

1 FEATURES

- Single chip LCD controller/driver
- 1 or 2-line display of up to 24 characters per line, or 2 or 4 lines of up to 12 characters per line
- 5 × 7 character format plus cursor; 5 × 8 for kana (Japanese syllabary) and user defined symbols
- On-chip:
  - generation of LCD supply voltage (external supply also possible)
  - generation of intermediate LCD bias voltages
  - oscillator requires no external components (external clock also possible)
- Display data RAM: 80 characters
- Character generator ROM: 240 characters
- Character generator RAM: 16 characters
- 4 or 8-bit parallel bus or 2-wire I²C-bus interface
- CMOS/TTL compatible
- 32 row, 60 column outputs
- MUX rates 1 : 32 and 1 : 16
- Uses common 11 code instruction set
- Logic supply voltage range, $V_{DD} - V_{SS}$: 2.5 to 6 V
- Display supply voltage range, $V_{DD} - V_{LCD}$: 3.5 to 9 V
- Low power consumption
- I²C-bus address: 011101 SA0.

2 APPLICATIONS

- Telecom equipment
- Portable instruments
- Point-of-sale terminals.

3 GENERAL DESCRIPTION

The PCF2116 family of LCD controller/drivers consists of the PCF2116x, the PCF2114x and the PCF2116K. The term 'PCF2116' is used to refer to all devices for common information. Specific information is given in separate paragraphs.

The 'x' in 'PCF2116x' and 'PCF2114x' represents a specific letter code for a character set in the character generator ROM (CGROM). The different character sets currently available are specified by the letters A, C, and G (see Figs 8 to 10). Other character sets are available on request.

The PCF2116 is a low-power CMOS LCD controller and driver, designed to drive a split screen dot matrix LCD display of 1 or 2 lines by 24 characters or 2 or 4 lines by 12 characters with 5 × 8 dot format. All necessary functions for the display are provided in a single chip, including on-chip generation of LCD bias voltages, resulting in a minimum of external components and lower system power consumption. The chip contains a character generator and displays alphanumeric and kana (Japanese) characters. The PCF2116 interfaces to most microcontrollers via a 4 or 8-bit bus or via the 2-wire I²C-bus. To allow partial V_{DD} shutdown the ESD protection system of the SCL and SDA pins does not use a diode connected to V_{DD}.

The PCF2116K differs from the other members of the family in that:

- V_{LCD}/V_{OP} generation is different (see Section 8.1)
- It is available with character set C only (see Fig.9).

4 ORDERING INFORMATION

TYPE NUMBER[1]	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF2116xU/10	–	chip on flexible film carrier	–
PCF2114xU/10	–	chip on flexible film carrier	–
PCF2116xU/12	–	chip with bumps on flexible film carrier	–
PCF2114xU/12	–	chip with bumps on flexible film carrier	–
PCF2116xHZ	LQFP128	plastic low profile quad flat package; 128 leads; body 14 × 20 × 1.4 mm	SOT425-1

Note

1. The letter 'x' in the type number represents the letter of the required built-in character set: A, C or G.

5 BLOCK DIAGRAM

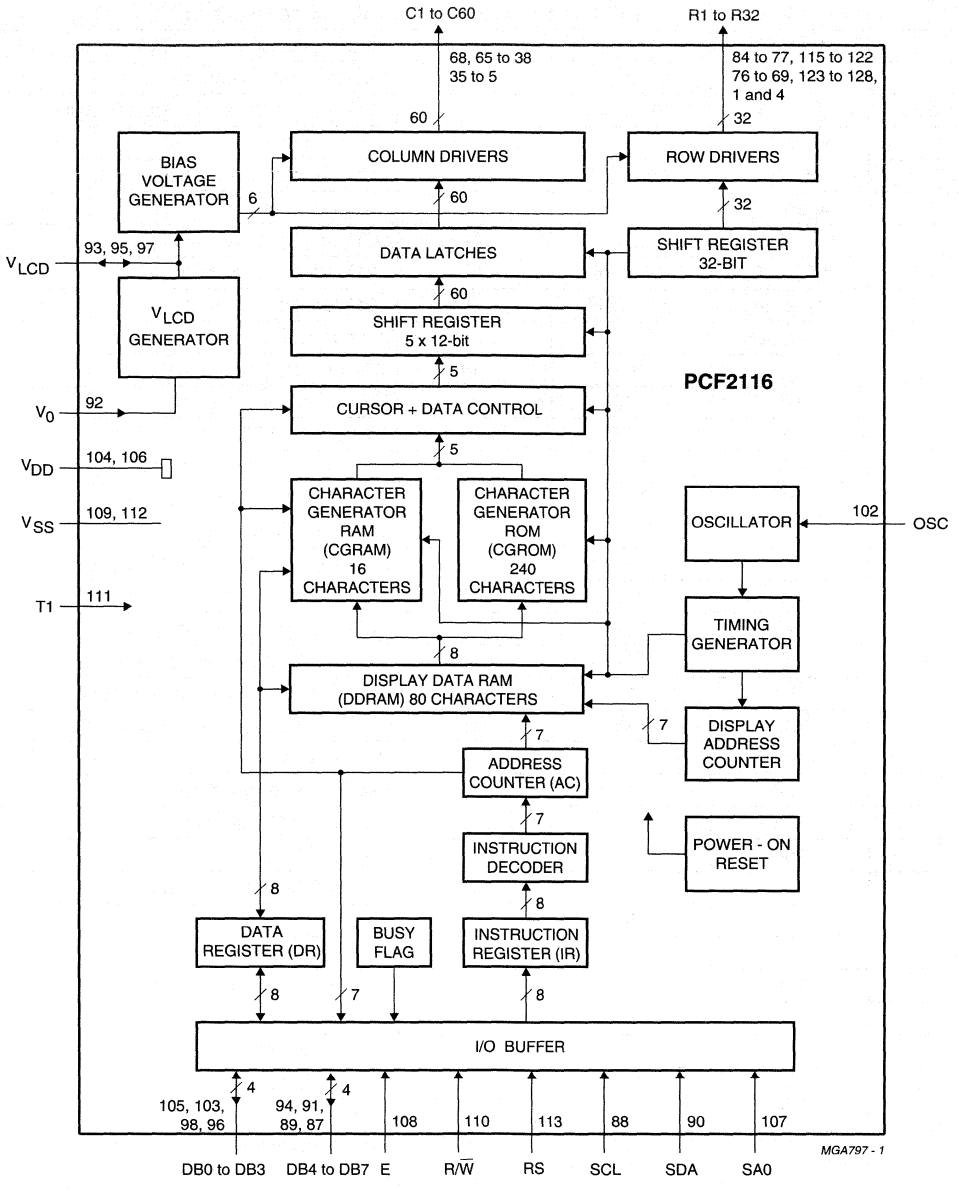


Fig.1 Block diagram (pin numbers for LQFP128 package).

6 PINNING

SYMBOL	LQFP128	FFC PAD	TYPE	DESCRIPTION
R31	1	27	O	LCD row driver output
n.c.	2 and 3	–	–	not connected
R32	4	28	O	LCD row driver output
C60 to C30	5 to 35	29 to 59	O	LCD column driver outputs 60 to 30
n.c.	36 and 37	–	–	not connected
C29 to C2	38 to 65	60 to 87	O	LCD column driver outputs 29 to 2
n.c.	66 and 67	–	–	not connected
C1	68	88	O	LCD column driver output 1
R24 to R17	69 to 76	89 to 96	O	LCD row driver outputs
R8 to R1	77 to 84	97 to 104	O	LCD row driver outputs
n.c.	85 and 86	–	–	not connected
DB7	87	105	I/O	1 bit of 8-bit bidirectional data bus
SCL	88	106	I	I^2C-bus serial clock input
DB6	89	107	I/O	1 bit of 8-bit bidirectional data bus
SDA	90	108	I/O	I^2C-bus serial data input/output
DB5	91	109	I/O	1 bit of 8-bit bidirectional data bus
V_0	92	110	I	control input for V_{LCD}
V_{LCD1}	93	111	I/O	LCD supply voltage input/output 1
DB4	94	112	I/O	1 bit of 8-bit bidirectional data bus
V_{LCD2}	95	113	I/O	LCD supply voltage input/output 2
DB3	96	114	I/O	1 bit of 8-bit bidirectional data bus
V_{LCD3}	97	115	I/O	LCD supply voltage input/output 3
DB2	98	116	I/O	1 bit of 8-bit bidirectional data bus
n.c.	99 to 101	–	–	not connected
OSC	102	1	I	oscillator/external clock input
DB1	103	2	I/O	1 bit of 8-bit bidirectional data bus
V_{DD2}	104	3	P	supply voltage 2
DB0	105	4	I/O	1 bit of 8-bit bidirectional data bus
V_{DD1}	106	5	P	supply voltage 1
SA0	107	6	I	I^2C-bus address pin
E	108	7	I	data bus clock input (parallel control)
V_{SS1}	109	8	P	ground (logic) 1
R/$\overline{W}$	110	9	I	read/write input (parallel control)
T1	111	10	I	test pad (connect to V_{SS})
V_{SS2}	112	11	P	ground (logic) 2
RS	113	12	I	register select input (parallel control)
n.c.	114	–	–	not connected
R9 to R16	115 to 122	13 to 20	O	LCD row driver outputs
R25 to R30	123 to 128	21 to 26	O	LCD row driver outputs

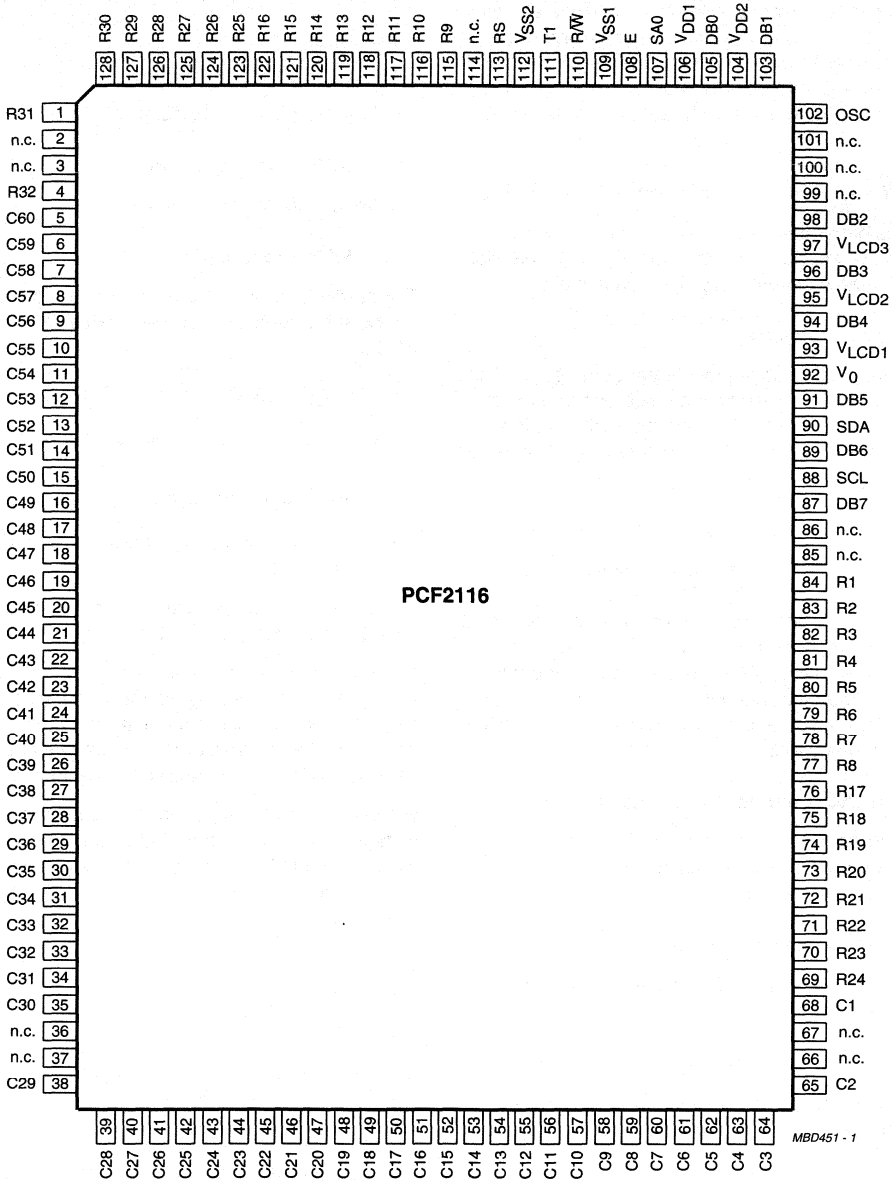


Fig.2 Pin configuration (LQFP128).

7 PIN FUNCTIONS

7.1 RS: register select (parallel control)

RS selects the register to be accessed for read and write when the device is controlled by the parallel interface. RS = logic 0 selects the instruction register for write and the Busy Flag and Address Counter for read. RS = logic 1 selects the data register for both read and write. There is an internal pull-up on pin RS.

7.2 R/$\overline{W}$: read/write (parallel control)

R/$\overline{W}$ selects either the read (R/$\overline{W}$ = logic 1) or write (R/$\overline{W}$ = logic 0) operation when control is by the parallel interface. There is an internal pull-up on this pin.

7.3 E: data bus clock

The E pin is set HIGH to signal the start of a read or write operation when the device is controlled by the parallel interface. Data is clocked in or out of the chip on the negative edge of the clock. Note that this pin must be tied to logic 0 (V_{SS}) when I²C-bus control is used.

7.4 DB0 to DB7: data bus

The bidirectional, 3-state data bus transfers data between the system controller and the PCF2116. DB7 may be used as the Busy Flag, signalling that internal operations are not yet completed. In 4-bit operations the 4 higher order lines DB4 to DB7 are used; DB0 to DB3 must be left open circuit. There is an internal pull-up on each of the data lines. Note that these pins must be left open circuit when I²C-bus control is used.

7.5 C1 to C60: column driver outputs

These pins output the data for pairs of columns. This arrangement permits optimized chip-on-glass (COG) layout for 4-line by 12 characters.

7.6 R1 to R32: row driver outputs

These pins output the row select waveforms to the left and right halves of the display.

7.7 V_{LCD}: LCD power supply

Negative power supply for the liquid crystal display. This may be generated on-chip or supplied externally.

7.8 V_0: V_{LCD} control input

The input level at this pin determines the generated V_{LCD} output voltage.

7.9 OSC: oscillator

When the on-chip oscillator is used this pin must be connected to V_{DD}. An external clock signal, if used, is input at this pin.

7.10 SCL: serial clock line

Input for the I²C-bus clock signal.

7.11 SDA: serial data line

Input/output for the I²C-bus data line.

7.12 SA0: address pin

The hardware sub-address line is used to program the device sub-address for 2 different PCF2116s on the same I²C-bus.

7.13 T1: test pad

Must be connected to V_{SS}. Not user accessible.

8 FUNCTIONAL DESCRIPTION (see Fig.1)

8.1 LCD supply voltage generator, PCF2114x and PCF2116x

The on-chip voltage generator is controlled by bit G of the 'Function set' instruction and V_0.

V_0 is a high-impedance input and draws no current from the system power supply. Its range is between V_{SS} and V_{DD} – 1 V. When V_0 is connected to V_{DD} the generator is switched off and an external voltage must be supplied to pin V_{LCD}. This may be more negative than V_{SS}.

When G = logic 1 the generator produces a negative voltage at pin V_{LCD}, controlled by the input voltage at pin V_0. The LCD operating voltage is given by the relationship:

$$V_{OP} = 1.8V_{DD} - V_0$$

Where:

$$V_{OP} = V_{DD} - V_{LCD}$$

$$V_{LCD} = V_0 - (0.8V_{DD})$$

When G = logic 0, the generated output voltage V_{LCD} is equal to V_0 (between V_{SS} and V_{DD}). In this instance:

$$V_{OP} = V_{DD} - V_0$$

When V_{LCD} is generated on-chip the V_{LCD} pin should be decoupled to V_{DD} with a suitable capacitor. V_{DD} and V_0 must be selected to limit the maximum value of V_{OP} to 9 V.

Figure 3 shows the two generator control characteristics.

8.2 LCD supply voltage generator, PCF2116K

In the PCF2116K version, V_0 is connected through an on-chip resistor (R_0) to V_{LCD}. Resistor R_0 has a nominal value of 1 MΩ and draws a typical current of 4 μA from the pin V_0. A constant voltage (equal to $1.34V_{DD}$) is always present across R_0.

The voltage range of the PCF2116K is between V_{SS} and $V_{DD} - 0.5$ V (see Fig.4). When V_0 is connected to V_{DD} the generator is switched off and an external voltage must be supplied to pin V_{LCD}. This may be more negative than V_{SS}.

When G = logic 1 the generator produces a negative voltage at pin V_{LCD}, controlled by the input voltage at pin V_0. The LCD operating voltage is given by the relationship:

$$V_{OP} = 2.34V_{DD} - V_0$$

Where:

$$V_{OP} = V_{DD} - V_{LCD}$$

$$V_{LCD} = V_0 - (1.34V_{DD})$$

When G = logic 0, the generated output voltage V_{LCD} is equal to V_0 (between V_{SS} and V_{DD}). In this instance:

$$V_{OP} = V_{DD} - V_0$$

8.3 Character generator ROM (CGROM)

The standard character sets A, C and G are available for the PCF2114x and PCF2116x. Standard character set C is available for the PCF2116K.

8.4 LCD bias voltage generator

The intermediate bias voltages for the LCD display are also generated on-chip. This removes the need for an external resistive bias chain and significantly reduces the system power consumption. The optimum levels depend on the multiplex rate and are selected automatically when the number of lines in the display is defined.

The optimum value of V_{OP} depends on the multiplex rate, the LCD threshold voltage (V_{th}) and the number of bias levels and is given by the relationships in Table 1.Using a 5-level bias scheme for 1 : 16 MUX rate allows $V_{OP} < 5$ V for most LCD liquids. The effect on the display contrast is negligible.

8.5 Oscillator

The on-chip oscillator provides the clock signal for the display system. No external components are required. Pin OSC must be connected to V_{DD}.

8.6 External clock

If an external clock is to be used, it must be input at pin OSC. The resulting display frame frequency is given by $f_{frame} = {}^1/_{2304} f_{osc}$. A clock signal must always be present, otherwise the LCD may be frozen in a DC state.

8.7 Power-on reset

The power-on reset block initializes the chip after power-on or power failure.

8.8 Registers

The PCF2116 has two 8-bit registers, an Instruction Register (IR) and a Data Register (DR). The Register Select signal (RS) determines which register will be accessed.

The instruction register stores instruction codes such as 'Display clear' and 'Cursor shift', and address information for the Display Data RAM (DDRAM) and Character Generator RAM (CGRAM). The instruction register can be written to, but not read, by the system controller.

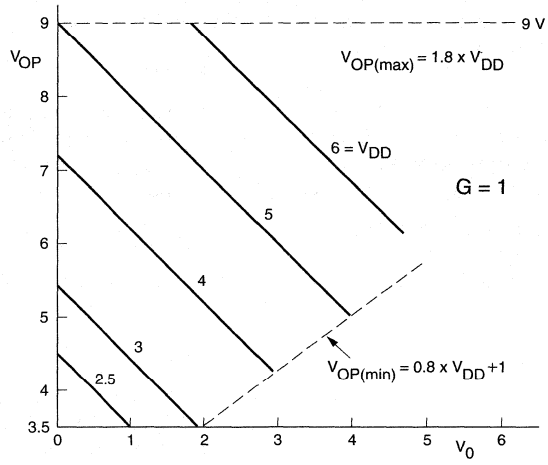
The data register temporarily stores data to be read from the DDRAM and CGRAM. When reading, data from the DDRAM or CGRAM corresponding to the address in the Address Counter is written to the data register prior to being read by the 'Read data' instruction.

8.9 Busy Flag

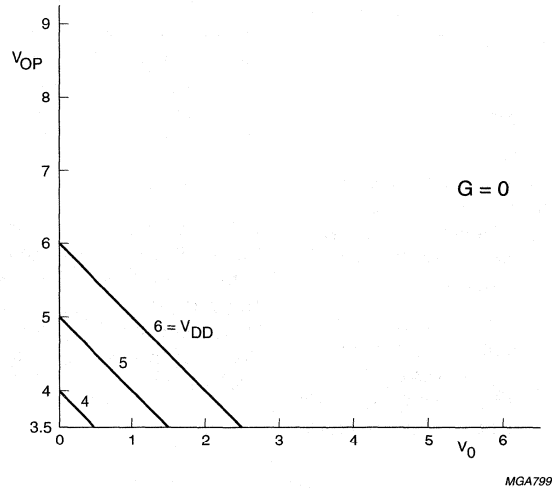
The Busy Flag indicates the free/busy status of the PCF2116. Logic 1 indicates that the chip is busy and further instructions will not be accepted. The Busy Flag is output to pin DB7 when RS = logic 0 and R/$\overline{W}$ = logic 1. Instructions should only be written after checking that the Busy Flag is logic 0 or waiting for the required number of clock cycles.

Table 1 Optimum values for V_{OP}

MUX RATE	NUMBER OF BIAS LEVELS	V_{OP}/V_{th}	DISCRIMINATION V_{on}/V_{off}
1 : 16	5	3.67	1.277
1 : 32	6	5.19	1.196

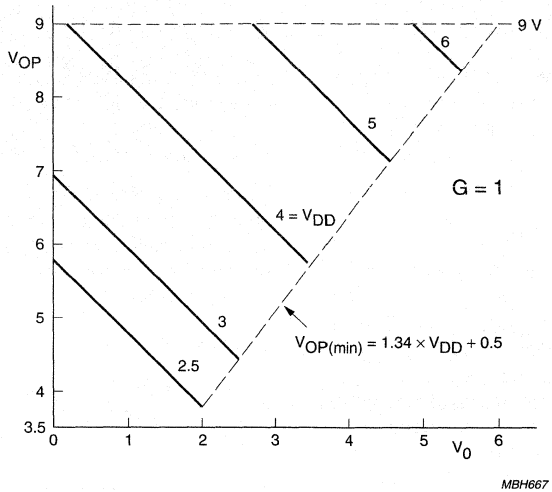


a. High-voltage mode $V_{OP} = 1.8V_{DD} - V_0$.

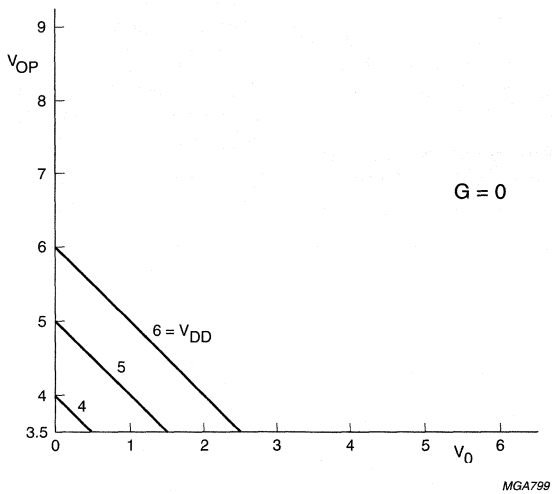


b. Buffer mode $V_{OP} = V_{DD} - V_0$.

Fig.3 V_{OP} as a function of V_0 control characteristics.



a. High-voltage mode $V_{OP} = 2.34V_{DD} - V_0$.



b. Buffer mode $V_{OP} = V_{DD} - V_0$.

Fig.4 V_{OP} as a function of V_0 control characteristics (PCF2116K).

8.10 Address Counter (AC)

The Address Counter assigns addresses to the DDRAM and CGRAM for reading and writing and is set by the instructions 'Set CGRAM address' and 'Set DDRAM address'. After a read/write operation the Address Counter is automatically incremented or decremented by 1.The Address Counter contents are output to the bus (DB0 to DB6) when RS = logic 0 and R/$\overline{W}$ = logic 1.

8.11 Display data RAM (DDRAM)

The display data RAM stores up to 80 characters of display data represented by 8-bit character codes. RAM locations not used for storing display data can be used as general purpose RAM. The basic DDRAM-to-display mapping scheme is shown in Fig.5. With no display shift the characters represented by the codes in the first 12 or 24 RAM locations starting at address 00 in line 1 are displayed. Subsequent lines display data starting at addresses 20, 40, or 60 Hex. Figs 6 and 7 show the DDRAM-to-display mapping principle when the display is shifted.

The address range for a 1-line display is 00 to 4F; for a 2-line display from 00 to 27 (line 1) and 40 to 67 (line 2); for a 4-line display from 00 to 13, 20 to 33, 40 to 53 and 60 to 73 for lines 1, 2, 3 and 4 respectively.
For 2 and 4-line displays the end address of one line and the start address of the next line are not consecutive. When the display is shifted each line wraps around independently of the others (Figs 6 and 7).

When data is written into the DDRAM wrap-around occurs from 4F to 00 in 1-line mode and from 27 to 40 and 67 to 00 in 2-line mode; from 13 to 20, 33 to 40, 53 to 60 and 73 to 00 in 4-line mode.

8.12 Character generator ROM (CGROM)

The character generator ROM generates 240 character patterns in 5 $\times$ 8 dot format from 8-bit character codes. Figures 8 to 10 show the character sets currently available.

8.13 Character generator RAM (CGRAM)

Up to 16 user-defined characters may be stored in the character generator RAM. The CGROM and CGRAM use a common address space, of which the first column is reserved for the CGRAM (see Fig.8). Figure 11 shows the addressing principle for the CGRAM.

8.14 Cursor control circuit

The cursor control circuit generates the cursor (underline and/or character blink as shown in Fig.12) at the DDRAM address contained in the Address Counter. When the Address Counter contains the CGRAM address the cursor will be inhibited.

8.15 Timing generator

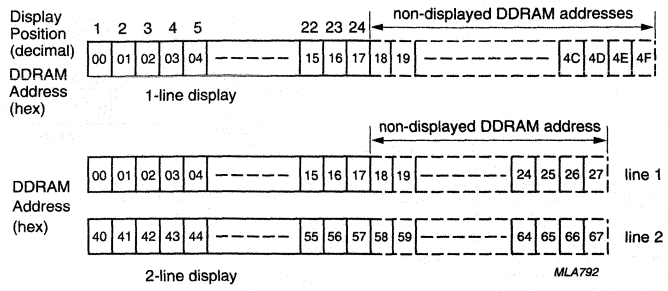
The timing generator produces the various signals required to drive the internal circuitry. Internal chip operation is not disturbed by operations on the data buses.

8.16 LCD row and column drivers

The PCF2116 contains 32 row and 60 column drivers, which connect the appropriate LCD bias voltages in sequence to the display, in accordance with the data to be displayed. The bias voltages and the timing are selected automatically when the number of lines in the display is selected. Figures 13 and 14 show typical waveforms.

In 1-line mode (1 : 16) the row outputs are driven in pairs: R1/R17, R2/R18 for example. This allows the output pairs to be connected in parallel, providing greater drive capability.

Unused outputs should be left unconnected.



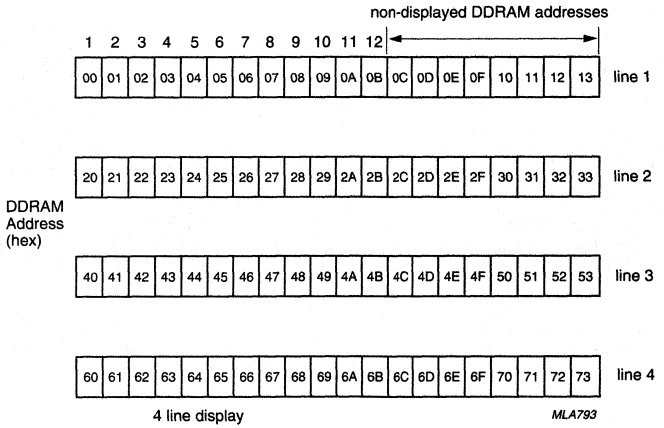


Fig.5 DDRAM-to-display mapping; no shift.

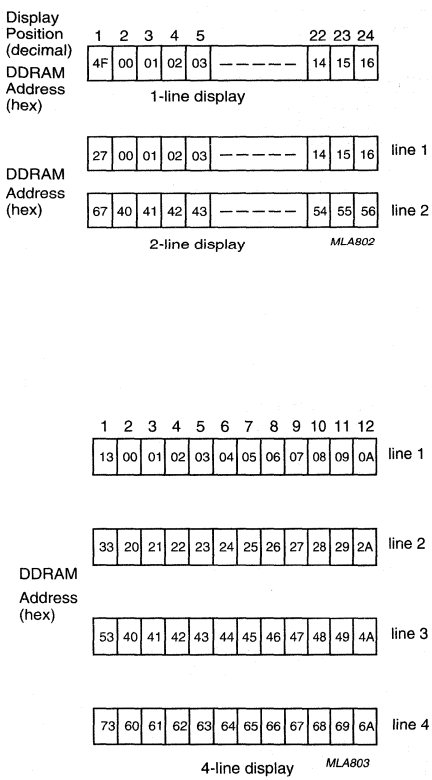


Fig.6 DDRAM-to-display mappi7ng; right shift.

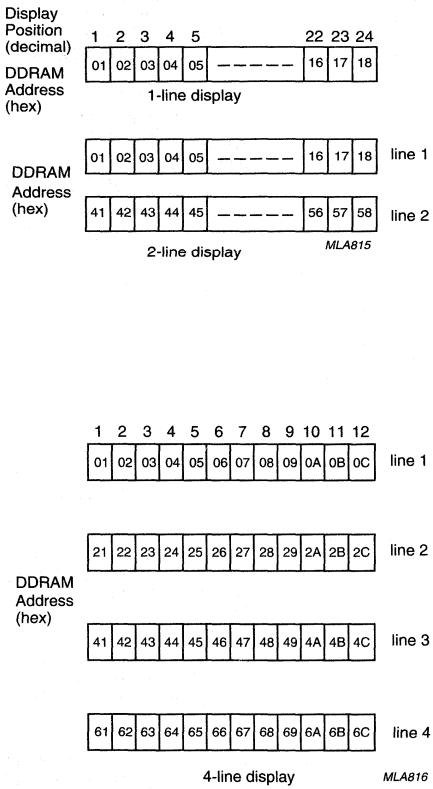


Fig.7 DDRAM-to-display mapping; left shift.

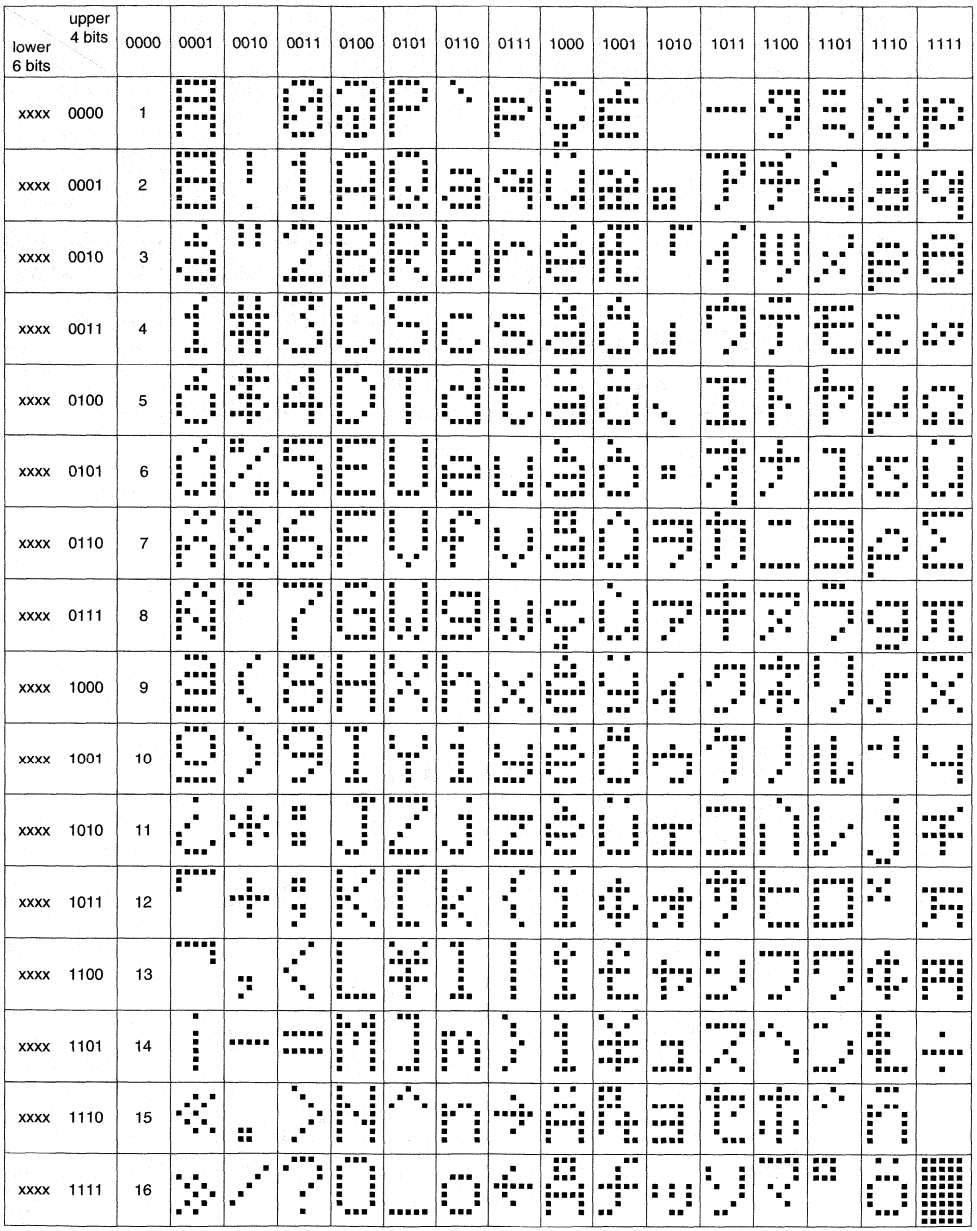


Fig.8 Character set 'A' in CGROM: **PCF2116A; PCF2114A.**

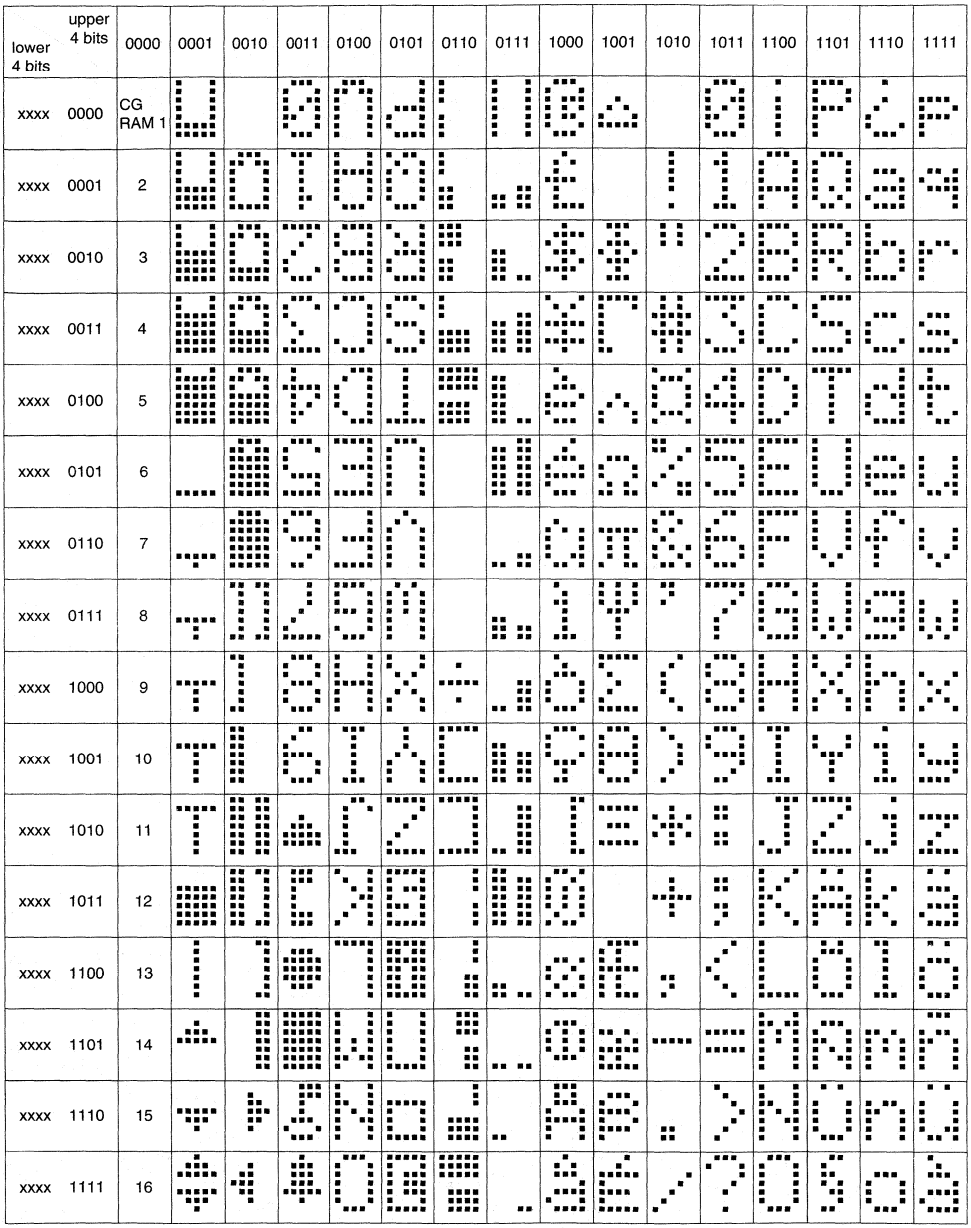


Fig.9 Character set 'C' in CGROM: **PCF2116C; PCF2114C**.

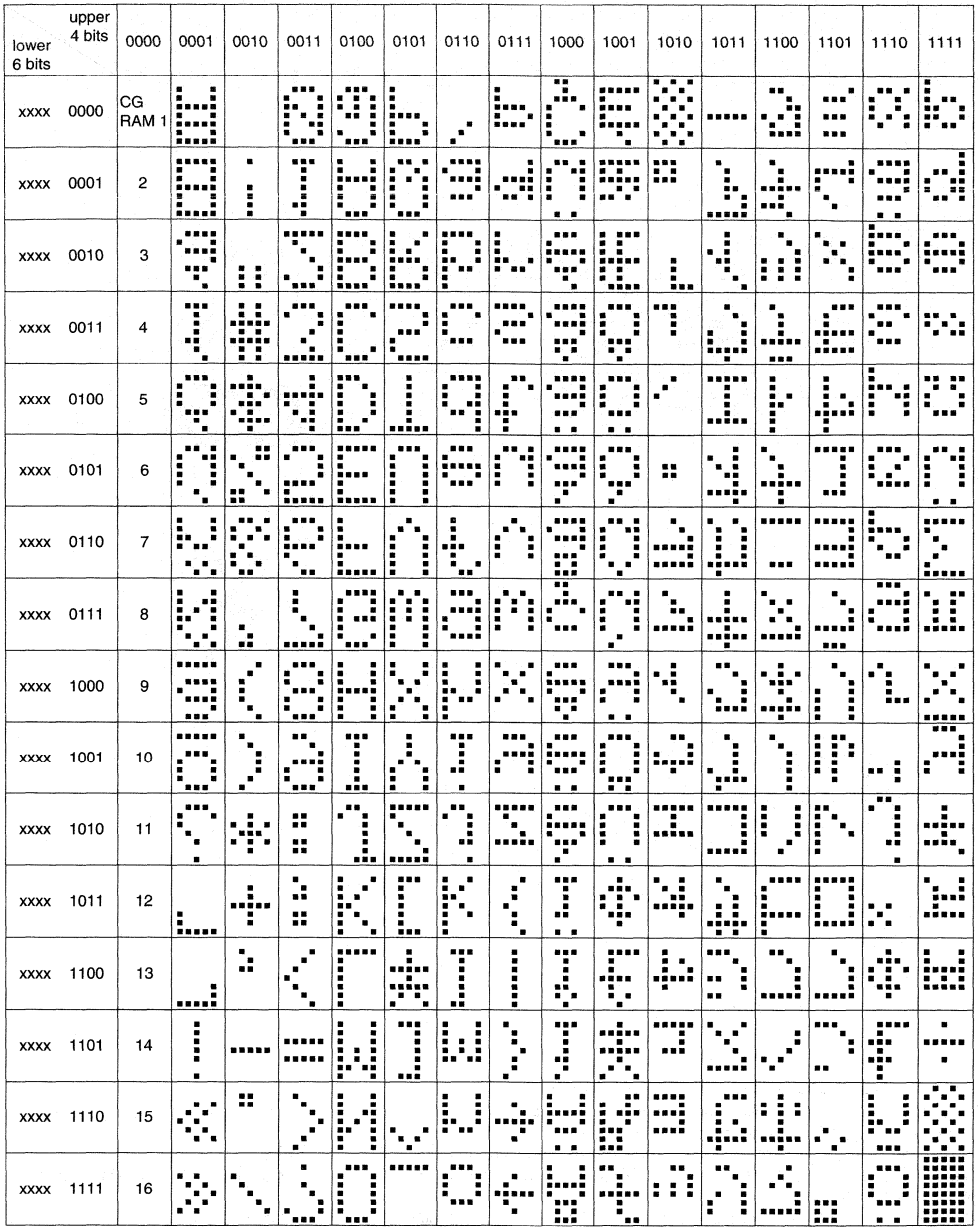
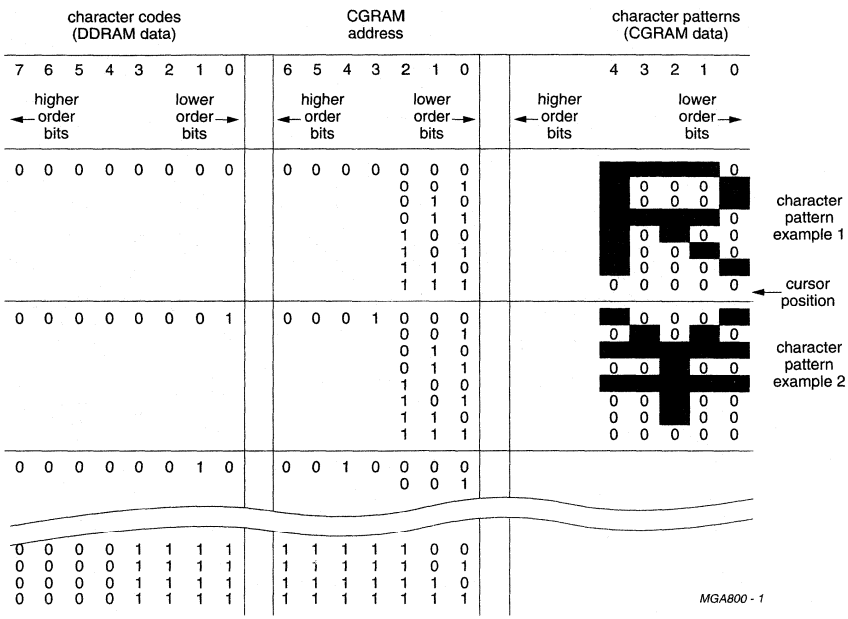


Fig.10 Character set 'G' in CGROM: **PCF2116G; PCF2114G**.



Character code bits 0 to 3 correspond to CGRAM address bits 3 to 6.

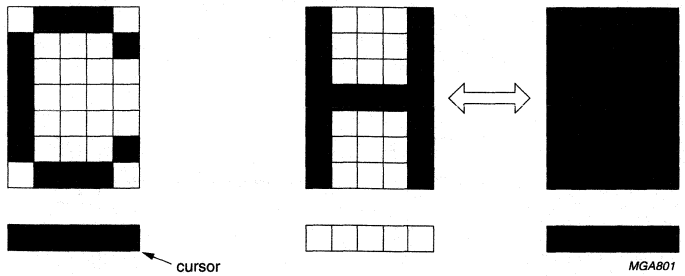
CGRAM address bits 0 to 2 designate character pattern line position. The 8th line is the cursor position and display is performed by logical OR with the cursor. Data in the 8th line will appear in the cursor position.

Character pattern column positions correspond to CGRAM data bits 0 to 4, as shown in Fig.11 (bit 4 being at the left end).

As shown in Figs 8 and 11, CGRAM character patterns are selected when character code bits 4 to 7 are all logic 0. CGRAM data = logic 1 corresponds to selection for display.

Only bits 0 to 5 of the CGRAM address are set by the 'Set CGRAM address' instruction. Bit 6 can be set using the 'Set DDRAM address' instruction or by using the auto-increment feature during CGRAM write. All bits 0 to 6 can be read using the 'Read busy flag and address' instruction.

Fig.11 Relationship between CGRAM addresses and data and display patterns.



5 x 7 dot character font

alternating display

cursor display example

blink display example

Fig.12 Cursor and blink display examples.

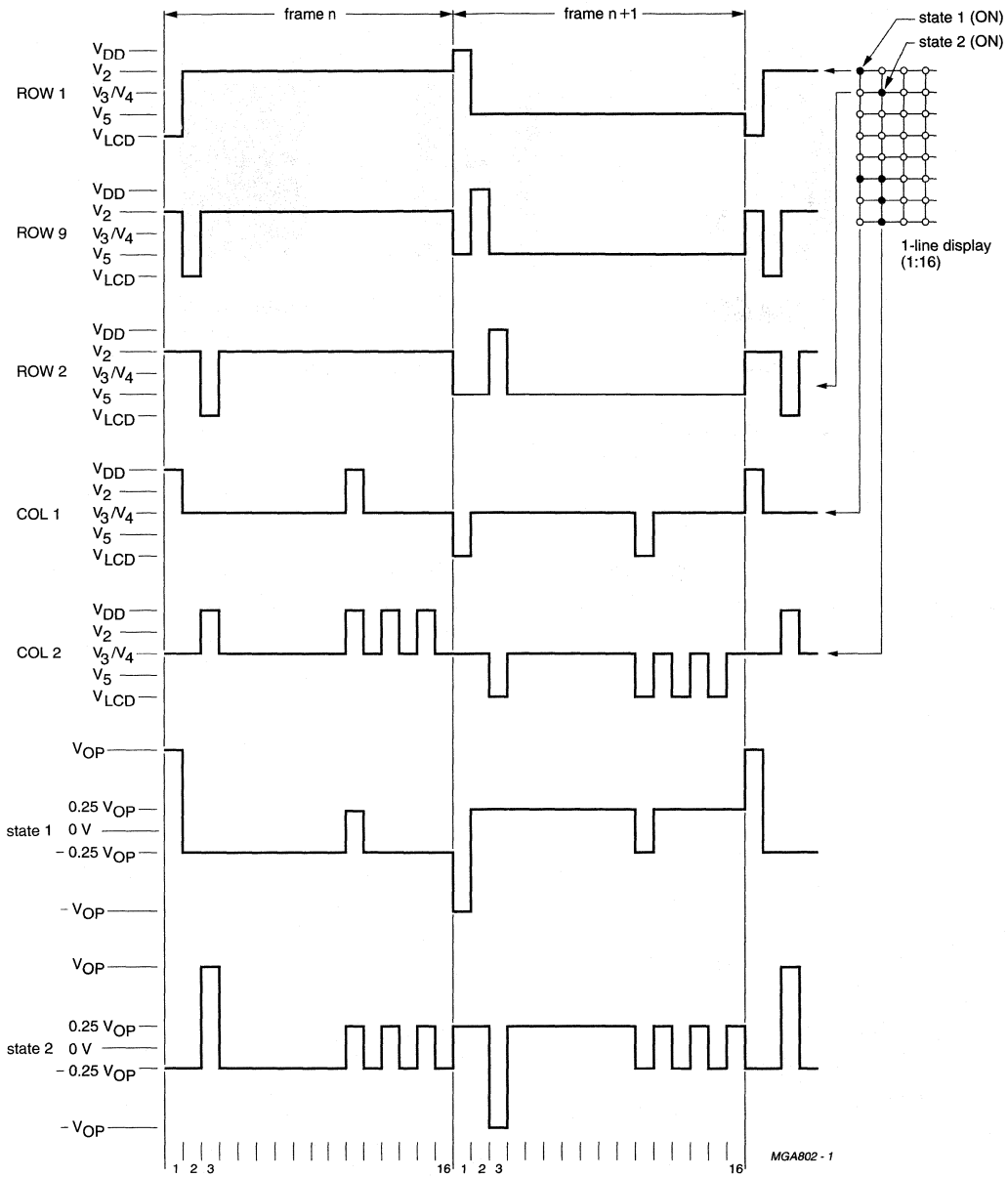


Fig.13 Typical LCD waveforms; 1-line mode.

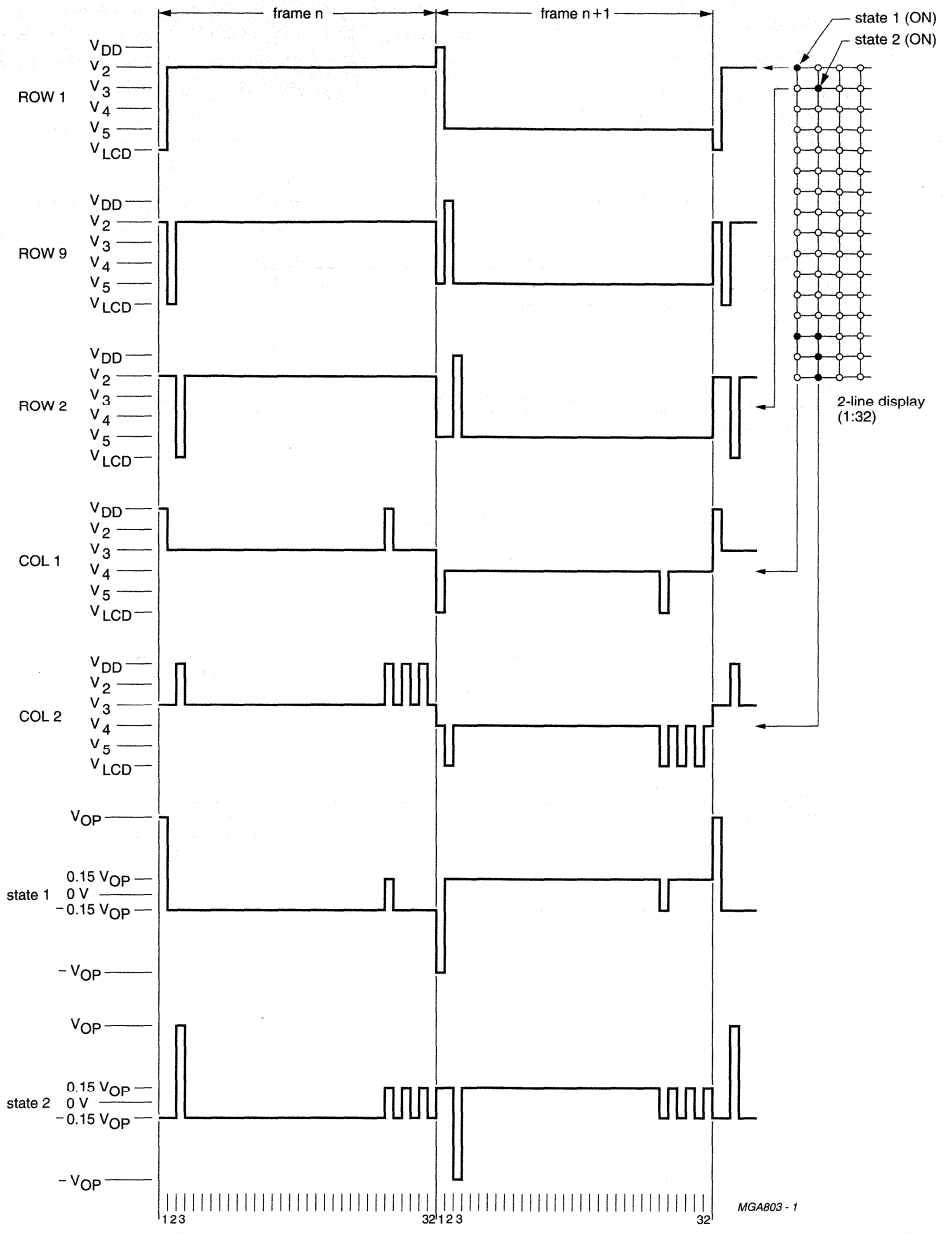


Fig.14 Typical LCD waveforms; 2-line mode.

8.17 Programming MUX 1 : 16 displays with the PCF2114x

The PCF2114x can be used in:

- 1-line mode to drive a 2-line display
- 2 × 12 characters with MUX rate 1 : 16, resulting in better contrast. The internal data flow of the chip is optimized for this purpose.

With the 'Function set' instruction M and N are set to 0, 0. Figures 15 to 17 show DDRAM addresses of the display characters. The second row of each table corresponds to either the right half of a 1-line display or to the second line of a 2-line display. Wrap around of data during display shift or when writing data is non-standard.

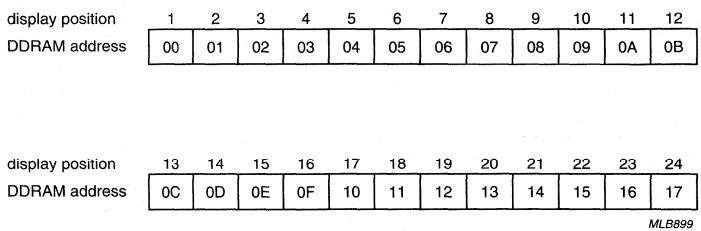


Fig.15 DDRAM-to-display mapping; no shift (PCF2114x).

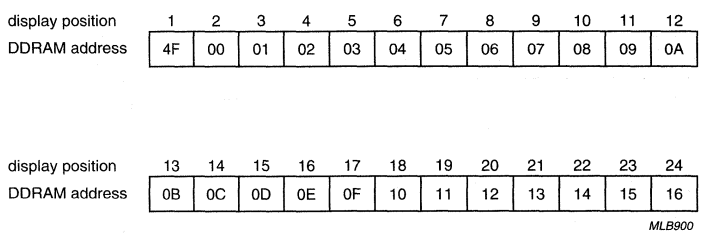


Fig.16 DDRAM-to-display mapping; right shift (PCF2114x).

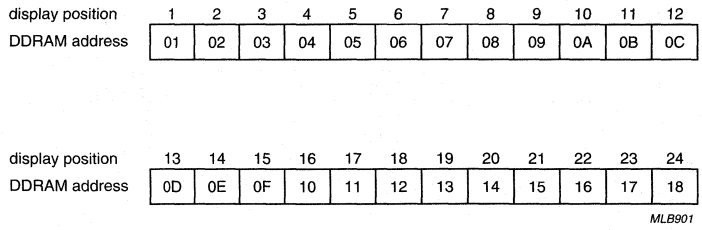


Fig.17 DDRAM-to-display mapping; left shift (PCF2114x).

8.18 Programming MUX 1 : 32 displays with the PCF2114x

To drive a 2-line by 24 characters MUX 1 : 32 display, use instruction 'Function set' M, N to 0, 1. Note that the right half of the display needs mirrored column connection compared to a display driven by a PCF2116x.

To drive a 4-line by 12 characters MUX 1 : 32 display the PCF2116x operating instructions apply. There is no functional difference between the PCF2114x and the PCF2116x in this mode. For such an application set M, N to 1, 1 with the 'Function set' instruction.

8.19 Reset function

The PCF2116 automatically initializes (resets) when power is turned on. After reset the chip has the following state.

Table 2 State after reset

STEP	DESCRIPTION		
1	display clear		
2	function set	DL = 1	8-bit interface
		M, N = 0	1-line display
		G = 0	voltage generator; $V_{LCD} = V_0$
3	display on/off control	D = 0	display off
		C = 0	cursor off
		B = 0	blink off
4	entry mode set	I/D = 1	+1 (increment)
		S = 0	no shift
5	Default address pointer to DDRAM. The Busy Flag (BF) indicates the busy state (BF = logic 1) until initialization ends. The busy state lasts 2 ms. The chip may also be initialized by software. See Figs 28 and 29.		
6	I^2C-bus interface reset		

9 INSTRUCTIONS

Only two PCF2116 registers, the Instruction Register (IR) and the Data Register (DR) can be directly controlled by the microcontroller. Before internal operation, control information is stored temporarily in these registers to allow interface to various types of microcontrollers which operate at different speeds or to allow interface to peripheral control ICs.
The PCF2116 operation is controlled by the instructions shown in Table 3 together with their execution time. Details are explained in subsequent sections.

Instructions are of 4 categories, those that:

1. Designate PCF2116 functions such as display format, data length, etc.
2. Set internal RAM addresses
3. Perform data transfer with internal RAM
4. Others.

In normal use, category 3 instructions are used most frequently. However, automatic incrementing by 1 (or decrementing by 1) of internal RAM addresses after each data write lessens the microcontroller program load. The display shift in particular can be performed concurrently with display data write, enabling the designer to develop systems in minimum time with maximum programming efficiency.

During internal operation, no instruction other than 'Read busy flag and address' will be executed.

Because the Busy Flag is set to logic 1 while an instruction is being executed, check to make sure it is on logic 0 before sending the next instruction or wait for the maximum instruction execution time, as given in Table 3. An instruction sent while the Busy Flag is HIGH will not be executed.

Table 3 Instructions (note 1)

INSTRUCTION	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DESCRIPTION	REQUIRED CLOCK CYCLES(2)
NOP	0	0	0	0	0	0	0	0	0	0	No operation.	0
Clear display	0	0	0	0	0	0	0	0	0	1	Clears entire display and sets DDRAM address 0 in Address Counter.	165
Return Home	0	0	0	0	0	0	0	0	1	0	Sets DDRAM address 0 in Address Counter. Also returns shifted display to original position. DDRAM contents remain unchanged.	3
Entry mode set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies shift of display. These operations are performed during data write and read.	3
Display control	0	0	0	0	0	0	1	D	C	B	Sets entire display on/off (D), cursor on/off (C) and blink of cursor position character (B).	3
Cursor/display shift	0	0	0	0	0	1	S/C	R/L	0	0	Moves cursor and shifts display without changing DDRAM contents.	3
Function set	0	0	0	0	1	DL	N	M	G	0	Sets interface data length (DL), number of display lines (N, M) and voltage generator control (G).	3
Set CGRAM address	0	0	0	1	A_{CG}						Sets CGRAM address.	3
Set DDRAM address	0	0	1	A_{DD}							Sets DDRAM address.	3
Read busy flag and address	0	1	BF	A_C							Reads Busy Flag (BF) indicating internal operation is being performed and reads Address Counter contents.	0
Read data	1	1	read data								Reads data from CGRAM or DDRAM.	3
Write data	1	0	write data								Writes data to CGRAM or DDRAM.	3

Notes

1. In the I^2C-bus mode the DL bit is don't care. 8-bit mode is assumed.
   In the I^2C-bus mode a control byte is required when RS or R/$\overline{W}$ is changed; control byte: Co, RS, R/$\overline{W}$, 0, 0, 0, 0, 0; command byte: DB7 to DB0.
2. Example: f_{osc} = 150 kHz, $T_{cy} = \frac{1}{f_{osc}}$ = 6.67 µs; 3 cycles = 20 µs, 165 cycles = 1.1 ms.

Table 4 Command bit identities

BIT	0	1
I/D	decrement	increment
S	display freeze	display shift
D	display off	display on
C	cursor off	cursor on
B	character at cursor position does not blink	character at cursor position blinks
S/C	cursor move	display shift
R/L	left shift	right shift
DL	4 bits	8 bits
G	voltage generator: $V_{LCD} = V_0$	voltage generator; $V_{LCD} = V_0 - 0.8V_{DD}$
N, (M = 0)		
PCF2116x	1 line × 24 characters; MUX 1 : 16	2 lines × 24 characters; MUX 1 : 32
PCF2114x	2 line × 12 characters; MUX 1 : 16	2 lines × 24 characters; MUX 1 : 32
N, (M = 1)	reserved	4 lines × 12 characters; MUX 1 : 32
BF	end of internal operation	internal operation in progress
Co	last control byte, only data bytes to follow	next two bytes are a data byte and another control byte

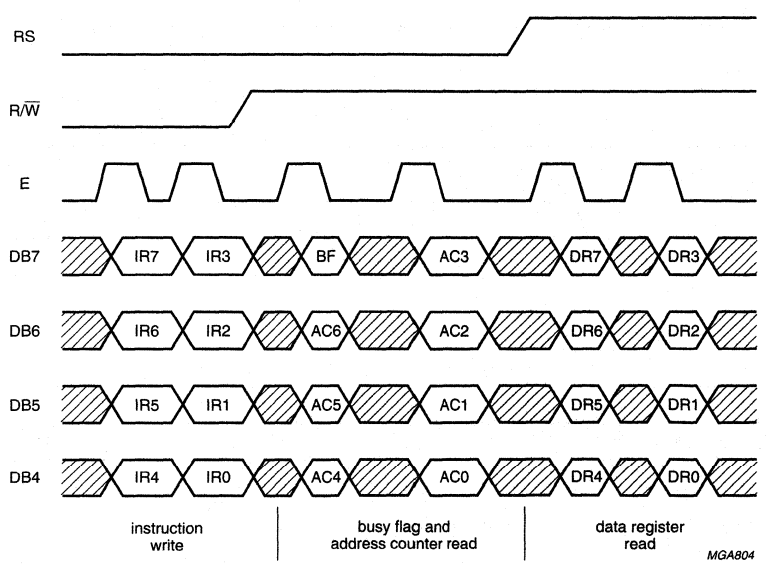
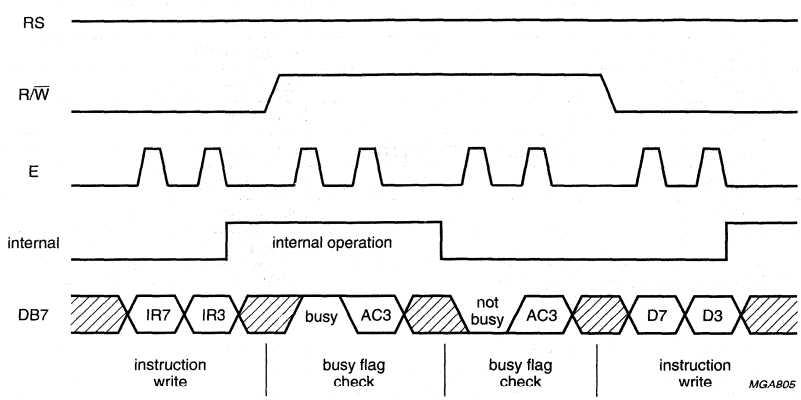


Fig.18 4-bit transfer example.



IR7, IR3: instruction 7th bit, 3rd bit.
AC3: Address Counter 3rd bit.

Fig.19 An example of 4-bit data transfer timing sequence.

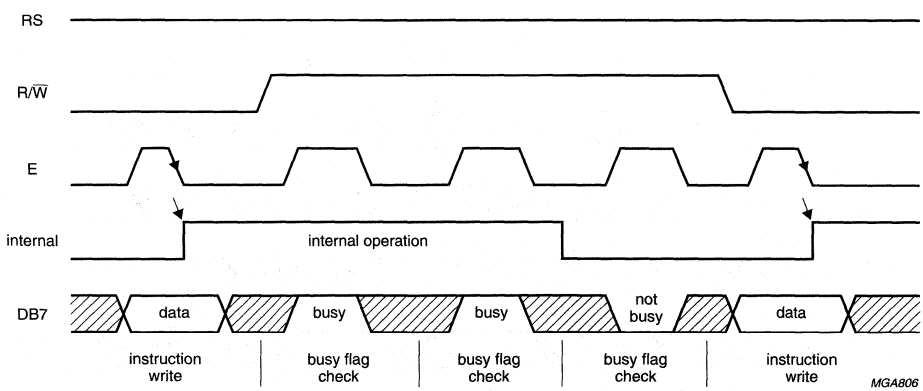


Fig.20 Example of Busy Flag check timing sequence.

9.1 Clear display

'Clear display' writes space code 20 (hexadecimal) into all DDRAM addresses (The character pattern for character code 20 must be blank pattern). Sets the DDRAM Address Counter to logic 0. Returns display to its original position if it was shifted. Thus, the display disappears and the cursor or blink position goes to the left edge of the display (the first line if 2 or 4 lines are displayed). Sets entry mode I/D = logic 1 (increment mode). S of entry mode does not change.

The instruction 'Clear display' requires extra execution time. This may be allowed for by checking the busy-flag (BF) or by waiting until 2 ms has elapsed. The latter must be applied where no read-back options are foreseen, as in some chip-on-glass (COG) applications.

9.2 Return home

'Return home' sets the DDRAM Address Counter to logic 0. Returns display to its original position if it was shifted. DDRAM contents do not change. The cursor or blink position goes to the left of the display (the first line if 2 or 4 lines are displayed). I/D and S of entry mode do not change.

9.3 Entry mode set

9.3.1 I/D

When I/D = logic 1 (0) the DDRAM or CGRAM address increments (decrements) by 1 when data is written into or read from the DDRAM or CGRAM. The cursor or blink position moves to the right when incremented and to the left when decremented. The cursor and blink are inhibited when the CGRAM is accessed.

9.3.2 S

When S = logic 1, the entire display shifts either to the right (I/D = logic 0) or to the left (I/D = logic 1) during a DDRAM write. Thus it looks as if the cursor stands still and the display moves. The display does not shift when reading from the DDRAM, or when writing into or reading out of the CGRAM. When S = logic 0 the display does not shift.

9.4 Display on/off control

9.4.1 D

The display is on when D = logic 1 and off when D = logic 0. Display data in the DDRAM are not affected and can be displayed immediately by setting D to logic 1.

9.4.2 C

The cursor is displayed when C = logic 1 and inhibited when C = logic 0. Even if the cursor disappears, the display functions I/D, etc. remain in operation during display data write. The cursor is displayed using 5 dots in the 8th line (see Fig.12).

9.4.3 B

The character indicated by the cursor blinks when B = logic 1. The blink is displayed by switching between display characters and all dots on with a period of 1 second when f_{osc} = 150 kHz (see Fig.12). At other clock frequencies the blink period is equal to 150 kHz/f_{osc}. The cursor and the blink can be set to display simultaneously.

9.5 Cursor/display shift

'Cursor/display shift' moves the cursor position or the display to the right or left without writing or reading display data. This function is used to correct a character or move the cursor through the display. In 2 or 4-line displays, the cursor moves to the next line when it passes the last position (40 or 20 decimal) of the line. When the displayed data is shifted repeatedly all lines shift at the same time; displayed characters do not shift into the next line. The Address Counter (AC) content does not change if the only action performed is shift display, but increments or decrements with the cursor shift.

9.6 Function set

9.6.1 DL (PARALLEL MODE ONLY)

Defines interface data width when the parallel data interface is used.

Data is sent or received in bytes (bits DB7 to DB0) when DL = logic 1, or in two 4-bit nibbles (DB7 to DB4) when DL = logic 0. When 4-bit width is selected, data is transmitted in two cycles using the parallel bus(1).

When using the I^{2}C-bus interface the DL should not previously have been set to 0 using the parallel interface.

9.6.2 N, M

Sets number of display lines.

(1) In a 4-bit application DB3 to DB0 are left open (internal pull-ups). Hence in the first 'Function set' instruction after power-on, G and H are set to 1. A second 'Function set' must then be sent (2 nibbles) to set G and H to their required values.

9.6.3 G

Controls the V_{LCD} voltage generator characteristic.

9.7 Set CGRAM address

'Set CGRAM address' sets bit 0 to 5 of the CGRAM address (A_{CG} in Table 3) into the Address Counter (binary A[5] to A[0]). Data can then be written to or read from the CGRAM.

Only bits 0 to 5 of the CGRAM address are set by the 'Set CGRAM address' instruction. Bit 6 can be set using the 'Set DDRAM address' instruction or by using the auto-increment feature during CGRAM write. All bits 0 to 6 can be read using the 'Read busy flag and address' instruction.

9.8 Set DDRAM address

'Set DDRAM address' sets the DDRAM address (A_{DD} in Table 3) into the Address Counter (binary A[6] to A[0]). Data can then be written to or read from the DDRAM.

Hexadecimal address ranges.

ADDRESS	FUNCTION
00 to 4F	1-line by 24; 2114x/2116x
00 to 0B and 0C to 4F	2-line by 12; 2114x
00 to 27 and 40 to 67	2-line by 24; 2114x/2116x
00 to 13, 20 to 33, 40 to 53 and 60 to 73	4-line by 12; 2114x/2116x

9.9 Read busy flag and address

'Read busy flag and address' reads the Busy Flag (BF). BF = logic 1 indicates that an internal operation is in progress. The next instruction will not be executed until BF = logic 0, so BF should be checked before sending another instruction.

At the same time, the value of the Address Counter (A_C in Table 3) expressed in binary A[6] to A[0] is read out. The Address Counter is used by both CGRAM and DDRAM, and its value is determined by the previous instruction.

9.10 Write data to CGRAM or DDRAM

Writes binary 8-bit data D[7] to D[0] to the CGRAM or the DDRAM.

Whether the CGRAM or DDRAM is to be written into is determined by the previous specification of CGRAM or DDRAM address setting.

After writing, the address automatically increments or decrements by 1, in accordance with the entry mode. Only bits D[4] to D[0] of CGRAM data are valid, bits D[7] to D[5] are 'don't care'.

9.11 Read data from CGRAM or DDRAM

Reads binary 8-bit data D[7] to D[0] from the CGRAM or DDRAM.

The most recent 'Set address' instruction determines whether the CGRAM or DDRAM is to be read.

The 'Read data' instruction gates the content of the data register (DR) to the bus while E = HIGH. After E goes LOW again, internal operation increments (or decrements) the AC and stores RAM data corresponding to the new AC into the DR.

Remark: the only three instructions that update the data register (DR) are:

- 'Set CGRAM address'
- 'Set DDRAM address'
- 'Read data' from CGRAM or DDRAM.

Other instructions (e.g. 'Write data', 'Cursor/Display shift', 'Clear display', 'Return home') will not modify the data register content.

10 INTERFACE TO MICROCONTROLLER (PARALLEL INTERFACE)

The PCF2116 can send data in either two 4-bit operations or one 8-bit operation and can thus interface to 4-bit or 8-bit microcontrollers.

In 8-bit mode data is transferred as 8-bit bytes using the 8 data lines DB0 to DB7. Three further control lines E, RS, and R/$\overline{W}$ are required.

In 4-bit mode data is transferred in two cycles of 4-bits each. The higher order bits (corresponding to DB4 to DB7 in 8-bit mode) are sent in the first cycle and the lower order bits (DB0 to DB3 in 8-bit mode) in the second.
Data transfer is complete after two 4-bit data transfers.
It should be noted that two cycles are also required for the Busy Flag check. 4-bit operation is selected by instruction. See Figs 18, 19 and 20 for examples of bus protocol.

In 4-bit mode pins DB3 to DB0 must be left open-circuit. They are pulled up to V_{DD} internally.

11 INTERFACE TO MICROCONTROLLER (I²C-BUS INTERFACE)

11.1 Characteristics of the I²C-bus

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

11.2 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

11.3 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P).

11.4 System configuration

A device generating a message is a 'transmitter', a device receiving a message is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves'.

11.5 Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

11.6 I²C-bus protocol

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always carried out with the first byte transmitted after the start procedure. The I²C-bus configuration for the different PCF2116 READ and WRITE cycles is shown in Figs 25 to 27.

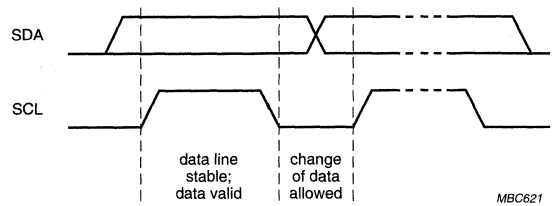


Fig.21 Bit transfer.

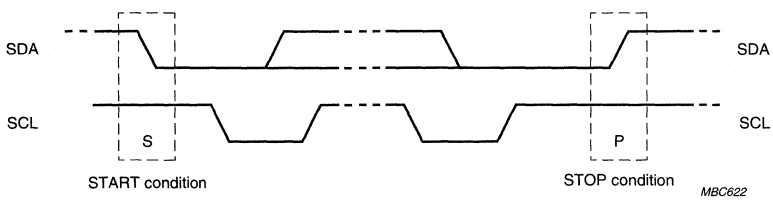


Fig.22 Definition of START and STOP conditions.

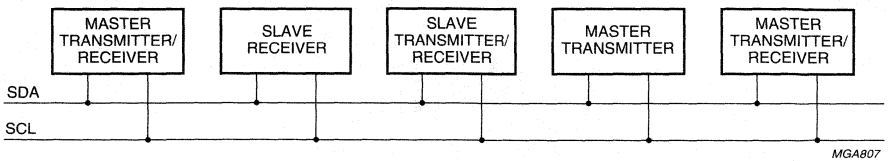


Fig.23 System configuration.

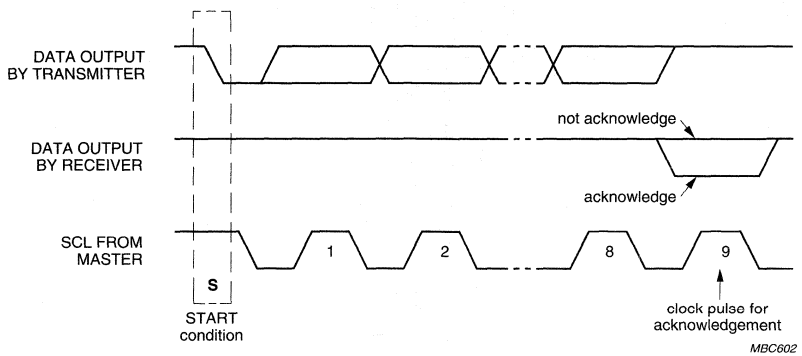


Fig.24 Acknowledgement on the I^2C-bus.

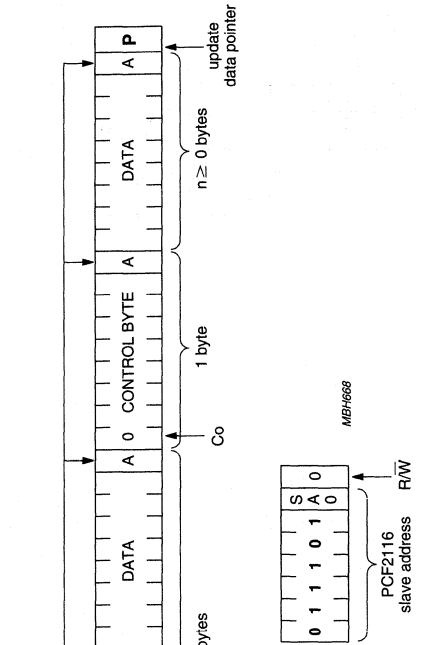
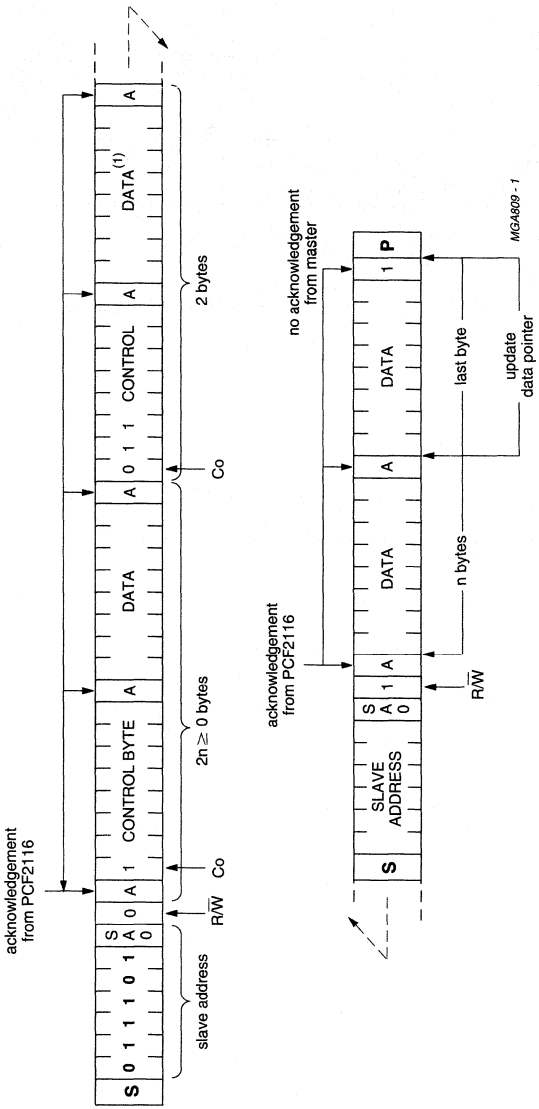


Fig.25 Master transmits to slave receiver; WRITE mode.



(1) Last data byte is a dummy byte (may be omitted).

Fig.26 Master reads after setting word address; write word address, set RS/$\overline{RW}$; READ data.

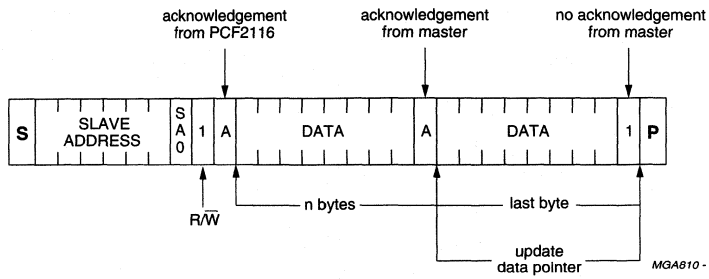


Fig.27 Master reads slave immediately after first byte; READ mode (RS previously defined).

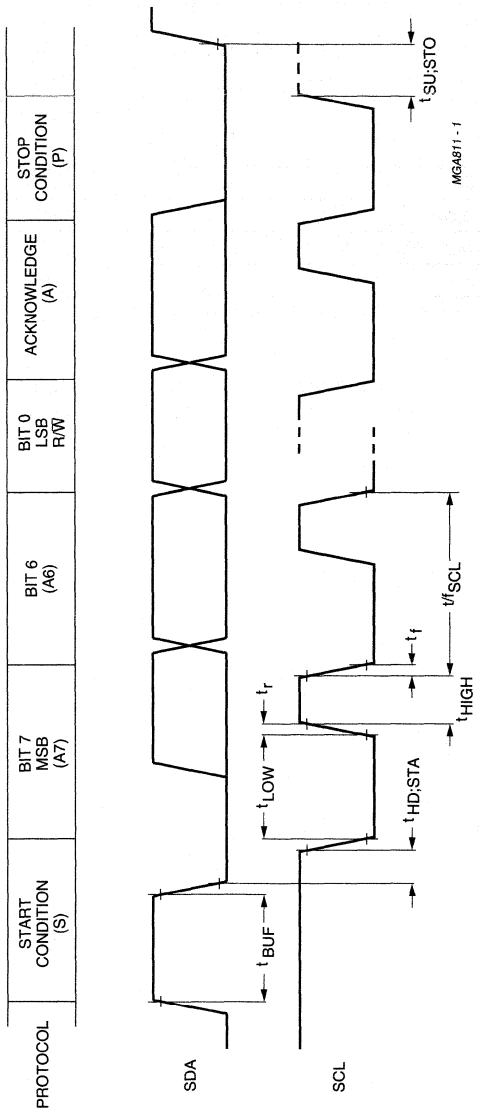


Fig.28 I²C-bus timing diagram; rise and fall times refer to V_{IL} and V_{IH}.

12 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.5	+8.0	V
V_{LCD}	LCD supply voltage	V_{DD} − 11	V_{DD}	V
V_I	input voltage OSC, V_0, RS, R/$\overline{W}$, E and DB0 to DB7	V_{SS} − 0.5	V_{DD} + 0.5	V
V_O	output voltage R1 to R32, C1 to C60 and V_{LCD}	V_{LCD} − 0.5	V_{DD} + 0.5	V
I_I	DC input current	−10	+10	mA
I_O	DC output current	−10	+10	mA
I_{DD}, I_{SS}, I_{LCD}	V_{DD}, V_{SS} or V_{LCD} current	−50	+50	mA
P_{tot}	total power dissipation	−	400	mW
P_O	power dissipation per output	−	100	mW
T_{stg}	storage temperature	−65	+150	°C

13 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see *"Handling MOS Devices"*).

14 DC CHARACTERISTICS

V_{DD} = 2.5 to 6 V; V_{SS} = 0 V; V_{LCD} = V_{DD} − 3.5 to V_{DD} − 9 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage		2.5	–	6.0	V
V_{LCD}	LCD supply voltage		V_{DD} − 9	–	V_{DD} − 3.5	V
I_{DD}	supply current external V_{LCD}	note 1				
I_{DD1}	supply current 1		–	200	500	μA
I_{DD2}	supply current 2	V_{DD} = 5 V; V_{OP} = 9 V; f_{osc} = 150 kHz; T_{amb} = 25 °C	–	200	300	μA
I_{DD3}	supply current 3	V_{DD} = 3 V; V_{OP} = 5 V; f_{osc} = 150 kHz; T_{amb} = 25 °C	–	150	200	μA
I_{DD}	supply current internal V_{LCD}	notes 1, 2 and 8				
I_{DD4}	supply current 4		–	700	1100	μA
I_{DD5}	supply current 5	V_{DD} = 5 V; V_{OP} = 9 V; f_{osc} = 150 kHz; T_{amb} = 25 °C	–	600	900	μA
I_{DD6}	supply current 6	V_{DD} = 3 V; V_{OP} = 5 V; f_{osc} = 150 kHz; T_{amb} = 25 °C	–	500	800	μA
I_{LCD}	V_{LCD} input current	notes 1 and 7	–	50	100	μA
V_{POR}	power-on reset voltage level	note 3	–	1.3	1.8	V
Logic						
V_{IL1}	LOW level input voltage E, RS, R/$\overline{W}$, DB0 to DB7 and SA0		V_{SS}	–	0.3V_{DD}	V
V_{IH1}	HIGH level input voltage E, RS, R/$\overline{W}$, DB0 to DB7 and SA0		0.7V_{DD}	–	V_{DD}	V
$V_{IL(osc)}$	LOW level input voltage OSC		V_{SS}	–	V_{DD} − 1.5	V
$V_{IH(osc)}$	HIGH level input voltage OSC		V_{DD} − 0.1	–	V_{DD}	V
$V_{IL(V0)}$	LOW level input voltage V_0		V_{SS}	–	V_{DD} − 0.5	V
$V_{IH(V0)}$	HIGH level input voltage V_0		V_{DD} − 0.05	–	V_{DD}	V
I_{pu}	pull-up current at DB0 to DB7	V_I = V_{SS}	0.04	0.15	1.00	μA
$I_{OL(DB)}$	LOW level output current DB0 to DB7	V_{OL} = 0.4 V; V_{DD} = 5 V	1.6	–	–	mA
$I_{OH(DB)}$	HIGH level output current DB0 to DB7	V_{OH} = 4 V; V_{DD} = 5 V	−1.0	–	–	mA
I_{L1}	leakage current OSC, V_0, E, RS, R/$\overline{W}$, DB0 to DB7 and SA0	V_I = V_{DD} or V_{SS}	−1	–	+1	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I²C-bus						
SDA, SCL						
V_{IL2}	LOW level input voltage	note 4	V_{SS}	–	$0.3V_{DD}$	V
V_{IH2}	HIGH level input voltage	note 4	$0.7V_{DD}$	–	V_{DD}	V
I_{L2}	leakage current	$V_I = V_{DD}$ or V_{SS}	−1	–	+1	μA
C_i	input capacitance	note 5	–	–	7	pF
$I_{OL(SDA)}$	LOW level output current (SDA)	V_{OL} = 0.4 V; V_{DD} = 5 V	3	–	–	mA
LCD outputs						
R_{ROW}	row output resistance R1 to R32	note 6	–	1.5	3	kΩ
R_{COL}	column output resistance C1 to C60	note 6	–	3	6	kΩ
V_{tol1}	bias voltage tolerance R1 to R32 and C1 to C60	note 7	–	±20	±130	mV
V_{tol2}	LCD supply voltage (V_{LCD}) tolerance	note 2	–	±40	±300	mV

Notes

1. LCD outputs are open-circuit; inputs at V_{DD} or V_{SS}; $V_0 = V_{DD}$; bus inactive; internal or external clock with duty cycle 50% (I_{DD1} only).
2. LCD outputs are open-circuit; LCD supply voltage generator is on; load current at V_{LCD} = 20 μA.
3. Resets all logic when $V_{DD} < V_{POR}$.
4. When the voltages are above or below the supply voltages V_{DD} or V_{SS}, an input current may flow; this current must not exceed ±0.5 mA.
5. Tested on sample basis.
6. Resistance of output terminals (R1 to R32 and C1 to C60) with load current = 150 μA; $V_{OP} = V_{DD} - V_{LCD}$ = 9 V; outputs measured one at a time; (external V_{LCD}).
7. LCD outputs open-circuit; external V_{LCD}.
8. Maximum value occurs at 85 °C.

15 DC CHARACTERISTICS (PCF2116K)

V_{DD} = 2.5 to 6 V; V_{SS} = 0 V; $V_{LCD} = V_{DD} - 3.5$ to $V_{DD} - 9$ V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		2.5	–	6.0	V
V_{LCD}	LCD supply voltage		$V_{DD} - 9$	–	$V_{DD} - 3.5$	V
V_0	voltage generator control input voltage		V_{SS}	–	$V_{DD} - 0.5$	V
R_0	voltage generator control input resistance	T_{amb} = 25 °C; note 1	700	1000	1300	kΩ

Note

1. R_0 has a temperature coefficient of resistance of +0.6%/K.

16 AC CHARACTERISTICS

V_{DD} = 2.5 to 6.0 V; V_{SS} = 0 V; V_{LCD} = V_{DD} − 3.5 V to V_{DD} − 9 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
f_{FR}	LCD frame frequency (internal clock); note 1	40	65	100	Hz
f_{osc}	external clock frequency	90	150	225	kHz
Bus timing characteristics: Parallel Interface; notes 1 and 2					
WRITE OPERATION (WRITING DATA FROM MICROCONTROLLER TO PCF2116)					
T_{cy}	enable cycle time	500	–	–	ns
PW_{EH}	enable pulse width	220	–	–	ns
t_{ASU}	address set-up time	50	–	–	ns
t_{AH}	address hold time	25	–	–	ns
t_{DSW}	data set-up time	60	–	–	ns
t_{HD}	data hold time	25	–	–	ns
READ OPERATION (READING DATA FROM PCF2116 TO MICROCONTROLLER)					
T_{cy}	enable cycle time	500	–	–	ns
PW_{EH}	enable pulse width	220	–	–	ns
t_{ASU}	address set-up time	50	–	–	ns
t_{AH}	address hold time	25	–	–	ns
t_{DHD}	data delay time	–	–	150	ns
t_{HD}	data hold time	20	–	100	ns
Timing characteristics: I^2C-bus interface; note 2					
f_{SCL}	SCL clock frequency	–	–	100	kHz
t_{SW}	tolerable spike width on bus	–	–	100	ns
t_{BUF}	bus free time	4.7	–	–	µs
$t_{SU;STA}$	set-up time for a repeated START condition	4.7	–	–	µs
$t_{HD;STA}$	START condition hold time	4	–	–	µs
t_{LOW}	SCL LOW time	4.7	–	–	µs
t_{HIGH}	SCL HIGH time	4	–	–	µs
t_r	SCL and SDA rise time	–	–	1	µs
t_f	SCL and SDA fall time	–	–	0.3	µs
$t_{SU;DAT}$	data set-up time	250	–	–	ns
$t_{HD;DAT}$	data hold time	0	–	–	ns
$t_{SU;STO}$	set-up time for STOP condition	4	–	–	µs

Notes

1. V_{DD} = 5 V.
2. All timing values are valid within the operating supply voltage and ambient temperature range and are referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

17 TIMING CHARACTERISTICS

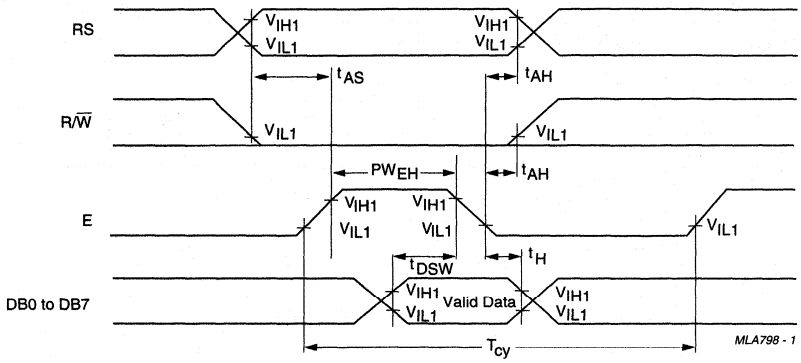


Fig.29 Parallel bus write operation sequence; writing data from microcontroller to PCF2116.

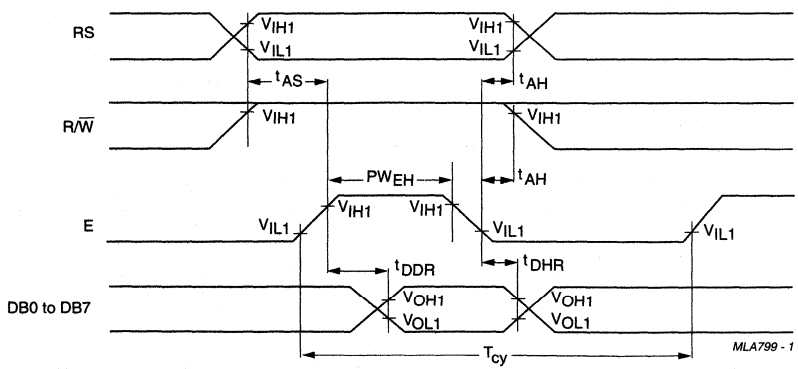


Fig.30 Parallel bus read operation sequence; reading data from PCF2116 to microcontroller.

18 APPLICATION INFORMATION

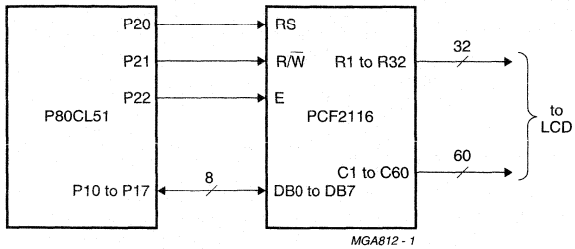


Fig.31 Direct connection to 8-bit microcontroller; 8-bit bus.

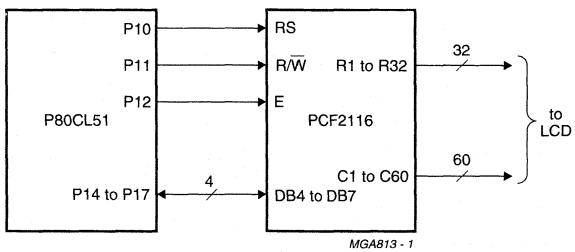


Fig.32 Direct connection to 8-bit microcontroller; 4-bit bus.

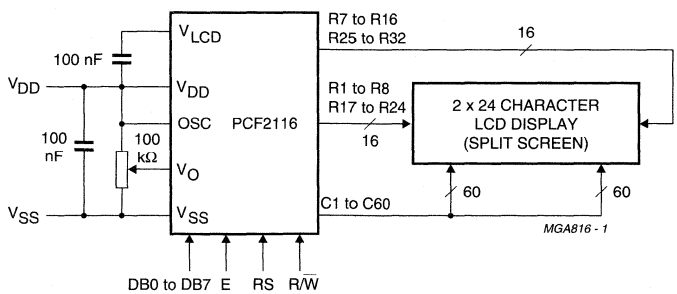


Fig.33 Typical application using parallel interface.

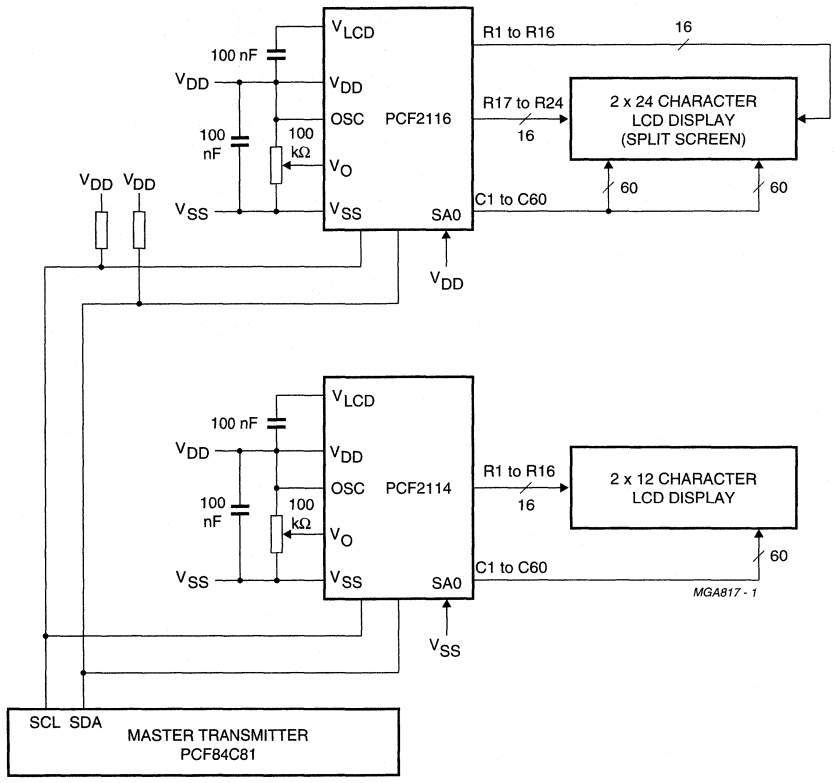


Fig.34 Application using I²C-bus interface.

18.1 8-bit operation, 1-line display using internal reset

Table 6 shows an example of a 1-line display in 8-bit operation. The PCF2116 functions must be set by the 'Function set' instruction prior to display. Since the display data RAM can store data for 80 characters, the RAM can be used for advertising displays when combined with display shift operation. Since the display shift operation changes display position only and DDRAM contents remain unchanged, display data entered first can be displayed when the Return Home operation is performed.

18.2 4-bit operation, 1-line display using internal reset

The program must set functions prior to 4-bit operation. Table 5 shows an example. When power is turned on, 8-bit operation is automatically selected and the PCF2116 attempts to perform the first write as an 8-bit operation. Since nothing is connected to DB0 to DB3, a rewrite is then required. However, since one operation is completed in two accesses of 4-bit operation, a rewrite is required to set the functions (see Table 5 step 3).

Thus, DB4 to DB7 of the function set are written twice.

18.3 8-bit operation, 2-line display

For a 2-line display, the cursor automatically moves from the first to the second line after the 40th digit of the first line has been written. Thus, if there are only 8 characters in the first line, the DDRAM address must be set after the eighth character is completed (see Table 7). Note that both lines of the display are always shifted together; data does not shift from one line to the other.

18.4 I²C operation, 1-line display

A control byte is required with most instructions (see Table 8).

18.5 Initializing by instruction

If the power supply conditions for correctly operating the internal reset circuit are not met, the PCF2116 must be initialized by instruction. Tables 9 and 10 show how this may be performed for 8-bit and 4-bit operation.

Table 5 4-bit operation, 1-line display example; using internal reset

STEP	INSTRUCTION						DISPLAY	OPERATION
1	power supply on (PCF2116 is initialized by the internal reset circuit)							Initialized. No display appears.
2	function set							
	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4		Sets to 4-bit operation. In this instance operation is handled as 8-bits by initialization and only this instruction completes with one write.
	0	0	0	0	1	0		
3	function set							
	0	0	0	0	1	0		Sets to 4-bit operation, selects 1-line display and $V_{LCD} = V_0$. 4-bit operation starts from this point and resetting is needed.
	0	0	0	0	0	0		
4	display on/off control							
	0	0	0	0	0	0	_	Turns on display and cursor. Entire display is blank after initialization.
	0	0	1	1	1	0		
5	entry mode set							
	0	0	0	0	0	0	_	Sets mode to increment the address by 1 and to shift the cursor to the right at the time of write to the DD/CGRAM. Display is not shifted.
	0	0	0	1	1	0		
6	write data to CGRAM/DDRAM							
	1	0	0	1	0	1	P_	Writes 'P'. The DDRAM has already been selected by initialization at power-on. The cursor is incremented by 1 and shifted to the right.
	1	0	0	0	0	0		

Table 6 8-bit operation, 1-line display example; using internal reset (character set 'A')

STEP	INSTRUCTION	DISPLAY	OPERATION
1	power supply on (PCF2116 is initialized by the internal reset function)		Initialized. No display appears.
2	function set RS R/$\overline{W}$ DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 1 1 0 0 0 0		Sets to 8-bit operation, selects 1-line display and $V_{LCD} = V_0$.
3	display mode on/off control 0 0 0 0 0 0 1 1 1 0	_	Turns on display and cursor. Entire display is blank after initialization.
4	entry mode set 0 0 0 0 0 0 0 1 1 0	_	Sets mode to increment the address by 1 and to shift the cursor to the right at the time of the write to the DD/CGRAM. Display is not shifted.
5	write data to CGRAM/DDRAM 1 0 0 1 0 1 0 0 0 0	**P**_	Writes 'P'. The DDRAM has already been selected by initialization at power-on. The cursor is incremented by 1 and shifted to the right.
6	write data to CGRAM/DDRAM 1 0 0 1 0 0 1 0 0 0	**PH**_	Writes 'H'.
7		|	
8	write data to CGRAM/DDRAM 1 0 0 1 0 1 0 0 1 1	**PHILIPS**_	Writes 'S'.
9	entry mode set 0 0 0 0 0 0 0 1 1 1	**PHILIPS**_	Sets mode for display shift at the time of write.
10	write data to CGRAM/DDRAM 1 0 0 0 1 0 0 0 0 0	**PHILIPS**_	Writes space.
11	write data to CGRAM/DDRAM 1 0 0 1 0 0 1 1 0 1	**PHILIPS M**_	Writes 'M'.

STEP	INSTRUCTION	DISPLAY	OPERATION
12			
13	write data to CGRAM/DDRAM 1 0 0 1 0 0 1 1 1 1	**MICROKO_**	Writes 'O'.
14	cursor or display shift 0 0 0 0 0 1 0 0 0 0	**MICROKO**	Shifts only the cursor position to the left.
15	cursor or display shift 0 0 0 0 0 1 0 0 0 0	**MICROKO**	Shifts only the cursor position to the left.
16	write data to CGRAM/DDRAM 1 0 0 1 0 0 0 0 1 1	**ICROCO**	Writes 'C' correction. The display moves to the left.
17	cursor or display shift 0 0 0 0 0 1 1 1 0 0	**MICROCO**	Shifts the display and cursor to the right.
Z18	cursor or display shift 0 0 0 0 0 1 0 1 0 0	**MICROCO_**	Shifts only the cursor to the right.
19	write data to CGRAM/DDRAM 1 0 0 1 0 0 1 1 0 1	**ICROCOM_**	Writes 'M'.
20			
21	Return Home 0 0 0 0 0 0 0 0 1 0	**PHILIPS M**	Returns both display and cursor to the original position (address 0).

Table 7 8-bit operation, 2-line display example; using internal reset

STEP	INSTRUCTION	DISPLAY	OPERATION
1	power supply on (PCF2116 is initialized by the internal reset function)		Initialized. No display appears.
2	function set RS R/$\overline{W}$ DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 1 1 1 0 0 0		Sets to 8-bit operation, selects 2-line display and voltage generator off.
3	display on/off control 0 0 0 0 0 0 1 1 1 0	_	Turns on display and cursor. Entire display is blank after initialization.
4	entry mode set 0 0 0 0 0 0 0 1 1 0	_	Sets mode to increment the address by 1 and to shift the cursor to the right at the time of write to the CG/DDRAM. Display is not shifted.
5	Write data to CGRAM/DDRAM w 1 0 0 1 0 1 0 0 0 0	**P**_	Writes 'P'. The DDRAM has already been selected by initialization at power-on. The cursor is incremented by 1 and shifted to the right.
6			
7	write data to CGRAM/DDRAM 1 0 0 1 0 1 0 0 1 1	**PHILIPS**_	Writes 'S'.
8	set DDRAM address 0 0 1 1 0 0 0 0 0 0	**PHILIPS** _	Sets DDRAM address to position the cursor at the head of the 2nd line.
9	write data to CGRAM/ DDRAM 1 0 0 1 0 0 1 1 0 1	**PHILIPS** **M**_	Writes 'M'.
10			

STEP	INSTRUCTION	DISPLAY	OPERATION
11	write data to CGRAM/ DDRAM 1 0 0 1 0 0 1 1 1 1	**PHILIPS** **MICROCO_**	Writes 'O'.
12	write data to CGRAM/ DDRAM 0 0 0 0 0 0 0 1 1 1	**PHILIPS** **MICROCO_**	Sets mode for display shift at the time of write.
13	write data to CGRAM/ DDRAM 1 0 0 1 0 0 1 1 0 1	**PHILIPS** **ICROCOM_**	Writes 'M'. Display is shifted to the left. The first and second lines shift together.
14			
15	return Home 0 0 0 0 0 0 0 0 1 0	**PHILIPS** **MICROCOM**	Returns both display and cursor to the original position (address 0).

Table 8 Example of I²C operation; 1-line display (using internal reset, assuming SA0 = V_{SS}; note 1)

STEP	I²C BYTE	DISPLAY	OPERATION
1	I²C START		Initialized. No display appears.
2	slave address for write SA6 SA5 SA4 SA3 SA2 SA1 SA0 R/$\overline{W}$ Ack 0 1 1 1 0 1 0 0 1		During the acknowledge cycle SDA will be pulled-down by the PCF2116.
3	send a control byte for function set Co RS R/$\overline{W}$ Ack 0 0 0 X X X X X 1		Control byte sets RS and R/$\overline{W}$ for following data bytes.
4	function set DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 0 1 X 0 0 0 0 1		Selects 1-line display and $V_{LCD} = V_0$; SCL pulse during acknowledge cycle starts execution of instruction.
5	display on/off control DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 0 0 0 1 1 1 0 1	_	Turns on display and cursor. Entire display shows character Hex 20 (blank in ASCII-like character sets).
6	entry mode set DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 0 0 0 0 1 1 0 1	_	Sets mode to increment the address by 1 and to shift the cursor to the right at the time of write to the DDRAM or CGRAM. Display is not shifted.
7	I²C START	_	For writing data to DDRAM, RS must be set to 1. Therefore a control byte is needed.
8	slave address for write SA6 SA5 SA4 SA3 SA2 SA1 SA0 R/$\overline{W}$ Ack 0 1 1 1 0 1 0 0 1	_	
9	send a control byte for write data Co RS R/$\overline{W}$ Ack 0 1 0 X X X X X 1	_	
10	write data to DDRAM DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 1 0 1 0 0 0 0 1	**P**_	Writes 'P'. The DDRAM has been selected at power-up. The cursor is incremented by 1 and shifted to the right.

STEP	I²C BYTE	DISPLAY	OPERATION
11	write data to DDRAM DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 1 0 0 1 0 0 0 1	**PH_**	Writes 'H'.
12 to 15			
16	write data to DDRAM DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 1 0 1 0 0 1 1 1	**PHILIPS_**	Writes 'S'.
17	(optional I²C stop) I²C start + slave address for write (as step 8)	**PHILIPS_**	
18	control byte Co RS R/$\overline{W}$ Ack 1 0 0 X X X X X 1	**PHILIPS_**	
19	Return Home DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 0 0 0 0 0 1 0 1	**PHILIPS**	Sets DDRAM address 0 in Address Counter. (also returns shifted display to original position. DDRAM contents unchanged). This instruction does not update the Data Register (DR).
20	control byte for read Co RS R/$\overline{W}$ Ack 0 1 1 X X X X X 1	**PHILIPS**	DDRAM content will be read from following instructions. The R/$\overline{W}$ has to be set to 1 while still in I²C-write mode.
21	I²C START	**PHILIPS**	
22	slave address for read SA6 SA5 SA4 SA3 SA2 SA1 SA0 R/$\overline{W}$ Ack 0 1 1 1 0 1 0 1 1	**PHILIPS**	During the acknowledge cycle the content of the DR is loaded into the internal I²C interface to be shifted out. In the previous instruction neither a 'Set address' nor a 'Read data' has been performed. Therefore the content of the DR was unknown.

STEP	I²C BYTE	DISPLAY	OPERATION
23	read data: 8 × SCL + master acknowledge; note 2 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack X X X X X X X X 0	PHILIPS	8 × SCL; content loaded into interface during previous acknowledge cycle is shifted out over SDA. MSB is DB7. During master acknowledge content of DDRAM address 01 is loaded into the I²C interface.
24	read data: 8 × SCL + master acknowledge; note 2 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 1 0 0 1 0 0 0 0	PHILIPS	8 × SCL; code of letter 'H' is read first. During master acknowledge code of 'I' is loaded into the I²C interface.
25	read data: 8 × SCL + no master acknowledge; note 2 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 1 0 0 1 0 0 1 1	PHILIPS	No master acknowledge; After the content of the I²C interface register is shifted out no internal action is performed. No new data is loaded to the interface register, Data Register (DR) is not updated, Address Counter (AC) is not incremented and cursor is not shifted.
26	I²C STOP	PHILIPS	

Notes

1. X = don't care.
2. SDA is left at high-impedance by the microcontroller during the READ acknowledge.

Table 9 Initialization by instruction, 8-bit interface (note 1)

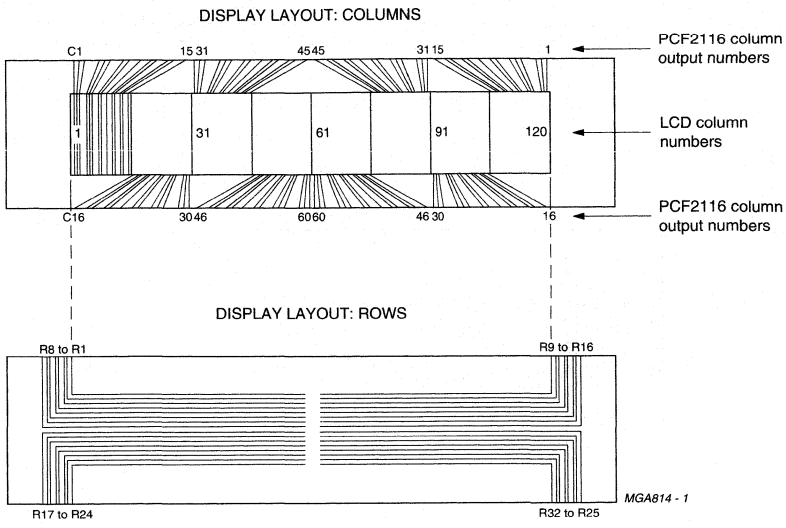
STEP										DESCRIPTION
power-on or unknown state										
wait 2 ms after V_{DD} rises above V_{POR}										
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	BF cannot be checked before this instruction.
0	0	0	0	1	1	X	X	X	X	Function set (interface is 8-bits long).
wait 2 ms										
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	BF cannot be checked before this instruction.
0	0	0	0	1	1	X	X	X	X	Function set (interface is 8-bits long).
wait more than 40 µs										
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	BF cannot be checked before this instruction.
0	0	0	0	1	1	X	X	X	X	Function set (interface is 8-bits long).
										BF can be checked after the following instructions. When BF is not checked, the waiting time between instructions is the specified instruction time (see Table 3).
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Function set (interface is 8-bits long). Specify the number of display lines and voltage generator characteristic.
0	0	0	0	1	1	N	M	G	0	
0	0	0	0	0	0	1	0	0	0	Display off.
0	0	0	0	0	0	0	0	0	1	Clear display.
0	0	0	0	0	0	0	1	I/D	S	Entry mode set.
Initialization ends										

Note

1. X = don't care.

Table 10 Initialization by instruction, 4-bit interface. Not applicable for I²C-bus operation

STEP						DESCRIPTION
power-on or unknown state						
wait 2 ms after V_{DD} rises above V_{POR}						
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	BF cannot be checked before this instruction.
0	0	0	0	1	1	Function set (interface is 8-bits long).
wait 2 ms						
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	BF cannot be checked before this instruction.
0	0	0	0	1	1	Function set (interface is 8-bits long).
wait 40 µs						
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	BF cannot be checked before this instruction.
0	0	0	0	1	1	Function set (interface is 8-bits long).
						BF can be checked after the following instructions. When BF is not checked, the waiting time between instructions is the specified instruction time. (See Table 3).
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	Function set (set interface to 4-bits long).
0	0	0	0	1	0	Interface is 8-bits long.
0	0	0	0	1	0	Function set (interface is 4-bits long).
0	0	N	M	G	0	Specify number of display lines and voltage generator characteristic.
0	0	0	0	0	0	
0	0	1	0	0	0	Display off.
0	0	0	0	0	0	Clear display.
0	0	0	0	0	1	
0	0	0	0	0	0	Entry mode set.
0	0	0	1	I/D	S	
Initialization ends						



2 x 24 character display

Fig.35 Example of 2 × 24 display layout (PCF2116x).

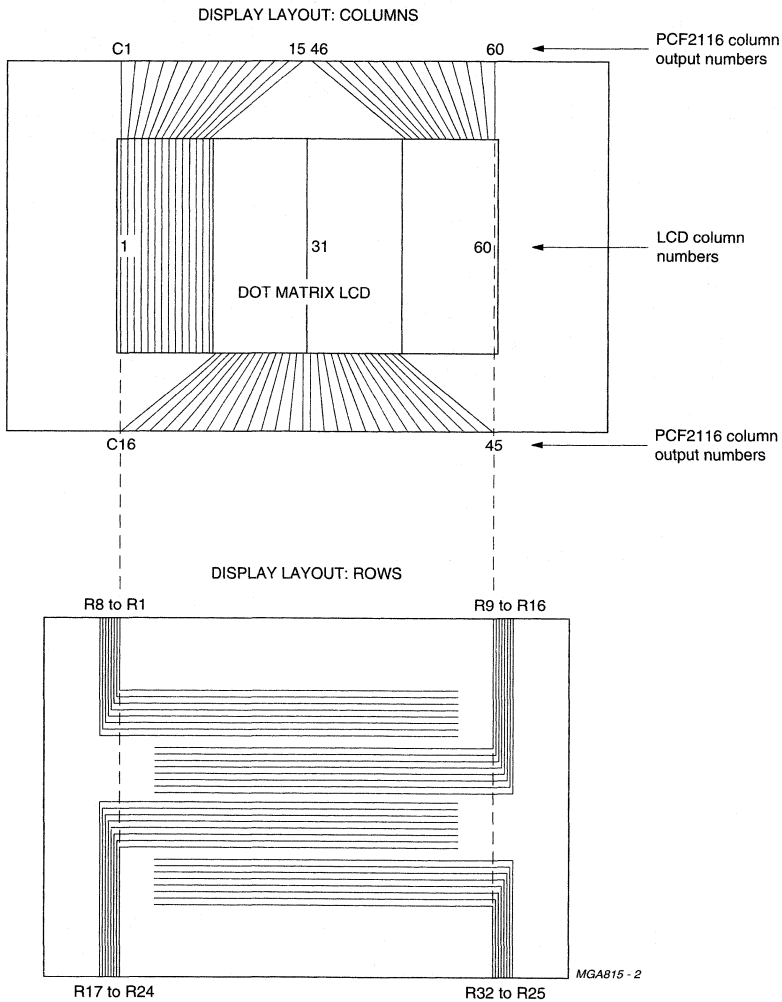


Fig.36 Example of 4 × 12 display layout (PCF2114x/PCF2116x).

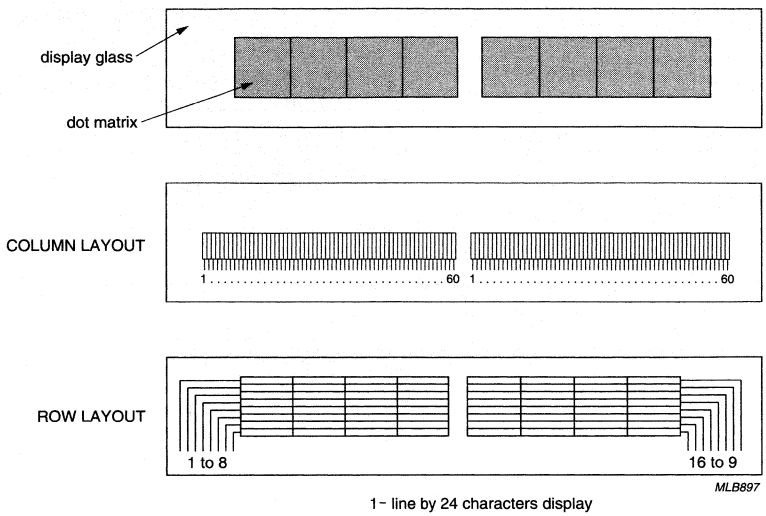


Fig.37 Display example (PCF2114x); 1-line by 24 characters.

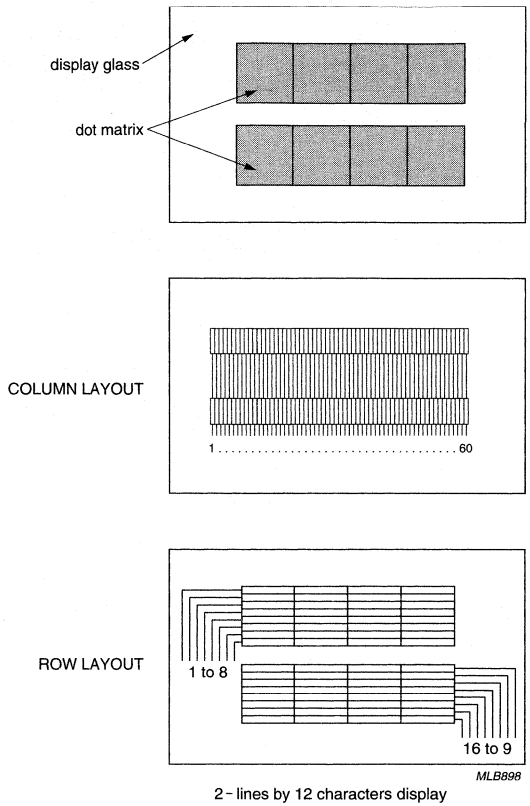


Fig.38 Display example (PCF2114x); 2-lines by 12 characters.

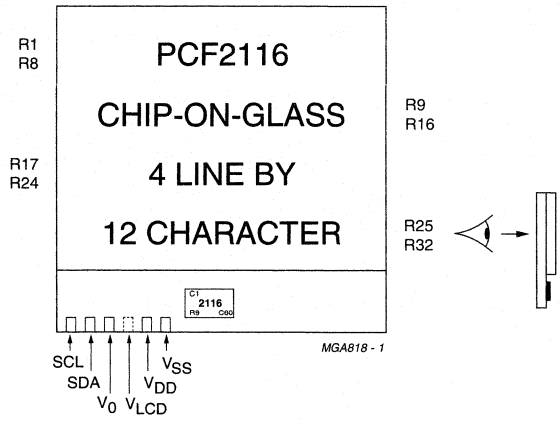
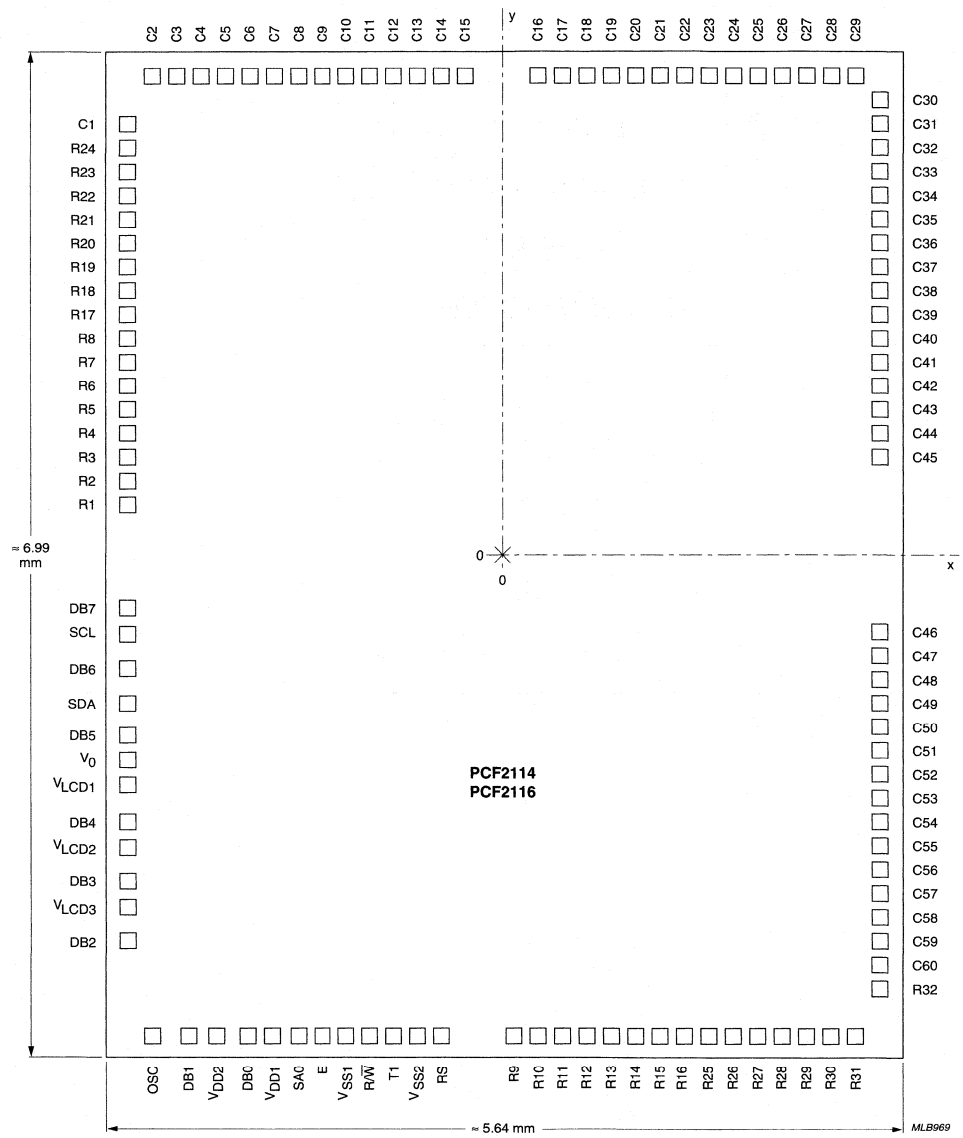


Fig.39 Chip on glass application.

19 BONDING PAD LOCATIONS



Chip dimensions: approximately 5.64 × 6.99 mm.
Pad area: 0.0121 mm^2.
Bonding pad dimensions: 110 × 110 µm.

Fig.40 Bonding pad locations.

Table 11 Bonding pad locations (dimensions in μm); all x/y coordinates are referenced to centre of chip, see Fig.40

SYMBOL	PAD	x	y
OSC	1	−2445	−3300
DB1	2	−2211	−3300
V_{DD2}	3	−2034	−3300
DB0	4	−1806	−3300
V_{DD1}	5	−1627	−3300
SA0	6	−1437	−3300
E	7	−1245	−3300
V_{SS1}	8	−1056	−3300
R/$\overline{W}$	9	−867	−3300
T1	10	−672	−3300
V_{SS2}	11	−486	−3300
RS	12	−297	−3300
R9	13	77	−3300
R10	14	247	−3300
R11	15	417	−3300
R12	16	587	−3300
R13	17	757	−3300
R14	18	927	−3300
R15	19	1097	−3300
R16	20	1267	−3300
R25	21	1436	−3300
R26	22	1606	−3300
R27	23	1776	−3300
R28	24	1946	−3300
R29	25	2116	−3300
R30	26	2286	−3300
R31	27	2456	−3300
R32	28	2626	−3013
C60	29	2626	−2760
C59	30	2626	−2590
C58	31	2626	−2420
C57	32	2626	−2250
C56	33	2626	−2080
C55	34	2626	−1910
C54	35	2626	−1740
C53	36	2626	−1570
C52	37	2626	−1400
C51	38	2626	−1230
C50	39	2626	−1060
C49	40	2626	−890
C48	41	2626	−720
C47	42	2626	−550
C46	43	2626	−380
C45	44	2626	582
C44	45	2626	752
C43	46	2626	922
C42	47	2626	1092
C41	48	2626	1262
C40	49	2626	1432
C39	50	2626	1602
C38	51	2626	1772
C37	52	2626	1942
C36	53	2626	2112
C35	54	2626	2282
C34	55	2626	2452
C33	56	2626	2622
C32	57	2626	2792
C31	58	2626	2962
C30	59	2626	3132
C29	60	2339	3302
C28	61	2169	3302
C27	62	1999	3302
C26	63	1829	3302
C25	64	1659	3302
C24	65	1489	3302
C23	66	1319	3302
C22	67	1149	3302
C21	68	979	3302
C20	69	809	3302
C19	70	639	3302
C18	71	469	3302
C17	72	299	3302
C16	73	129	3302
C15	74	−245	3302
C14	75	−415	3302
C13	76	−585	3302

SYMBOL	PAD	x	y
C12	77	−755	3302
C11	78	−925	3302
C10	79	−1095	3302
C9	80	−1265	3302
C8	81	−1435	3302
C7	82	−1605	3302
C6	83	−1775	3302
C5	84	−1945	3302
C4	85	−2115	3302
C3	86	−2285	3302
C2	87	−2455	3302
C1	88	−2625	3015
R24	89	−2625	2846
R23	90	−2625	2676
R22	91	−2625	2506
R21	92	−2625	2336
R20	93	−2625	2166
R19	94	−2625	1996
R18	95	−2625	1826
R17	96	−2625	1656
R8	97	−2625	1487
R7	98	−2625	1317
R6	99	−2625	1147
R5	100	−2625	977
R4	101	−2625	807
R3	102	−2625	637
R2	103	−2625	467
R1	104	−2625	297
DB7	105	−2625	−290
SCL	106	−2625	−479
DB6	107	−2625	−716
SDA	108	−2625	−976
DB5	109	−2625	−1202
V_0	110	−2625	−1388
V_{LCD1}	111	−2625	−1580
DB4	112	−2625	−1808
V_{LCD2}	113	−2625	−1985
DB3	114	−2625	−2213
V_{LCD3}	115	−2625	−2390
DB2	116	−2625	−2621

CONTENTS

1 FEATURES

- Single-chip LCD controller/driver
- 2-line display of up to 16 characters + 160 icons, or 1-line display of up to 32 characters + 160 icons
- 5 × 7 character format plus cursor; 5 × 8 for kana (Japanese) and user defined symbols
- Icon mode: reduced current consumption while displaying icons only
- Icon blink function
- On-chip:
  - Generation of LCD supply voltage, independent of V_{DD}, programmable by instruction (external supply also possible)
  - Temperature compensation of on-chip generated V_{LCD}: –8 to –12 mV/K at 5.0 V (programmable by instruction)
  - Generation of intermediate LCD bias voltages
  - Oscillator requires no external components (external clock also possible).
- Display Data RAM: 80 characters
- Character Generator ROM: 240, 5 × 8 characters
- Character Generator RAM: 16, 5 × 8 characters; 4 characters used to drive 160 icons, 8 characters used if icon blink feature is used in application
- 4 or 8-bit parallel bus and 2-wire I²C-bus interface
- CMOS compatible
- 18 row and 80 column outputs
- Multiplex rates 1 : 18 (for normal operation), 1 : 9 (for single line operation) and 1 : 2 (for icon only mode)
- Uses common 11 code instruction set (extended)
- Logic supply voltage range, $V_{DD} - V_{SS}$ = 2.2 to 4.0 V (up to 5.5 V if external V_{LCD} is used); chip may be driven with two battery cells
- Display supply voltage range, $V_{LCD} - V_{SS}$ = 2.2 to 6.5 V
- Very low current consumption (20 to 200 μA):
  - Icon mode: <25 μA
  - Power-down mode: <2 μA.

1.1 Note

Icon mode is used to save current. When only icons are displayed, a much lower operating voltage V_{LCD} can be used and the switching frequency of the LCD outputs is reduced. In most applications it is possible to use V_{DD} as V_{LCD}.

2 APPLICATIONS

- Telecom equipment
- Portable instruments
- Point-of-sale terminals.

3 GENERAL DESCRIPTION

The PCF2119x is a low power CMOS LCD controller and driver, designed to drive a dot matrix LCD display of 2-line by 16 or 1-line by 32 characters with 5 × 8 dot format. All necessary functions for the display are provided in a single chip, including on-chip generation of LCD bias voltages, resulting in a minimum of external components and lower system current consumption. The PCF2119x interfaces to most microcontrollers via a 4 or 8-bit bus or via the 2-wire I²C-bus. The chip contains a character generator and displays alphanumeric and kana (Japanese) characters. The letter 'x' in PCF2119x characterizes the built-in character set. Various character sets can be manufactured on request.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PC2119RU/2	–	chip with bumps in tray	–
PC2119SU/2	–	chip with bumps in tray	–
PC2119VU/2	–	chip with bumps in tray	–

5 BLOCK DIAGRAM

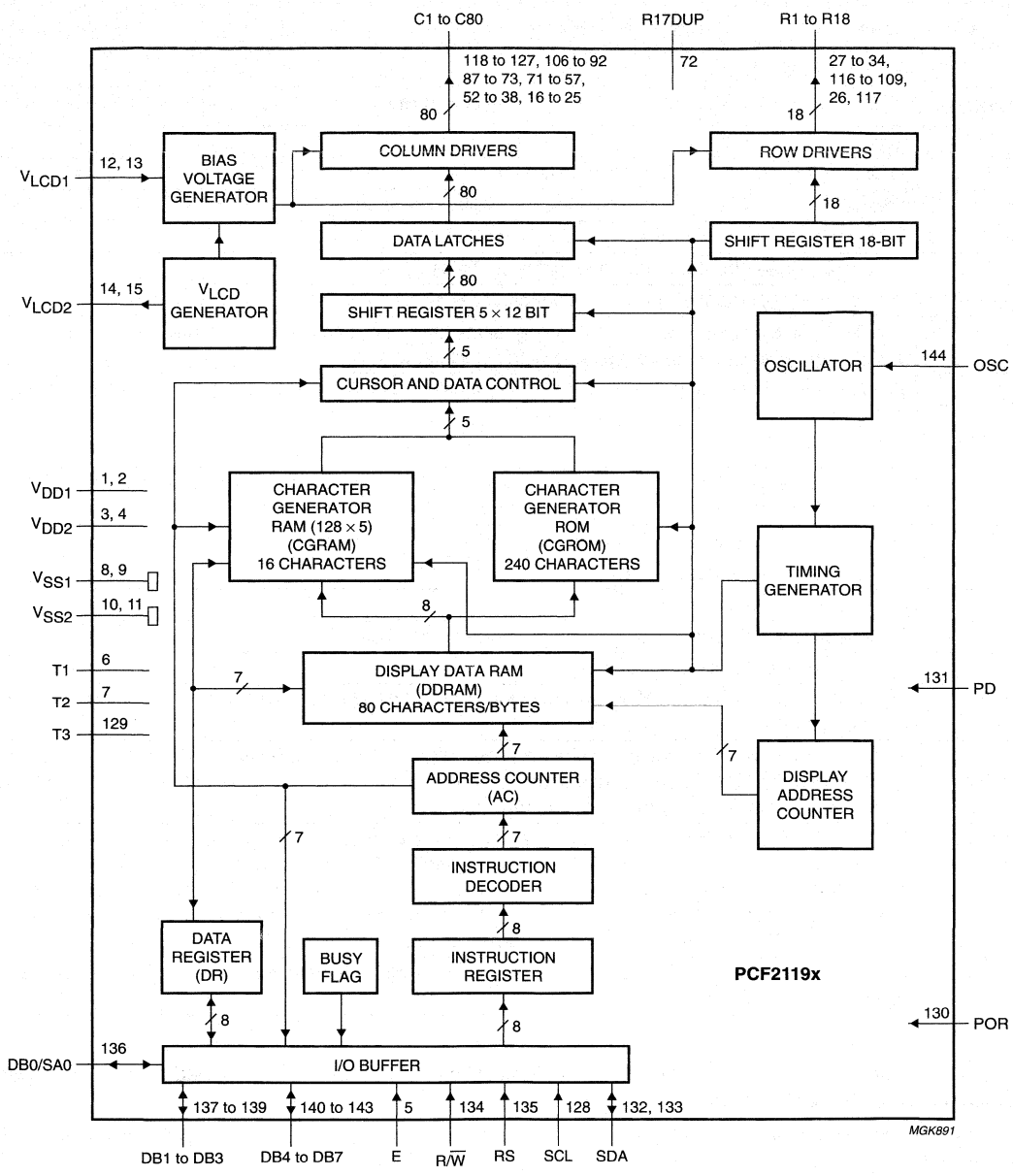


Fig.1 Block diagram.

6 PAD INFORMATION

The identification of each pad and its location is given in Chapter 17.

6.1 Pad functions

Table 1 Pad function description

SYMBOL	DESCRIPTION
V_{DD1}	Supply voltage for all except the high voltage generator.
V_{DD2}	Supply voltage for the high voltage generator.
V_{SS1}	This is the ground pad for all except the high voltage generator.
V_{SS2}	This is the ground pad for the high voltage generator.
V_{LCD1}	This input is used for the generation of the LCD bias levels.
V_{LCD2}	This is the V_{LCD} output pad if V_{LCD} is generated internally. This pad must be connected to V_{LCD1}.
E	The data bus clock input is set HIGH to signal the start of a read or write operation; data is clocked in or out of the chip on the negative edge of the clock; note 1.
T1	These are three test pads. T1 and T2 must be connected to V_{SS1}; T3 is left open-circuit and is not user accessible.
T2	
T3	
R1 to R18; R17DUP	LCD row driver outputs R1 to R18; these pads output the row select waveforms to the display; R17 and R18 drive the icons. R17 has two pads R17 and R17DUP.
C1 to C80	LCD column driver outputs C1 to C80.
SCL	I^2C-bus serial clock input; note 1.
POR	External power-on reset input.
PD	PD selects the chip power-down mode; for normal operation PD = 0.
SDA	I^2C-bus serial data input/output; note 1.
R/$\overline{W}$	This is the read/write input. R/$\overline{W}$ selects either the read (R/$\overline{W}$ = 1) or write (R/$\overline{W}$ = 0) operation. This pad has an internal pull-up resistor.
RS	The RS input selects the register to be accessed for read and write. RS = 0, selects the instruction register for write and the busy flag and address counter for read. RS = 1, selects the data register for both read and write. This pad has an internal pull-up resistor.
DB0 to DB7	The 8-bit bidirectional data bus (3-state) transfers data between the system controller and the PCF2119x. DB7 may be used as the busy flag, signalling that internal operations are not yet completed. In 4-bit operations the 4 higher order lines DB7 to DB4 are used; DB3 to DB0 must be left open-circuit. Data bus line DB3 has an alternative function (SA0), when selected this is the I^2C-bus address pad. Each data line has its own internal pull-up resistor; note 1.
OSC	Oscillator or external clock input. When the on-chip oscillator is used this pad must be connected to V_{DD1}.

Note

1. When the I^2C-bus is used, the parallel interface pad E must be at logic 0. In the I^2C-bus read mode DB7 to DB0 should be connected to V_{DD1} or left open-circuit.
   a) When the parallel bus is used, pads SCL and SDA must be connected to V_{SS1} or V_{DD1}; they must not be left open-circuit.
   b) If the 4-bit interface is used without reading out from the PCF2119x (i.e. R/$\overline{W}$ is set permanently to logic 0), the unused ports DB0 to DB4 can either be set to V_{SS1} or V_{DD1} instead of leaving them open-circuit.

7 FUNCTIONAL DESCRIPTION

7.1 LCD supply voltage generator

The LCD supply voltage may be generated on-chip. The voltage generator is controlled by two internal 6-bit registers: V_A and V_B. The nominal LCD operating voltage at room temperature is given by the relationship:

$$V_{OP(nom)} = (\text{integer value of register} \times 0.082) + 1.82$$

7.2 Programming ranges

Programmed value: 1 to 63. Voltage: 1.902 to 6.986 V. T_{ref} = 27 °C.

Values producing more than 6.5 V at operating temperature are not allowed. Operation above this voltage may damage the device. When programming the operating voltage the V_{LCD} temperature coefficient must be taken into account.

Values below 2.2 V are below the specified operating range of the chip and are therefore not allowed.

Value 0 for V_A and V_B switches the generator off (i.e. V_A = 0 in character mode, V_B = 0 in icon mode).

Usually register V_A is programmed with the voltage for character mode and register V_B with the voltage for icon mode.

When V_{LCD} is generated on-chip the V_{LCD} pads should be decoupled to V_{SS} with a suitable capacitor. The generated V_{LCD} is independent of V_{DD} and is temperature compensated. When the generator is switched off an external voltage may be supplied at connected pads $V_{LCD1,2}$. $V_{LCD1,2}$ may be higher or lower than V_{DD}.

The LCD supply voltage generator ensures that, as long as V_{DD} is in the valid range (2.2 to 4 V), the required peak voltage V_{OP} = 5.2 V can be generated at any time.

7.3 LCD bias voltage generator

The intermediate bias voltages for the LCD display are also generated on-chip. This removes the need for an external resistive bias chain and significantly reduces the system current consumption. The optimum value of V_{LCD} depends on the multiplex rate, the LCD threshold voltage (V_{th}) and the number of bias levels. Using a 5-level bias scheme for 1 : 18 maximum rate allows $V_{LCD} < 5$ V for most LCD liquids. The intermediate bias levels for the different multiplex rates are shown in Table 2. These bias levels are automatically set to the given values when switching to the corresponding multiplex rate.

Table 2 Bias levels as a function of multiplex rate

MULTIPLEX RATE	NUMBER OF LEVELS	V_1	V_2	V_3	V_4	V_5	V_6
1 : 18	5	V_{op}	3/4[1]	1/2	1/2	1/4	V_{ss}
1 : 9	5	V_{op}	3/4	1/2	1/2	1/4	V_{ss}
1 : 2	4	V_{op}	2/3	2/3	1/3	1/3	V_{ss}

Note

1. The values in the above table are given relative to $V_{op} - V_{ss}$, e.g. 3/4 means $3/4 \times (V_{op} - V_{ss})$.

7.4 Oscillator

The on-chip oscillator provides the clock signal for the display system. No external components are required and the OSC pad must be connected to V_{DD}.

7.5 External clock

If an external clock is to be used this is input at the OSC pad. The resulting display frame frequency is given by:

$$f_{frame} = \frac{f_{OSC}}{3072}$$

Only in the power-down state is the clock allowed to be stopped (OSC connected to V_{SS}), otherwise the LCD is frozen in a DC state.

7.6 Power-on reset

The PC2119x must be reset externally. This is an internal synchronous reset that requires 3 OSC cycles to be executed after release of the external reset signal. If no external reset is performed, the chip might start-up in an unwanted state. The external reset is active HIGH.

7.7 Power-down mode

The chip can be put into power-down mode where all static currents are switched off (no internal oscillator, no bias level generation and all LCD outputs are internally connected to V_{SS}) when PD = 1.

During power-down, information in the RAMs and the chip state are preserved. Instruction execution during power-down is possible when pad OSC is externally clocked.

7.8 Registers

The PCF2119x has two 8-bit registers, an Instruction Register (IR) and a Data Register (DR). The Register Select signal (RS) determines which register will be accessed. The instruction register stores instruction codes such as 'display clear' and 'cursor shift', and address information for the Display Data RAM (DDRAM) and Character Generator RAM (CGRAM).

The instruction register can be written to but not read from by the system controller. The data register temporarily stores data to be read from the DDRAM and CGRAM.

When reading, data from the DDRAM or CGRAM corresponding to the address in the instruction register is written to the data register prior to being read by the 'read data' instruction.

7.9 Busy flag

The busy flag indicates the internal status of the PCF2119x. A logic 1 indicates that the chip is busy and further instructions will not be accepted. The busy flag is output to pad DB7 when RS = 0 and R/$\overline{W}$ = 1. Instructions should only be written after checking that the busy flag is at logic 0 or waiting for the required number of cycles.

7.10 Address Counter (AC)

The address counter assigns addresses to the DDRAM and CGRAM for reading and writing and is set by the commands 'set CGRAM address' and 'set DDRAM address'. After a read/write operation the address counter is automatically incremented or decremented by 1. The address counter contents are output to the bus (DB6 to DB0) when RS = 0 and R/$\overline{W}$ = 1.

7.11 Display Data RAM (DDRAM)

The DDRAM stores up to 80 characters of display data represented by 8-bit character codes. RAM locations which are not used for storing display data can be used as general purpose RAM. The basic RAM to display addressing scheme is shown in Fig.2. With no display shift the characters represented by the codes in the first 32 RAM locations starting at address 00H in line 1 are displayed. Figures 3 and 4 show the display mapping for right and left shift respectively.

When data is written to or read from the DDRAM wrap-around occurs from the end of one line to the start of the next line. When the display is shifted each line wraps around within itself, independently of the others. Thus all lines are shifted and wrapped around together.
The address ranges and wrap-around operations for the various modes are shown in Table 3.

Table 3 Address space and wrap-around operation

MODE	1 × 32	2 × 16	1 × 9
Address space	00 to 4F	00 to 27; 40 to 67	00 to 27
Read/write wrap-around (moves to next line)	4F to 00	27 to 40; 67 to 00	27 to 00
Display shift wrap-around (stays within line)	Do not use (make sure, that 4F and 00 are not displayed at the same time.)	27 to 00; 67 to 40	27 to 00

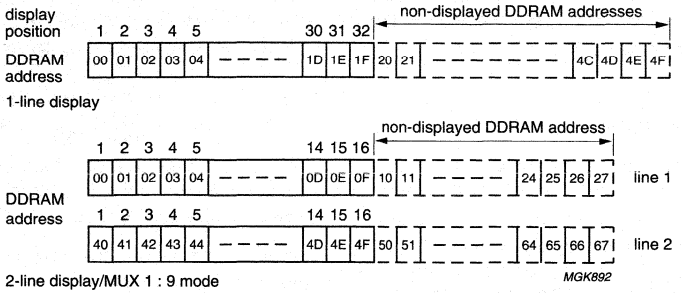


Fig.2 DDRAM to display mapping: no shift.

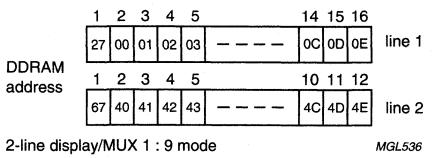


Fig.3 DDRAM to display mapping: right shift: (For 1 × 32 only as long as 4F and 00 positions are not on display simultaneously).

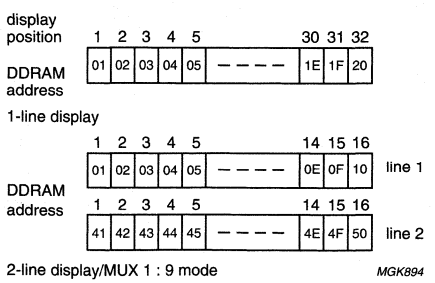


Fig.4 DDRAM to display mapping; left shift: (For 1 × 32 only as long as 4F and 00 positions are not on display simultaneously).

7.12 Character Generator ROM (CGROM)

The Character Generator ROM generates 240 character patterns in a 5 × 8 dot format from 8-bit character codes. Figure 6 shows the character set that is currently implemented.

7.13 Character Generator RAM (CGRAM)

Up to 16 user defined characters may be stored in the Character Generator RAM. Some CGRAM characters (see Fig.17) are also used to drive icons (6 if icons blink and both icon rows are used in the application; 3 if no blink but both icon rows are used in the application; 0 if no icons are driven by the icon rows). The CGROM and CGRAM use a common address space, of which the first column is reserved for the CGRAM (see Fig.6). Figure 9 shows the addressing principle for the CGRAM.

7.14 Cursor control circuit

The cursor control circuit generates the cursor (underline and/or cursor blink as shown in Fig.5) at the DDRAM address contained in the address counter.

When the address counter contains the CGRAM address the cursor will be inhibited.

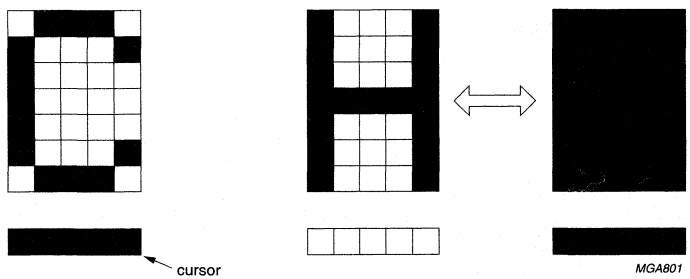
7.15 Timing generator

The timing generator produces the various signals required to drive the internal circuitry. Internal chip operation is not disturbed by operations on the data buses.

7.16 LCD row and column drivers

The PCF2119x contains 18 row and 80 column drivers, which connect the appropriate LCD bias voltages in sequence to the display in accordance with the data to be displayed. R17 and R18 drive the icon rows.

The bias voltages and the timing are selected automatically when the number of lines in the display is selected. Figures 10 to 13 show typical waveforms. Unused outputs should be left unconnected.



5 x 7 dot character font

alternating display

cursor display example

blink display example

Fig.5 Cursor and blink display examples.

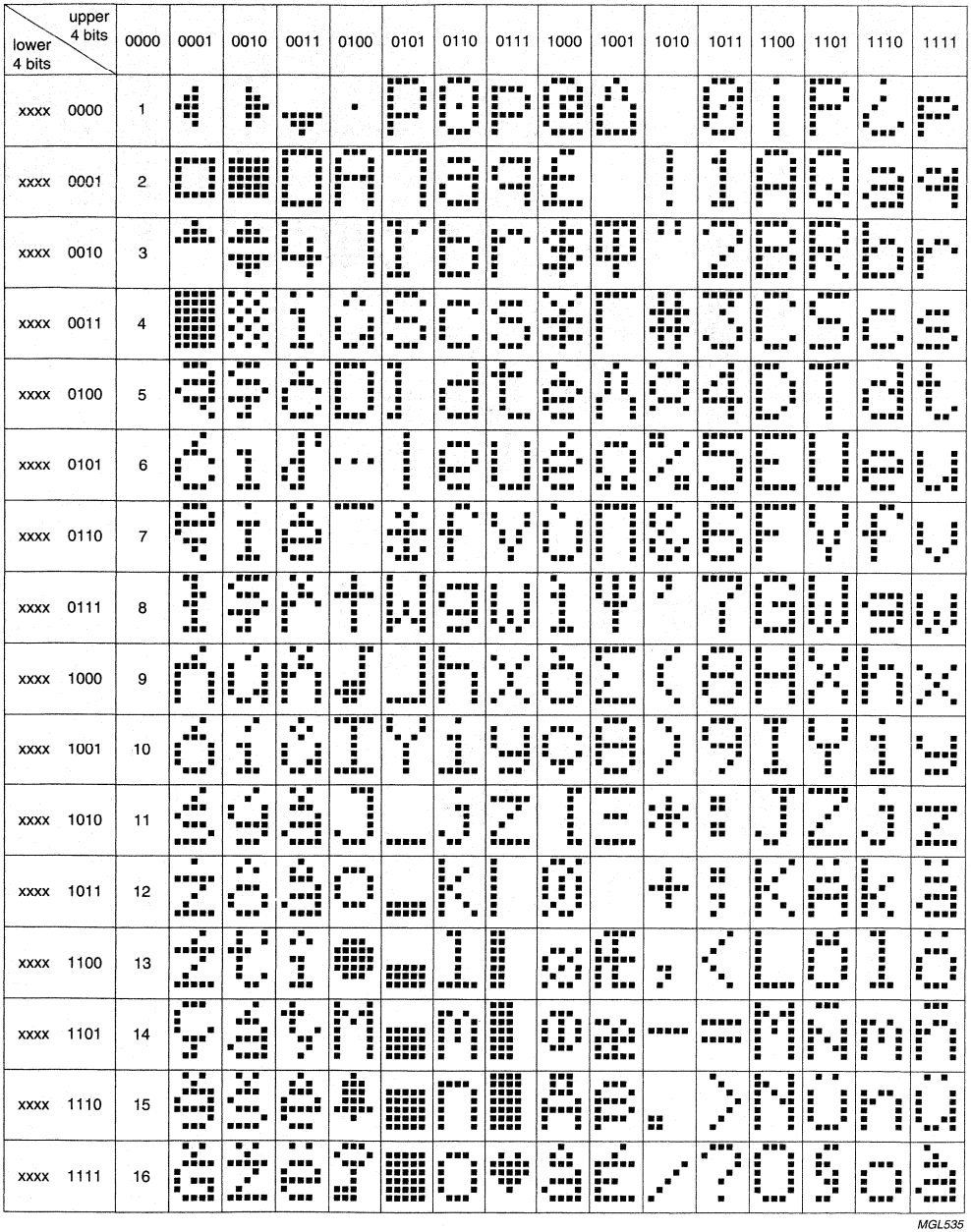


Fig.6 Character set 'R' in CGROM.

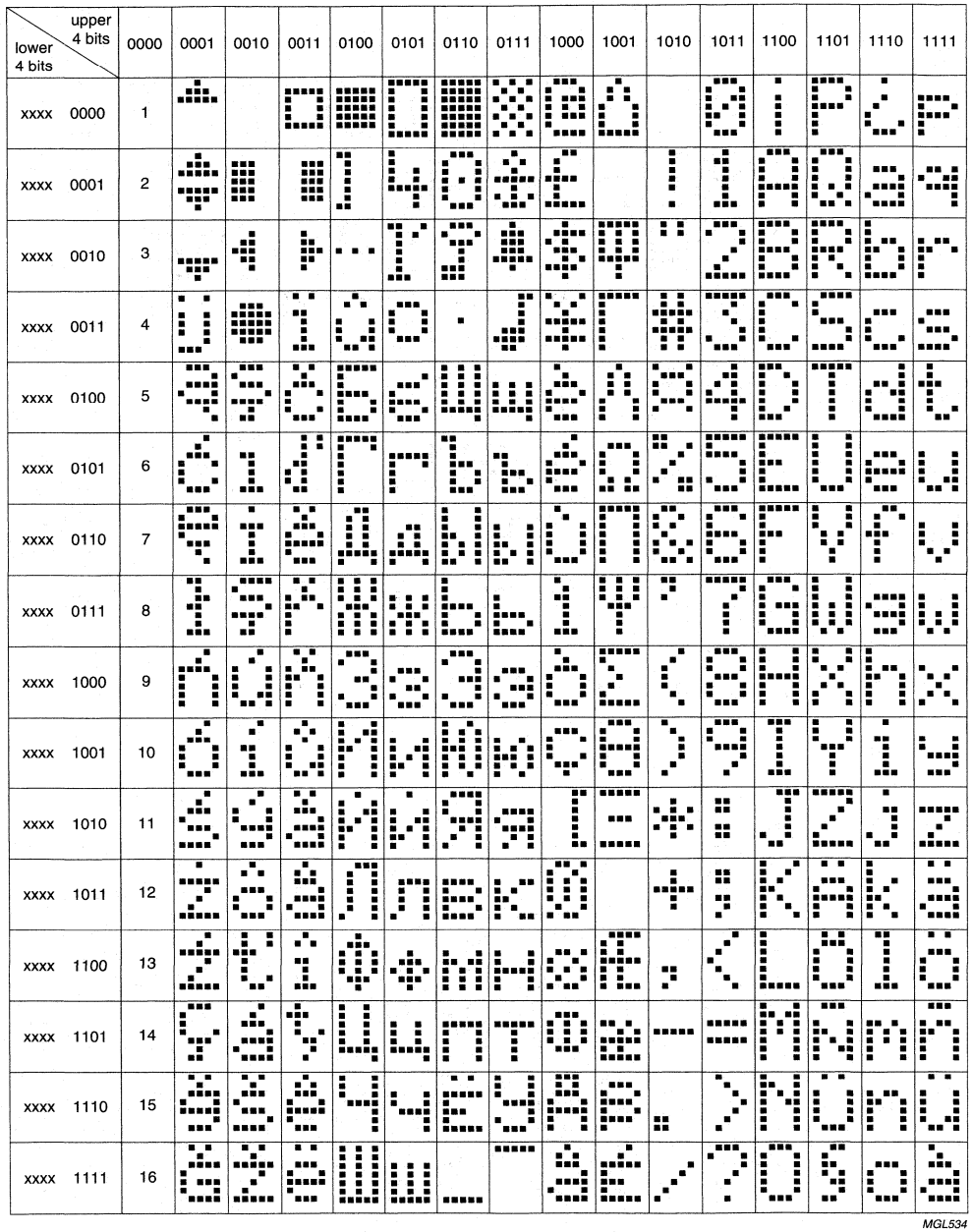


Fig.7 Character set 'S' in CGROM.

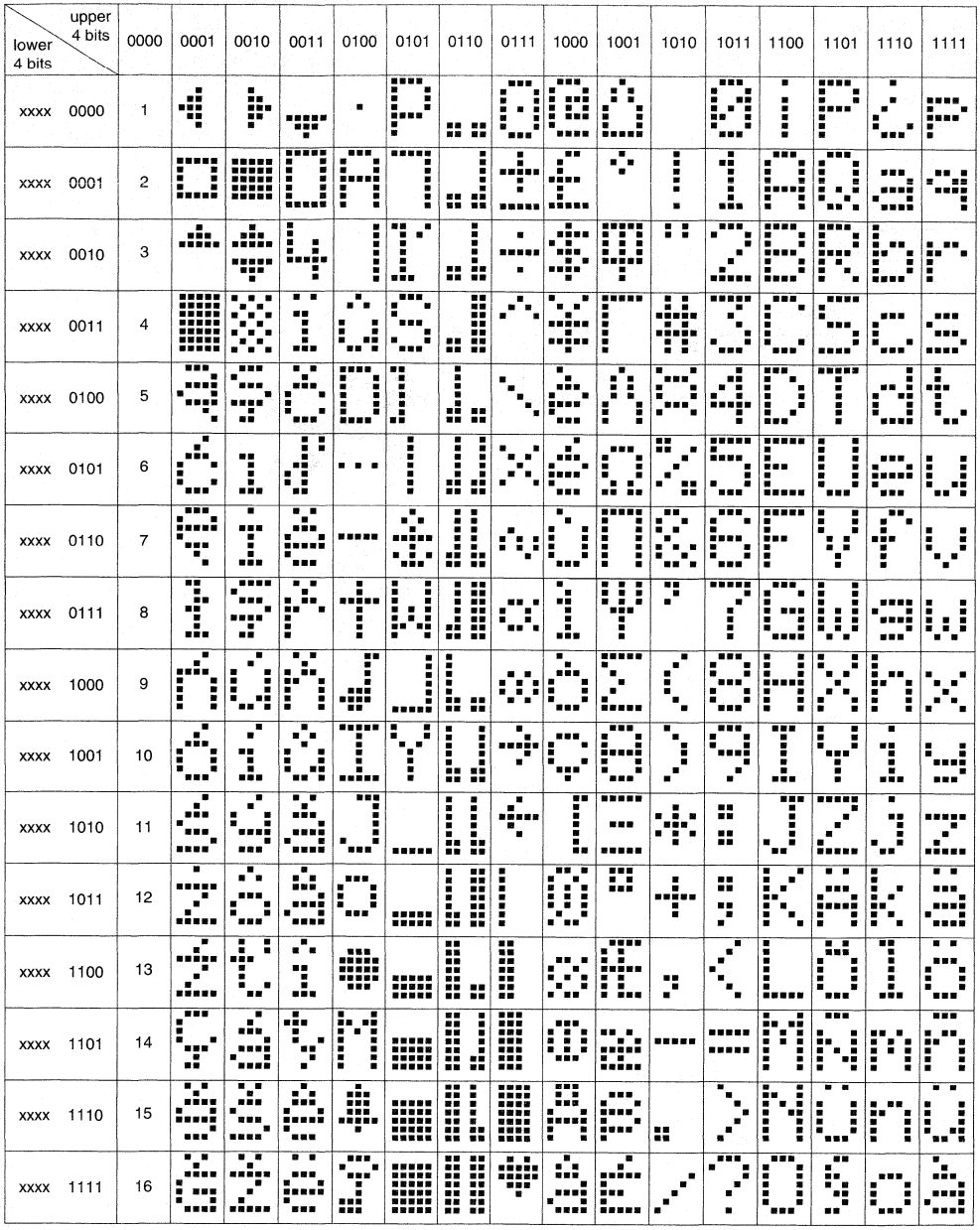
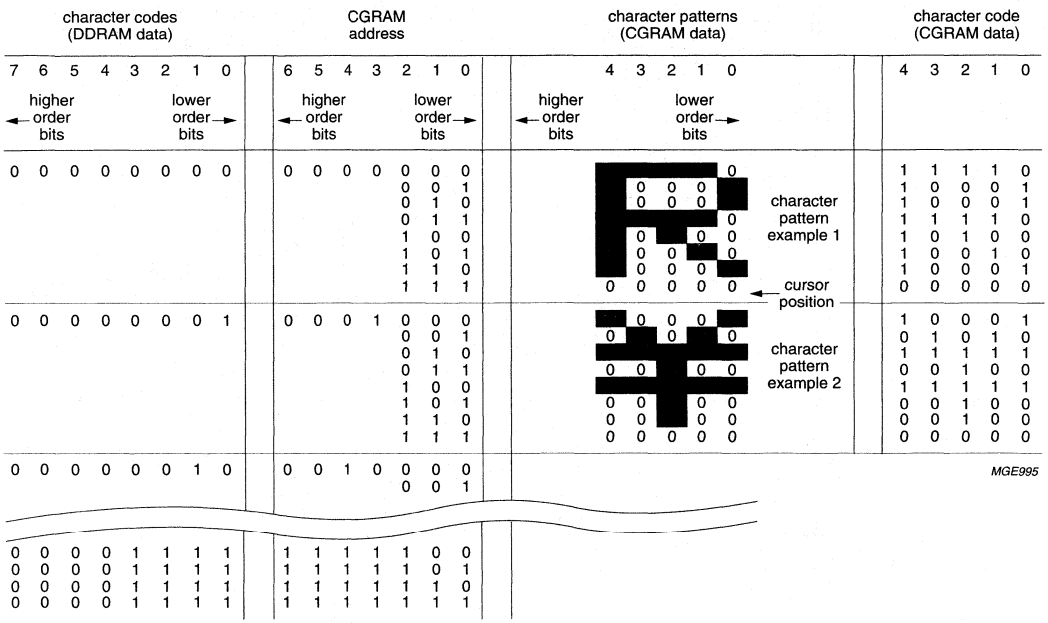


Fig.8 Character set 'V' in CGROM.



Character code bits 0 to 3 correspond to CGRAM address bits 3 to 6.

CGRAM address bits 0 to 2 designate the character pattern line position. The 8th line is the cursor position and display is performed by logical OR with the cursor. Data in the 8th position will appear in the cursor position.

Character pattern column positions correspond to CGRAM data bits 0 to 4, as shown in Fig.6.

As shown in Figs 6 and 7, CGRAM character patterns are selected when character code bits 4 to 7 are all logic 0. CGRAM data = logic 1 corresponds to selection for display.

Only bits 0 to 5 of the CGRAM address are set by the 'set CGRAM address' command. Bit 6 can be set using the 'set DDRAM address' command in the valid address range or by using the auto-increment feature during CGRAM write. All bits 0 to 6 can be read using the 'read busy flag and address counter' command.

Fig.9 Relationship between CGRAM addresses, data and display patterns.

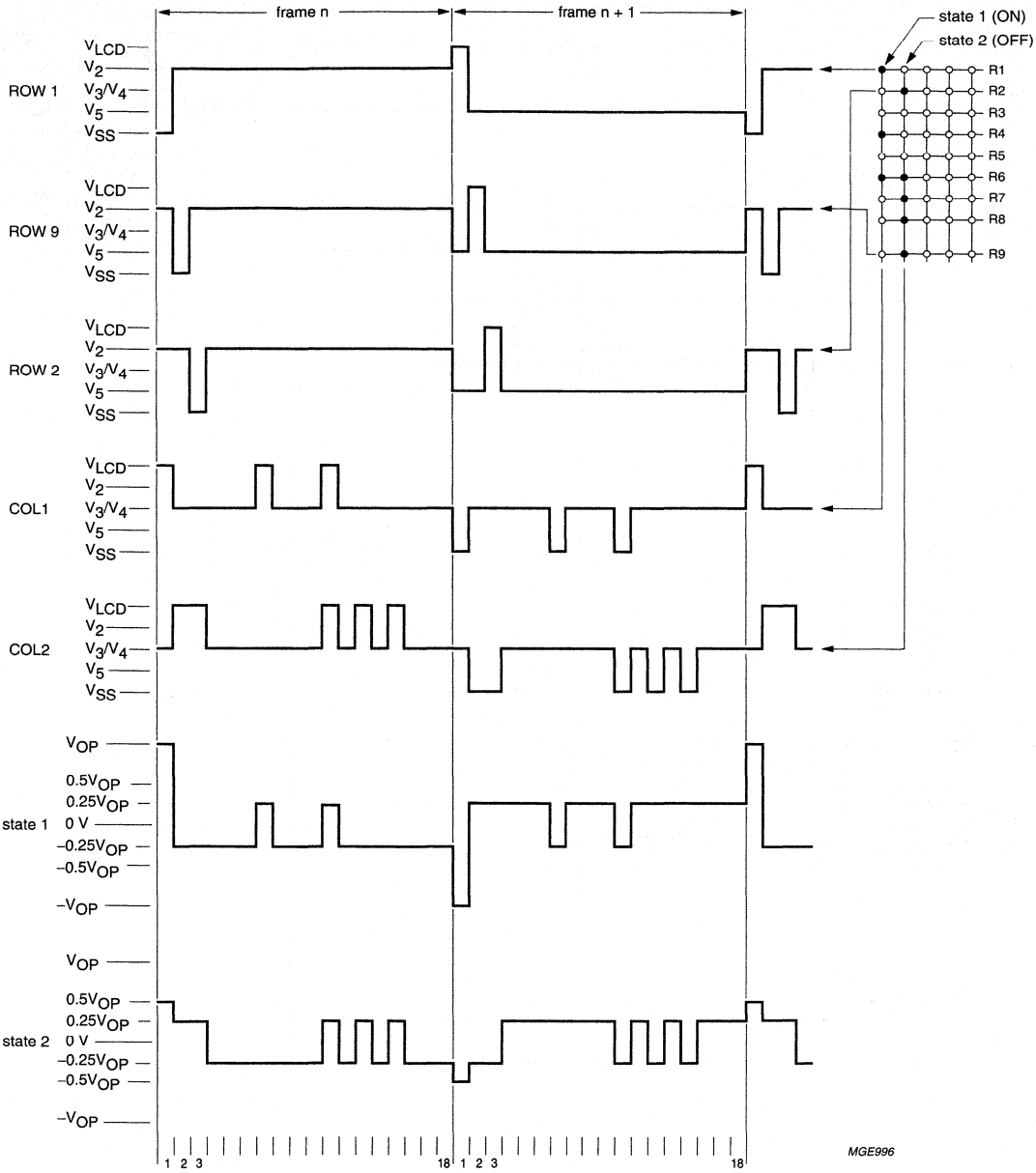


Fig.10 MUX 1 : 18 LCD waveforms; character mode.

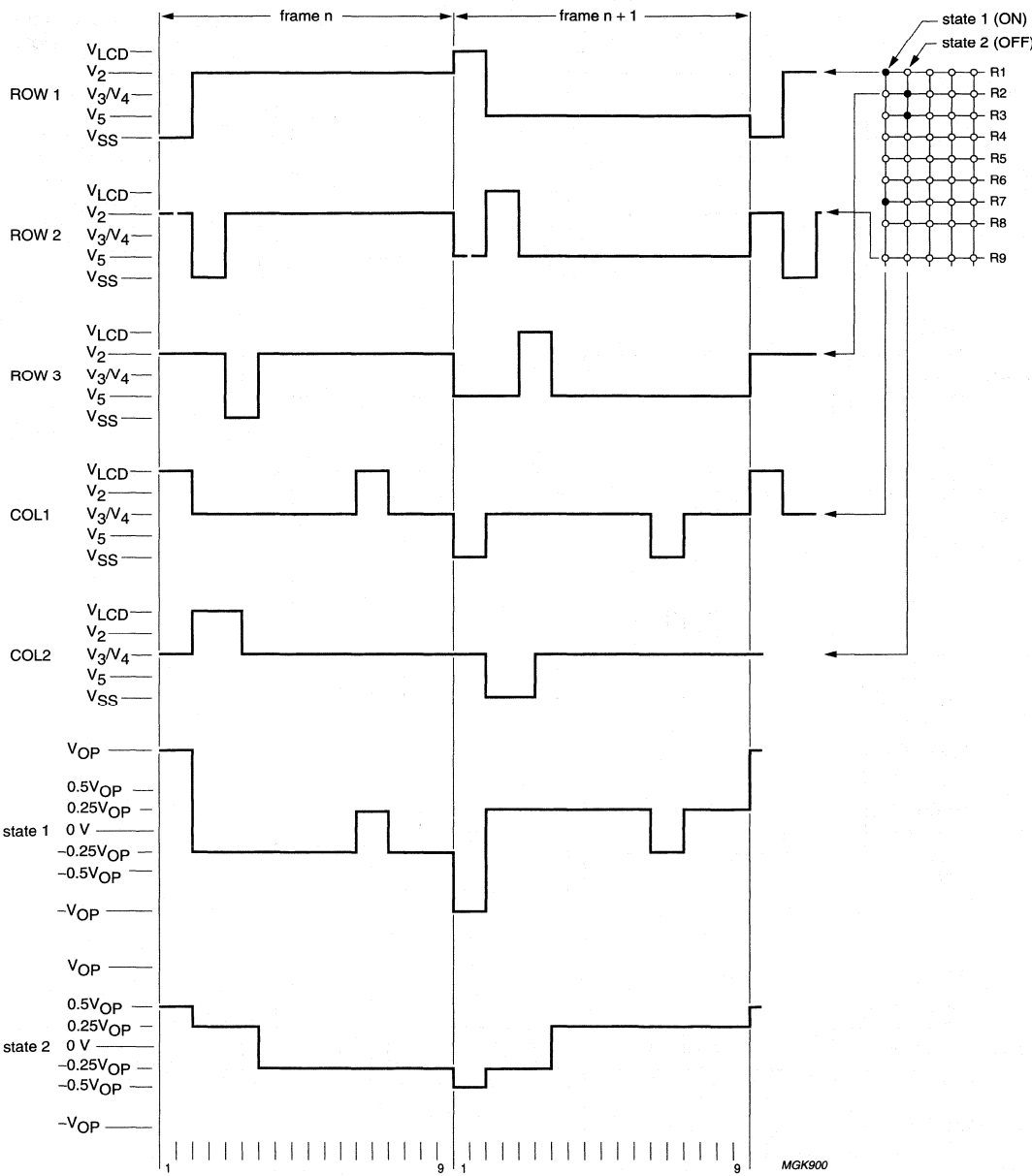


Fig.11 MUX 1 : 9 LCD waveforms; character mode. R10 to 18 to be left open.

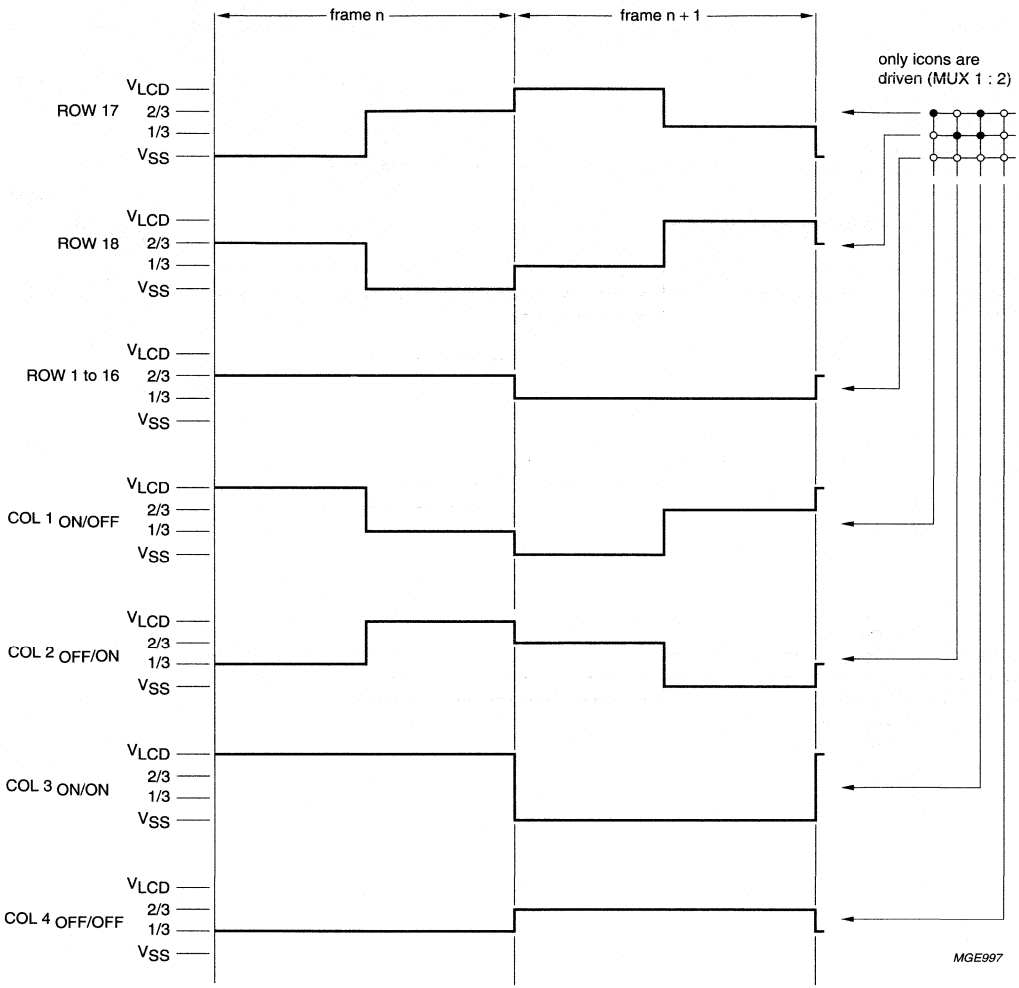
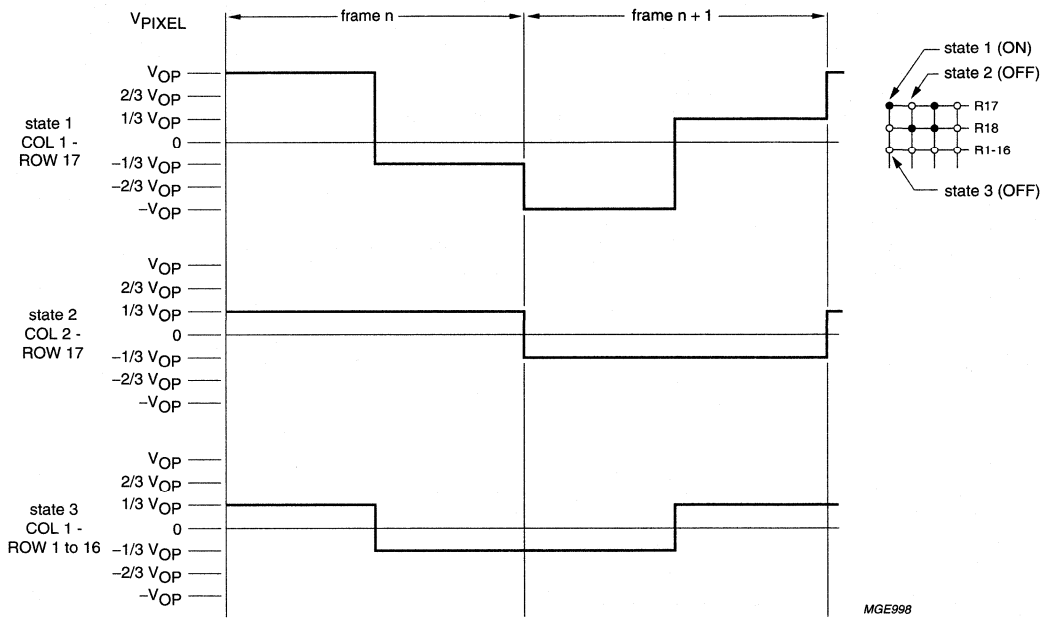


Fig.12 MUX 1 : 2 LCD waveforms; icon mode.



$V_{ON(rms)} = 0.745V_{OP}$

$V_{OFF(rms)} = 0.333V_{OP}$

$$D = \frac{V_{ON}}{V_{OFF}} = 2.23$$

Fig.13 MUX 1 : 2 LCD waveforms; icon mode.

7.17 Reset function

The PCF2119x must be reset externally when power is turned on. The reset executes a 'clear display', requiring 165 oscillator cycles. After the reset the chip has the state shown in Table 4.

Table 4 State after reset

STEP	FUNCTION	CONTROL BIT STATE	CONDITION
1	clear display		
2	entry mode set	I/D = 1	+1 (increment)
		S = 0	no shift
3	display control	D = 0	display off
		C = 0	cursor off
		B = 0	cursor character blink off
4	function set	DL = 1	8-bit interface
		M = 0	1-line display
		H = 0	normal instruction set
		SL = 0	MUX 1 : 18 mode
5	default address pointer to DDRAM; the Busy Flag (BF) indicates the busy state (BF = 1) until initialization ends; the busy state lasts 2 ms; the chip may also be initialized by software; see Tables 17 and 18		
6	icon control	IM, IB = 00	icons/icon blink disabled
7	display/screen configuration	L = 0; P = 0; Q = 0	default configurations
8	V_{LCD} temperature coefficient	TC1 = 0; TC2 = 0	default temperature coefficient
9	set V_{LCD}	$V_A = 0$; $V_B = 0$ (V_{LCD} generator off)	
10	I^2C-bus interface reset		

8 INSTRUCTIONS

Only two PCF2119x registers, the Instruction Register (IR) and the Data Register (DR) can be directly controlled by the MPU. Before internal operation, control information is stored temporarily in these registers, to allow interfacing to various types of MPUs which operate at different speeds or to allow interface to peripheral control ICs.
The PCF2119x operation is controlled by the instructions shown in Table 6 together with their execution time. Details are explained in subsequent sections.

Instructions are of 4 types, those that:

1. Designate PCF2119x functions such as display format, data length, etc.
2. Set internal RAM addresses
3. Perform data transfer with internal RAM
4. Others.

In normal use, category 3 instructions are used most frequently. However, automatic incrementing by 1 (or decrementing by 1) of internal RAM addresses after each data write lessens the MPU program load.
The display shift in particular can be performed concurrently with display data write, enabling the designer to develop systems in minimum time with maximum programming efficiency.

During internal operation, no instructions other than the 'read busy flag' and 'read address' instructions will be executed. Because the busy flag is set to a logic 1 while an instruction is being executed, check to ensure it is a logic 0 before sending the next instruction or wait for the maximum instruction execution time, as given in Table 6. An instruction sent while the busy flag is logic 1 will not be executed.

Table 5 Instruction set for I²C-bus commands

CONTROL BYTE								COMMAND BYTE								I²C-BUS COMMANDS
Co	RS	0	0	0	0	0	0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	note 1

Note

1. R/$\overline{W}$ is set together with the slave address.

Table 6 Instruction set with parallel bus commands; note 1

INSTRUCTION	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DESCRIPTION	REQUIRED CLOCK CYCLES
H = 0 or 1												
NOP	0	0	0	0	0	0	0	0	0	0	no operation	3
Function set	0	0	0	0	1	DL	0	M	SL	H	sets interface Data Length (DL) and number of display lines (M); single line/MUX 1 : 9 (SL), extended instruction set control (H)	3
Read busy flag and address counter	0	1	BF	A_C							reads the Busy Flag (BF) indicating internal operating is being performed and reads address counter contents	0
Read data	1	1	read data								reads data from CGRAM or DDRAM	3
Write data	1	0	write data								writes data from CGRAM or DDRAM	3
H = 0												
Clear display	0	0	0	0	0	0	0	0	0	1	clears entire display and sets DDRAM address 0 in address counter	165
Return home	0	0	0	0	0	0	0	0	1	0	sets DDRAM address 0 in address counter; also returns shifted display to original position; DDRAM contents remain unchanged	3
Entry mode set	0	0	0	0	0	0	0	1	I/D	S	sets cursor move direction and specifies shift of display; these operations are performed during data write and read	3
Display control	0	0	0	0	0	0	1	D	C	B	sets entire display on/off (D), cursor on/off (C) and blink of cursor position character (B); D = 0 (display off) puts chip into the power-down mode	3
Cursor/display shift	0	0	0	0	0	1	S/C	R/L	0	0	moves cursor and shifts display without changing DDRAM contents	3
Set CGRAM address	0	0	0	1	A_{CG}						sets CGRAM address; bit 6 is to be set by the command 'set DDRAM address'; look at the description of the commands	3
Set DDRAM address	0	0	1	A_{DD}							sets DDRAM address	3

INSTRUCTION	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DESCRIPTION	REQUIRED CLOCK CYCLES
H = 1												
Reserved	0	0	0	0	0	0	0	0	0	1	do not use	–
Screen configuration	0	0	0	0	0	0	0	0	1	L	set screen configuration	3
Display configuration	0	0	0	0	0	0	0	1	P	Q	set display configuration	3
Icon control	0	0	0	0	0	0	1	IM	IB	0	set icon mode (IM), icon blink (IB)	3
Temperature control	0	0	0	0	0	1	0	0	TC1	TC2	set temperature coefficient (TCx)	3
Reserved	0	0	0	1	X	X	X	X	X	X	do not use	–
Set V_{LCD}	0	0	1	V	voltage						store V_{LCD} in register V_A or V_B (V)	3

Note

1. X = don't care.

Table 7 Explanations of symbols used in Table 6

BIT	STATE	
	LOGIC 0	LOGIC 1
I/D	decrement	increment
S	display freeze	display shift
D	display off	display on
C	cursor off	cursor on
B	cursor character blink off: character at cursor position does not blink	cursor character blink on: character at cursor position blinks
S/C	cursor move	display shift
R/L	left shift	right shift
DL	4 bits	8 bits
H	use basic instruction set	use extended instruction set
L (no impact, if M = 1 or SL = 1)	left/right screen: standard connection (as in PCF2114)	left/right screen: mirrored connection (as in PCF2116)
	1st 16 characters of 32: columns are from 1 to 80	1st 16 characters of 32: columns are from 1 to 80
	2nd 16 characters of 32: columns are from 1 to 80	2nd 16 characters of 32: columns are from 80 to 1
P	column data: left to right (as in PCF2116); column data is displayed from 1 to 80	column data: right to left; column data is displayed from 80 to 1
Q	row data: top to bottom (as in PCF2116); row data is displayed from 1 to 16 and icon row data is in 17 and 18	row data: bottom to top; row data is displayed from 16 to 1 and icon row data is in 18 and 17
IM	character mode; full display	icon mode; only icons displayed
IB	icon blink disabled	icon blink enabled
V	set V_A	set V_B
M (no impact, if SL = 1)	1-line by 32 display	2-line by 16 display
SL	MUX 1 : 18 (1 × 32 or 2 × 16 character display)	MUX 1 : 9 (1 × 16 character display)
C_0	last control byte; see Table 5	another control byte follows after data/command

Table 8 Explanation of TC1 and TC2 used in Table 6

TC1	TC2	DESCRIPTION
0	0	V_{LCD} temperature coefficient 0
1	0	V_{LCD} temperature coefficient 1
0	1	V_{LCD} temperature coefficient 2
1	1	V_{LCD} temperature coefficient 3; for ranges for TC see Chapter 13

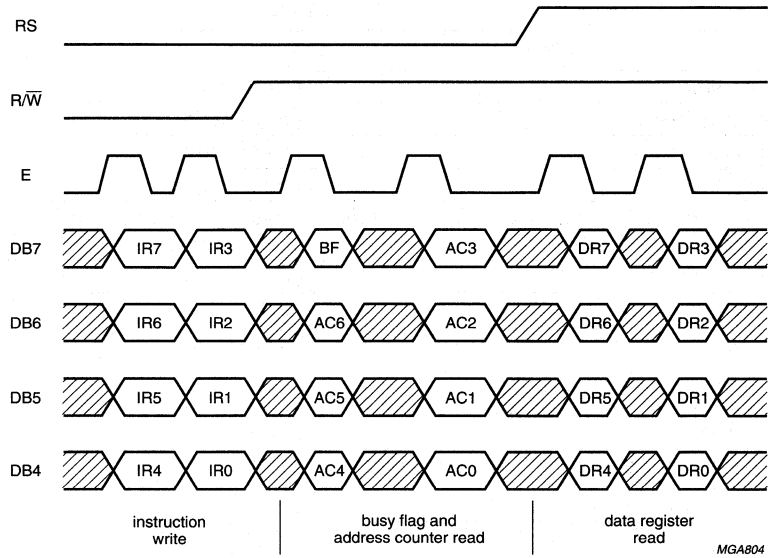
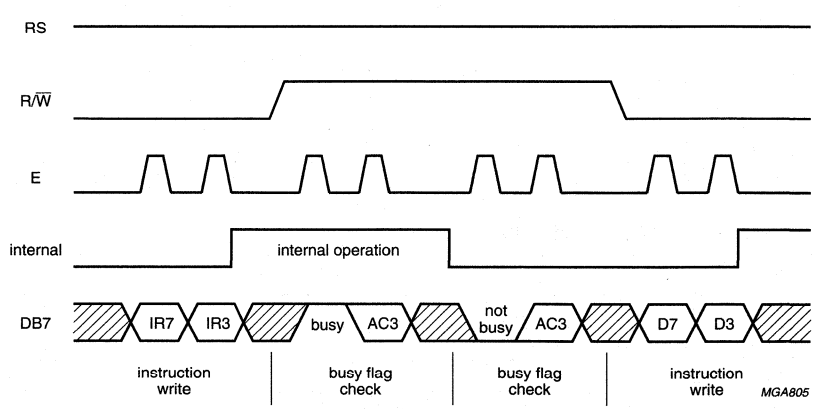


Fig.14 4-bit transfer example.



IR7, IR3: instruction 7th, 3rd bit.
AC3: address counter 3rd bit.
D7, D3: data 7th, 3rd bit.

Fig.15 An example of 4-bit data transfer timing sequence.

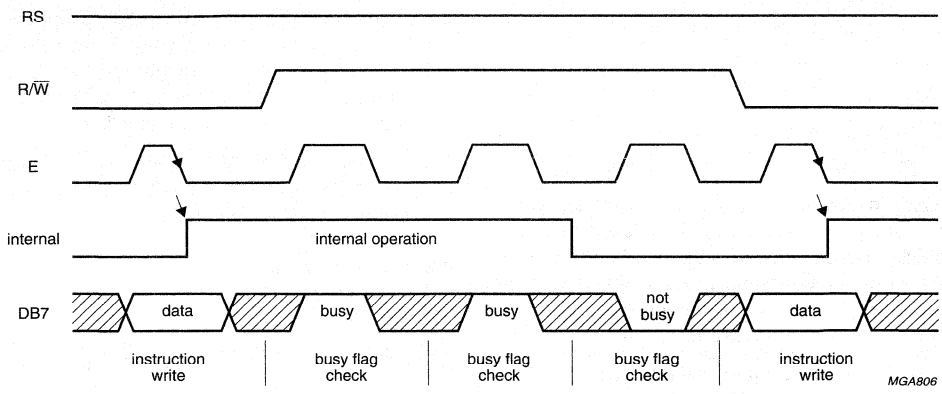


Fig.16 Example of busy flag checking timing sequence.

8.1 Clear display

'Clear display' writes character code 20H into all DDRAM addresses (the character pattern for character code 20H must be a blank pattern), sets the DDRAM address counter to logic 0 and returns the display to its original position, if it was shifted. Thus, the display disappears and the cursor or blink position goes to the left edge of the display. Sets entry mode I/D = 1 (increment mode). S of entry mode does not change.

The instruction 'clear display' requires extra execution time. This may be allowed by checking the Busy Flag (BF) or by waiting until the 165 clock cycles have elapsed. The latter must be applied where no read-back options are foreseen, as in some Chip-On-Glass (COG) applications.

8.2 Return home

'Return home' sets the DDRAM address counter to logic 0 and returns the display to its original position if it was shifted. DDRAM contents do not change. The cursor or blink position goes to the left of the first display line. I/D and S of entry mode do not change.

8.3 Entry mode set

8.3.1 I/D

When I/D = 1 (0) the DDRAM or CGRAM address increments (decrements) by 1 when data is written into or read from the DDRAM or CGRAM. The cursor or blink position moves to the right when incremented and to the left when decremented. The cursor underline and cursor character blink are inhibited when the CGRAM is accessed.

8.3.2 S

When S = 1, the entire display shifts either to the right (I/D = 0) or to the left (I/D = 1) during a DDRAM write. Thus it appears as if the cursor stands still and the display moves. The display does not shift when reading from the DDRAM, or when writing to or reading from the CGRAM. When S = 0, the display does not shift.

8.4 Display control (and partial power-down mode)

8.4.1 D

The display is on when D = 1 and off when D = 0. Display data in the DDRAM is not affected and can be displayed immediately by setting D to a logic 1.

When the display is off (D = 0) the chip is in partial power-down mode:

- The LCD outputs are connected to V_{SS}
- The LCD generator and bias generator are turned off.

Three oscillator cycles are required after sending the 'display off' instruction to ensure all outputs are at V_{SS}, afterwards OSC can be stopped. If the oscillator is running during partial power-down mode ('display off') the chip can still execute instructions. Even lower current consumption is obtained by inhibiting the oscillator (OSC = V_{SS}).

To ensure I_{DD} <1 μA, the parallel bus pads DB7 to DB0 should be connected to V_{DD}; RS and R/$\overline{W}$ to V_{DD} or left open-circuit and PD to V_{DD}. Recovery from power-down mode: PD back to logic 0, if necessary OSC back to V_{DD} and send a 'display control' instruction with D = 1.

8.4.2 C

The cursor is displayed when C = 1 and inhibited when C = 0. Even if the cursor disappears, the display functions I/D, etc. remain in operation during display data write. The cursor is displayed using 5 dots in the 8th line (see Fig.5).

8.4.3 B

The character indicated by the cursor blinks when B = 1. The cursor character blink is displayed by switching between display characters and all dots on with a period of approximately 1 second, with $f_{blink} = \frac{f_{OSC}}{52224}$

The cursor underline and the cursor character blink can be set to display simultaneously.

8.5 Cursor or display shift

'Cursor/display shift' moves the cursor position or the display to the right or left without writing or reading display data. This function is used to correct a character or move the cursor through the display. In 2-line displays, the cursor moves to the next line when it passes the last position (40) of the line. When the displayed data is shifted repeatedly all lines shift at the same time; displayed characters do not shift into the next line.

The Address Counter (AC) content does not change if the only action performed is shift display, but increments or decrements with the 'cursor shift'.

8.6 Function set

8.6.1 DL (PARALLEL MODE ONLY)

Sets interface data width. Data is sent or received in bytes (DB7 to DB0) when DL = 1 or in two nibbles (DB7 to DB4) when DL = 0. When 4-bit width is selected, data is transmitted in two cycles using the parallel bus. In a 4-bit application DB3 to DB0 should be left open-circuit (internal pull-ups). Hence in the first 'function set' instruction after power-on, N and H are set to logic 1. A second 'function set' must then be sent (2 nibbles) to set N and H to their required values.

'Function set' from the I^2C-bus interface sets the DL bit to logic 1.

8.6.2 M

Selects either 1-line by 32 display (M = 0) or 2-line by 16 display (M = 1).

8.6.3 SL

Selects MUX 1 : 9, 1-line by 16 display (independent of M and L). Only rows 1 to 8 and 17 are to be used. All other rows must be left open-circuit. The DDRAM map is the same as in the 2-line by 16 display mode, however, the second line is not displayable.

8.6.4 H

When H = 0 the chip can be programmed via the standard 11 instruction codes used in the PCF2116 and other LCD controllers.

When H = 1 the extended range of instructions will be used. These are mainly for controlling the display configuration and the icons.

8.7 Set CGRAM address

'Set CGRAM address' sets bits 5 to 0 of the CGRAM address A_{CG} into the address counter (binary A5 to A0). Data can then be written to or read from the CGRAM.

Attention: the CGRAM address uses the same address register as the DDRAM address and consists of 7 bits (binary A6 to A0). With the 'set CGRAM address' command, only bits 5 to 0 are set. Bit 6 can be set using the 'set DDRAM address' command first, or by using the auto-increment feature during CGRAM write. All bits 6 to 0 can be read using the 'read busy flag' and 'read address' command.

When writing to the lower part of the CGRAM, ensure that bit 6 of the address is not set (e.g. by an earlier DDRAM write or read action).

8.8 Set DDRAM address

'Set DDRAM address' sets the DDRAM address A_{DD} into the address counter (binary A6 to A0). Data can then be written to or read from the DDRAM.

8.9 Read busy flag and read address

'Read busy flag' and 'read address' read the Busy Flag (BF) and Address Counter (AC). BF = 1 indicates that an internal operation is in progress. The next instruction will not be executed until BF = 0. It is recommended that the BF status is checked before the next write operation is executed.

At the same time, the value of the address counter expressed in binary A6 to A0 is read out. The address counter is used by both CGRAM and DDRAM, and its value is determined by the previous instruction.

8.10 Write data to CGRAM or DDRAM

'Write data' writes binary 8-bit data D7 to D0 to the CGRAM or the DDRAM.

Whether the CGRAM or DDRAM is to be written into is determined by the previous 'set CGRAM address' or 'set DDRAM address' command. After writing, the address automatically increments or decrements by 1, in accordance with the entry mode. Only bits D4 to D0 of CGRAM data are valid, bits D7 to D5 are 'don't care'.

8.11 Read data from CGRAM or DDRAM

'Read data' reads binary 8-bit data D7 to D0 from the CGRAM or DDRAM.

The most recent 'set address' command determines whether the CGRAM or DDRAM is to be read.

The 'read data' instruction gates the content of the Data Register (DR) to the bus while E is HIGH. After E goes LOW again, internal operation increments (or decrements) the AC and stores RAM data corresponding to the new AC into the DR.

There are only three instructions that update the data register:

- 'set CGRAM address'
- 'set DDRAM address'
- 'read data' from CGRAM or DDRAM.

Other instructions (e.g. 'write data', 'cursor/display shift', 'clear display' and 'return home') do not modify the data register content.

9 EXTENDED FUNCTION SET INSTRUCTIONS AND FEATURES

9.1 New instructions

H = 1, sets the chip into alternate instruction set mode.

9.2 Icon control

The PCF2119x can drive up to 160 icons. See Fig.17 for CGRAM to icon mapping.

9.3 IM

When IM = 0, the chip is in character mode. In the character mode characters and icons are driven (MUX 1 : 18). The V_{LCD} generator, if used, produces the V_{LCD} voltage programmed in register V_A.

When IM = 1, the chip is in icon mode. In the icon mode only the icons are driven (MUX 1 : 2) and the V_{LCD} voltage generator, if used, produces the V_{LCD} voltage as programmed in register V_B.

9.4 IB

Icon blink control is independent of the cursor/character blink function.

When IB = 0, icon blink is disabled. Icon data is stored in CGRAM character 0 to 3 ($4 \times 8 \times 5 = 160$ bits for 160 icons).

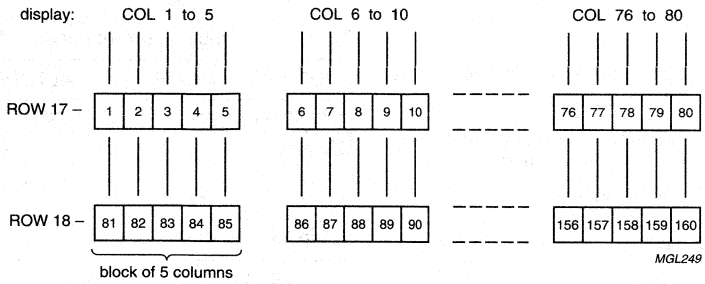
When IB = 1, icon blink is enabled. In this case each icon is controlled by two bits. Blink consists of two half phases (corresponding to the cursor on and off phases called even and odd phases hereafter).

Icon states for the even phase are stored in CGRAM characters 0 to 3 ($4 \times 8 \times 5 = 160$ bits for 160 icons). These bits also define icon state when icon blink is not used.

Icon states for the odd phase are stored in CGRAM character 4 to 7 (another 160 bits for the 160 icons). When icon blink is disabled CGRAM characters 4 to 6 may be used as normal CGRAM characters.

Table 9 Blink effect for icons and cursor character blink

PARAMETER	EVEN PHASE	ODD PHASE
Cursor underline	on	off
Cursor character blink	block (all on)	normal (display character)
Icons	state 1: CGRAM character 0 to 2	state 2: CGRAM character 4 to 6



icon no.	phase	ROW/COL	character codes	CGRAM address	CGRAM data	icon view
			7 6 5 4 3 2 1 0 MSB LSB	6 5 4 3 2 1 0 MSB LSB	4 3 2 1 0 MSB LSB	
1-5	even	17/1-5	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0	1 0 1 0 1	
6-10	even	17/6-10	0 0 0 0 0 0 0 0	0 0 0 0 0 0 1	0 1 0 1 0	
11-15	even	17/11-15	0 0 0 0 0 0 0 0	0 0 0 0 0 1 0	0 1 1 1 0	
⋮	⋮	⋮	⋮	⋮	⋮	⋮
76-80	even	17/76-80	0 0 0 0 0 0 0 1	0 0 0 1 1 1 1	1 1 1 1 1	
81-85	even	18/1-5	0 0 0 0 0 0 1 0	0 0 1 0 0 0 0	1 1 0 0 0	
⋮	⋮	⋮	⋮	⋮	⋮	⋮
156-160	even	18/76-80	0 0 0 0 0 0 1 1	0 0 1 1 1 1 1	1 1 1 0 1	
1-5	odd (blink)	17/1-5	0 0 0 0 0 1 0 0	0 1 0 0 0 0 0	0 0 0 0 0	
⋮	⋮	⋮	⋮	⋮	⋮	⋮
156-160	odd (blink)	18/76-80	0 0 0 0 0 1 1 1	0 1 1 1 1 1 1	0 0 1 1 0	

MGK999

CGRAM data bit = logic 1 turns the icon on, data bit = logic 0 turns the icon off.
Data in character codes 0 to 2 define the icon state when icon blink is disabled or during the even phase when icon blink is enabled.
Data in character codes 4 to 6 define the icon state during the odd phase when icon blink is enabled (not used for icons when icon blink is disabled).

Fig.17 CGRAM to icon mapping.

9.5 Normal/icon mode operation

IM	CONDITION	V_{LCD}
0	character mode	generates V_A
1	icon mode	generates V_B

9.6 Screen configuration

L: default is L = 0.

L = 0: the two halves of a split screen are connected in a standard way i.e. column 1/81, 2/82 to 80/160.

L = 1: the two halves of a split screen are connected in a mirrored way i.e. column 1/160, 2/159 to 80/81. This allows single layer PCB or glass layout.

9.7 Display configuration

P, Q: default is P, Q = 0.

P = 1: mirrors the column data.

Q = 1: mirrors the row data.

9.8 TC1 and TC2

Default is TC1 and TC2 = 0. This selects the default temperature coefficient for the internally generated V_{LCD}. TC1 and TC2 = 10, 01 and 11 selects alternative temperature coefficients 1, 2 and 3 respectively.

9.9 Set V_{LCD}

The V_{LCD} value is programmed by instruction. Two on-chip registers hold V_{LCD} values for the character mode and the icon mode respectively (V_A and V_B). The generated V_{LCD} value is independent of V_{DD}, allowing battery operation of the chip.

V_{LCD} programming:

1. Send 'function set' instruction with H = 1
2. Send 'set V_{LCD}' instruction to write to voltage register:
   a) DB7, DB6 = 10: DB5 to DB0 are V_{LCD} of character mode (V_A)
   b) DB7, DB6 = 11: DB5 to DB0 are V_{LCD} of icon mode (V_B)
   c) DB5 to DB0 = 000000 switches V_{LCD} generator off (when selected)
   d) During 'display off' and power-down the V_{LCD} generator is also disabled.
3. Send 'function set' instruction with H = 0 to resume normal programming.

9.10 Reducing current consumption

Reducing current consumption can be achieved by one of the options given in Table 10.

When V_{LCD} lies outside the V_{DD} range and must be generated, it is usually more efficient to use the on-chip generator than an external regulator.

Table 10 Reducing current consumption

ORIGINAL MODE	ALTERNATIVE MODE
Character mode	icon mode (control bit IM)
Display on	display off (control bit D)
Any mode	power-down (PD pad)

Table 11 Use of the V_A and V_B registers

MODE	V_A	V_B
Normal operation	V_{LCD} character mode	V_{LCD} icon mode

10 INTERFACES TO MPU

10.1 Parallel interface

The PCF2119x can send data in either two 4-bit operations or one 8-bit operation and can thus interface to 4-bit or 8-bit microcontrollers.

In 8-bit mode data is transferred as 8-bit bytes using the 8 data lines DB7 to DB0. Three further control lines E, RS and R/$\overline{W}$ are required; see Section 6.1.

In 4-bit mode data is transferred in two cycles of 4 bits each using pads DB7 to DB4 for the transaction. The higher order bits (corresponding to DB7 to DB4 in 8-bit mode) are sent in the first cycle and the lower order bits (DB3 to DB0 in 8-bit mode) in the second. Data transfer is complete after two 4-bit data transfers. It should be noted that two cycles are also required for the busy flag check. 4-bit operation is selected by instruction, see Figs 14 to 16 for examples of bus protocol.

In 4-bit mode, pads DB3 to DB0 must be left open-circuit. They are pulled up to V_{DD} internally.

10.2 I²C-bus interface

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are the Serial Data line (SDA) and the Serial Clock Line (SCL). Both lines must be connected to a positive supply via pull-up resistors. Data transfer may be initiated only when the bus is not busy.

Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte.

Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration).

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

10.2.1 I²C-BUS PROTOCOL

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always carried out with the first byte transmitted after the START procedure. The I²C-bus configuration for the different PCF2119x read and write cycles is shown in Figs 22 to 24. The slow down feature of the I²C-bus protocol (receiver holds SCL LOW during internal operations) is not used in the PCF2119x.

10.2.2 DEFINITIONS

- Transmitter: the device which sends the data to the bus
- Receiver: the device which receives the data from the bus
- Master: the device which initiates a transfer, generates clock signals and terminates a transfer
- Slave: the device addressed by a master
- Multi-master: more than one master can attempt to control the bus at the same time without corrupting the message
- Arbitration: procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted
- Synchronization: procedure to synchronize the clock signals of two or more devices.

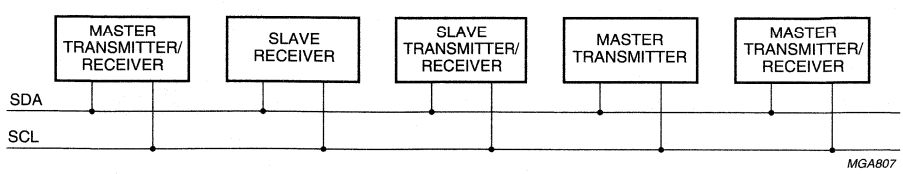


Fig.18 System configuration.

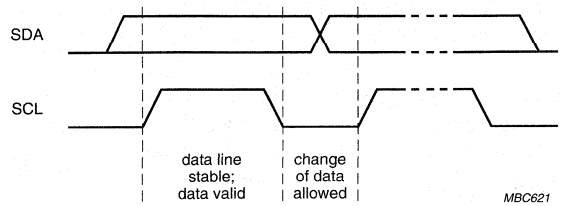


Fig.19 Bit transfer.

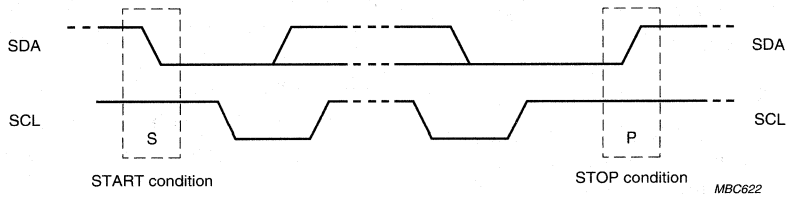


Fig.20 Definition of START and STOP conditions.

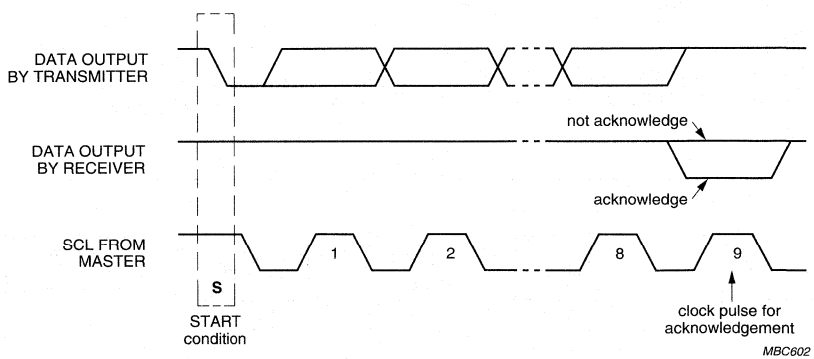


Fig.21 Acknowledgement on the I^2C-bus.

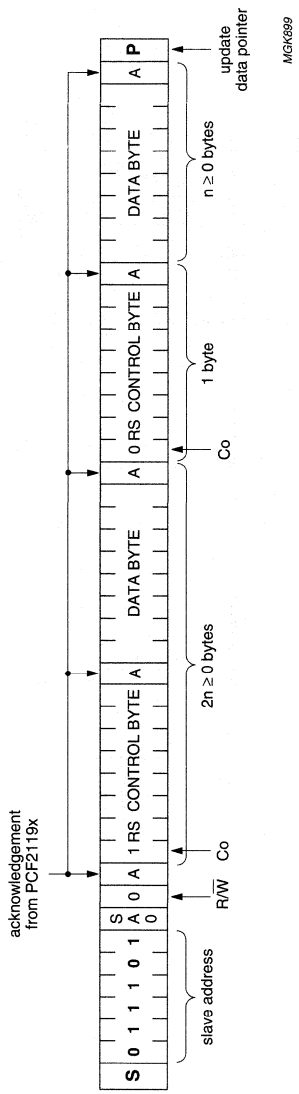
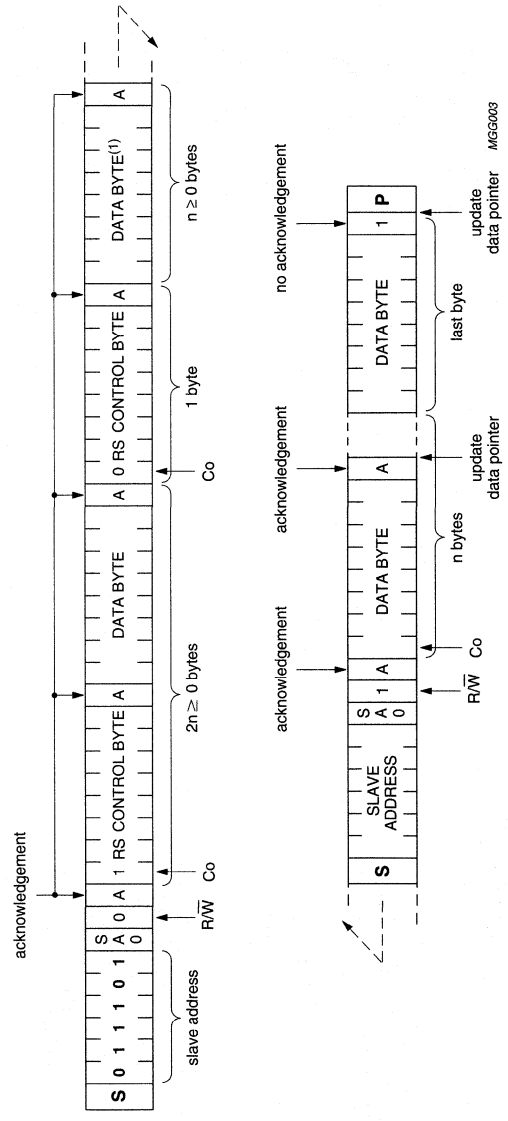


Fig.22 Master transmits to slave receiver; write mode.



(1) Last data byte is a dummy byte (may be omitted).

Fig.23 Master reads after setting word address; writes word address, set RS; 'read data'.

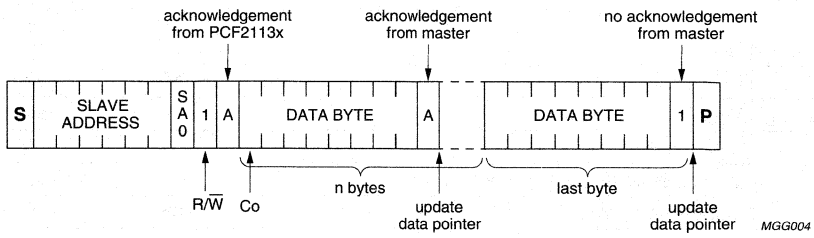


Fig.24 Master reads slave immediately after first byte; read mode (RS previously defined).

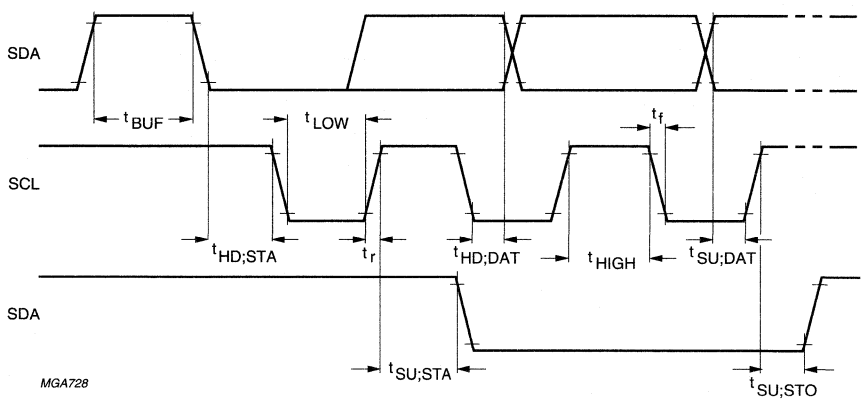


Fig.25 I²C-bus timing diagram.

11 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.5	+6.5	V
V_{LCD}	LCD supply voltage	−0.5	+7.5	V
V_I	input voltage pads OSC, RS, R/$\overline{W}$, E and DB7 to DB0	−0.5	V_{DD} + 0.5	V
V_O	output voltage pads R1 to R18, C1 to C80 and V_{LCD}	−0.5	V_{LCD} + 0.5	V
I_I	DC input current	−10	+10	mA
I_O	DC output current	−10	+10	mA
I_{DD}, I_{SS} and I_{LCD}	V_{DD}, V_{SS} or V_{LCD} current	−50	+50	mA
P_{tot}	total power dissipation	–	400	mW
P_O	power dissipation per output	–	100	mW
T_{stg}	storage temperature	−65	+150	°C

12 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see *"Handling MOS Devices"*).

13 DC CHARACTERISTICS

V_{DD} = 2.2 to 4.0 V (external V_{LCD}: V_{DD} = 2.2 to 5.5 V); V_{SS} = 0 V; V_{LCD} = 2.2 to 6.5 V; T_{amb} = −30 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD1}	supply voltage	internal V_{LCD} generation	2.2	–	4.0	V
		external V_{LCD} generation	2.2	–	5.5	V
V_{DD2}	high voltage generator supply voltage	internal V_{LCD} generation	2.2	–	4.0	
V_{LCD}	LCD supply voltage		2.2	–	6.5	V
I_{SS}	ground supply current	external V_{LCD}; note 1				
		internal V_{LCD}; notes 1 and 3				
I_{SS1}	ground supply current 1		–	70	120	µA
I_{SS3}	ground supply current 3	V_{DD} = 3 V; V_{LCD} = 5 V; note 2	–	45	80	µA
I_{SS4}	ground supply current 4	icon mode; V_{DD} = 3 V; V_{LCD} = 2.5 V; note 2	–	25	45	µA
I_{SS5}	ground supply current 5	power-down mode; V_{DD} = 3 V; V_{LCD} = 2.5 V; DB7 to DB0, RS and R/$\overline{W}$ = 1; OSC = 0; PD = 1	–	2	5	µA
I_{SS6}	ground supply current 6		–	190	400	µA
I_{SS8}	ground supply current 8	V_{DD} = 3 V; V_{LCD} = 5 V; note 2	–	160	400	µA
I_{SS9}	ground supply current 9	icon mode; V_{DD} = 3 V; V_{LCD} = 2.5 V; note 2	–	120	–	µA
Logic						
V_{IL1}	LOW-level input voltage pads T1, E, RS, R/$\overline{W}$, DB7 to DB0 and SA0		0	–	0.3V_{DD}	V
V_{IH1}	HIGH-level input voltage pads T1, E, RS, R/$\overline{W}$, DB7 to DB0 and SA0		0.7V_{DD}	–	V_{DD}	V
$V_{IL(PD)}$	LOW-level input voltage pad PD		0	–	0.2V_{DD}	V
$V_{IH(PD)}$	HIGH-level input voltage pad PD		0.8V_{DD}	–	V_{DD}	V
$V_{IL(osc)}$	LOW-level input voltage pad OSC		0	–	V_{DD} − 1.5	V
$V_{IH(osc)}$	HIGH-level voltage pad OSC		V_{DD} − 0.1	–	V_{DD}	V
$I_{OL(DB)}$	LOW-level output current pads DB7 to DB0	V_{OL} = 0.4 V; V_{DD} = 5 V	1.6	4	–	mA
$I_{OH(DB)}$	HIGH-level output current pads DB7 to DB0	V_{OH} = 4 V; V_{DD} = 5 V	−1	−8	–	mA
I_{pu}	pull-up current pads DB7 to DB0	V_I = V_{SS}	0.04	0.15	1	µA
I_L	leakage current pads OSC, E, RS, R/$\overline{W}$, DB7 to DB0 and SA0	V_I = V_{DD} or V_{SS}	−1	–	+1	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I²C-bus						
SDA AND SCL						
V_{IL2}	LOW-level input voltage		0	–	$0.3V_{DD}$	V
V_{IH2}	HIGH-level input voltage		$0.7V_{DD}$	–	5.5	V
I_{LI}	input leakage current	$V_I = V_{DD}$ or V_{SS}	–1	–	+1	µA
C_i	input capacitance	note 4	–	–	10	pF
$I_{OL(SDA)}$	LOW-level output current SDA	V_{OL} = 0.4 V; V_{DD} = 5 V	3	–	–	mA
LCD outputs						
$R_{O(ROW)}$	row output resistance pads R1 to R18	note 5	–	10	30	kΩ
$R_{O(COL)}$	column output resistance pads C1 to C80	note 5	–	15	40	kΩ
$V_{bias(tol)}$	bias tolerance pads R1 to R18 and C1 to C80	note 6	–	20	130	mV
$V_{VLCD(tol)}$	V_{LCD} tolerance	T_{amb} = 25 °C; note 3				
		V_{LCD} < 3 V	–	–	220	mV
		V_{LCD} < 4 V	–	–	270	mV
		V_{LCD} < 5 V	–	–	340	mV
		V_{LCD} < 6 V	–	–	440	mV
		V_{LCD} = 5.018 V ($V_{A/B}$ = 27H)	–	–	340	mV
TC0	V_{LCD} temperature coefficient 0	note 7	–	–8.0	–	mV/K
TC1	V_{LCD} temperature coefficient 1	note 7	–	–9.0	–	mV/K
TC2	V_{LCD} temperature coefficient 2	note 7	–	–10.5	–	mV/K
TC3	V_{LCD} temperature coefficient 3	note 7	–	–11.8	–	mV/K

Notes

1. LCD outputs are open-circuit; inputs at V_{DD} or V_{SS}; bus inactive.
2. T_{amb} = 25 °C; f_{OSC} = 200 kHz.
3. LCD outputs are open-circuit; HV generator is on; load current I_{VLCD} (at V_{LCD}) = 5 µA.
4. Tested on sample basis.
5. Resistance of output terminals (R1 to R18 and C1 to C80) with a load current of 20 µA; outputs measured one at a time; external V_{LCD}.
6. LCD outputs open-circuit; external V_{LCD}.
7. Temperature coefficient at V_{OP} = 5.0 V. Typical range ±2 mV/K.

14 AC CHARACTERISTICS

V_{DD} = 2.2 to 5.5 V; V_{SS} = 0 V; V_{LCD} = 2.2 to 6.5 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{FR}	LCD frame frequency (internal clock)	V_{DD} = 5.0 V	45	95	147	Hz
f_{OSC}	oscillator frequency (not available at any pad)		140	250	450	kHz
$f_{OSC(ext)}$	external clock frequency		140	–	450	kHz
t_{OSCST}	oscillator start-up time after power-down		–	200	300	µs
Bus timing characteristics: parallel interface; note 1						
WRITE OPERATION (WRITING DATA FROM MPU TO PCF2119X)						
$T_{cy(en)}$	enable cycle time		500	–	–	ns
$t_{W(en)}$	enable pulse width		220	–	–	ns
$t_{su(A)}$	address set-up time		50	–	–	ns
$t_{h(A)}$	address hold time		25	–	–	ns
$t_{su(D)}$	data set-up time		60	–	–	ns
$t_{h(D)}$	data hold time		25	–	–	ns
READ OPERATION (READING DATA FROM PCF2119X TO MPU)						
$T_{cy(en)}$	enable cycle time		500	–	–	ns
$t_{W(en)}$	enable pulse width		220	–	–	ns
$t_{su(A)}$	address set-up time		50	–	–	ns
$t_{h(A)}$	address hold time		25	–	–	ns
$t_{d(D)}$	data delay time		–	–	150	ns
$t_{h(D)}$	data hold time		20	–	100	ns
Timing characteristics: I^2C-bus interface; note 1						
f_{SCL}	SCL clock frequency		–	–	400	kHz
t_{LOW}	SCL clock low period		1.3	–	–	µs
t_{HIGH}	SCL clock high period		0.6	–	–	µs
$t_{SU;DAT}$	data set-up time		100	–	–	ns
$t_{HD;DAT}$	data hold time		0	–	–	ns
t_r	SCL, SDA rise time		–	–	300	ns
t_f	SCL, SDA fall time		–	–	300	ns
C_B	capacitive bus line load		–	–	400	pF
$t_{SU;STA}$	set-up time for a repeated START condition		0.6	–	–	µs
$t_{HD;STA}$	START condition hold time		0.6	–	–	µs
$t_{SU;STO}$	set-up time for STOP condition		0.6	–	–	µs
t_{SW}	tolerable spike width on bus		–	–	50	ns

Note

1. All timing values are valid within the operating supply voltage and ambient temperature range and are referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

15 TIMING CHARACTERISTICS

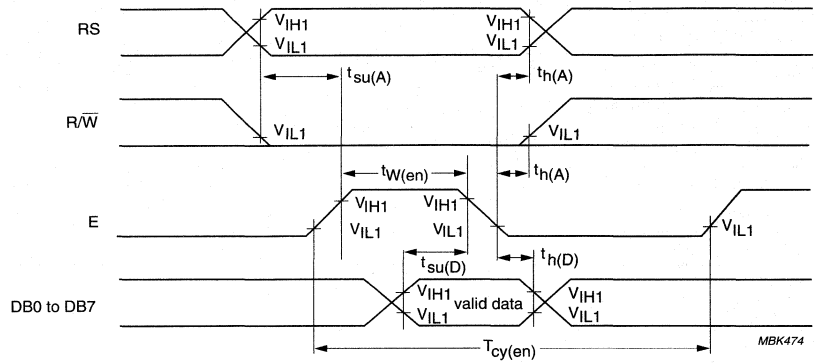


Fig.26 Parallel bus write operation sequence; writing data from MPU to PCF2119x.

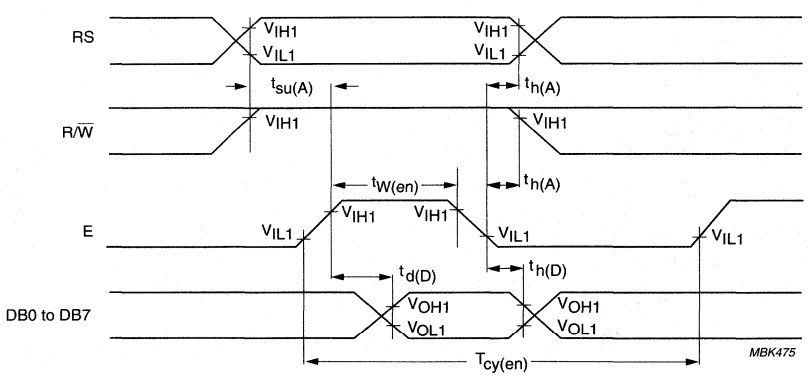


Fig.27 Parallel bus read operation sequence; reading data from PCF2119x to MPU.

16 APPLICATION INFORMATION

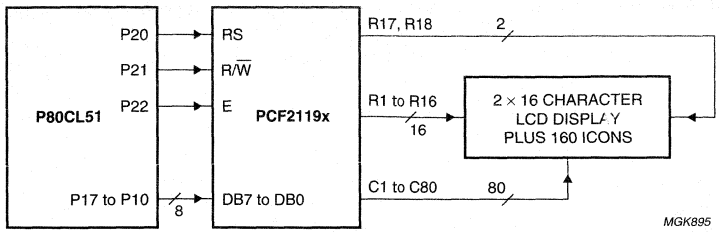


Fig.28 Direct connection to 8-bit MPU; 8-bit bus.

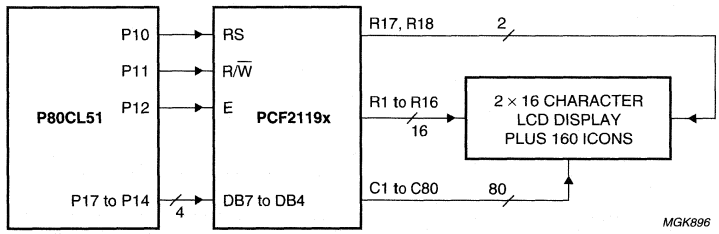


Fig.29 Direct connection to 8-bit MPU; 4-bit bus.

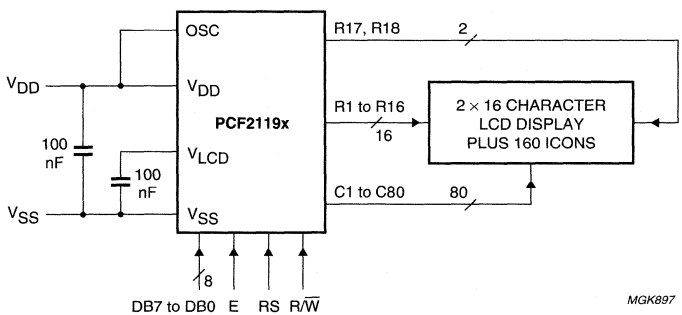


Fig.30 Typical application using parallel interface.

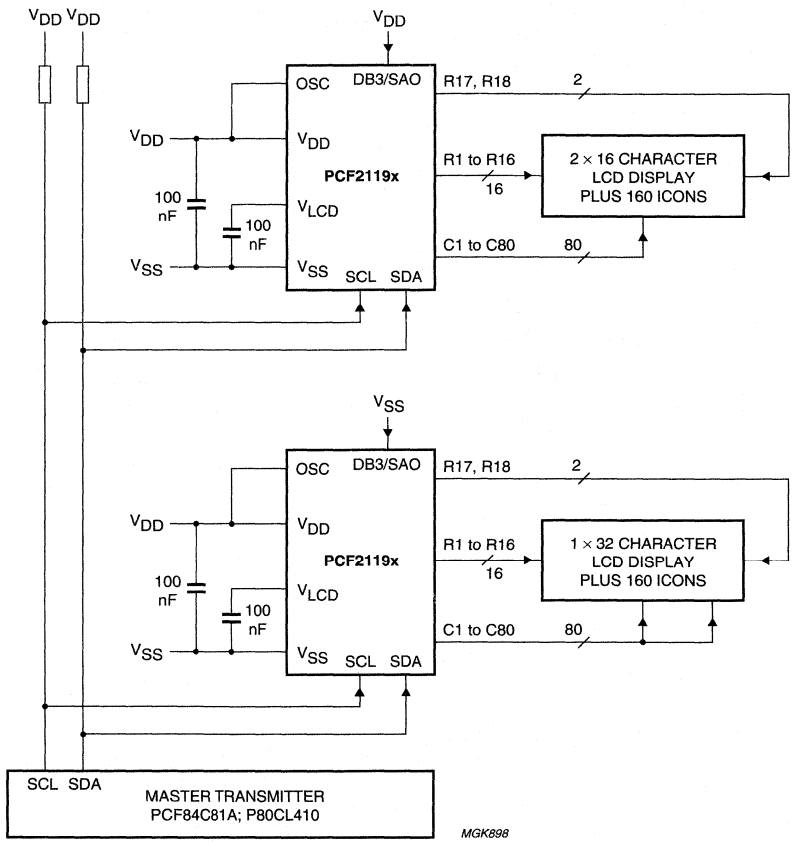


Fig.31 Application using I²C-bus interface.

16.1 8-bit operation, 1-line display using external reset

Table 13 shows an example of a 1-line display in 8-bit operation. The PCF2119x functions must be set by the 'function set' instruction prior to display. Since the DDRAM can store data for 80 characters, the RAM can be used for advertising displays when combined with display shift operation. Since the display shift operation changes display position only and the DDRAM contents remain unchanged, display data entered first can be displayed when the 'return home' operation is performed.

16.2 4-bit operation, 1-line display using external reset

The program must set functions prior to a 4-bit operation, see Table 12. When power is turned on, 8-bit operation is automatically selected and the PCF2119x attempts to perform the first write as an 8-bit operation. Since nothing is connected to DB0 to DB3, a rewrite is then required. However, since one operation is completed in two accesses of 4-bit operation, a rewrite is required to set the functions (see Table 12 step 3). Thus, DB4 to DB7 of the 'function set' are written twice.

16.3 8-bit operation, 2-line display

For a 2-line display, the cursor automatically moves from the first to the second line after the 40th digit of the first line has been written. Thus, if there are only 8 characters in the first line, the DDRAM address must be set after the 8th character is completed (see Table 6). It should be noted that both lines of the display are always shifted together; data does not shift from one line to the other.

16.4 I²C-bus operation, 1-line display

A control byte is required with most commands (see Table 16).

Table 12 4-bit operation, 1-line display example; using external reset

STEP	INSTRUCTION	DISPLAY	OPERATION
1	power supply on (PCF2119x is initialized by the external reset)		initialized; no display appears
2	function set RS R/$\overline{W}$ DB7 DB6 DB5 DB4 0 0 0 0 1 0		sets to 4-bit operation; in this instance operation is handled as 8-bits by initialization and only this instruction completes with one write
3	function set 0 0 0 0 1 0 0 0 0 0 0 0		sets to 4-bit operation, selects 1-line display and $V_{LCD} = V_0$; 4-bit operation starts from this point and resetting is needed
4	display on/off control 0 0 0 0 0 0 0 0 1 1 1 0	_	turns on display and cursor; entire display is blank after initialization
5	entry mode set 0 0 0 0 0 0 0 0 0 1 1 0	_	sets mode to increment the address by 1 and to shift the cursor to the right at the time of write to the DD/CGRAM; display is not shifted
6	'write data' to CGRAM/DDRAM 1 0 0 1 0 1 1 0 0 0 0 0	P_	writes 'P'; the DDRAM has already been selected by initialization at power-on; the cursor is incremented by 1 and shifted to the right

Table 13 8-bit operation, 1-line display example; using external reset (character set 'A')

STEP	INSTRUCTION	DISPLAY	OPERATION
1	power supply on (PCF2119x is initialized by the external reset)		initialized; no display appears
2	function set RS R/$\overline{W}$ DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 1 1 0 0 0 0		sets to 8-bit operation, selects 1-line display and $V_{LCD} = V_0$
3	display mode on/off control 0 0 0 0 0 0 1 1 1 0	_	turns on display and cursor; entire display is blank after initialization
4	entry mode set 0 0 0 0 0 0 0 1 1 0	_	sets mode to increment the address by 1 and to shift the cursor to the right at the time of the write to the DD/CGRAM; display is not shifted
5	'write data' to CGRAM/DDRAM 1 0 0 1 0 1 0 0 0 0	**P_**	writes 'P'; the DDRAM has already been selected by initialization at power-on; the cursor is incremented by 1 and shifted to the right
6	'write data' to CGRAM/DDRAM 1 0 0 1 0 0 1 0 0 0	**PH_**	writes 'H'
7 to 11			
12	'write data' to CGRAM/DDRAM 1 0 0 1 0 1 0 0 1 1	**PHILIPS_**	writes 'S'
13	entry mode set 0 0 0 0 0 0 0 1 1 1	**PHILIPS_**	sets mode for display shift at the time of write
14	'write data' to CGRAM/DDRAM 1 0 0 0 1 0 0 0 0 0	**HILIPS _**	writes space
15	'write data' to CGRAM/DDRAM 1 0 0 1 0 0 1 1 0 1	**ILIPS M_**	writes 'M'
16			

STEP	INSTRUCTION										DISPLAY	OPERATION
17	'write data' to CGRAM/DDRAM											
	1	0	0	1	0	0	1	1	1	1	**MICROKO_**	writes 'O'
18	cursor/display shift											
	0	0	0	0	0	1	0	0	0	0	**MICROKO**	shifts only the cursor position to the left
19	cursor/display shift											
	0	0	0	0	0	1	0	0	0	0	**MICROKO**	shifts only the cursor position to the left
20	'write data' to CGRAM/DDRAM											
	1	0	0	1	0	0	0	0	1	1	**ICROCO**	writes 'C' correction; the display moves to the left
21	cursor/display shift											
	0	0	0	0	0	1	1	1	0	0	**MICROCO**	shifts the display and cursor to the right
22	cursor/display shift											
	0	0	0	0	0	1	0	1	0	0	**MICROCO_**	shifts only the cursor to the right
23	'write data' to CGRAM/DDRAM											
	1	0	0	1	0	0	1	1	0	1	**ICROCOM_**	writes 'M'
24												
25	return home											
	0	0	0	0	0	0	0	0	1	0	**PHILIPS M**	returns both display and cursor to the original position (address 0)

Table 14 8-bit operation, 1-line display and icon example; using external reset (character set 'A')

STEP	INTRODUCTION	DISPLAY	OPERATION
1	power supply on (PCF2119x is initialized by the external reset)		initialized; no display appears
2	function set RS R/$\overline{W}$ DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 1 1 0 0 0 0		sets to 8-bit operation, selects 1-line display and $V_{LCD} = V_0$
3	display mode on/off control 0 0 0 0 0 0 1 1 1 0	_	turns on display and cursor; entire display is blank after initialization
4	entry mode set 0 0 0 0 0 0 0 1 1 0	_	sets mode to increment the address by 1 and to shift the cursor to the right at the time of the write to the DD/CGRAM; display is not shifted
5	set CGRAM address 0 0 0 1 0 0 0 0 0 0	_	sets the CGRAM address to position of character 0; the CGRAM is selected
6	'write data' to CGRAM/DDRAM 1 0 0 0 0 0 1 0 1 0	_	writes data to CGRAM for icon even phase; icons appears
7			
8	set CGRAM address 0 0 0 1 1 1 0 0 0 0	_	sets the CGRAM address to position of character 4; the CGRAM is selected
9	'write data' to CGRAM/DDRAM 1 0 0 0 0 0 1 0 1 0	_	writes data to CGRAM for icon odd phase
10			
11	function set 0 0 0 0 1 1 0 0 0 1	_	sets H = 1
12	icon control 0 0 0 0 0 0 1 0 1 0	_	icons blink
13	function set 0 0 0 0 1 1 0 0 0 1	_	sets H = 0

STEP	INTRODUCTION	DISPLAY	OPERATION
14	set DDRAM address 0 0 1 0 0 0 0 0 0 0		sets the DDRAM address to the first position; DDRAM is selected
15	'write data' to CGRAM/DDRAM 1 0 0 1 0 1 0 0 0 0	**P_**	writes 'P'; the cursor is incremented by 1 and shifted to the right
16	'write data' to CGRAM/DDRAM 1 0 0 1 0 0 1 0 0 0	**PH_**	writes 'H'
17 to 20			
21	return home 0 0 0 0 0 0 0 0 1 0	**PHILIPS**	returns both display and cursor to the original position (address 0)

Table 15 8-bit operation, 2-line display example; using external reset

STEP	INTRODUCTION	DISPLAY	OPERATION
1	power supply on (PCF2119x is initialized by the external reset)		initialized; no display appears
2	function set RS R/$\overline{W}$ DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 1 1 1 0 0 0		sets to 8-bit operation; selects 2-line display and voltage generator off
3	display on/off control 0 0 0 0 0 0 1 1 1 0	_	turns on display and cursor; entire display is blank after initialization
4	entry mode set 0 0 0 0 0 0 0 1 1 0	_	sets mode to increment the address by 1 and to shift the cursor to the right at the time of write to the CG/DDRAM; display is not shifted
5	'write data' to CGRAM/DDRAM 1 0 0 1 0 1 0 0 0 0	**P**_	writes 'P'; the DDRAM has already been selected by initialization at power-on; the cursor is incremented by 1 and shifted to the right
6 to 10			
11	'write data' to CGRAM/DDRAM 1 0 0 1 0 1 0 0 1 1	**PHILIPS**_	writes 'S'
12	set DDRAM address 0 0 1 1 0 0 0 0 0 0	**PHILIPS** _	sets DDRAM address to position the cursor at the head of the 2nd line
13	'write data' to CGRAM/ DDRAM 1 0 0 1 0 0 1 1 0 1	**PHILIPS** **M**_	writes 'M'
14 to 19			

STEP	INTRODUCTION	DISPLAY	OPERATION
20	'write data' to CGRAM/DDRAM 1 0 0 1 0 0 1 1 1 1	**PHILIPS MICROCO_**	writes 'O'
21	'write data' to CGRAM/DDRAM 0 0 0 0 0 0 0 1 1 1	**PHILIPS MICROCO_**	sets mode for display shift at the time of write
22	'write data' to CGRAM/DDRAM 1 0 0 1 0 0 1 1 0 1	**HILIPS ICROCOM_**	writes 'M'; display is shifted to the left; the first and second lines shift together
23			
24	return home 0 0 0 0 0 0 0 0 1 0	**PHILIPS MICROCOM**	returns both display and cursor to the original position (address 0)

Table 16 Example of I²C-bus operation; 1-line display (using external reset, assuming SA0 = V_{SS}; note 1)

STEP	I²C BYTE	DISPLAY	OPERATION
1	I²C-bus start		initialized; no display appears
2	slave address for write SA6 SA5 SA4 SA3 SA2 SA1 SA0 R/$\overline{W}$ Ack 0 1 1 1 0 1 0 0 1		during the acknowledge cycle SDA will be pulled-down by the PCF2119x
3	send a control byte for 'function set' Co RS 0 0 0 0 0 0 Ack 0 0 0 0 0 0 0 0 1		control byte sets RS for following data bytes
4	function set DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 0 1 X 0 0 0 0 1		selects 1-line display and $V_{LCD} = V_0$; SCL pulse during acknowledge cycle starts execution of instruction
5	display on/off control DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 0 0 0 1 1 1 0 1	_	turns on display and cursor; entire display shows character 20H (blank in ASCII-like character sets)
6	entry mode set DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 0 0 0 0 1 1 0 1	_	sets mode to increment the address by 1 and to shift the cursor to the right at the time of write to the DDRAM or CGRAM; display is not shifted
7	I²C start	_	for writing data to DDRAM, RS must be set to 1; therefore a control byte is needed
8	slave address for write SA6 SA5 SA4 SA3 SA2 SA1 SA0 R/$\overline{W}$ Ack 0 1 1 1 0 1 0 0 1	_	
9	send a control byte for 'write data' Co RS 0 0 0 0 0 0 Ack 0 1 0 0 0 0 0 0 1	_	
10	'write data' to DDRAM DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 1 0 1 0 0 0 0 1	**P**_	writes 'P'; the DDRAM has been selected at power-up; the cursor is incremented by 1 and shifted to the right
11	'write data' to DDRAM DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 1 0 0 1 0 0 0 1	**PH**_	writes 'H'

STEP	I²C BYTE	DISPLAY	OPERATION
12 to 15			
16	'write data' to DDRAM DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 1 0 1 0 0 1 1 1	**PHILIPS_**	writes 'S'
17	(optional I²C stop) I²C start + slave address for write (as step 8)	**PHILIPS_**	
18	control byte Co RS 0 0 0 0 0 0 Ack 1 0 0 0 0 0 0 0 1	**PHILIPS_**	
19	return home DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 0 0 0 0 0 1 0 1	**PHILIPS**	sets DDRAM address 0 in address counter (also returns shifted display to original position; DDRAM contents unchanged); this instruction does not update the Data Register (DR)
20	I²C start	**PHILIPS**	
21	slave address for read SA6 SA5 SA4 SA3 SA2 SA1 SA0 R/$\overline{W}$ Ack 0 1 1 1 0 1 0 1 1	**PHILIPS**	during the acknowledge cycle the content of the DR is loaded into the internal I²C-bus interface to be shifted out; in the previous instruction neither a 'set address' nor a 'read data' has been performed; therefore the content of the DR was unknown; the R/W has to be set to 1 while still in I²C-write mode
22	control byte for read Co RS 0 0 0 0 0 0 Ack 0 1 1 0 0 0 0 0 1	**PHILIPS**	DDRAM content will be read from following instructions
23	'read data': 8 × SCL + master acknowledge; note 2 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack X X X X X X X X 0	**PHILIPS**	8 × SCL; content loaded into interface during previous acknowledge cycle is shifted out over SDA; MSB is DB7; during master acknowledge content of DDRAM address 01 is loaded into the I²C-bus interface

STEP	I²C BYTE	DISPLAY	OPERATION
24	'read data': 8 × SCL + master acknowledge; note 2 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 1 0 0 1 0 0 0 0	**PHILIPS**	8 × SCL; code of letter 'H' is read first; during master acknowledge code of 'I' is loaded into the I²C interface
25	'read data': 8 × SCL + no master acknowledge; note 2 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 1 0 0 1 0 0 1 1	**PHILIPS**	no master acknowledge; after the content of the I²C-bus interface register is shifted out no internal action is performed; no new data is loaded to the interface register, data register is not updated, address counter is not incremented and cursor is not shifted
26	I²C stop	**PHILIPS**	

Notes

1. X = don't care.
2. SDA is left at high-impedance by the microcontroller during the read acknowledge.

Table 17 Initialization by instruction, 8-bit interface (note 1)

STEP										DESCRIPTION
power-on or unknown state										
					↓					
wait 2 ms after external reset has been applied										
					↓					
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	BF cannot be checked before this instruction
0	0	0	0	1	1	X	X	X	X	function set (interface is 8 bits long)
					↓					
wait 2 ms										
					↓					
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	BF cannot be checked before this instruction
0	0	0	0	1	1	X	X	X	X	function set (interface is 8 bits long)
					↓					
wait more than 40 μs										
					↓					
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	BF cannot be checked before this instruction
0	0	0	0	1	1	X	X	X	X	function set (interface is 8 bits long)
					↓					BF can be checked after the following instructions; when BF is not checked, the waiting time between instructions is the specified instruction time (see Table 3)
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	function set (interface is 8 bits long); specify the number of display lines
0	0	0	0	1	1	0	M	0	H	
0	0	0	0	0	0	1	0	0	0	display off
0	0	0	0	0	0	0	0	0	1	clear display
0	0	0	0	0	0	0	1	I/D	S	entry mode set
					↓					
Initialization ends										

Note

1. X = don't care.

Table 18 Initialization by instruction, 4-bit interface; not applicable for I²C-bus operation

STEP						DESCRIPTION
power-on or unknown state						
Wait 2 ms after external reset has been applied						
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	BF cannot be checked before this instruction
0	0	0	0	1	1	function set (interface is 8 bits long)
Wait 2 ms						
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	BF cannot be checked before this instruction
0	0	0	0	1	1	function set (interface is 8 bits long)
Wait 40 μs						
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	BF cannot be checked before this instruction
0	0	0	0	1	1	function set (interface is 8 bits long)
						BF can be checked after the following instructions; when BF is not checked, the waiting time between instructions is the specified instruction time (see Table 3)
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	function set (set interface to 4 bits long)
0	0	0	0	1	0	interface is 8 bits long
0	0	0	0	1	0	function set (interface is 4 bits long)
0	0	0	M	0	H	specify number of display lines
0	0	0	0	0	0	
0	0	1	0	0	0	display off
0	0	0	0	0	0	clear display
0	0	0	0	0	1	
0	0	0	0	0	0	entry mode set
0	0	0	1	I/D	S	
Initialization ends						

17 BONDING PAD LOCATIONS

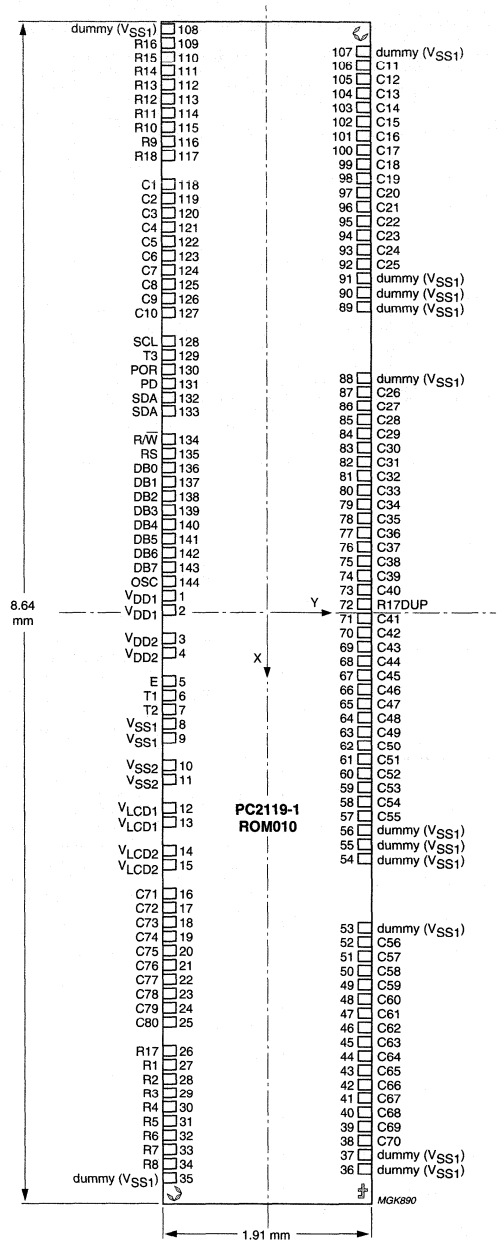


Fig.32 Bonding pad locations.

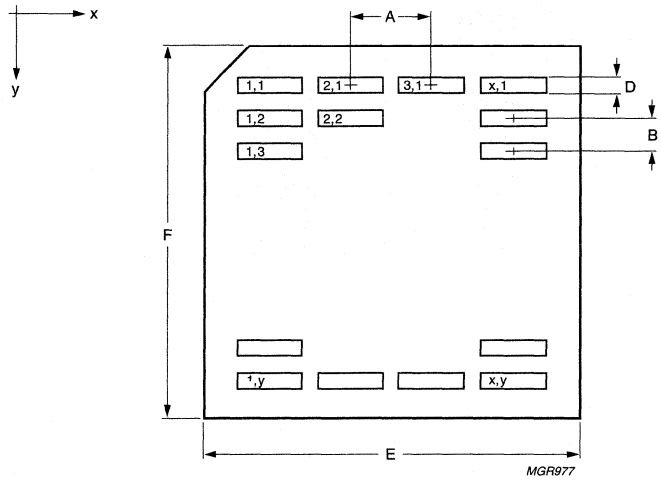
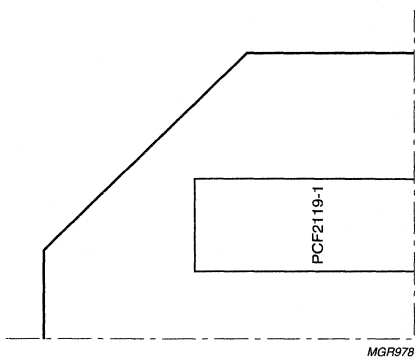


Fig.33 Tray details.



The orientation of the IC in a pocket is indicated by the position of the IC type name on the die surface with respect to the chamfer on the upper left corner of the tray. Refer to the bonding pad location diagram for the orientating and position of the type name on the die surface.

Fig.34 Tray alignment.

Table 19 Dimensions for Fig.33

DIM.	DESCRIPTION	VALUE
A	pocket pitch, x direction	10.89 mm
B	pocket pitch, y direction	4.34 mm
C	pocket width, x direction	8.74 mm
D	pocket width, y direction	2.01 mm
E	tray width, x direction	50.67 mm
F	tray width, y direction	50.67 mm
x	number of pockets in x direction	4
y	number of pockets in y direction	10

Table 20 Bonding pad locations
Dimensions in μm; all x/y coordinates are referenced to centre of chip; see Fig.32

SYMBOL	PAD	x	y
V_{DD1}	1	−117	−779
V_{DD1}	2	−16	−779
V_{DD2}	3	+185	−779
V_{DD2}	4	+286	−779
E	5	+486	−779
T1	6	+587	−779
T2	7	+688	−779
V_{SS1}	8	+789	−779
V_{SS1}	9	+889	−779
V_{SS2}	10	+1090	−779
V_{SS2}	11	+1191	−779
V_{LCD1}	12	+1393	−779
V_{LCD1}	13	+1493	−779
V_{LCD2}	14	+1695	−779
V_{LCD2}	15	+1795	−779
C71	16	+1996	−779
C72	17	+2097	−779
C73	18	+2198	−779
C74	19	+2298	−779
C75	20	+2399	−779
C76	21	+2499	−779
C77	22	+2600	−779
C78	23	+2701	−779
C79	24	+2801	−779
C80	25	+2902	−779
R17	26	+3103	−779
R1	27	+3204	−779
R2	28	+3304	−779
R3	29	+3405	−779
R4	30	+3505	−779
R5	31	+3606	−779
R6	32	+3707	−779
R7	33	+3807	−779
R8	34	+3908	−779
Dummy (V_{SS1})	35	+4008	−779
Dummy (V_{SS1})	36	3957	779
Dummy (V_{SS1})	37	3856	779
C70	38	3756	779
C69	39	3655	779
C68	40	3555	779
C67	41	3454	779
C66	42	3353	779
C65	43	3253	779
C64	44	3152	779
C63	45	3052	779
C62	46	2951	779
C61	47	2850	779
C60	48	2750	779
C59	49	2649	779
C58	50	2549	779
C57	51	2448	779
C56	52	2347	779
Dummy (V_{SS1})	53	2247	779
Dummy (V_{SS1})	54	1744	779
Dummy (V_{SS1})	55	1643	779
Dummy (V_{SS1})	56	1543	779
C55	57	1442	779
C54	58	1341	779
C53	59	1241	779
C52	60	1140	779
C51	61	1040	779
C50	62	939	779
C49	63	838	779
C48	64	738	779
C47	65	637	779
C46	66	537	779
C45	67	436	779
C44	68	335	779
C43	69	235	779
C42	70	134	779
C41	71	34	779
R17DUP	72	−67	+779
C40	73	−168	+779
C39	74	−268	+779
C38	75	−369	+779
C37	76	−469	+779
C36	77	−570	+779
C35	78	−671	+779
C34	79	−771	+779
C33	80	−872	+779
C32	81	−972	+779
C31	82	−1073	+779

SYMBOL	PAD	x	y
C30	83	−1174	+779
C29	84	−1274	+779
C28	85	−1375	+779
C27	86	−1475	+779
C26	87	−1576	+779
Dummy (V_{SS1})	88	−1677	+779
Dummy (V_{SS1})	89	−2180	+779
Dummy (V_{SS1})	90	−2280	+779
Dummy (V_{SS1})	91	−2381	+779
C25	92	−2481	+779
C24	93	−2582	+779
C23	94	−2683	+779
C22	95	−2783	+779
C21	96	−2884	+779
C20	97	−2984	+779
C19	98	−3085	+779
C18	99	−3186	+779
C17	100	−3286	+779
C16	101	−3387	+779
C15	102	−3487	+779
C14	103	−3588	+779
C13	104	−3689	+779
C12	105	−3789	+779
C11	106	−3890	+779
Dummy (V_{SS1})	107	−3990	+779
Dummy (V_{SS1})	108	−4141	−779
R16	109	−4041	−779
R15	110	−3940	−779
R14	111	−3840	−779
R13	112	−3739	−779
R12	113	−3638	−779
R11	114	−3538	−779
R10	115	−3437	−779
R9	116	−3337	−779
R18	117	−3236	−779
C1	118	−3035	−779
C2	119	−2934	−779
C3	120	−2834	−779
C4	121	−2733	−779
C5	122	−2633	−779
C6	123	−2532	−779
C7	124	−2431	−779
C8	125	−2331	−779
C9	126	−2230	−779
C10	127	−2129	−779
SCL	128	−1928	−779
T3	129	−1827	−779
POR	130	−1726	−779
PD	131	−1626	−779
SDA	132	−1525	−779
SDA	133	−1425	−779
R/$\overline{W}$	134	−1223	−779
RS	135	−1123	−779
DB0/SA0	136	−1022	−779
DB1	137	−922	−779
DB2	138	−821	−779
DB3	139	−720	−779
DB4	140	−620	−779
DB5	141	−519	−779
DB6	142	−419	−779
DB7	143	−318	−779
OSC	144	−217	−779
Rec. Pat. C1	−	+4125	−762
Rec. Pat. C2	−	−4125	+762
Rec. Pat. +	−	4095	762

Table 21 Bump size

PARAMETER	VALUE	UNIT
Type	galvanic pure Au	−
Bump width	70 ±6	µm
Bump length	90 ±6	µm
Bump height	17.5 ±5	µm
Height difference in one die	<2	µm
Convex deformation	<5	µm
Pad size, aluminium	85 × 100	µm
Passivation opening CBB	58 × 78	µm
Wafer thickness	380 ±25	µm

CONTENTS

1 FEATURES

- Supply voltage 2.25 to 6.0 V
- Low current consumption
- Serial data input
- CBUS control
- One-point built-in oscillator
- Stand-alone or expanded system
- Power-on reset clear
- LCD segments
  - 40 (PCF2100C)
  - 64 (PCF2111C)
  - 32 (PCF2112C)
- Multiplex rate
  - 1 : 2 (PCF2100C)
  - 1 : 2 (PCF2111C)
  - 1 : 1 (PCF2112C)
- Word length
  - 22 bits (PCF2100C)
  - 34 bits (PCF2111C)
  - 34 bits (PCF2112C).

2 GENERAL DESCRIPTION

The PCF21xxC family are single-chip, silicon gate CMOS LCD driver circuits. A 3-line bus (CBUS) structure enables serial data transfer with microcontrollers. All inputs are CMOS/NMOS compatible.

The devices have the same function and performance as those of the PCF21xx family, which they supersede. The maximum operating voltage required is reduced from 6.5 to 6.0 V.

3 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		2.25	–	6.0	V
I_{DD1}	supply current 1	outputs open; CBUS inactive	–	20	50	µA
I_{DD2}	supply current 2	outputs open; CBUS inactive; T_{amb} = 25 °C	–	20	30	µA
P_O	power dissipation per output		–	–	100	mW
T_{amb}	operating ambient temperature		–40	–	+85	°C
T_{stg}	storage temperature		–65	–	+150	°C

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF2100CP	DIP28	plastic dual in-line package; 28 leads (600 mil)	SOT117-1
PCF2100CT	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1
PCF2111CP	DIP40	plastic dual in-line package; 40 leads (600 mil)	SOT129-1
PCF2111CT	VSO40	plastic very small outline package; 40 leads	SOT158-1
PCF2112CP	DIP40	plastic dual in-line package; 40 leads (600 mil)	SOT129-1
PCF2112CT	VSO40	plastic very small outline package; 40 leads	SOT158-1

5 BLOCK DIAGRAMS

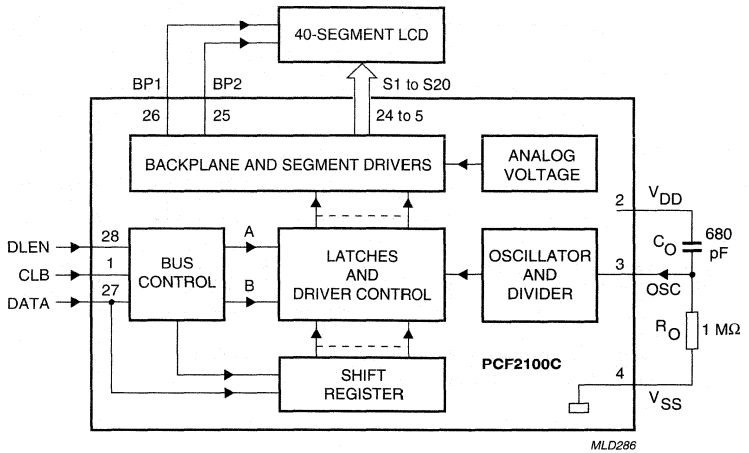


Fig.1 Block diagram; PCF2100C.

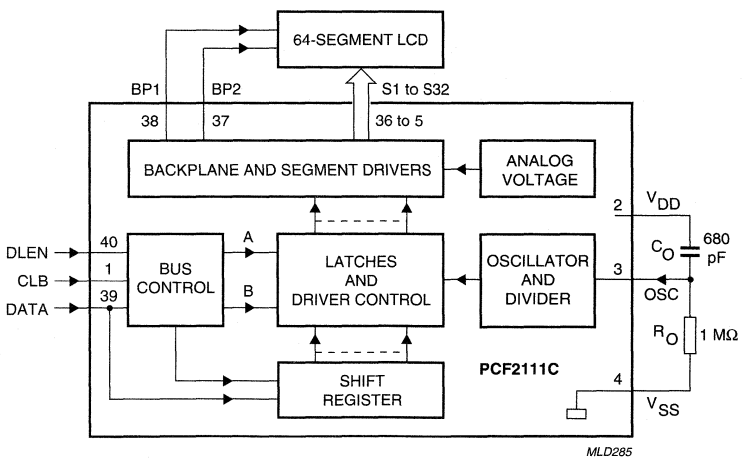


Fig.2 Block diagram; PCF2111C.

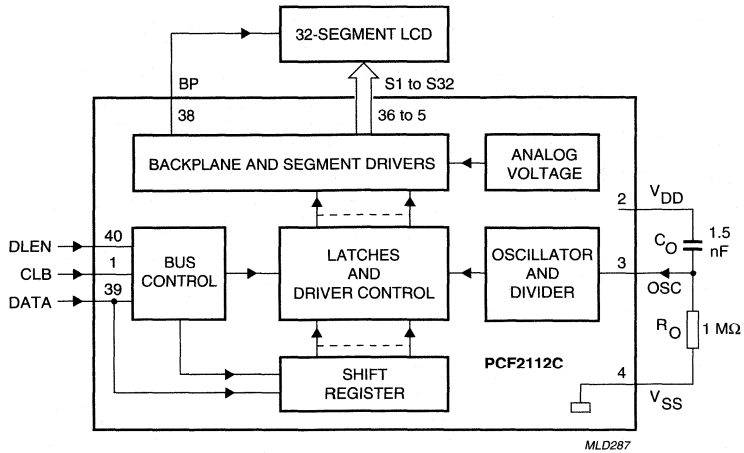


Fig.3 Block diagram; PCF2112C.

6 PINNING

6.1 PCF2100C

SYMBOL	PIN	DESCRIPTION
CLB	1	clock burst input (CBUS)
V_{DD}	2	supply voltage
OSC	3	oscillator input
V_{SS}	4	supply voltage ground
S20	5	LCD driver output 20
S19	6	LCD driver output 19
S18	7	LCD driver output 18
S17	8	LCD driver output 17
S16	9	LCD driver output 16
S15	10	LCD driver output 15
S14	11	LCD driver output 14
S13	12	LCD driver output 13
S12	13	LCD driver output 12
S11	14	LCD driver output 11
S10	15	LCD driver output 10
S9	16	LCD driver output 9
S8	17	LCD driver output 8
S7	18	LCD driver output 7
S6	19	LCD driver output 6
S5	20	LCD driver output 5
S4	21	LCD driver output 4
S3	22	LCD driver output 3
S2	23	LCD driver output 2
S1	24	LCD driver output 1
BP2	25	backplane driver output 2
BP1	26	backplane driver output 1
DATA	27	data input line (CBUS)
DLEN	28	data input line enable (CBUS)

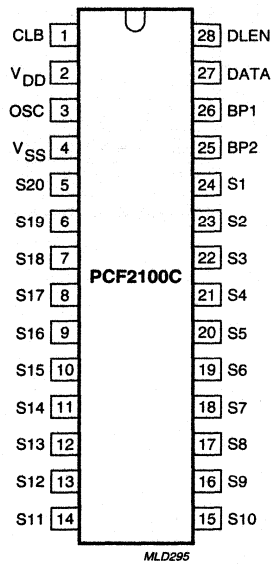


Fig.4 Pin configuration; SOT117-1 and SOT136-1.

6.2 PCF2111C

SYMBOL	PIN	DESCRIPTION
CLB	1	clock burst input (CBUS)
V_{DD}	2	supply voltage
OSC	3	oscillator input
V_{SS}	4	supply voltage ground
S32	5	LCD driver output 32
S31	6	LCD driver output 31
S30	7	LCD driver output 30
S29	8	LCD driver output 29
S28	9	LCD driver output 28
S27	10	LCD driver output 27
S26	11	LCD driver output 26
S25	12	LCD driver output 25
S24	13	LCD driver output 24
S23	14	LCD driver output 23
S22	15	LCD driver output 22
S21	16	LCD driver output 21
S20	17	LCD driver output 20
S19	18	LCD driver output 19
S18	19	LCD driver output 18
S17	20	LCD driver output 17
S16	21	LCD driver output 16
S15	22	LCD driver output 15
S14	23	LCD driver output 14
S13	24	LCD driver output 13
S12	25	LCD driver output 12
S11	26	LCD driver output 11
S10	27	LCD driver output 10
S9	28	LCD driver output 9
S8	29	LCD driver output 8
S7	30	LCD driver output 7
S6	31	LCD driver output 6
S5	32	LCD driver output 5
S4	33	LCD driver output 4
S3	34	LCD driver output 3
S2	35	LCD driver output 2
S1	36	LCD driver output 1
BP2	37	backplane driver output 2
BP1	38	backplane driver output 1
DATA	39	data input line (CBUS)
DLEN	40	data input line enable (CBUS)

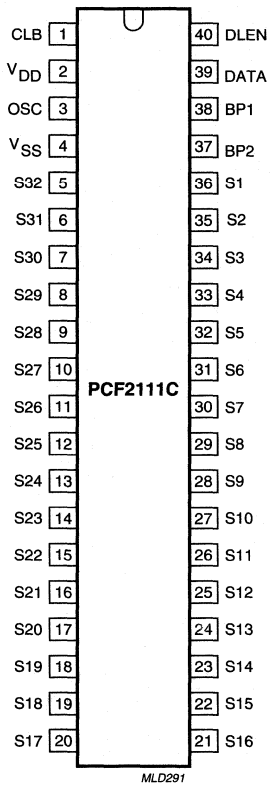


Fig.5 Pin configuration; SOT129-1 and SOT158-1.

6.3 PCF2112C

SYMBOL	PIN	DESCRIPTION
CLB	1	clock burst input (CBUS)
V_{DD}	2	supply voltage
OSC	3	oscillator input
V_{SS}	4	supply voltage ground
S32	5	LCD driver output 32
S31	6	LCD driver output 31
S30	7	LCD driver output 30
S29	8	LCD driver output 29
S28	9	LCD driver output 28
S27	10	LCD driver output 27
S26	11	LCD driver output 26
S25	12	LCD driver output 25
S24	13	LCD driver output 24
S23	14	LCD driver output 23
S22	15	LCD driver output 22
S21	16	LCD driver output 21
S20	17	LCD driver output 20
S19	18	LCD driver output 19
S18	19	LCD driver output 18
S17	20	LCD driver output 17
S16	21	LCD driver output 16
S15	22	LCD driver output 15
S14	23	LCD driver output 14
S13	24	LCD driver output 13
S12	25	LCD driver output 12
S11	26	LCD driver output 11
S10	27	LCD driver output 10
S9	28	LCD driver output 9
S8	29	LCD driver output 8
S7	30	LCD driver output 7
S6	31	LCD driver output 6
S5	32	LCD driver output 5
S4	33	LCD driver output 4
S3	34	LCD driver output 3
S2	35	LCD driver output 2
S1	36	LCD driver output 1
n.c.	37	not connected
BP	38	backplane driver output
DATA	39	data input line (CBUS)
DLEN	40	data input line enable (CBUS)

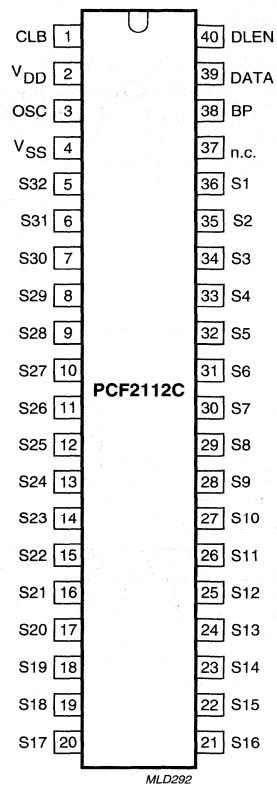


Fig.6 Pin configuration; SOT129-1 and SOT158-1.

7 FUNCTIONAL DESCRIPTION

An LCD segment or LED output is activated when the corresponding DATA bit is HIGH.

7.1 PCF2100C

When DATA bit 21 is HIGH, the A-latches (BP1) are loaded. With DATA bit 21 LOW, the B-latches (BP2) are loaded. CLB pulse 23 transfers data from the shift register to the selected latches.

7.2 PCF2111C

When DATA bit 33 is HIGH, the A-latches (BP1) are loaded. With DATA bit 33 LOW, the B-latches (BP2) are loaded. CLB pulse 35 transfers data from the shift register to the selected latches.

7.3 PCF2112C

When DATA bit 33 is HIGH, the latches are loaded. CLB pulse 35 transfers data from the shift register to the selected latches.

7.4 Bus control logic

The following tests are carried out by the bus control logic:

1. Test on leading zero
2. Test on number of DATA bits
3. Test of disturbed DLEN and DATA signals during transmission.

If one of the test conditions is not fulfilled, no action follows the load condition (load pulse with DLEN LOW) and the driver is ready to receive new data.

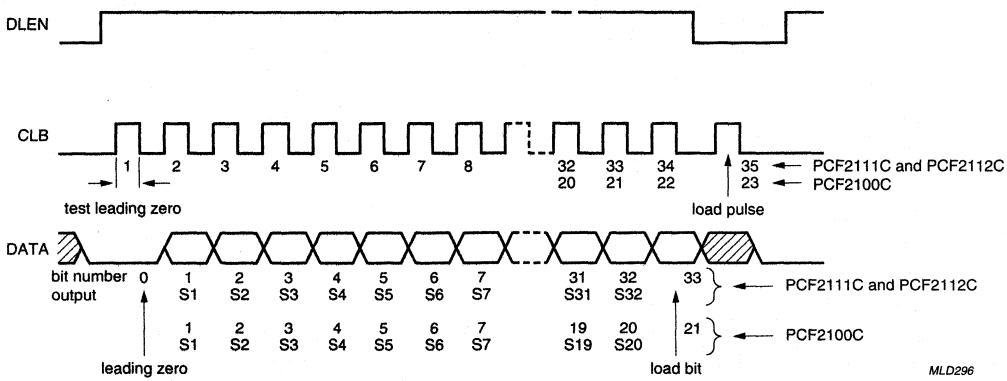


Fig.7 CBUS data format.

7.5 Timing

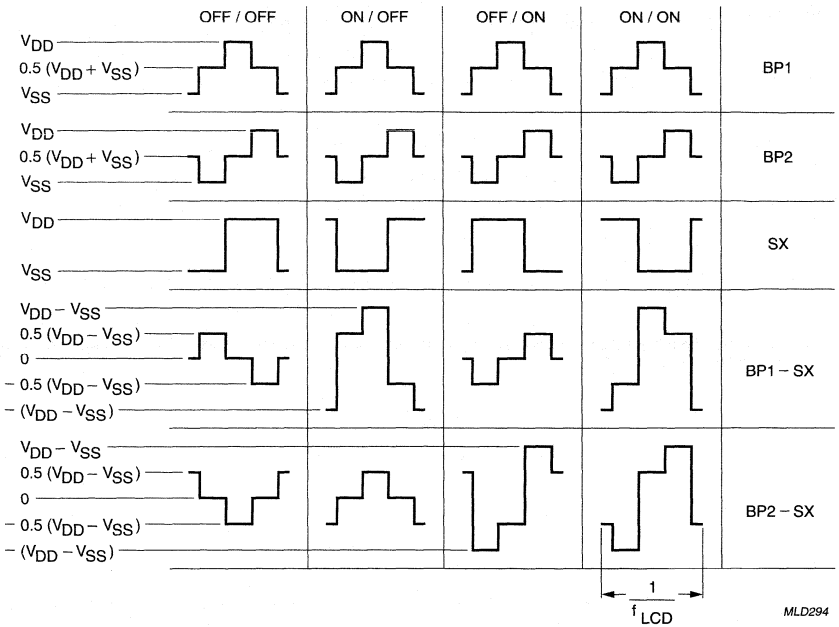


Fig.8 Timing diagram for PCF2100C and PCF2111C.

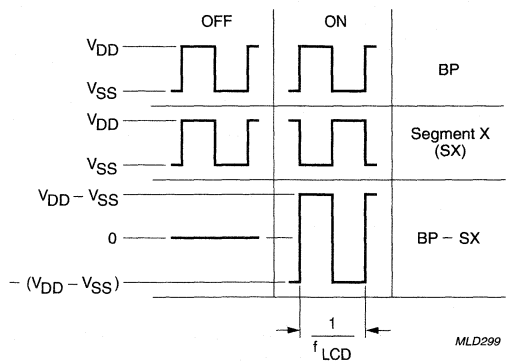
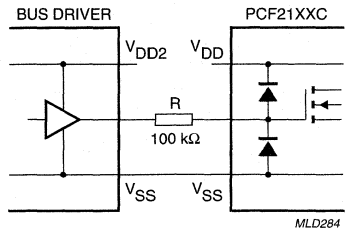


Fig.9 Timing diagram for PCF2112C.

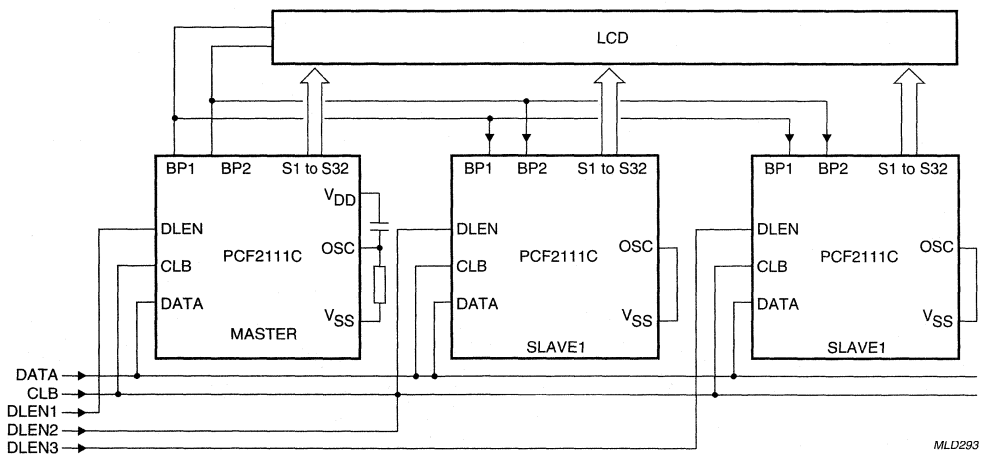
7.6 Input circuitry



V_{SS} line is common. In systems where it is expected that $V_{DD2} > V_{DD1} + 0.5$ V, a resistor should be inserted to reduce the current flowing through the input protection. Maximum input current ≤40 μA.

Fig.10 Input circuitry.

7.7 Expansion



By connecting OSC to V_{SS} the BP pins become inputs and generate signals synchronized to the single oscillator frequency, thus allowing expansion of several members of the PCF21xxC family up to the BP drive capability of the master. The PCF2112C can only function as a master for other PCF2112Cs.

Fig.11 Expansion possibility (using PCF2111C).

8 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		−0.5	+8.0	V
V_I	input voltage DLEN, CLB, DATA and OSC		V_{SS} − 0.5	V_{DD} + 0.5	V
V_O	output voltage BP1, BP2 and S1 to S32		V_{SS} − 0.5	V_{DD} + 0.5	V
I_{DD}, I_{SS}	supply current		−50	+50	mA
I_I	DC input current		−20	+20	mA
I_O	DC output current		−25	+25	mA
P_{tot}	total power dissipation per package	note 1	−	500	mW
P_O	power dissipation per output		−	100	mW
T_{stg}	storage temperature		−65	+150	°C

Note

1. Derate by 7.7 mW/K when T_{amb} > 60 °C.

9 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices. See *"Handling MOS devices"*.

ESD in accordance with *"MIL STD 883C, Method 3015"*.

10 DC CHARACTERISTICS

V_{DD} = 2.25 to 6.0 V; V_{SS} = 0 V; T_{amb} = −40 to +80 °C; R_O = 1 MΩ; C_O = 680 pF; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		2.25	–	6.0	V
I_{DD}	supply current	note 1; see Fig.13	–	20	50	μA
		note 1; T_{amb} = 25 °C; see Fig.13	–	20	30	μA
V_{POR}	power-on reset voltage level	note 2	–	1.0	1.6	V
Inputs CLB, DATA and DLEN						
V_{IL}	LOW level input voltage		–	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	–	V
I_{LI}	input leakage current	$V_I = V_{SS}$ or V_{DD}	–	–	±1	μA
C_i	input capacitance	note 3	–	–	10	pF
Input OSC						
I_{osc}	oscillator start-up current	$V_I = V_{SS}$	0.5	1.2	5.0	μA
LCD outputs						
V_{BP}	DC voltage of backplane drivers		–	±20	–	mV
$Z_{O(BP)}$	backplane driver output impedance	note 4; V_{DD} = 5 V	–	0.5	5.0	kΩ
$Z_{O(S)}$	segment driver output impedance	note 4; V_{DD} = 5 V	–	1	7	kΩ

Notes

1. Outputs open; CBUS inactive.
2. Resets all logic, when $V_{DD} < V_{POR}$.
3. Periodically sampled (not 100% tested).
4. Outputs measured one at a time.

11 AC CHARACTERISTICS

V_{DD} = 2.25 to 6.0 V; V_{SS} = 0 V; T_{amb} = −40 to +80 °C; R_O = 1 MΩ; C_O = 680 pF; all timing values are referenced to V_{IH} and V_{IL} levels with an input voltage swing of V_{SS} to V_{DD}; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Inputs CLB, DATA and DLEN (see Fig.12)						
t_{SUDA}	data set-up time		3	–	–	µs
t_{HDDA}	data hold time		3	–	–	µs
t_{SUEN}	enable set-up time		1	–	–	µs
t_{SUDI}	disable set-up time		2	–	–	µs
t_{SULD}	load pulse set-up time		2.5	–	–	µs
t_{BUSY}	busy time		3	–	–	µs
t_{WH}	CLB HIGH time		1	–	–	µs
t_{WL}	CLB LOW time		5	–	–	µs
t_{CLB}	CLB cycle time		10	–	–	µs
t_r	rise time		–	–	10	µs
t_f	fall time		–	–	10	µs
LCD timing (see Figs. 12, 14, 15, 16 and 17)						
f_{LCD}	LCD frame frequency					
	PCF2100C, PCF2111C		60	75	100	Hz
	PCF2112C	C_O = 1.5 nF	30	35	50	Hz
t_{BS}	transfer time with test loads	V_{DD} = 5 V	–	20	100	µs
t_{PLCD}	driver delay time with test loads	V_{DD} = 5 V	–	20	100	µs

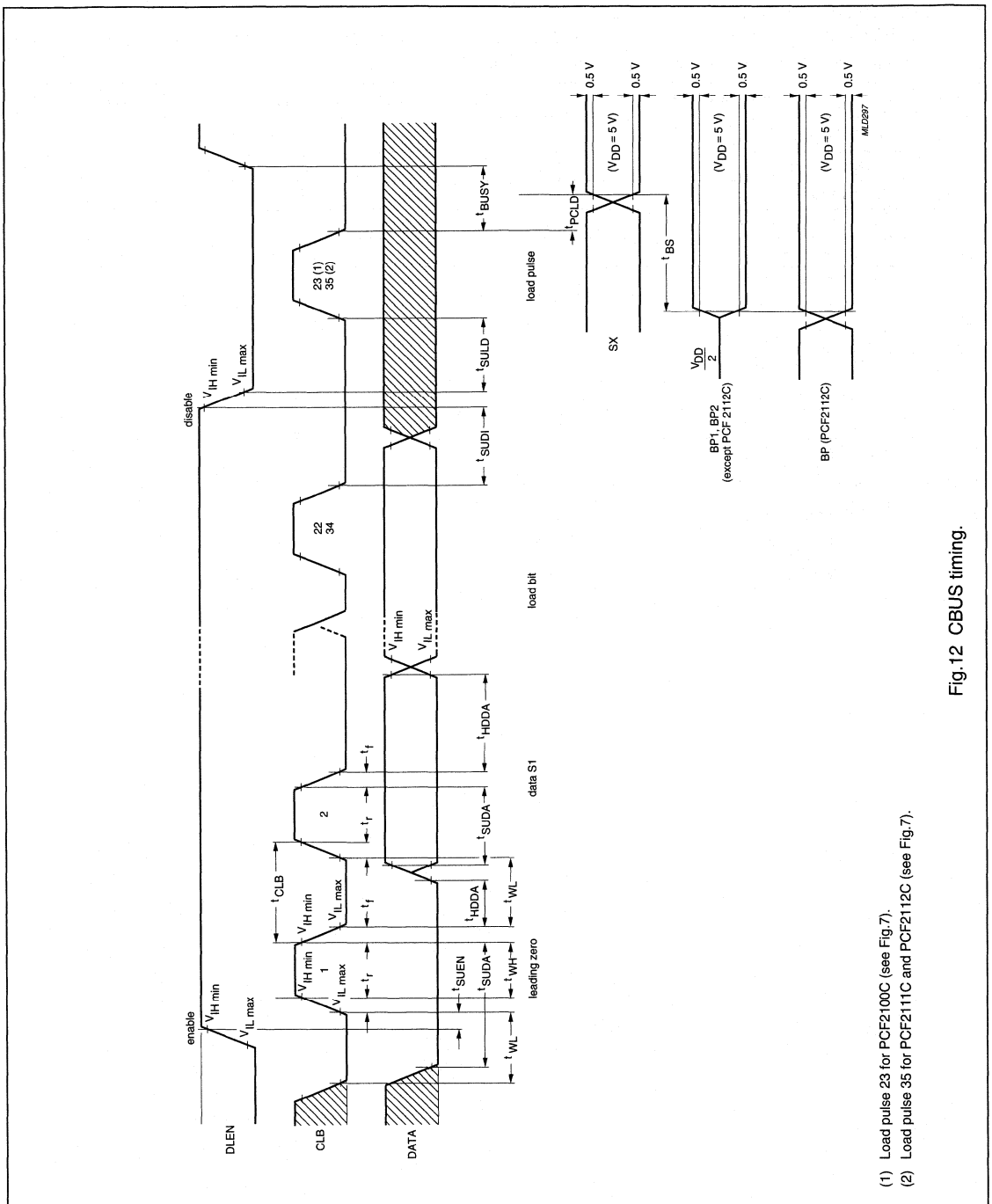
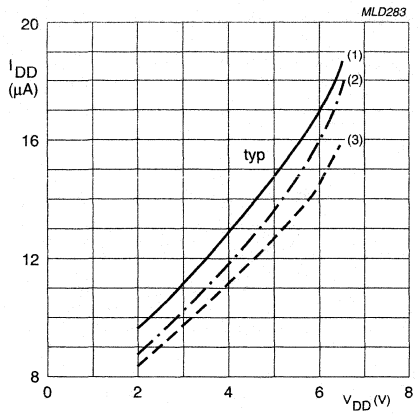


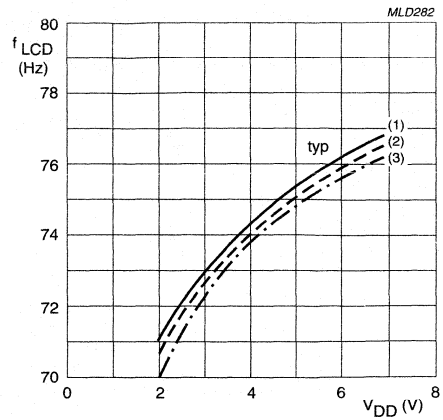
Fig.12 CBUS timing.

(1) Load pulse 23 for PCF2100C (see Fig.7).
(2) Load pulse 35 for PCF2111C and PCF2112C (see Fig.7).



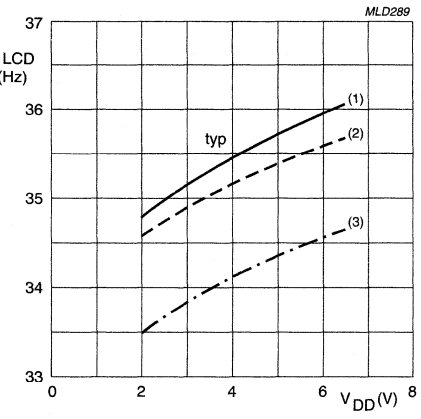
(1) T_{amb} = −40 °C.
(2) T_{amb} = +85 °C.
(3) T_{amb} = +25 °C.

Fig.13 Supply current as a function of supply voltage.



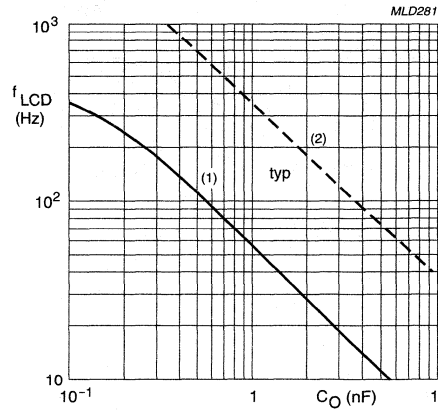
(1) T_{amb} = −40 °C.
(2) T_{amb} = +25 °C.
(3) T_{amb} = +85 °C.

Fig.14 Display frequency as a function of supply voltage; C_O = 680 pF (except PCF2112C).



(1) T_{amb} = −40 °C.
(2) T_{amb} = +25 °C.
(3) T_{amb} = +85 °C.

Fig.15 Display frequency as a function of supply voltage; C_O = 1.5 nF (only PCF2112C).



(1) R_O = 1 MΩ.
(2) R_O = 100 kΩ.

Fig.16 Display frequency as a function of R_O and C_O; T_{amb} = 25 °C; V_{DD} = 5 V.

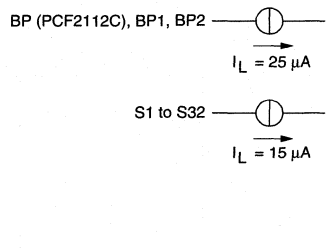
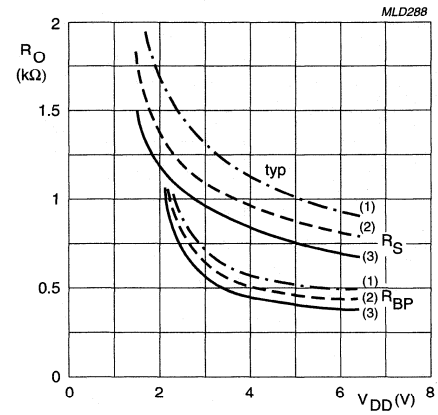
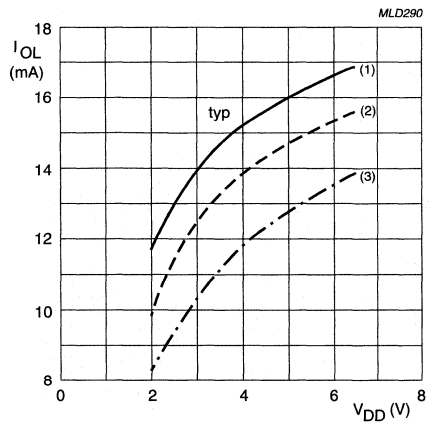


Fig.17 Test loads.



(1) T_{amb} = +85 °C.
(2) T_{amb} = +25 °C.
(3) T_{amb} = −40 °C.

Fig.18 Output resistance of backplane and segments.



(1) T_{amb} = −40 °C.
(2) T_{amb} = +25 °C.
(3) T_{amb} = +85 °C.

Fig.19 LOW level output current as a function of supply voltage (only PCF2112C).

2048 × 8-bit CMOS EEPROM with I²C-bus interface

PCF85116-3

CONTENTS

2048 × 8-bit CMOS EEPROM with I²C-bus interface

PCF85116-3

1 FEATURES

- Low power CMOS:
  - maximum operating current 1.0 mA
  - maximum standby current 10 μA (at 5.5 V), typical 4 μA
- Non-volatile storage of 16 kbits organized as eight blocks of 256 × 8-bit each
- Single supply with full operation down to 2.7 V
- On-chip voltage multiplier
- Serial input/output I²C-bus (100 kbits/s standard-mode and 400 kbits/s fast-mode)
- Write operations: multi byte write mode up to 32 bytes
- Write-protection input
- Read operations:
  - sequential read
  - random read
- Internal timer for writing (no external components)
- Power-on-reset
- High reliability by using redundant EEPROM cells
- Endurance: 1000000 Erase/Write (E/W) cycles at T_{amb} = 22 °C
- 20 years non-volatile data retention time (minimum)
- Pin and address compatible to the PCx85xxC-2 family (see also Section 2.1)
- 2 kV ESD protection (Human Body model).

2 DESCRIPTION

The PCF85116-3 is an 16 kbits (2048 × 8-bit) floating gate Electrically Erasable Programmable Read Only Memory (EEPROM). By using redundant EEPROM cells it is fault tolerant to single bit errors. In most cases multi bit errors are also covered. This feature dramatically increases reliability compared to conventional EEPROM memories. Power consumption is low due to the full CMOS technology used. The programming voltage is generated on-chip, using a voltage multiplier.

As data bytes are received and transmitted via the serial I²C-bus, a package using eight pins is sufficient. Only one PCF85116-3 device is required to support all eight blocks of 256 × 8-bit each.

Timing of the E/W cycle is carried out internally, thus no external components are required. A write-protection input at pin 7 (WP) allows disabling of write-commands from the master by a hardware signal. When pin 7 is HIGH the data bytes received will not be acknowledged by the PCF85116-3 and the EEPROM contents are not changed.

2.1 Remark

The PCF85116-3 is pin and address compatible to the PCx85xxC-2 family. The PCF85116-3 covers the whole address space of 16 kbits; address inputs are no longer needed. Therefore, pins 1 to 3 are not connected. The write-protection input is at pin 7.

3 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		2.7	5.5	V
I_{DDR}	supply current read	f_{SCL} = 400 kHz; V_{DD} = 5.5 V	–	1.0	mA
I_{DDW}	supply current E/W	f_{SCL} = 400 kHz; V_{DD} = 5.5 V	–	1.0	mA
I_{stb}	standby supply current	V_{DD} = 2.7 V	–	6	μA
		V_{DD} = 5.5 V	–	10	μA

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF85116-3P	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1
PCF85116-3T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

5 DEVICE SELECTION

Table 1 Device selection code

SELECTION	DEVICE CODE				CHIP ENABLE			R/$\overline{W}$
Bit	b7[1]	b6	b5	b4	b3	b2	b1	b0
Device	1	0	1	0	MEM SEL	MEM SEL	MEM SEL	R/$\overline{W}$

Note

1. The Most Significant Bit (MSB) 'b7' is sent first.

6 BLOCK DIAGRAM

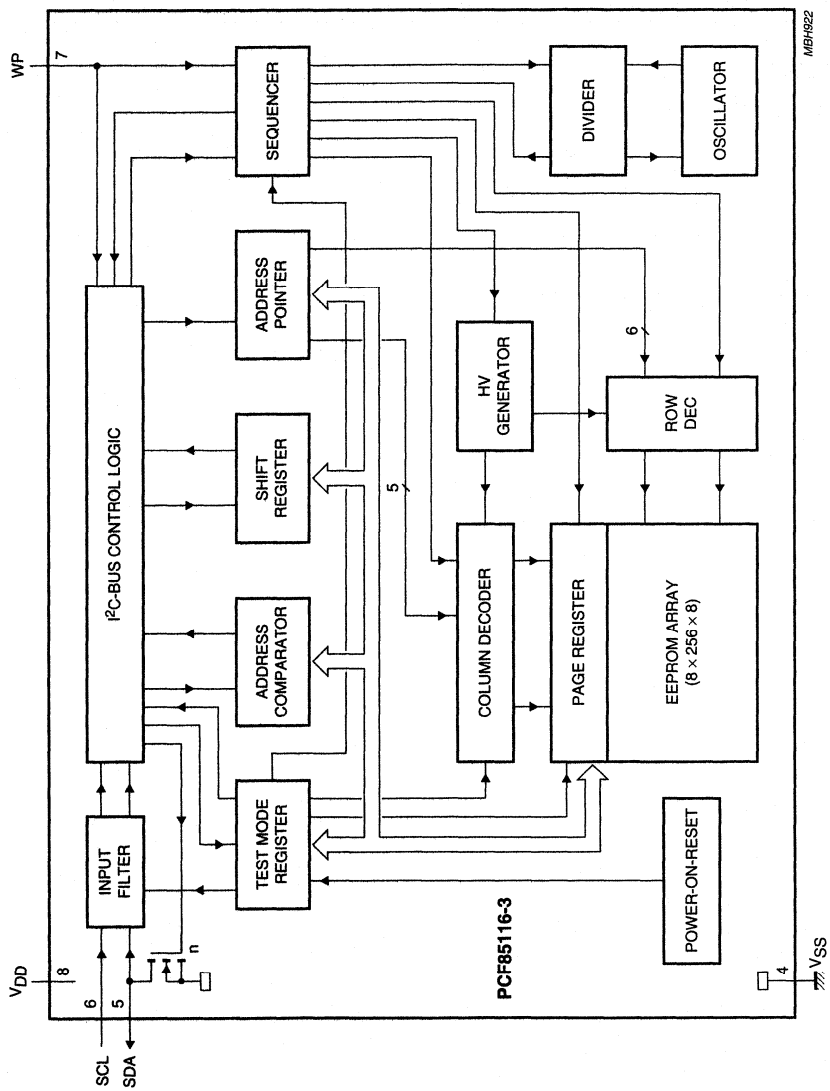


Fig.1 Block diagram.

7 PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
n.c.	2	not connected
n.c.	3	not connected
V_{SS}	4	negative supply voltage
SDA	5	serial data input/output (I²C-bus)
SCL	6	serial clock input (I²C-bus)
WP	7	write-protection input
V_{DD}	8	positive supply voltage

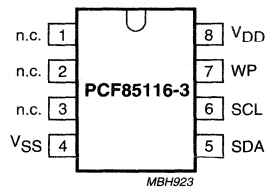


Fig.2 Pin configuration.

8 I²C-BUS PROTOCOL

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The serial bus consists of two bidirectional lines: one for data signals (SDA), and one for clock signals (SCL).

Both the SDA and SCL lines must be connected to a positive supply voltage via a pull-up resistor.

The following protocol has been defined:

- Data transfer may be initiated only when the bus is not busy
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as control signals.

8.1 Bus conditions

The following bus conditions have been defined:

- Bus not busy: both data and clock lines remain HIGH.
- Start data transfer: a change in the state of the data line, from HIGH-to-LOW, while the clock is HIGH, defines the START condition
- Stop data transfer: a change in the state of the data line, from LOW-to-HIGH, while the clock is HIGH, defines the STOP condition
- Data valid: the state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. There is one clock pulse per bit of data.

8.2 Data transfer

Each data transfer is initiated with a START condition and terminated with a STOP condition; the number of the data bytes, transferred between the START and STOP conditions is limited to 32 bytes in the E/W mode.

Data transfer is unlimited in the read mode.
The information is transmitted in bytes and each receiver acknowledges with a ninth bit.

Within the I²C-bus specifications a low-speed mode (2 kHz clock rate), a high speed mode (100 kHz clock rate) and a fast speed mode (400 kHz clock rate) are defined.
The PCF85116-3 operates in all three modes.

By definition a device that sends a signal is called a 'transmitter', and the device which receives the signal is called a 'receiver'. The device which controls the signal is called the 'master'. The devices that are controlled by the master are called 'slaves'.

Each byte is followed by one acknowledge bit.
This acknowledge bit is a HIGH level, put on the bus by the transmitter. The master generates an extra acknowledge related clock pulse. The slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte.

The master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse.

Set-up and hold times must be taken into account.
A master receiver must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master generation of the STOP condition.

8.3 Device addressing

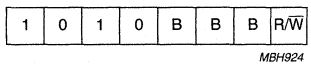


Fig.3 Slave address.

Following a START condition the bus master must output the address of the slave it is accessing. The 4 MSBs of the slave address are the device type identifier (see Fig.3). For the PCF85116-3 this is fixed to '1010'.

The next three significant bits of the slave address field are the block selection bits. It is used by the host to select one out of eight blocks (1 block = 256 bytes of memory). These are, in effect, the three most significant bits of the word address.

The last bit of the slave address defines the operation to be performed. When R/$\overline{W}$ is set to logic 1 a read operation is selected.

8.4 Write operations

8.4.1 BYTE/WORD WRITE

For a write operation the PCF85116-3 requires a second address field. This address field is a word address providing access to any one of the eight blocks of memory. Upon receipt of the word address the PCF85116-3 responds with an acknowledge and awaits the next eight bits of data, again responding with an acknowledge. Word address is automatically incremented. The master terminates the transfer by generating a STOP condition.

After this stop condition the E/W cycle starts and the bus is free for another transmission. Its duration is maximum 10 ms.

During the E/W cycle the slave receiver does not send an acknowledge bit if addressed via the I²C-bus.

8.4.2 PAGE WRITE

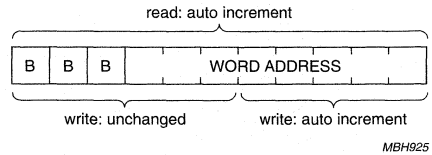


Fig.4 Auto increment of memory address.

The PCF85116-3 is capable of an 32-byte page write operation. It is initiated in the same manner as the byte write operation. The master can transmit up to 32 data bytes within one transmission. After receipt of each byte the PCF85116-3 will respond with an acknowledge. The master terminates the transfer by generating a STOP condition. The maximum total E/W time in this mode is 10 ms.

After the receipt of each data byte the six high order bits of the memory address providing access to one of the 64 pages of the memory remain unchanged. The five low order bits of the memory address will be incremented only (see Fig.3). By these five bits a single byte within the page in access is selected. By an increment the memory address may change from 31 to 0, from 63 to 32, etc. If the master transmits more than 32 bytes prior to generating the STOP condition, data within the addressed page may be overwritten and unpredictable results may occur. As in the byte write operation, all inputs are disabled until completion of the internal write cycles.

8.4.3 REMARK

Write accesses to the EEPROM are enabled if the pin WP is LOW. When WP is HIGH the EEPROM is write-protected and no acknowledge will be given by the PCF85116-3 when data is sent. However, an acknowledge will be given after the slave address and the word address.

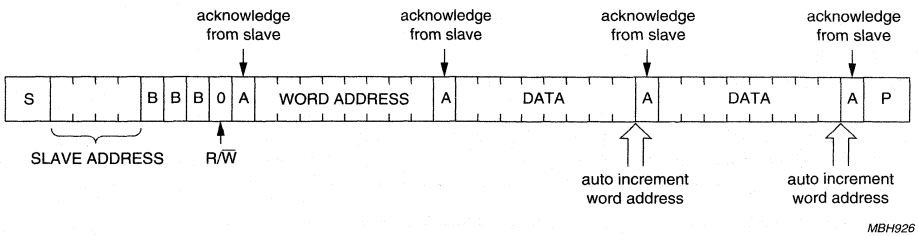


Fig.5 Auto increment memory address; two byte write.

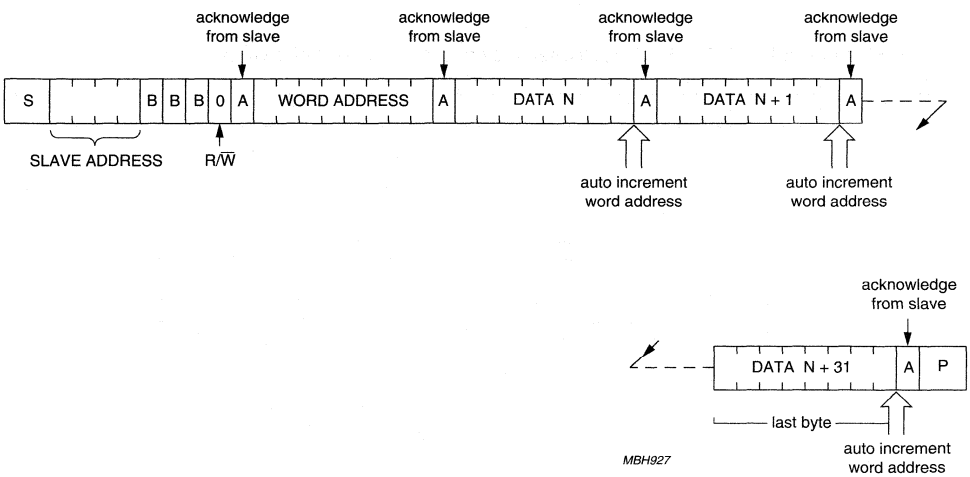


Fig.6 Page write operation; 32 bytes.

8.5 Read operations

Read operations are initiated in the same manner as write operations with the exception that the LSB of the slave address (R/$\overline{W}$) is set to logic 1. There are three basic read operations; current address read, random read and sequential read.

8.5.1 REMARK

During read operations all bits of the memory address are incremented after each transmission of a data byte. Contrary to write operations an overflow of the memory address occurs from 2047 to 0 (see Fig.3).

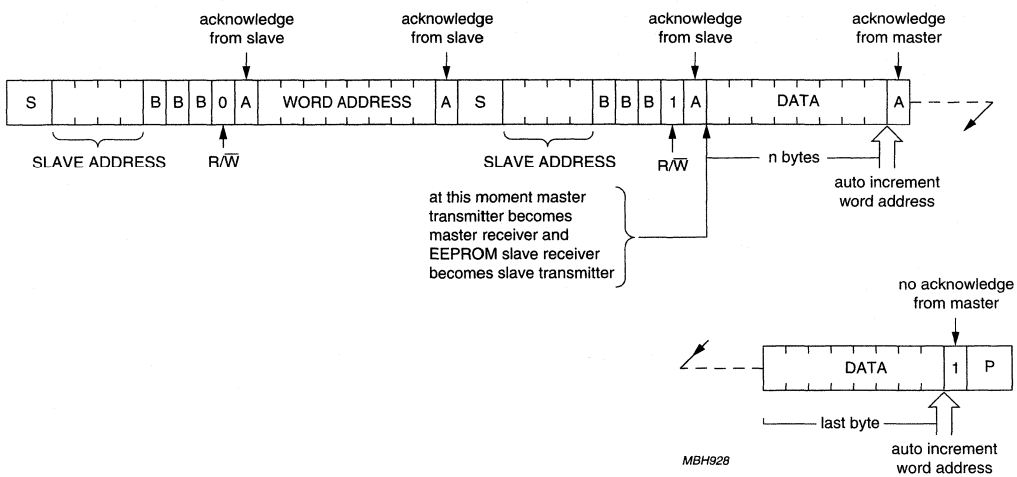


Fig.7 Master reads PCx85116-3 slave after setting word address (write word address; read data).

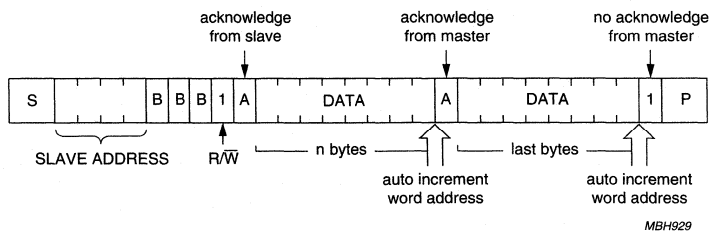


Fig.8 Master reads PCx85116-3 immediately after first byte (read mode).

9 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		−0.3	+6.5	V
V_I	input voltage on any pin	$\|Z_i\| > 500\ \Omega$	V_{SS} − 0.8	+6.5	V
I_I	input current on any pin		−	1	mA
I_O	output current		−	10	mA
T_{stg}	storage temperature		−65	+150	°C
T_{amb}	operating ambient temperature		−40	+85	°C
V_{esd}	electrostatic discharge voltage	note 1	2	−	kV

Note

1. ESD Human Body model Q22 at T_{amb} = 22 °C; discharge procedure according to MIL-STD-883C Method 3015.

10 CHARACTERISTICS

V_{DD} = 2.7 to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Supplies					
V_{DD}	supply voltage		2.7	5.5	V
I_{DDR}	supply current read	f_{SCL} = 400 kHz; V_{DD} = 5.5 V	−	1.0	mA
I_{DDW}	supply current E/W	f_{SCL} = 400 kHz; V_{DD} = 5.5 V	−	1.0	mA
$I_{DD(stb)}$	standby supply current	V_{DD} = 2.7 V	−	6	µA
		V_{DD} = 5.5 V	−	10	µA
SDA input/output (pin 5)					
V_{IL}	LOW level input voltage		−0.8	+0.3V_{DD}	V
V_{IH}	HIGH level input voltage		0.7V_{DD}	6.5	V
V_{OL1}	LOW level output voltage	I_{OL} = 3 mA; $V_{DD(min)}$	−	0.4	V
V_{OL2}		I_{OL} = 6 mA; $V_{DD(min)}$	−	0.6	V
I_{LO}	output leakage current	$V_{OH} = V_{DD}$	−	1	µA
$t_{o(f)}$	output fall time from V_{IHmin} to V_{ILmax}	note 1			
	with up to 3 mA sink current at V_{OL1}		20 + 0.1C_b	250	ns
	with up to 6 mA sink current at V_{OL2}		20 + 0.1C_b	250	ns
t_{SP}	pulse width of spikes suppressed by filter		0	100	ns
C_I	input capacitance	$V_I = V_{SS}$	−	10	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
SCL input (pin 6)					
V_{IL}	LOW level input voltage		−0.8	$+0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	6.5	V
I_{LI}	input leakage current	$V_I = V_{DD}$ or V_{SS}	–	±1	µA
f_{SCL}	clock input frequency		0	400	kHz
t_{SP}	pulse width of spikes suppressed by filter		0	100	ns
C_I	input capacitance	$V_I = V_{SS}$	–	7	pF
WP input (pin 7)					
V_{IL}	LOW level input voltage		−0.8	$+0.1V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.9V_{DD}$	$V_{DD} + 0.8$	V
Data retention time					
t_S	data retention time	$T_{amb} = 55$ °C	20	–	years

Note

1. The bus capacitance ranges from 10 to 400 pF (C_b = total capacitance of one bus line in pF).

11 I²C-BUS CHARACTERISTICS

All of the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing from V_{SS} to V_{DD}.

SYMBOL	PARAMETER	CONDITIONS	STANDARD MODE		FAST MODE		UNIT
			MIN.	MAX.	MIN.	MAX.	
f_{SCL}	clock frequency		0	100	0	400	kHz
t_{BUF}	time the bus must be free before new transmission can start		4.7	–	1.3	–	µs
$t_{HD;STA}$	START condition hold time after which first clock pulse is generated		4.0	–	0.6	–	µs
t_{LOW}	LOW level clock period		4.7	–	1.3	–	µs
t_{HIGH}	HIGH level clock period		4.0	–	0.6	–	µs
$t_{SU;STA}$	set-up time for START condition	repeated start	4.7	–	0.6	–	µs
$t_{HD;DAT}$	data hold time						
	for CBUS compatible masters		5	–	–	–	µs
	for I²C-bus devices	note 1	0	–	0	–	ns
$t_{SU;DAT}$	data set-up time		250	–	100	–	ns
t_r	SDA and SCL rise time		–	1000	$20 + 0.1C_b$ (2)	300	ns
t_f	SDA and SCL fall time		–	300	$20 + 0.1C_b$ (2)	300	ns
$t_{SU;STO}$	set-up time for STOP condition		4.0	–	0.6	–	µs

Notes

1. The hold time required (not greater than 300 ns) to bridge the undefined region of the falling edge of SCL must be internally provided by a transmitter.
2. C_b = total capacitance of one bus line in pF.

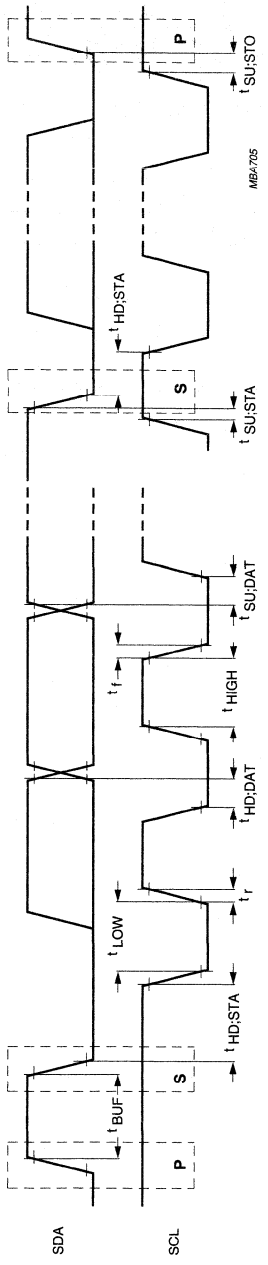


Fig.9 Timing requirements for the I²C-bus.

P = STOP condition; **S** = START condition.

12 WRITE CYCLE LIMITS

The Power-on-reset circuit resets the I²C-bus logic with a set-up time of ≤10 µs.Enabling the chip is achieved by connecting the WP input to V_{SS}.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
E/W cycle timing						
$t_{E/W}$	E/W cycle time		–	–	10	ms
Endurance						
$N_{E/W}$	E/W cycle per byte	T_{amb} = −40 to +85 °C	100000	–	–	cycles
		T_{amb} = 22 °C	1000000	–	–	cycles

CONTENTS

34 × 128 pixel matrix driver PCF8531

1 FEATURES

- Single-chip LCD controller/driver
- 34 row and 128 column outputs
- Display data RAM 34 × 128 bits
- 128 icons (last row is used for icons)
- Fast mode I²C-bus interface (400 kbit/s)
- Software selectable multiplex rates: 1 : 17, 1 : 26 and 1 : 34
- Icon mode with Mux rate 1 : 2:
  - Featuring reduced current consumption while displaying icons only.
- On-chip:
  - Generation of V_{LCD} (external supply also possible)
  - Selectable linear temperature compensation
  - Oscillator requires no external components (external clock also possible)
  - Generation of intermediate LCD bias voltages
  - Power-on reset.
- No external components required
- Software selectable bias configuration
- Logic supply voltage range V_{DD1} to V_{SS1} 1.8 to 5.5 V
- Supply voltage range for on-chip voltage generator V_{DD2} and V_{DD3} to V_{SS1} and V_{SS2} 2.5 to 4.5 V
- Display supply voltage range V_{LCD} to V_{SS}:
  - Normal mode 4 to 9 V
  - Icon mode 3 to 9 V.
- Low power consumption, suitable for battery operated systems
- CMOS compatible inputs
- Manufactured in silicon gate CMOS process.

2 APPLICATIONS

- Telecommunication systems
- Automotive information systems
- Point-of-sale terminals
- Instrumentation.

3 GENERAL DESCRIPTION

The PCF8531 is a low power CMOS LCD row/column driver, designed to drive dot matrix graphic displays at multiplex rates of 1 : 17, 1 : 26 and 1 : 34. Furthermore, it can drive up to 128 icons. All necessary functions for the display are provided in a single chip, including on-chip generation of V_{LCD} and the LCD bias voltages, resulting in a minimum of external components and low power consumption. The PCF8531 is compatible with most microcontrollers and communicates via a two-line bidirectional bus (I²C-bus). All inputs are CMOS compatible.

Remark: Icon mode is used to save current. When only icons are displayed, a much lower operating voltage (V_{LCD}) can be used and the switching frequency of the LCD outputs is reduced. In most applications it is possible to use V_{DD} as V_{LCD}.

4 PACKAGES

The PCF8531 is available as chip with bumps in tray.

5 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8531U	–	chip with bumps in tray	–

6 BLOCK DIAGRAM

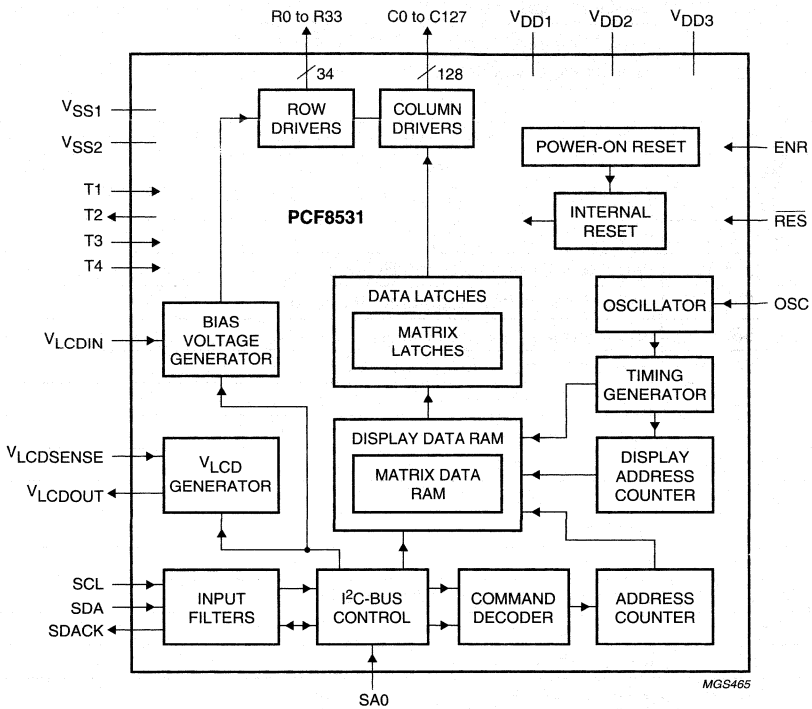


Fig.1 Block diagram.

7 PINNING

SYMBOL	PAD	DESCRIPTION
	1 to 14	dummy pad
OSC	15	oscillator input; note 1
$V_{LCDSENSE}$	16	voltage multiplier regulation input (V_{LCD}); note 2
V_{LCDOUT}	17 to 23	voltage multiplier output (V_{LCD}); note 3
V_{LCDIN}	24 to 30	LCD supply voltage (V_{LCD}); note 2
$\overline{RES}$	31	external reset input (active LOW); note 4
V_{DD3}	32 to 34	supply voltage 3; note 5
V_{DD2}	35 to 42	supply voltage 2; note 5
V_{DD1}	43 to 49	supply voltage 1; note 5
SDA	50 and 51	serial data line input of the I^2C-bus
SDACK	52	serial data acknowledge output; note 6
	53	dummy pad
SA0	54	I^2C-bus slave address input; bit 0
ENR	55	enable internal Power-on reset input; note 7
T4	56	test 4 input; note 8
V_{SS2}	57 to 63	ground 2; note 9
V_{SS1}	64 to 70	ground 1; note 9
T3	71	test 3 input; note 8
T1	72	test 1 input; note 8
SCL	73 and 74	serial clock line input of the I^2C-bus
	75 to 77	dummy pad
T2	78	test 2 output; note 10
	79 to 86	dummy pad
R0	87	LCD row driver output
R2	88	LCD row driver output
R4	89	LCD row driver output
R6	90	LCD row driver output
R8	91	LCD row driver output
R10	92	LCD row driver output
R12	93	LCD row driver output
R14	94	LCD row driver output
R16	95	LCD row driver output
R18	96	LCD row driver output
R20	97	LCD row driver output
R22	98	LCD row driver output
R24	99	LCD row driver output
R26	100	LCD row driver output
R28	101	LCD row driver output
R30	102	LCD row driver output
R32	103	LCD row driver output

SYMBOL	PAD	DESCRIPTION
C0 to C127	104 to 231	LCD column driver outputs
R33	232	LCD row driver output; icon row
R31	233	LCD row driver output
R29	234	LCD row driver output
R27	235	LCD row driver output
R25	236	LCD row driver output
R23	237	LCD row driver output
R21	238	LCD row driver output
R19	239	LCD row driver output
R17	240	LCD row driver output
R15	241	LCD row driver output
R13	242	LCD row driver output
R11	243	LCD row driver output
R9	244	LCD row driver output
R7	245	LCD row driver output
R5	246	LCD row driver output
R3	247	LCD row driver output
R1	248	LCD row driver output

Notes

1. If the on-chip oscillator is used this input must be connected to V_{DD1}.
2. If the internal V_{LCD} generation is used, V_{LCDOUT}, V_{LCDIN} and $V_{LCDSENSE}$ must be connected together.
3. If in the application an external V_{LCD} is used, then the V_{LCDOUT} pin must be left open-circuit, otherwise the chip will be damaged.
4. If only the internal Power-on reset is used this input must be connected to V_{DD1}.
5. V_{DD1} is for the logic supply, V_{DD2}, and V_{DD3} are for the voltage multiplier. For split power supplies V_{DD2} and V_{DD3} must be connected together. If only one supply voltage is available V_{DD1}, V_{DD2} and V_{DD3} must be connected together.
6. Serial data acknowledge for the I^2C-bus. By connecting SDACK to SDA externally, the SDA line becomes fully I^2C-bus compatible. Having the acknowledge output separated from the serial data line is advantageous in Chip-On-Glass (COG) applications. In COG applications where the track resistance from the SDACK pad to the system SDA line can be significant, a potential divider is generated by the bus pull-up resistor and the Indium Tin Oxide (ITO) track resistance. It is possible that during the acknowledge cycle the PCF8531 will not be able to create a valid logic 0 level. By splitting the SDA input from the SDACK output the device could be used in a mode that ignores the acknowledge bit. In COG applications where the acknowledge cycle is required, it is necessary to minimize the track resistance from the SDACK pad to the system SDA line to guarantee a valid LOW level.
7. If ENR is connected to V_{SS} Power-on reset is disabled; to enable Power-on reset ENR should be connected to V_{DD1}.
8. In the application this input must be connected to V_{SS}.
9. V_{SS1} and V_{SS2} must be connected together.
10. In the application T2 must be left open-circuit.

8 FUNCTIONAL DESCRIPTION

8.1 Oscillator

The on-chip oscillator provides the clock signal for the display system. No external components are required and the OSC input must be connected to V_{DD}. An external clock signal, if used, is connected to this input.

8.2 Power-on reset

The on-chip Power-on reset initializes the chip after Power-on or power failure.

8.3 I²C-bus controller

The I²C-bus controller receives and executes the commands. The PCF8531 acts as an I²C-bus slave receiver and therefore cannot control bus communication.

8.4 Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

8.5 Display data RAM

The PCF8531 contains a 34 × 128 bits static RAM, which stores the display data. The RAM is divided into 6 banks of 128 bytes (6 × 8 × 128 bits). Bank 6 is used for icon data. During RAM access, data is transferred to the RAM via the I²C-bus interface. There is a direct correspondence between the X address and column output number.

8.6 Timing generator

The timing generator produces the various signals required to drive the internal circuitry. Internal chip operation is not disturbed by operations on the data buses.

8.7 Address counter

The address counter sets the addresses of the display data RAM for writing.

8.8 Display address counter

The display address counter generates the addresses for read out of the display data.

8.9 Command decoder

The command decoder identifies command words that arrive on the I²C-bus and determines the destination for the following data bytes.

8.10 Bias voltage generator

The bias voltage generator generates 4 buffered intermediate bias voltages. This block contains the generator for the reference voltages and the 4 buffers. This block can operate in two voltage ranges:

- Normal mode; 4.0 to 9.0 V
- Power save mode; 3.0 to 9.0 V.

8.11 V_{LCD} generator

The V_{LCD} voltage generator contains a configurable 2 to 5 times voltage multiplier; this is software programmable.

8.12 Reset

The PCF8531 has the possibility of two reset modes, internal Power-on reset or external reset ($\overline{RES}$). The reset mode is selected using the ENR signal. After a reset the chip has the following state:

- All row and column outputs are set to V_{SS} (display off)
- RAM data is undefined
- Power-down mode.

8.13 Power-down

During power-down all static currents are switched off (no internal oscillator, no timing and no LCD segment drive system), and all LCD outputs are internally connected to V_{SS}. The I²C-bus function remains operational.

8.14 Column driver outputs

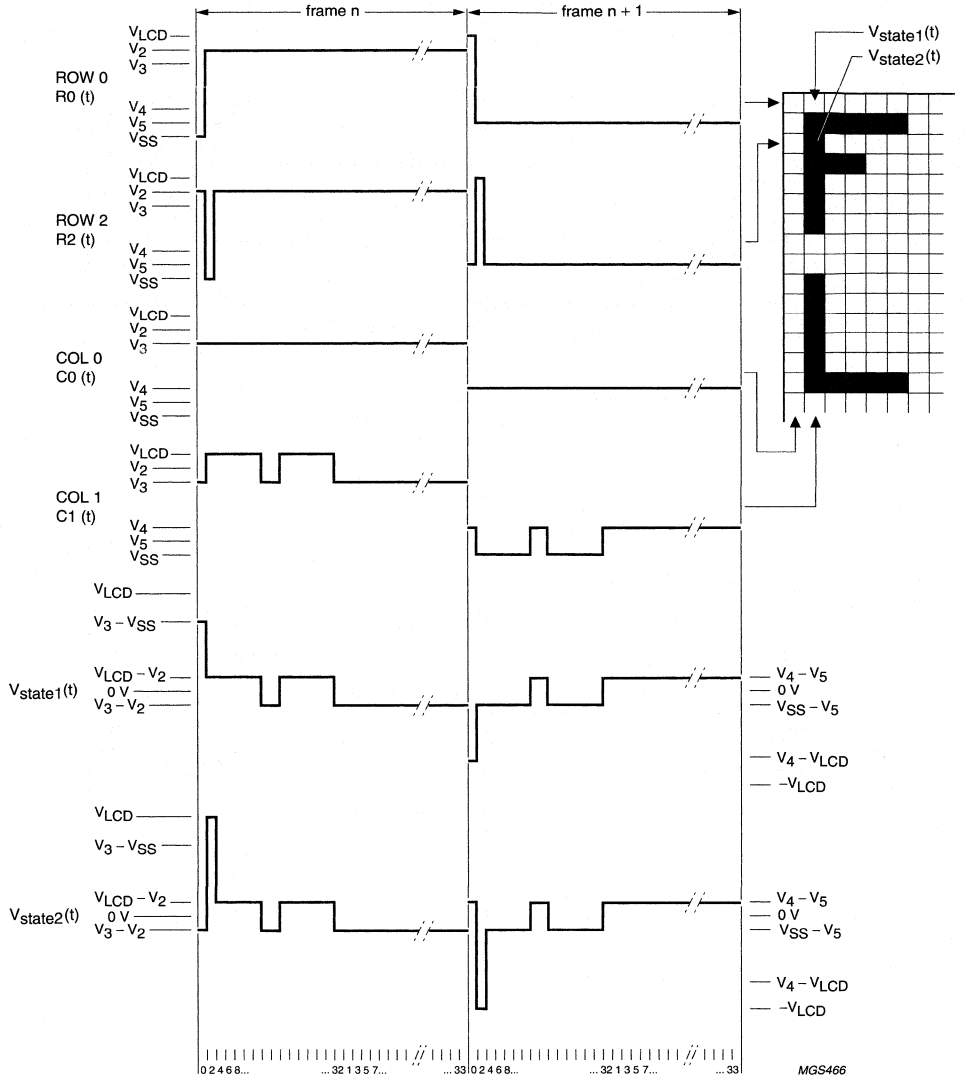
The LCD drive section includes 128 column outputs (C0 to C127) which should be connected directly to the LCD. The column output signals are generated in accordance with the multiplexed row signals and with the data in the display latch. When less than 128 columns are required the unused column outputs should be left open-circuit.

8.15 Row driver outputs

The LCD drive section includes 34 row outputs (R0 to R33) which should be connected directly to the LCD. The row output signals are generated in accordance with the selected LCD drive mode. If less than 34 rows or lower Mux rates are required the unused outputs must be left open-circuit. The row signals are interlaced i.e. the selection order is R0, R2, ..., R1, R3 etc.

8.16 LCD waveforms and DDRAM to data mapping

The LCD waveforms and the DDRAM to display data mapping are shown in Figs 2, 3 and 4.



$V_{state1}(t) = C1(t) - R0(t)$.
$V_{state2}(t) = C1(t) - R2(t)$.

Fig.2 Typical LCD driver waveforms.

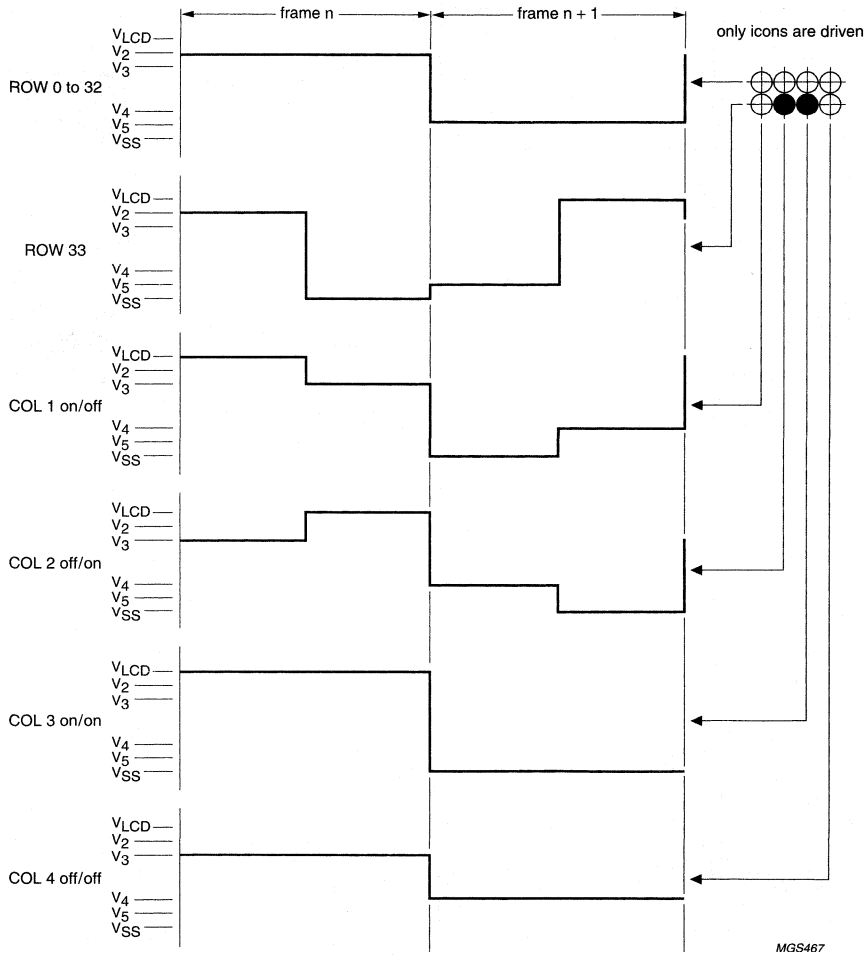


Fig.3 Icon mode; Mux 1 : 2 LCD waveforms.

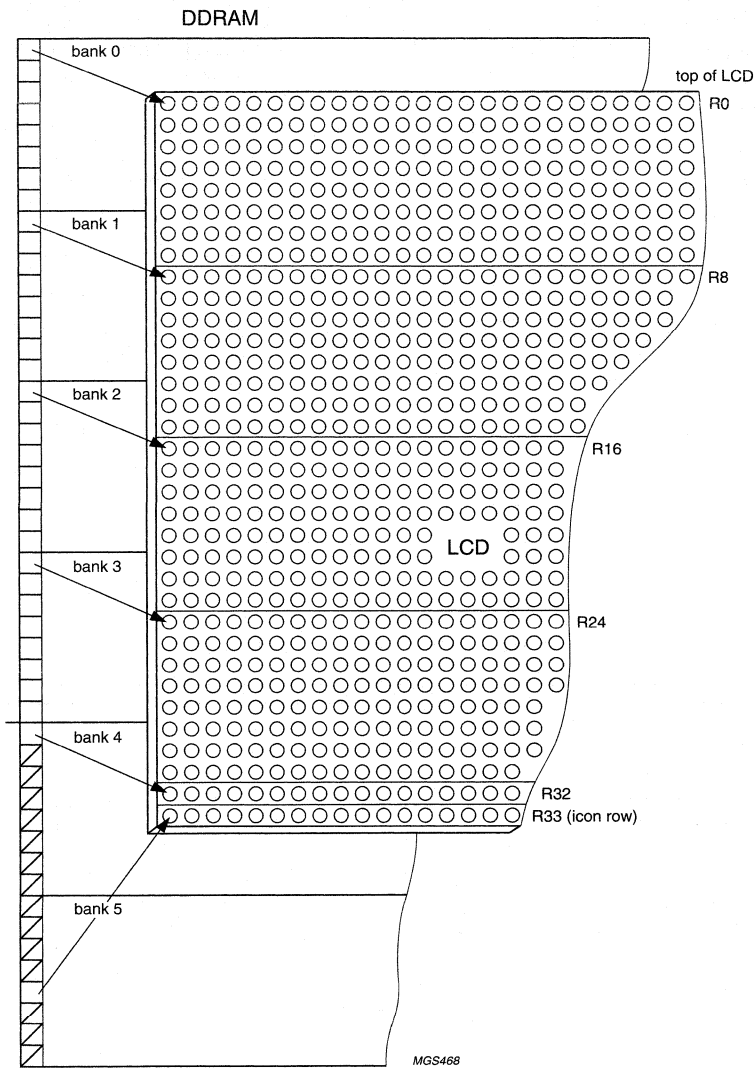


Fig.4 DDRAM to display mapping.

8.17 Addressing

Data is written in bytes into the RAM matrix of the PCF8531 as illustrated in Figs 5, 6 and 7. The display RAM has a matrix of 34 × 128 bits. The columns are addressed by the address pointer. The address ranges are X 0 to X 127 (7FH) and Y 0 to Y 5 (5H). Addresses outside of these ranges are not allowed. In vertical addressing mode (V = 1) the Y address increments after each byte (see Fig.6). After the last Y address (Y = 4) Y wraps around to 0 and X increments to address the next column. In horizontal addressing mode (V = 0) the X address increments after each byte (see Fig.7). After the last X address (X = 127) X wraps around to 0 and Y increments to address the next row. After the very last address (X = 127 and Y = 4) the address pointers wrap around to address (X = 0 and Y = 0). It should be noted that in bank 4 only the LSB (DB0) of the data will be written into the RAM. The Y address 5 is reserved for icon data and is not affected by the addressing mode; it should be noted that in bank 5 only the 5th data bit (DB4) will be written into the RAM.

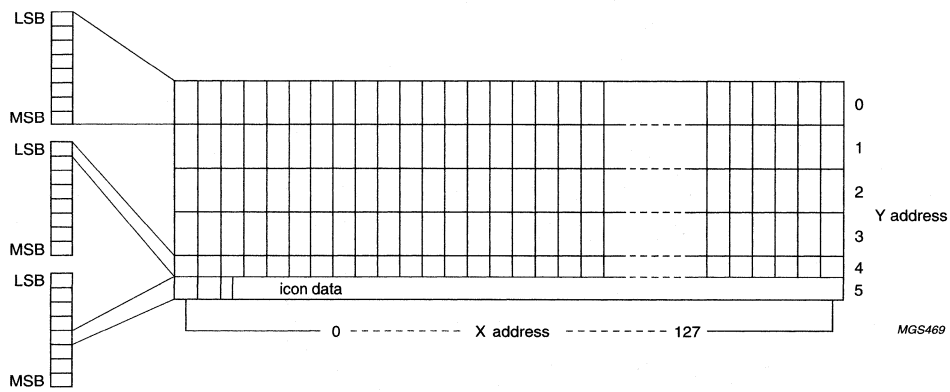


Fig.5 RAM format and addressing.

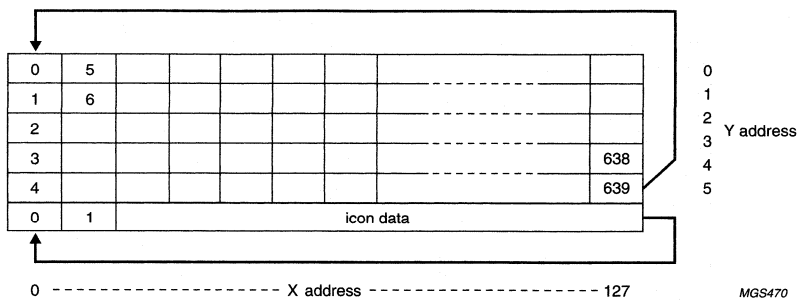


Fig.6 Sequence of writing data bytes into RAM with vertical addressing (V = 1).

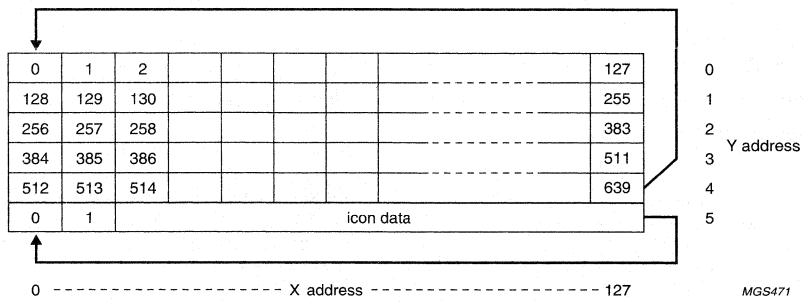


Fig.7 Sequence of writing data bytes into RAM with horizontal addressing (V = 0).

8.18 Instructions

Only two PCF8531 registers, the Instruction Register (IR) and the Data Register (DR) can be directly controlled by the MPU. Before internal operation, control information is stored temporarily in these registers to allow interfacing to various types of MPUs which operate at different speeds or to allow interfacing to peripheral control ICs.
The PCF8531 operation is controlled by the instructions given in Table 1. Details are explained in subsequent sections.

Instructions are of 4 types, those that:

1. Define PCF8531 functions such as display configuration, etc.
2. Set internal RAM addresses
3. Perform data transfer with internal RAM
4. Others.

In normal use, category 3 instructions are used most frequently. Automatic incrementing by 1 of internal RAM addresses after each data write reduces the MPU program load.

8.18.1 RESET

After reset or internal Power-on reset (depending on application), the LCD driver will be set into the following state:

- Power-down mode (PD = 1)
- Horizontal addressing (V = 0)
- Display blank (D = 0; E = 0), no icon mode (IM = 0)
- Address counter X[6:0] = 0; Y[2:0] = 0
- Bias system BS[2:0] = 0
- Multiplex rate M[1:0] = 0 (Mux rate 1 : 17)
- Temperature control mode TC[2:0] = 0
- HV-gen control, HVE = 0 the HV generator is switched off, PRS = 0 and S[1:0] = 0
- V_{LCD} = 0 V
- RAM data is undefined
- Command page definition H[1:0] = 0.

8.18.2 Function set

8.18.2.1 PD

When PD = 1, the Power-down mode of the LCD driver is active:

- All LCD outputs at V_{SS} (display off)
- Power-on reset detection active, oscillator off
- V_{LCD} can be disconnected
- I^2C-bus is operational, commands can be executed
- RAM contents not cleared; RAM data can be written
- Register settings remain unchanged.

8.18.2.2 V

When V = 0 the horizontal addressing is selected. The data is written into the DDRAM as shown in Fig.7. When V = 1 the vertical addressing is selected. The data is written into the DDRAM as shown in Fig.6. Icon data is written independently of V when Y address is 5.

8.18.3 Set Y address

Y_2, Y_1 and Y_0 defines the Y address vector of the display RAM.

Table 1 Y address

Y_2	Y_1	Y_0	BANK
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5 (icons)

8.18.4 Set X address

The X address points to the columns. The range of X is 0 to 127 (7FH).

8.18.5 Set multiplex rate

M[1:0] selects the multiplex rate (see Table 8).

8.18.6 Display control (D, E and IM)

Bits D and E select the display mode (see Table 6). Bit IM sets the display to icon mode.

8.18.7 Set bias system

Different multiplex rates require different bias settings. These are programmed by BS[2:0], which sets the binary number n. The optimum value for n is given by

$$n = \sqrt{\text{Mux rate}} - 3$$

Supported values of n are given in Table 2. Table 3 shows the intermediate bias voltages.

Table 2 Programming the required bias system

BS[2]	BS[1]	BS[0]	n	BIAS SYSTEM	COMMENT
0	0	0	7	1/11	
0	0	1	6	1/10	
0	1	0	5	1/9	
0	1	1	4	1/8	
1	0	0	3	1/7	recommended for 1 : 34
1	0	1	2	1/6	recommended for 1 : 26
1	1	0	1	1/5	recommended for 1 : 17
1	1	1	0	1/4	recommended for icon mode

8.18.8 LCD BIAS VOLTAGE

Table 3 Intermediate LCD bias voltages

SYMBOL	BIAS VOLTAGES	EXAMPLE FOR 1/7 BIAS
V1	V_{LCD}	V_{LCD}
V2	$\frac{n+3}{n+4} \times V_{LCD}$	$^6/_7 \times V_{LCD}$
V3	$\frac{n+2}{n+4} \times V_{LCD}$	$^5/_7 \times V_{LCD}$
V4	$\frac{2}{n+4} \times V_{LCD}$	$^2/_7 \times V_{LCD}$
V5	$\frac{1}{n+4} \times V_{LCD}$	$^1/_7 \times V_{LCD}$
V6	V_{SS}	V_{SS}

8.18.9 SET V_{OP} VALUE:

The operating voltage V_{LCD} can be set by software. The voltage at reference temperature [V_{LCD} ($T = T_{cut}$)] can be calculated as: V_{LCD} (T_{cut}) = (a + V_{OP} × b).

The generated voltage is dependent on the temperature, programmed Temperature Coefficient (TC) and the programmed voltage at reference temperature (T_{cut}). $V_{LCD} = V_{LCD}$ (T_{cut}) × [1 + TC × ($T - T_{cut}$)].

The parameter values are given in Table 4. Two overlapping V_{LCD} ranges are selectable via the command 'HV-gen control' (see Table 4 and Fig.8). The maximum voltage that can be generated is dependent on the V_{DD2} and V_{DD3} voltage and the display load current. For Mux 1 : 34 the optimum operating voltage of the liquid can be calculated as:

$$V_{LCD} = \frac{1+\sqrt{34}}{\sqrt{2\times\left(1-\frac{1}{\sqrt{34}}\right)}} \times V_{th} = 5.30 \times V_{th}$$

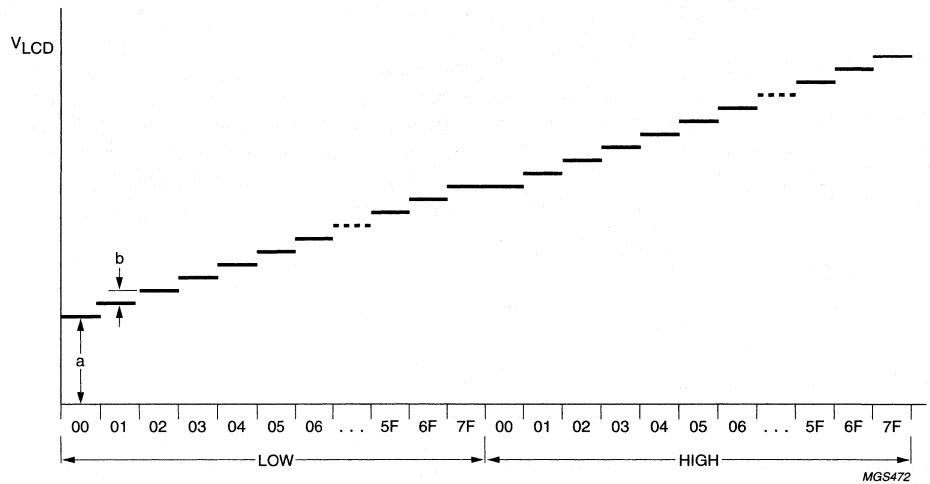
Where V_{th} is the threshold voltage of the liquid crystal material used.

The practical value for V_{OP} is determined by equating $V_{off(rms)}$ with defined LCD threshold voltage (V_{th}), typically when the LCD exhibits approximately 10% contrast.

As the programming range for the internally generated V_{LCD} allows values above the maximum allowed V_{LCD}, the user has to ensure while setting the V_{OP} register and selecting the temperature compensation, that under all conditions and including all tolerances the V_{LCD} limit of maximum 9 V will never be exceeded.

Table 4 Parameter values for the HV generator programming

SYMBOL	VALUE		UNIT
	PRS = 0	PRS = 1	
T_{cut}	27	27	°C
a	2.94	6.75	V
b	0.03	0.03	V
Programming range	2.94 to 6.75	6.75 to 10.56	V



V_{OP}[6:0] (programmed) [00H to 7FH] programme range LOW and HIGH.

Fig.8 V_{OP} programming of PCF8531.

8.18.10 Voltage multiplier control S[1:0]

The PCF8531 incorporates a software configurable voltage multiplier. After reset (internal or external) the voltage multiplier is set to 2 × V_{DD2}. The voltage multiplier factors are set via the command 'HV-gen configuration' (see Tables 4, 5 and 6).

8.18.11 Temperature compensation

Due to the temperature dependency of the liquid crystal's viscosity the LCD controlling voltage V_{LCD} should usually be increased at lower temperatures to maintain optimum contrast. Figure 9 shows V_{LCD} for high multiplex rates.

Linear temperature compensation is supported in the PCF8531. The temperature coefficient of V_{LCD} can be selected from 8 values by setting bits TC[2:0] (see Tables 4, 5 and 6).

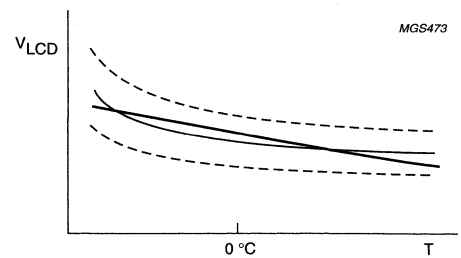


Fig.9 V_{LCD} as a function of liquid crystal temperature.

Table 5 Instruction set

INSTRUCTION	I²C-BUS COMMAND[1]		I²C-BUS COMMAND BYTE								DESCRIPTION
	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
H_1 and H_0 = don't care (H independent command page)											
NOP	0	0	0	0	0	0	0	0	0	0	no operation
Write data	1	0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	write data to display RAM
Set default H[1:0]	0	0	0	0	0	0	0	0	0	1	select H[1:0] = 0
H_1 = 0 and H_0 = 0 (function and RAM command page)											
Instruction set	0	0	0	0	0	0	1	0	H1	H0	select command page
Function set	0	0	0	0	1	0	0	PD	V	0	power-down control; entry mode
Set Y address of RAM	0	0	0	1	0	0	0	Y_2	Y_1	Y_0	set Y address of RAM; $0 \leq Y \leq 5$
Set X address of RAM	0	0	1	X_6	X_5	X_4	X_3	X_2	X_1	X_0	set X address part of RAM; $0 \leq X \leq 127$
H_1 = 0 and H_0 = 1 (display setting command page)											
Multiplex rate	0	0	0	0	0	0	0	1	M1	M0	select multiplex rate
Display control	0	0	0	0	0	0	1	D	IM	E	set display configuration
Bias system	0	0	0	0	0	1	0	BS_2	BS_1	BS_0	set Bias System (BSx)
H_1 = 1 and H_0 = 0 (HV-gen command page)											
HV-gen control	0	0	0	0	0	0	0	1	PRS	HVE	set V_{LCD} programming range
HV-gen configuration	0	0	0	0	0	0	1	0	S1	S0	set voltage multiplication factor
Temperature control	0	0	0	0	1	0	0	TC_2	TC_1	TC_0	set temperature coefficient
Test modes	0	0	0	1	X	X	X	X	X	X	do not use (reserved for test)
V_{LCD} control	0	0	1	V_{OP6}	V_{OP5}	V_{OP4}	V_{OP3}	V_{OP2}	V_{OP1}	V_{OP0}	set V_{LCD} register $0 \leq V_{OP} \leq 127$

Note

1. R/$\overline{W}$ is set in the slave address byte; Co and RS are set in the control byte.

Table 6 Explanations for symbols in Table 5

BIT	0	1
PD	chip is active	chip is in Power-down mode
V	horizontal addressing	vertical addressing
IM	normal mode; full display + icons	icon mode; only icons are displayed
H[1:0][1]	see Table 7	
D and E	see Table 7	
HVE	voltage multiplier disabled	voltage multiplier enabled
PRS	V_{LCD} programming range LOW	V_{LCD} programming range HIGH
TC[2:0]	see Table 7	
S[1:0]	see Table 7	

Note

1. The H-bits identify the command page (use set default H[1:0] command to set H[1:0] = 0.

Table 7 Description of bits H, D and E, TC and S

BITS	VALUE	DESCRIPTION
Command page (H)		
H[1:0]	00	function and RAM command page
	01	display setting command page
	10	HV-gen command page
Display modes (D, E)		
D and E	00	display blank
	10	normal mode
	01	all display segments
	11	inverse video mode
Temperature coefficient (TC)		
TC[2:0]	000	temperature coefficient 0
	001	temperature coefficient 1
	010	temperature coefficient 2
	011	temperature coefficient 3
	100	temperature coefficient 4
	101	temperature coefficient 5
	110	temperature coefficient 6
	111	temperature coefficient 7
Voltage multiplier factor (S)		
S[1:0]	00	2 × voltage multiplier
	01	3 × voltage multiplier
	10	4 × voltage multiplier
	11	5 × voltage multiplier

Table 8 Multiplex rates

MUX RATE	M1	M0
1 : 17	0	0
1 : 26	1	0
1 : 34	0	1

9 I²C-BUS INTERFACE

9.1 Characteristics of the I²C-bus

The I²C-bus is for bi-directional, two-line communication between different ICs or modules. The two lines are a Serial Data line (SDA) and a Serial Clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

9.1.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal (see Fig.10).

9.1.2 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P). The START and STOP conditions are illustrated in Fig.11.

9.1.3 System configuration

The system configuration is illustrated in Fig.12

- Transmitter: the device which sends the data to the bus
- Receiver: the device which receives the data from the bus
- Master: the device which initiates a transfer, generates clock signals and terminates a transfer
- Slave: the device addressed by a master
- Multi-Master: more than one master can attempt to control the bus at the same time without corrupting the message
- Arbitration: procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted
- Synchronization: procedure to synchronize the clock signals of two or more devices.

9.1.4 Acknowledge

Acknowledge on the I²C-bus is illustrated in Fig.13. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

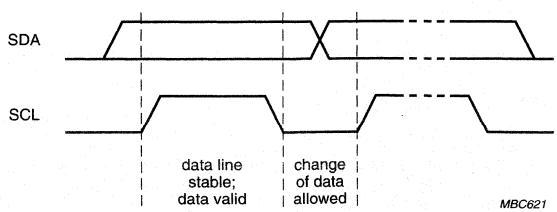


Fig.10 Bit transfer.

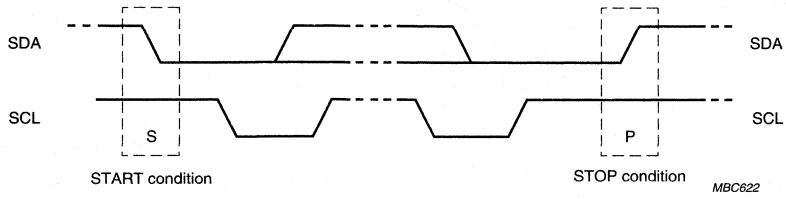


Fig.11 Definition of START and STOP conditions.

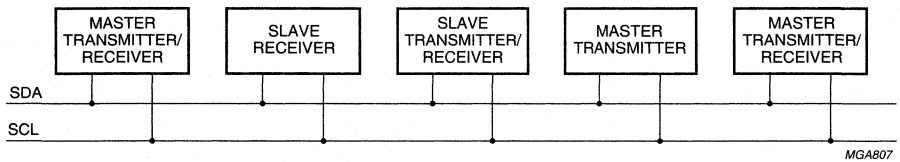


Fig.12 System configuration.

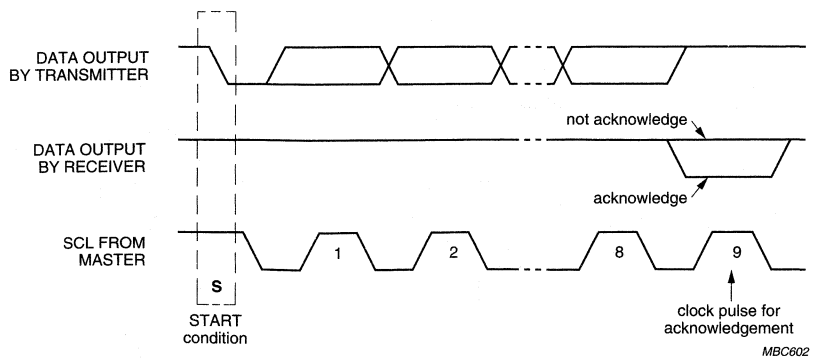


Fig.13 Acknowledge on the I²C-bus.

9.2 I²C-bus protocol

This driver does not support 'read'. The PCF8531 is a slave receiver. Therefore, it only responds when R/$\overline{W}$ = 0 in the slave address byte.

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. Two 7-bit slave addresses (0111100 and 0111101) are reserved for the PCF8531. The least significant bit of the slave address is set by connecting the input SA0 to either logic 0 (V_{SS}) or logic 1 (V_{DD}).

The I²C-bus protocol is illustrated in Fig.14.

The sequence is initiated with a START condition (S) from the I²C-bus master which is followed by the slave address. All slaves with the corresponding address acknowledge in parallel, all the others will ignore the I²C-bus transfer. After acknowledgement, one or more command words follow which define the status of the addressed slaves.
A command word consists of a control byte, which defines Co and RS, plus a data byte (see Fig.14 and Table 1).

The last control byte is tagged with a cleared most significant bit, the continuation bit Co. The control and data bytes are also acknowledged by all addressed slaves on the bus.

After the last control byte, depending on the RS bit setting, either a series of display data bytes or command data bytes may follow. If the RS bit was set to logic 1, these display bytes are stored in the display RAM at the address specified by the data pointer.

The data pointer is automatically updated and the data is directed to the intended PCF8531 device. If the RS bit of the last control byte was set to logic 0, these command bytes will be decoded and the setting of the device will be changed according to the received commands.
The acknowledgement after each byte is made only by the addressed PCF8531. At the end of the transmission the I²C-bus master issues a STOP condition (P).

9.3 Command decoder

- Pairs of bytes; information in 2nd byte, first byte determines whether information is display or instruction data
- Stream of information bytes after Co = 0; display or instruction data depending on last RS (Register Selection).

The command decoder identifies command words that arrive on the I²C-bus. The most significant bit of a control byte is the continuation bit Co. If this bit is logic 1, it indicates that only one data byte, either command or RAM data, will follow. If this bit is logic 0, it indicates that a series of data bytes, either command or RAM data, may follow. The DB6 bit of a control byte is the RAM data/command bit RS. When this bit is at logic 1, it indicates that another RAM data byte will be transferred next. If the bit is at logic 0, it indicates that another command byte will be transferred next.

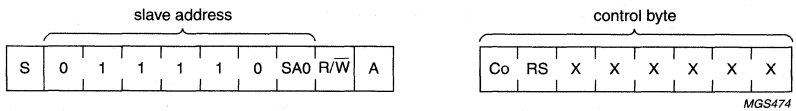


Fig.14 Slave address and control byte.

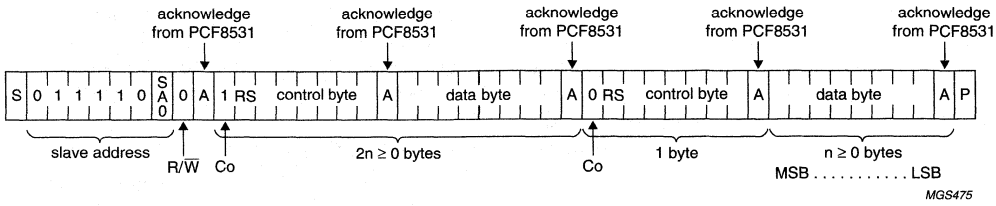


Fig.15 Master transmits to slave receiver; write mode.

10 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); note 1.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD1}	logic supply voltage	−0.5	+5.5	V
V_{DD2}, V_{DD3}	multiplier supply voltage	−0.5	+4.5	V
I_{DD}	supply current	−50	+50	mA
V_{LCD}	LCD supply voltage	−0.5	+9.0	V
I_{LCD}	LCD supply current	−50	+50	mA
I_{SS}	negative supply current	−50	+50	mA
V_I/V_O	input/output voltage (any input/output)	−0.5	V_{DD} + 0.5	V
I_I	DC input current	−10	+10	mA
I_O	DC output current	−10	+10	mA
P_{tot}	total power dissipation per package	−	300	mW
P/out	power dissipation per output	−	30	mW
T_{stg}	storage temperature	−65	+150	°C
T_j	junction temperature	−	150	°C

Note

1. Parameters are valid over the operating temperature range unless otherwise specified. All voltages referenced to V_{SS} unless otherwise noted.

11 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is recommended to take normal precautions appropriate to handling MOS devices (see *"Handling MOS Devices"*).

12 DC CHARACTERISTICS

V_{DD1} = 1.8 (1.9) to 5.5 V; V_{DD2} and V_{DD3} = 2.5 to 4.5 V; $V_{SS1,2}$ = 0 V; V_{DD1} to $V_{DD3} \leq V_{LCD} \leq 9.0$ V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{LCD}	LCD supply voltage	note 1	4.0	–	9.0	V
		icon mode; note 1	3.0	–	9.0	V
V_{DD1}	logic supply voltage		1.9	–	5.5	V
		$T_{amb} \geq -25$ °C	1.8	–	5.5	V
V_{DD2}, V_{DD3}	multiplier supply voltage	LCD voltage internally generated	2.5	–	4.5	V
I_{DD}	supply current	Power-down mode; internal V_{LCD}	–	2	10	μA
		normal mode; internal V_{LCD}; notes 2 and 3	–	170	350	μA
		normal mode; external V_{LCD}; note 2	–	10	50	μA
I_{LCD}	LCD input current	normal mode; external V_{LCD}; notes 2 and 4	–	25	100	μA
		icon mode; external V_{LCD}; notes 2 and 5	–	15	70	μA
V_{POR}	Power-on reset level	note 6	0.9	1.2	1.6	V
Logic						
V_{IL}	LOW-level input voltage		V_{SS}	–	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	–	V_{DD}	V
I_{OL}	LOW-level output current (SDA)	V_{OL} = 0.4 V; V_{DD} = 5 V	3.0	–	–	mA
I_{LI}	input leakage current	$V_I = V_{DD}$ or V_{SS}	−1	–	+1	μA
Column and row outputs						
$R_{o(col)}$	column output resistance C0 to C127	note 7	–	12	20	kΩ
$R_{o(row)}$	row output resistance R0 to R33	note 7	–	12	20	kΩ
$V_{bias(col)}$	bias tolerance C0 to C127		−100	0	+100	mV
$V_{bias(row)}$	bias tolerance R0 to R33		−100	0	+100	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{LCD} generation						
$V_{LCD(tol)}$	LCD voltage tolerance, internal V_{LCD}	TC1 to TC7; note 8	–	–	±3.9	%
TC0	LCD voltage temperature coefficient 0	T_{amb} = −20 to +70 °C	–	0	–	%/°C
TC1	LCD voltage temperature coefficient 1	T_{amb} = −20 to +70 °C	–	−0.026	–	%/°C
TC2	LCD voltage temperature coefficient 2	T_{amb} = −20 to +70 °C	–	−0.039	–	%/°C
TC3	LCD voltage temperature coefficient 3	T_{amb} = −20 to +70 °C	–	−0.052	–	%/°C
TC4	LCD voltage temperature coefficient 4	T_{amb} = −20 to +70 °C	–	−0.078	–	%/°C
TC5	LCD voltage temperature coefficient 5	T_{amb} = −20 to +70 °C	–	−0.13	–	%/°C
TC6	LCD voltage temperature coefficient 6	T_{amb} = −20 to +70 °C	–	−0.19	–	%/°C
TC7	LCD voltage temperature coefficient 7	T_{amb} = −20 to +70 °C	–	−0.26	–	%/°C
T_{cut}	cut point temperature		–	27	–	°C

Notes

1. As the programming range for the internally generated V_{LCD} allows values above the maximum allowed V_{LCD}, the user has to ensure while setting the V_{OP} register and selecting the temperature compensation, that under all conditions and including all tolerances the V_{LCD} limit of maximum 9 V will never be exceeded.
2. LCD outputs are open-circuit, inputs at V_{DD} or V_{SS}; bus inactive.
3. V_{DD1} to V_{DD3} = 2.85 V; V_{LCD} = 7.0 V; voltage multiplier = 3 × V_{DD}; f_{OSC} = 34 kHz.
4. V_{DD1} to V_{DD3} = 2.75 V; V_{LCD} = 9.0 V; f_{OSC} = 34 kHz.
5. V_{DD1} to V_{DD3} = 2.75 V; V_{LCD} = 3.5 V; f_{OSC} = 34 kHz.
6. Resets all logic when $V_{DD1} < V_{POR}$.
7. $|I_{LOAD}| \leq 50$ μA; outputs tested one at a time.
8. $V_{LCD} \leq 7.7$ V.

13 AC CHARACTERISTICS

V_{DD1} = 1.8 to 5.5 V; V_{DD2} and V_{DD3} = 2.5 to 4.5 V; V_{SS1} and V_{SS2} = 0 V; V_{DD1} to $V_{DD3} \leq V_{LCD} \leq 9.0$ V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{frame}	LCD frame frequency (internal clock)	V_{DD} = 3.0 V; note 1	40	66	135	Hz
f_{OSC}	oscillator frequency (not available at any pin)		20	34	65	kHz
$f_{clk(ext)}$	external clock frequency		20	–	65	kHz
$t_{W(RESL)}$	reset LOW pulse width	note 2	300	–	–	ns
$t_{SU;RESL}$	reset LOW pulse set-up time after Power-on		–	–	30	µs
Serial-bus interface; note 3						
f_{SCL}	SCL clock frequency		0	–	400	kHz
t_{SCLL}	SCL clock LOW period		1.3	–	–	µs
t_{SCLH}	SCL clock HIGH period		0.6	–	–	µs
$t_{SU;DAT}$	data set-up time		100	–	–	ns
$t_{HD;DAT}$	data hold time		0	–	0.9	µs
t_r	SCL, SDA rise time	note 4	20 + 0.1C_b	–	300	ns
t_f	SCL, SDA fall time	note 4	20 + 0.1C_b	–	300	ns
C_b	capacitive load represented by each bus line		–	–	400	pF
$t_{SU;STA}$	set-up time for a repeated START condition		0.6	–	–	µs
$t_{HD;STA}$	start condition hold time		0.6	–	–	µs
$t_{SU;STO}$	set-up time for STOP condition		0.6	–	–	µs
t_{SW}	tolerable spike width on bus		–	–	50	ns
t_{BUF}	bus free time between a STOP and START condition		1.3	–	–	µs

Notes

1. $f_{frame} = f_{clk(ext)}/480$; $f_{OSC}/480$.
2. For $t_{W(RESL)} > 3$ ns a reset may be generated.
3. All timing values are valid within the operating supply voltage and ambient temperature range and are referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.
4. C_b = total capacitance of one bus line in pF.

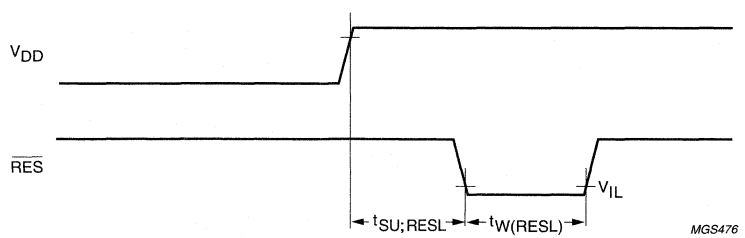


Fig.16 Reset timing.

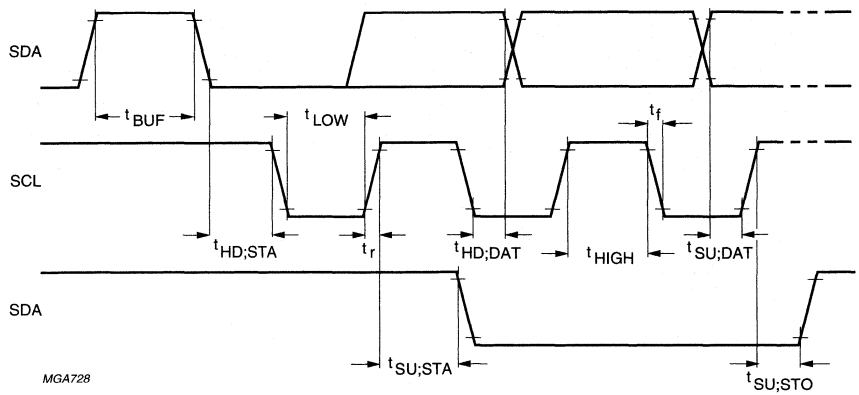
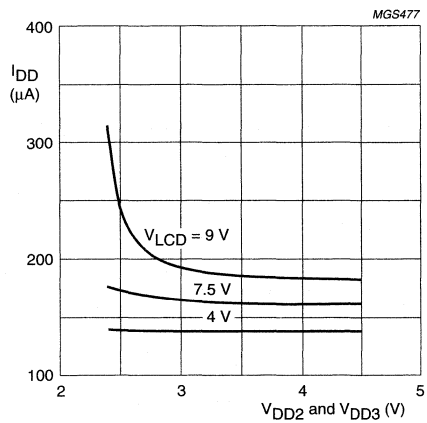
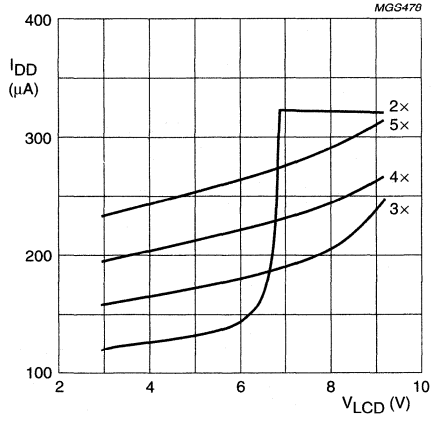


Fig.17 I²C-bus timing diagram.



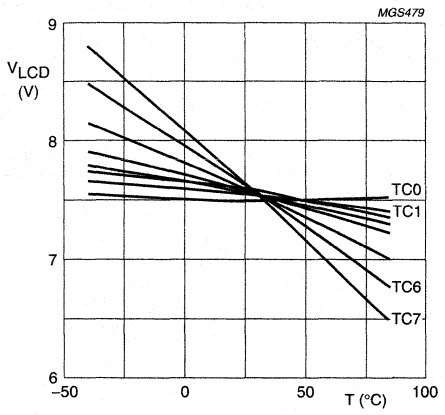
V_{DD1} = 2 V; 4 × voltage multiplier; T_{amb} = 27 °C; TC = 0; BS = 100; no V_{LCD} load.

Fig.18 I_{DD}, internal V_{LCD} generation.



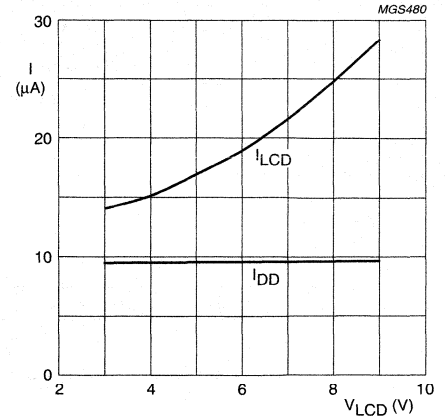
V_{DD1} = 1.8 V; V_{DD2} and V_{DD3} = 2.6 V; T_{amb} = 27 °C; f_{OSC} = 34 kHz; no V_{LCD} load.

Fig.19 I_{DD} for different multiplication factors.



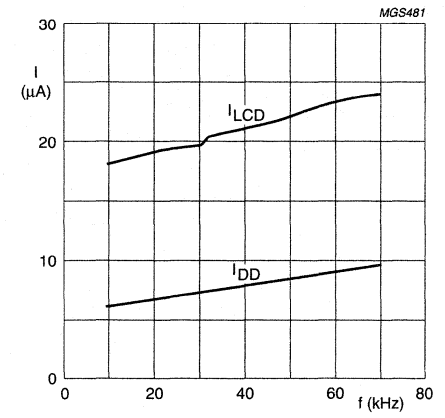
V_{LCD} = 7.5 V; V_{DD1} to V_{DD3} = 2.7 V; T_{amb} = 27 °C; no V_{LCD} load.

Fig.20 Temperature coefficient.



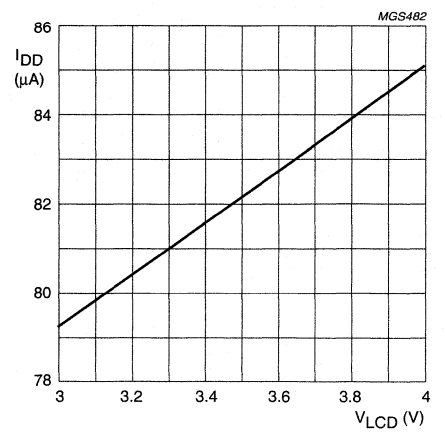
V_{DD1} = 1.8 V; V_{DD2} and V_{DD3} = 2.5 V; external V_{LCD}; T_{amb} = 27 °C; TC = 0; BS = 100; no V_{LCD} load.

Fig.21 I_{DD} and I_{LCD} with external V_{LCD}.



V_{DD1} = 2.5 V; V_{DD2} and V_{DD3} = 2.5 V; external V_{LCD}; T_{amb} = 27 °C; TC = 0; BS = 100; no V_{LCD} load.

Fig.22 I_{DD} and I_{LCD} dependent from frequency.



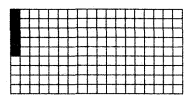
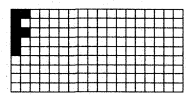
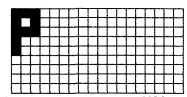
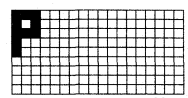
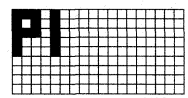
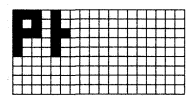
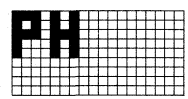
V_{DD1} = 1.8 V; V_{DD1} = 2.5 V; 2 × voltage multiplier; T_{amb} = 27 °C; TC = 0; BS = 111; no V_{LCD} load.

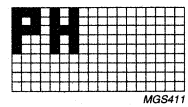
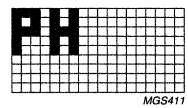
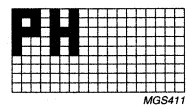
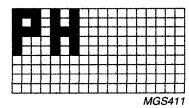
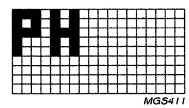
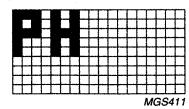
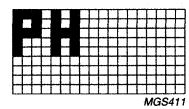
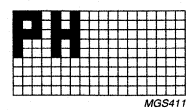
Fig.23 Internal V_{LCD}, icon mode.

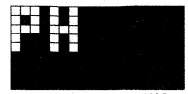
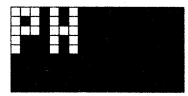
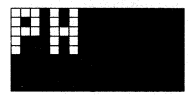
14 APPLICATION INFORMATION

Table 9 Programming example for PCF8531

STEP	SERIAL BUS BYTE								DISPLAY	OPERATION
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
1	0	1	1	1	1	0	SA0	0		start; slave address; R/$\overline{W}$ = 0
2	1	0	0	0	0	0	0	0		control byte; Co = 1; RS = 0
3	0	0	0	0	0	0	0	1		H[1:0] independent command; select function and RAM command page (H[1:0] = 00)
4	1	0	0	0	0	0	0	0		control byte; Co = 1; RS = 0
5	0	0	1	0	0	0	1	0		function and RAM command page PD = 0 and V = 1
6	1	0	0	0	0	0	0	0		control byte; Co = 1; RS = 0
7	0	0	0	0	1	0	0	1		function and RAM command page select display setting command page H[1:0] = 01
8	1	0	0	0	0	0	0	0		control byte; Co = 1; RS = 0
9	0	0	0	0	1	1	0	0		display setting command page; set normal mode (D = 1; IM = 0 and E = 0)
10	1	0	0	0	0	0	0	0		control byte; Co = 1; RS = 0
11	0	0	0	0	0	1	0	1		select Mux rate 1 : 34
12	1	0	0	0	0	0	0	0		control byte; Co = 1; RS = 0
13	0	0	0	0	0	0	0	1		H[2:0] independent command; select function and RAM command page H[1:0] = 00
14	1	0	0	0	0	0	0	0		control byte; Co = 1; RS = 0
15	0	0	0	0	1	0	1	0		function and RAM command page; select HV-gen command page H[1:0] = 10
16	1	0	0	0	0	0	0	0		control byte; Co = 1; RS = 0
17	0	0	0	0	1	0	1	1		HV-gen command page; select voltage multiplication factor 5 S[1:0] = 11
18	1	0	0	0	0	0	0	0		control byte; Co = 1; RS = 0
19	0	0	1	0	0	0	1	0		HV-gen command page; select temperature coefficient 2 TC[2:0] = 010
20	0	0	0	0	0	1	1	0		HV-gen command page; select high V_{LCD} programming range (PRS = 1); voltage multiplier off (HVE = 0)

STEP	SERIAL BUS BYTE								DISPLAY	OPERATION
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
21	1	0	0	0	0	0	0	0		control byte; Co = 1; RS = 0
22	1	0	1	0	0	0	0	0		HV-gen command page; set V_{LCD} = 7.71 V; V_{OP}[6:0] = 0100000
23	0	1	0	0	0	0	0	0		control byte; Co = 0; RS = 1
24	0	0	0	1	1	1	1	1	 MGS405	data write; Y and X are initialized to 0 by default, so they are not set here
25	0	0	0	0	0	1	0	1	 MGS406	data write
26	0	0	0	0	0	1	1	1	 MGS407	data write
27	0	0	0	0	0	0	0	0	 MGS407	data write
28	0	0	0	1	1	1	1	1	 MGS409	data write
29	0	0	0	0	0	1	0	0	 MGS410	data write
30	0	0	0	1	1	1	1	1	 MGS411	data write; last data and stop transmission

STEP	SERIAL BUS BYTE								DISPLAY	OPERATION
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
31	0	1	1	1	1	0	SA0	0	 MGS411	repeated start; slave address; R/$\overline{W}$ = 0
32	1	0	0	0	0	0	0	0	 MGS411	control byte; Co = 1; RS = 0
33	0	0	0	0	0	0	0	1	 MGS411	H[1:0] independent command; select function and RAM command page H[1:0] = 00
34	1	0	0	0	0	0	0	0	 MGS411	control byte; Co = 1; RS = 0
35	0	0	0	0	1	0	0	1	 MGS411	function and RAM command page; select display setting command page H[1:0] = 01
36	1	0	0	0	0	0	0	0	 MGS411	control byte; Co = 1; RS = 0
37	0	0	0	0	0	0	0	1	 MGS411	H[1:0] independent command; select function and RAM command page H[1:0] = 00
38	1	0	0	0	0	0	0	0	 MGS411	control byte; Co = 1; RS = 0

STEP	SERIAL BUS BYTE								DISPLAY	OPERATION
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
39	0	0	0	0	1	1	0	1	 MGS412	display control; set inverse video mode (D = 1; E = 1 and IM = 0)
40	1	0	0	0	0	0	0	0	 MGS412	control byte; Co = 1; RS = 0
41	1	0	0	0	0	0	0	0	 MGS412	set X address of RAM; set address to '0000000'
42	0	1	0	0	0	0	0	0	 MGS412	control byte; Co = 0; RS = 1
43	0	0	0	0	0	0	0	0	 MGS414	data write

The pinning of the PCF8531 is optimized for single plane wiring e.g. for chip-on-glass display modules. Display size: 34 × 128 pixels.

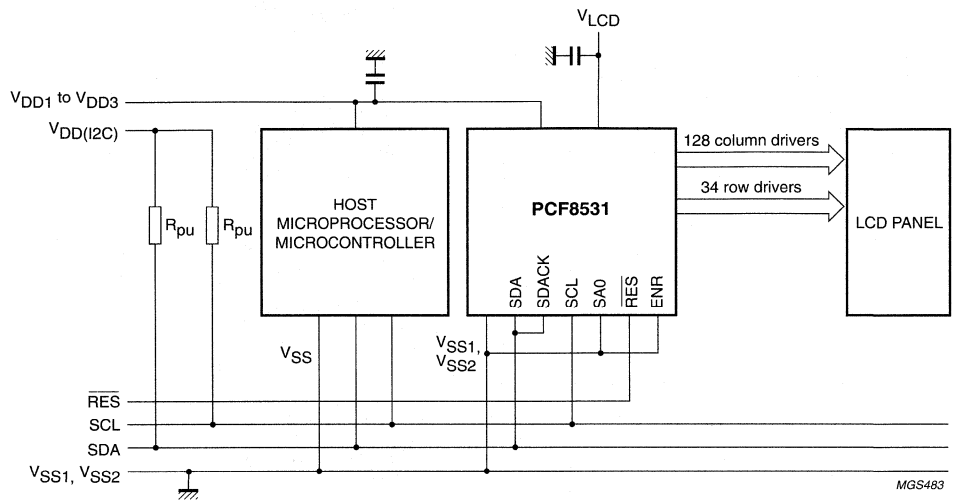


Fig.24 Typical system configuration.

The host microprocessor/microcontroller and the PCF8531 are both connected to the I²C-bus. The SDA and SCL lines must be connected to the positive power supply via pull-up resistors. The internal oscillator requires no external components. The appropriate intermediate biasing voltage for the multiplexed LCD waveforms are generated on-chip. The only other connections required to complete the system are to the power supplies (V_{DD}, V_{SS} and V_{LCD}) and suitable capacitors for decoupling V_{LCD} and V_{DD}.

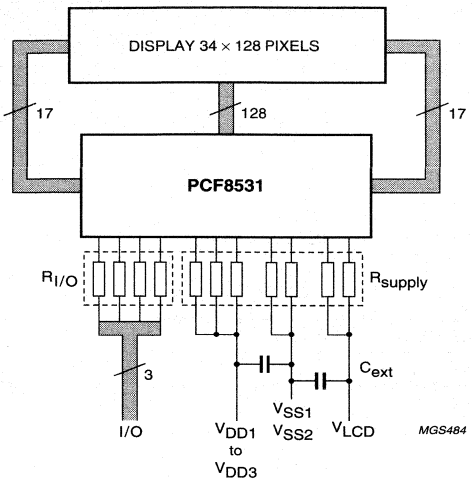


Fig.25 Chip-on-glass application.

The required minimum values for the external capacitors in an application with the PCF8531 are as follows:

- C_{ext} = 100 nF for V_{LCD} and V_{SS1} and V_{SS2}, and C_{ext} = 470 nF for V_{DD1} to V_{DD3} and V_{SS1} and V_{SS2}
- Higher capacitor values are recommended for ripple reduction
- For COG applications the recommended ITO track resistance is to be minimized for the I/O and supply connections. Optimized values for these tracks are below 50 Ω for the supply (R_{supply}) and below 100 Ω for the I/O connections ($R_{I/O}$).
- To reduce the sensitivity of the reset to ESD/EMC disturbances for a chip-on-glass application, it is strongly recommended to implement on the glass (ITO) a series input resistance in the reset line (recommended minimum value 8 kΩ). If the reset input is not used, it should be connected to V_{DD1} using a short connection.

15 BONDING PAD LOCATIONS

Table 10 Bonding pad location

All x and y coordinates are referenced to the centre of the chip (dimensions in μm; see Fig.28).

SYMBOL	PAD	x	y
dummy	1	+5973.6	−821.7
dummy	2	+5969.5	+823.4
dummy	3	+5899.5	+823.4
dummy	4	+5829.5	+823.4
dummy	5	+5479.5	+823.4
dummy	6	+5409.5	+823.4
dummy	7	+5059.5	+823.4
dummy	8	+4989.5	+823.4
dummy	9	+4639.5	+823.4
dummy	10	+4569.5	+823.4
dummy	11	+4219.5	+823.4
dummy	12	+4149.5	+823.4
dummy	13	+3799.5	+823.4
dummy	14	+3729.5	+823.4
OSC	15	+3449.5	+823.4
$V_{LCDSENSE}$	16	+3169.5	+823.4
V_{LCDOUT}	17	+3099.5	+823.4
V_{LCDOUT}	18	+3029.5	+823.4
V_{LCDOUT}	19	+2959.5	+823.4
V_{LCDOUT}	20	+2889.5	+823.4
V_{LCDOUT}	21	+2819.5	+823.4
V_{LCDOUT}	22	+2749.5	+823.4
V_{LCDOUT}	23	+2679.5	+823.4
V_{LCDIN}	24	+2539.5	+823.4
V_{LCDIN}	25	+2469.5	+823.4
V_{LCDIN}	26	+2399.5	+823.4
V_{LCDIN}	27	+2329.5	+823.4
V_{LCDIN}	28	+2259.5	+823.4
V_{LCDIN}	29	+2189.5	+823.4
V_{LCDIN}	30	+2119.5	+823.4
$\overline{RES}$	31	+1979.5	+823.4
V_{DD3}	32	+1699.5	+823.4
V_{DD3}	33	+1629.5	+823.4
V_{DD3}	34	+1559.5	+823.4
V_{DD2}	35	+1279.5	+823.4
V_{DD2}	36	+1209.5	+823.4
V_{DD2}	37	+1139.5	+823.4
V_{DD2}	38	+1069.5	+823.4
V_{DD2}	39	+999.5	+823.4
V_{DD2}	40	+929.5	+823.4
V_{DD2}	41	+859.5	+823.4
V_{DD2}	42	+789.5	+823.4
V_{DD1}	43	+649.5	+823.4
V_{DD1}	44	+579.5	+823.4
V_{DD1}	45	+509.5	+823.4
V_{DD1}	46	+439.5	+823.4
V_{DD1}	47	+369.5	+823.4
V_{DD1}	48	+299.5	+823.4
V_{DD1}	49	+229.5	+823.4
SDA	50	+19.5	+823.4
SDA	51	−50.5	+823.4
SDACK	52	−400.5	+823.4
dummy	53	−750.5	+823.4
SA0	54	−820.5	+823.4
ENR	55	−1100.5	+823.4
T4	56	−1380.5	+823.4
V_{SS2}	57	−1660.5	+823.4
V_{SS2}	58	−1730.5	+823.4
V_{SS2}	59	−1800.5	+823.4
V_{SS2}	60	−1870.5	+823.4
V_{SS2}	61	−1940.5	+823.4
V_{SS2}	62	−2010.5	+823.4
V_{SS2}	63	−2080.5	+823.4
V_{SS1}	64	−2220.5	+823.4
V_{SS1}	65	−2290.5	+823.4
V_{SS1}	66	−2360.5	+823.4
V_{SS1}	67	−2430.5	+823.4
V_{SS1}	68	−2500.5	+823.4
V_{SS1}	69	−2570.5	+823.4
V_{SS1}	70	−2640.5	+823.4
T3	71	−2780.5	+823.4
T1	72	−3060.5	+823.4
SCL	73	−3410.5	+823.4
SCL	74	−3480.5	+823.4
dummy	75	−3830.5	+823.4
dummy	76	−4180.5	+823.4
dummy	77	−4530.5	+823.4
T2	78	−4600.5	+823.4

SYMBOL	PAD	x	y
dummy	79	−4880.5	+823.4
dummy	80	−4950.5	+823.4
dummy	81	−5230.5	+823.4
dummy	82	−5300.5	+823.4
dummy	83	−5650.5	+823.4
dummy	84	−5720.5	+823.4
dummy	85	−5930.5	+823.4
dummy	86	−5926.4	−821.7
R0	87	−5786.4	−821.7
R2	88	−5716.4	−821.7
R4	89	−5646.4	−821.7
R6	90	−5576.4	−821.7
R8	91	−5506.4	−821.7
R10	92	−5436.4	−821.7
R12	93	−5366.4	−821.7
R14	94	−5296.4	−821.7
R16	95	−5226.4	−821.7
R18	96	−5156.4	−821.7
R20	97	−5086.4	−821.7
R22	98	−5016.4	−821.7
R24	99	−4946.4	−821.7
R26	100	−4876.4	−821.7
R28	101	−4806.4	−821.7
R30	102	−4736.4	−821.7
R32	103	−4666.4	−821.7
C0	104	−4526.4	−821.7
C1	105	−4456.4	−821.7
C2	106	−4386.4	−821.7
C3	107	−4316.4	−821.7
C4	108	−4246.4	−821.7
C5	109	−4176.4	−821.7
C6	110	−4106.4	−821.7
C7	111	−4036.4	−821.7
C8	112	−3966.4	−821.7
C9	113	−3896.4	−821.7
C10	114	−3826.4	−821.7
C11	115	−3756.4	−821.7
C12	116	−3686.4	−821.7
C13	117	−3616.4	−821.7
C14	118	−3546.4	−821.7
C15	119	−3476.4	−821.7

SYMBOL	PAD	x	y
C16	120	−3406.4	−821.7
C17	121	−3336.4	−821.7
C18	122	−3266.4	−821.7
C19	123	−3196.4	−821.7
C20	124	−3126.4	−821.7
C21	125	−3056.4	−821.7
C22	126	−2986.4	−821.7
C23	127	−2916.4	−821.7
C24	128	−2846.4	−821.7
C25	129	−2776.4	−821.7
C26	130	−2706.4	−821.7
C27	131	−2636.4	−821.7
C28	132	−2566.4	−821.7
C29	133	−2496.4	−821.7
C30	134	−2426.4	−821.7
C31	135	−2356.4	−821.7
C32	136	−2216.4	−821.7
C33	137	−2146.4	−821.7
C34	138	−2076.4	−821.7
C35	139	−2006.4	−821.7
C36	140	−1936.4	−821.7
C37	141	−1866.4	−821.7
C38	142	−1796.4	−821.7
C39	143	−1726.4	−821.7
C40	144	−1656.4	−821.7
C41	145	−1586.4	−821.7
C42	146	−1516.4	−821.7
C43	147	−1446.4	−821.7
C44	148	−1376.4	−821.7
C45	149	−1306.4	−821.7
C46	150	−1236.4	−821.7
C47	151	−1166.4	−821.7
C48	152	−1096.4	−821.7
C49	153	−1026.4	−821.7
C50	154	−956.4	−821.7
C51	155	−886.4	−821.7
C52	156	−816.4	−821.7
C53	157	−746.4	−821.7
C54	158	−676.4	−821.7
C55	159	−606.4	−821.7
C56	160	−536.4	−821.7

SYMBOL	PAD	x	y
C57	161	−466.4	−821.7
C58	162	−396.4	−821.7
C59	163	−326.4	−821.7
C60	164	−256.4	−821.7
C61	165	−186.4	−821.7
C62	166	−116.4	−821.7
C63	167	−46.4	−821.7
C64	168	+93.6	−821.7
C65	169	+163.6	−821.7
C66	170	+233.6	−821.7
C67	171	+303.6	−821.7
C68	172	+373.6	−821.7
C69	173	+443.6	−821.7
C70	174	+513.6	−821.7
C71	175	+583.6	−821.7
C72	176	+653.6	−821.7
C73	177	+723.6	−821.7
C74	178	+793.6	−821.7
C75	179	+863.6	−821.7
C76	180	+933.6	−821.7
C77	181	+1003.6	−821.7
C78	182	+1073.6	−821.7
C79	183	+1143.6	−821.7
C80	184	+1213.6	−821.7
C81	185	+1283.6	−821.7
C82	186	+1353.6	−821.7
C83	187	+1423.6	−821.7
C84	188	+1493.6	−821.7
C85	189	+1563.6	−821.7
C86	190	+1633.6	−821.7
C87	191	+1703.6	−821.7
C88	192	+1773.6	−821.7
C89	193	+1843.6	−821.7
C90	194	+1913.6	−821.7
C91	195	+1983.6	−821.7
C92	196	+2053.6	−821.7
C93	197	+2123.6	−821.7
C94	198	+2193.6	−821.7
C95	199	+2263.6	−821.7
C96	200	+2403.6	−821.7
C97	201	+2473.6	−821.7

SYMBOL	PAD	x	y
C98	202	+2543.6	−821.7
C99	203	+2613.6	−821.7
C100	204	+2683.6	−821.7
C101	205	+2753.6	−821.7
C102	206	+2823.6	−821.7
C103	207	+2893.6	−821.7
C104	208	+2963.6	−821.7
C105	209	+3033.6	−821.7
C106	210	+3103.6	−821.7
C107	211	+3173.6	−821.7
C108	212	+3243.6	−821.7
C109	213	+3313.6	−821.7
C110	214	+3383.6	−821.7
C111	215	+3453.6	−821.7
C112	216	+3523.6	−821.7
C113	217	+3593.6	−821.7
C114	218	+3663.6	−821.7
C115	219	+3733.6	−821.7
C116	220	+3803.6	−821.7
C117	221	+3873.6	−821.7
C118	222	+3943.6	−821.7
C119	223	+4013.6	−821.7
C120	224	+4083.6	−821.7
C121	225	+4153.6	−821.7
C122	226	+4223.6	−821.7
C123	227	+4293.6	−821.7
C124	228	+4363.6	−821.7
C125	229	+4433.6	−821.7
C126	230	+4503.6	−821.7
C127	231	+4573.6	−821.7
R33	232	+4713.6	−821.7
R31	233	+4783.6	−821.7
R29	234	+4853.6	−821.7
R27	235	+4923.6	−821.7
R25	236	+4993.6	−821.7
R23	237	+5063.6	−821.7
R21	238	+5133.6	−821.7
R19	239	+5203.6	−821.7
R17	240	+5343.6	−821.7
R15	241	+5413.6	−821.7
R13	242	+5483.6	−821.7

SYMBOL	PAD	x	y
R11	243	+5553.6	−821.7
R9	244	+5623.6	−821.7
R7	245	+5693.6	−821.7
R5	246	+5763.6	−821.7
R3	247	+5833.6	−821.7
R1	248	+5903.6	−821.7

Table 11 Bonding pads

PAD	SIZE	UNIT
Pad pitch	min. 70	µm
Pad size; Al	62 × 100	µm
Bump dimensions	50 × 90 × 17.5 (±5)	µm
Wafer thickness (excluding bumps)	381	µm

Table 12 Alignment marks

MARKS	x	y
C1	−5402.0	+823.1
C2	+5292.4	+823.4
F	+5890.3	+401.9
Circle 1	−5543.0	+798.4
Circle 2	+5637.4	+798.4

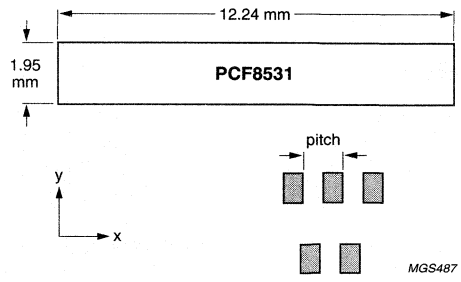


Fig.26 Bonding pads.

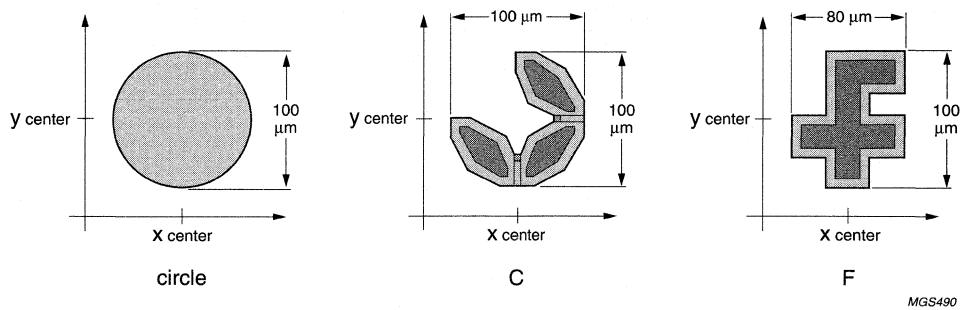


Fig.27 Shapes of recognition pattern.

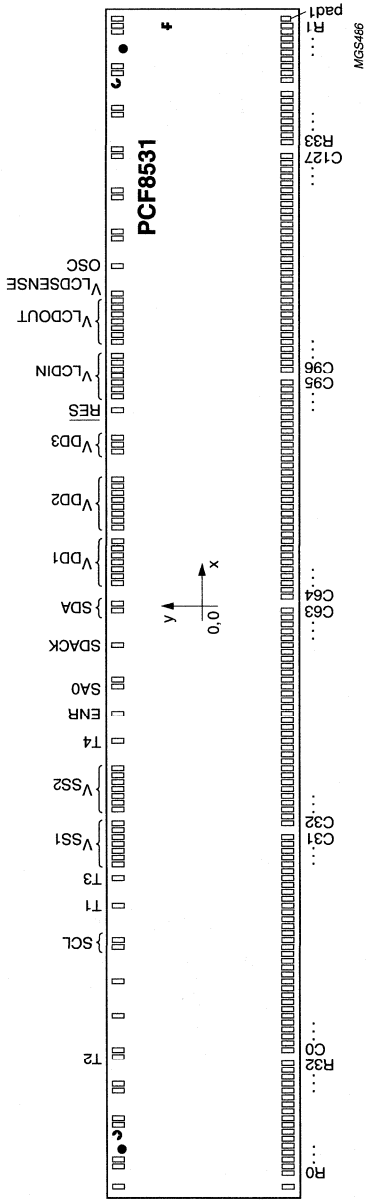


Fig.28 Bonding pad location.

The positioning of the bonding pads is not to scale.

16 DEVICE PROTECTION DIAGRAM

For all diagrams: the maximum forward current is 5 mA and the maximum reverse voltage is 5 V.

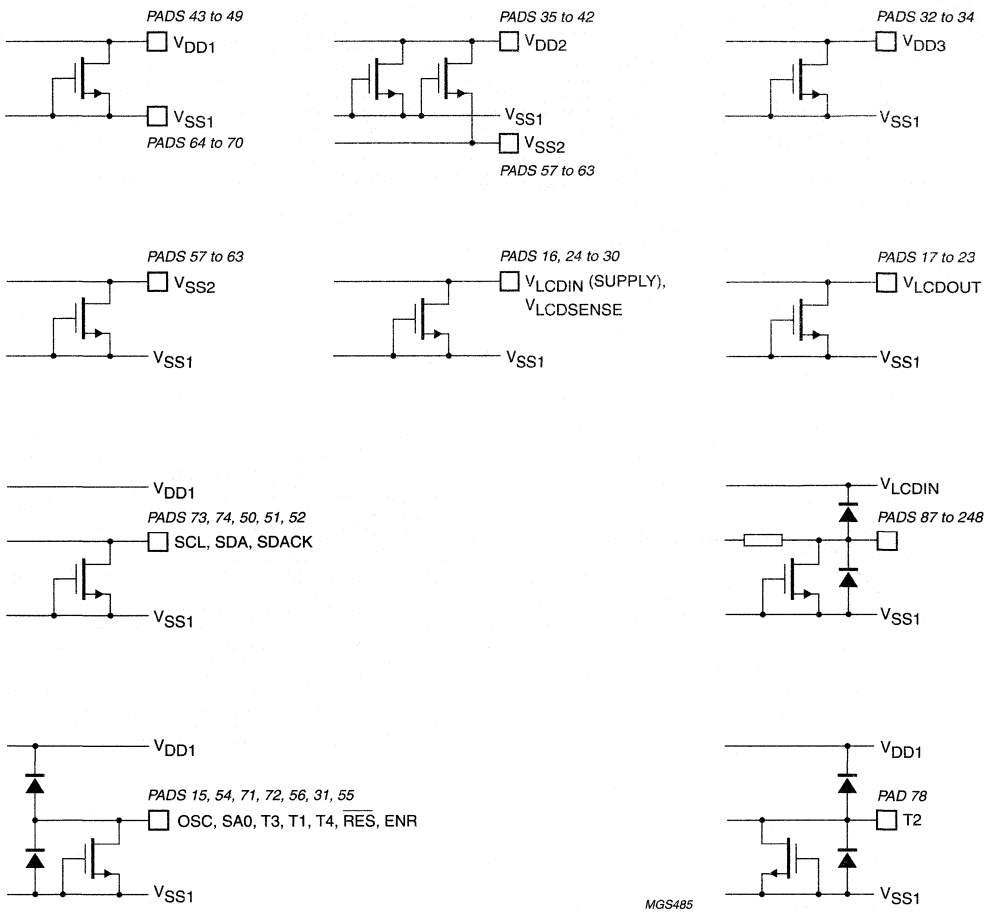
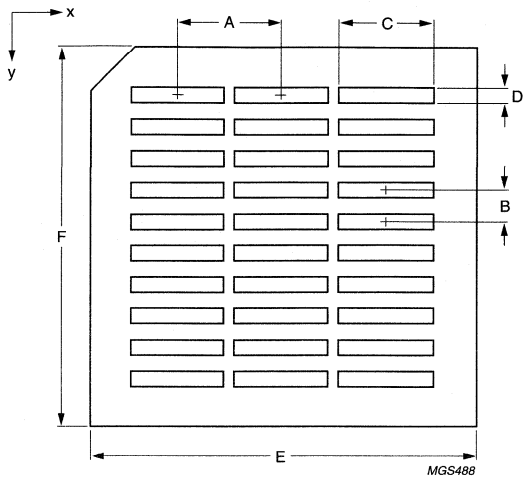


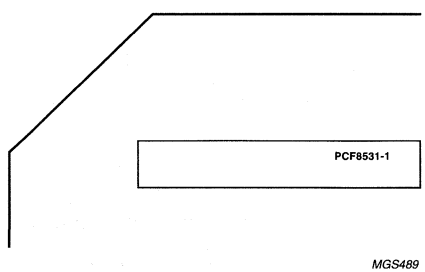
Fig.29 Device protection diagrams.

17 TRAY INFORMATION



The dimensions are given in Table 13.

Fig.30 Tray details.



The orientation of the IC in a pocket is indicated by the position of the IC type name on the die surface with respect to the chamfer on the upper left corner of the tray. Refer to the bonding pad location diagram for the orientating and position of the type name on the die surface.

Fig.31 Tray alignment.

Table 13 Dimensions

DIM.	DESCRIPTION	VALUE
A	pocket pitch; x direction	13.72 mm
B	pocket pitch; y direction	4.17 mm
C	pocket width; x direction	12.34 mm
D	pocket width; y direction	2.05 mm
E	tray width; x direction	50.8 mm
F	tray width; y direction	50.8 mm
x	number of pockets in x direction	3
y	number of pockets in y direction	10

Universal LCD driver for low multiplex rates PCF8533

CONTENTS

Universal LCD driver for low multiplex rates PCF8533

1 FEATURES

- Single-chip LCD controller/driver
- Selectable backplane drive configuration: static or 2/3/4 backplane multiplexing
- Selectable display bias configuration: static, $\frac{1}{2}$ or $\frac{1}{3}$
- Internal LCD bias generation with voltage-follower buffers
- 80 segment drives: up to forty 8-segment numeric characters; up to twentyone 15-segment alphanumeric characters; or any graphics of up to 320 elements
- 80 × 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- LCD and logic supplies may be separated
- Wide power supply range: from 1.8 to 5.5 V
- Wide LCD supply range: from 2.5 V for low threshold LCDs and up to 6.5 V for guest-host LCDs and high threshold (automobile) twisted nematic LCDs
- Low power consumption
- 400 kHz I²C-bus interface
- TTL/CMOS compatible
- Compatible with 4-bit, 8-bit or 16-bit microprocessors/microcontrollers
- May be cascaded for large LCD applications (up to 5120 segments possible)
- No external components
- Compatible with Chip-On-Glass (COG) technology
- Manufactured in silicon gate CMOS process.

2 GENERAL DESCRIPTION

The PCF8533 is a peripheral device which interfaces to almost any Liquid Crystal Display (LCD) with low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 80 segments and can easily be cascaded for larger LCD applications. The PCF8533 is compatible with most microprocessors/microcontrollers and communicates via a two-line bidirectional I²C-bus. Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8533U	–	chip with bumps in tray	–

4 BLOCK DIAGRAM

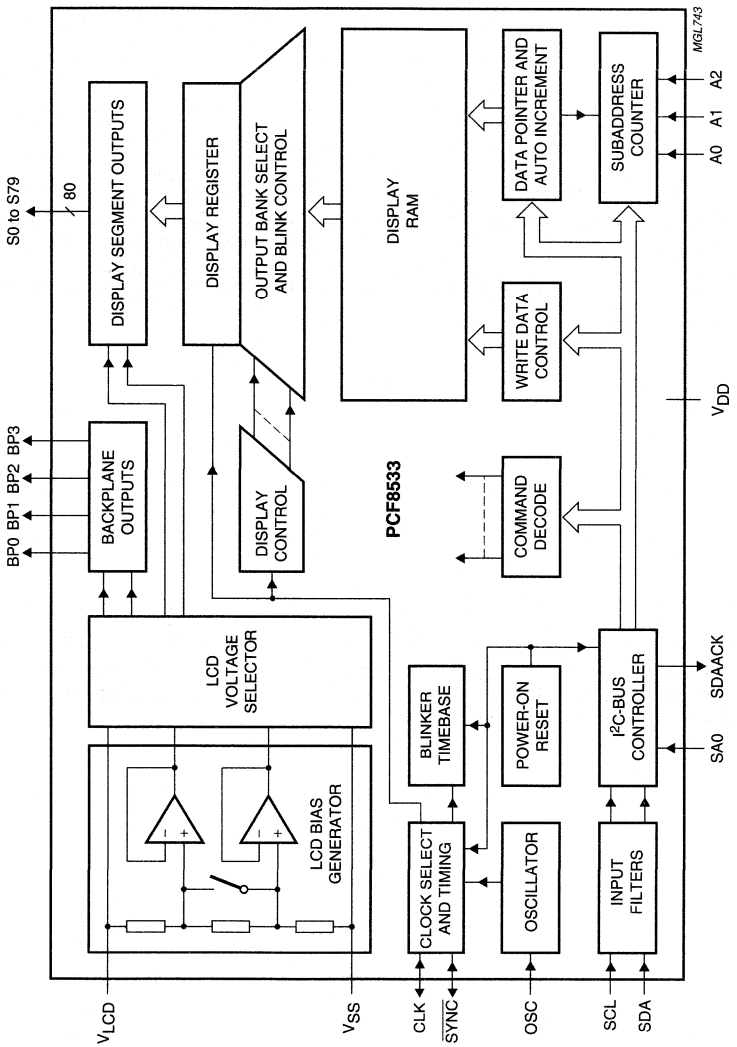


Fig.1 Block diagram.

5 PINNING

SYMBOL	PAD	DESCRIPTION
SDAACK	1	I²C-bus acknowledge output; note 1
SDA	2 and 3	I²C-bus serial data input; note 1
SCL	4 and 5	I²C-bus serial clock input
CLK	6	external clock input/output
V_{DD}	7	supply voltage
$\overline{SYNC}$	8	cascade synchronization input/output
OSC	9	internal oscillator enable input
A0, A1 and A2	10, 11 and 12	subaddress inputs
SA0	13	I²C-bus slave address input; bit 0
V_{SS}	14	logic ground
V_{LCD}	15	LCD supply voltage
BP0, BP1, BP2 and BP3	17, 99, 16 and 98	LCD backplane outputs
S0 to S79	18 to 97	LCD segment outputs

Note

1. For most applications SDA and SDAACK will be shorted together; see Chapter 7.

6 FUNCTIONAL DESCRIPTION

The PCF8533 is a versatile peripheral device designed to interface any microprocessor/microcontroller to a wide variety of LCDs. It can directly drive any static or multiplexed LCD containing up to four backplanes and up to 80 segments. The display configurations possible with the PCF8533 depend on the number of active backplane outputs required; a selection of display configurations is given in Table 1.

All of the display configurations given in Table 1 can be implemented in the typical system shown in Fig.2.

The host microprocessor/microcontroller maintains the 2-line I²C-bus communication channel with the PCF8533. The internal oscillator is selected by connecting pad OSC to V_{SS}. The appropriate biasing voltages for the multiplexed LCD waveforms are generated internally. The only other connections required to complete the system are to the power supplies (V_{DD}, V_{SS} and V_{LCD}) and the LCD panel selected for the application.

Table 1 Selection of display configurations

NUMBER OF		7-SEGMENTS NUMERIC		14-SEGMENTS ALPHANUMERIC		DOT MATRIX
BACKPLANES	SEGMENTS	DIGITS	INDICATOR SYMBOLS	CHARACTERS	INDICATOR SYMBOLS	
4	320	40	40	20	40	320 dots (4 × 80)
3	240	30	30	16	16	240 dots (3 × 80)
2	160	20	20	10	20	160 dots (2 × 80)
1	80	10	10	5	10	80 dots (1 × 80)

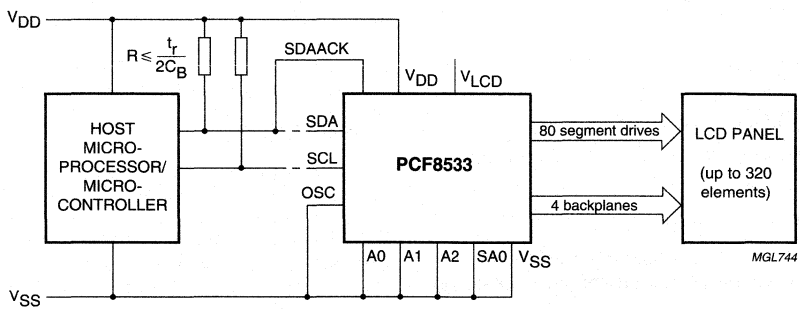


Fig.2 Typical system configuration.

6.1 Power-on reset

At Power-on the PCF8533 resets to a starting condition as follows:

1. All backplane outputs are set to V_{LCD}.
2. All segment outputs are set to V_{LCD}.
3. The drive mode '1 : 4 multiplex with $\frac{1}{3}$bias' is selected.
4. Blinking is switched off.
5. Input and output bank selectors are reset (as defined in Table 5).
6. The I²C-bus interface is initialized.
7. The data pointer and the subaddress counter are cleared.
8. Display disabled.

Data transfers on the I²C-bus should be avoided for 1 ms following Power-on to allow completion of the reset action.

6.2 LCD bias generator

Fractional LCD biasing voltages are obtained from an internal voltage divider of the three series resistors connected between V_{LCD} and V_{SS}. The centre resistor can be switched out of the circuit to provide a $\frac{1}{2}$bias voltage level for the 1 : 2 multiplex configuration.

6.3 LCD voltage selector

The LCD voltage selector co-ordinates the multiplexing of the LCD in accordance with the selected LCD drive configuration. The operation of the voltage selector is controlled by MODE SET commands from the command decoder.

The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of V_{OP} and the resulting discrimination ratios (D), are given in Table 2.

A practical value for V_{OP} is determined by equating $V_{off(rms)}$ with a defined LCD threshold voltage (V_{th}), typically when the LCD exhibits approximately 10% contrast. In the static drive mode a suitable choice is $V_{OP} > 3V_{th}$.

Multiplex drive ratios of 1 : 3 and 1 : 4 with $\frac{1}{2}$bias are possible but the discrimination and hence the contrast ratios are smaller ($\sqrt{3} = 1.732$ for 1 : 3 multiplex or $\frac{\sqrt{21}}{3} = 1.528$ for 1 : 4 multiplex).

The advantage of these modes is a reduction of the LCD full-scale voltage V_{OP} as follows:

- 1 : 3 multiplex ($\frac{1}{2}$bias):

  $V_{OP} = \sqrt{6} \times V_{off(rms)} = 2.449 V_{off(rms)}$

- 1 : 4 multiplex ($\frac{1}{2}$bias):

  $V_{OP} = \left[\frac{(4 \times \sqrt{3})}{3}\right] = 2.309 V_{off(rms)}$

These compare with $V_{OP} = 3V_{off(rms)}$ when $\frac{1}{3}$bias is used.
Note: $V_{OP} = V_{LCD}$.

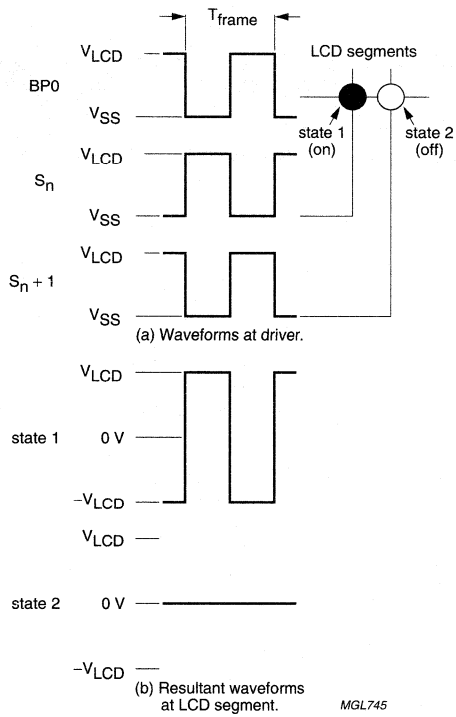
Table 2 Preferred LCD drive modes: summary of characteristics

LCD DRIVE MODE	NUMBER OF		LCD BIAS CONFIGURATION	$\frac{V_{off(rms)}}{V_{OP}}$	$\frac{V_{on(rms)}}{V_{OP}}$	$D = \frac{V_{on(rms)}}{V_{off(rms)}}$
	BACKPLANES	LEVELS				
static	1	2	static	0	1	∞
1 : 2	2	3	$\frac{1}{2}$	0.354	0.791	2.236
1 : 2	2	4	$\frac{1}{3}$	0.333	0.745	2.236
1 : 3	3	4	$\frac{1}{3}$	0.333	0.638	1.915
1 : 4	4	4	$\frac{1}{3}$	0.333	0.577	1.732

6.4 LCD drive mode waveforms

6.4.1 STATIC DRIVE MODE

The static LCD drive mode is used when a single backplane is provided in the LCD. Backplane and segment drive waveforms for this mode are shown in Fig.3.

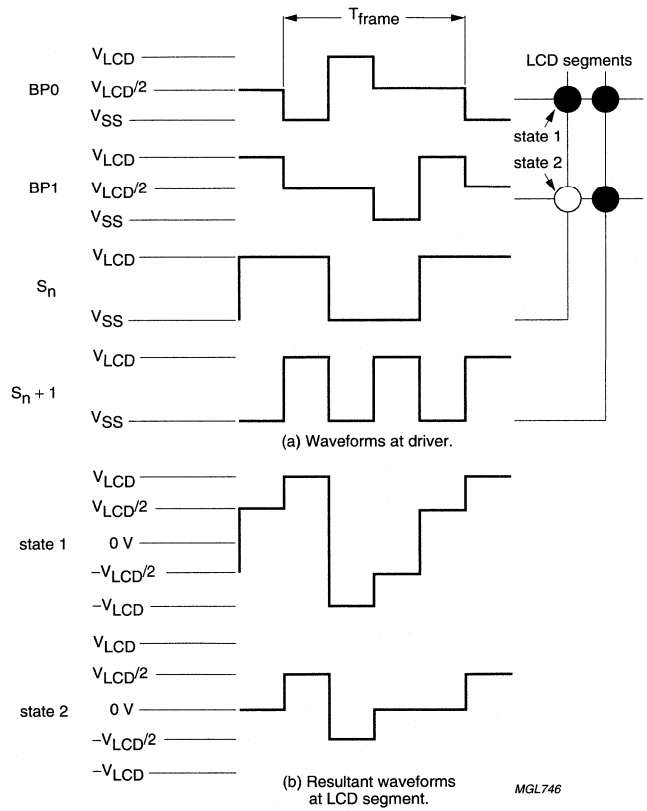


$V_{state1}(t) = V_{sn}(t) - V_{BP0}(t)$.
$V_{on(rms)} = V_{LCD}$.
$V_{state2}(t) = V_{sn+1}(t) - V_{BP0}(t)$.
$V_{off(rms)} = 0$ V.

Fig.3 Static drive mode waveforms.

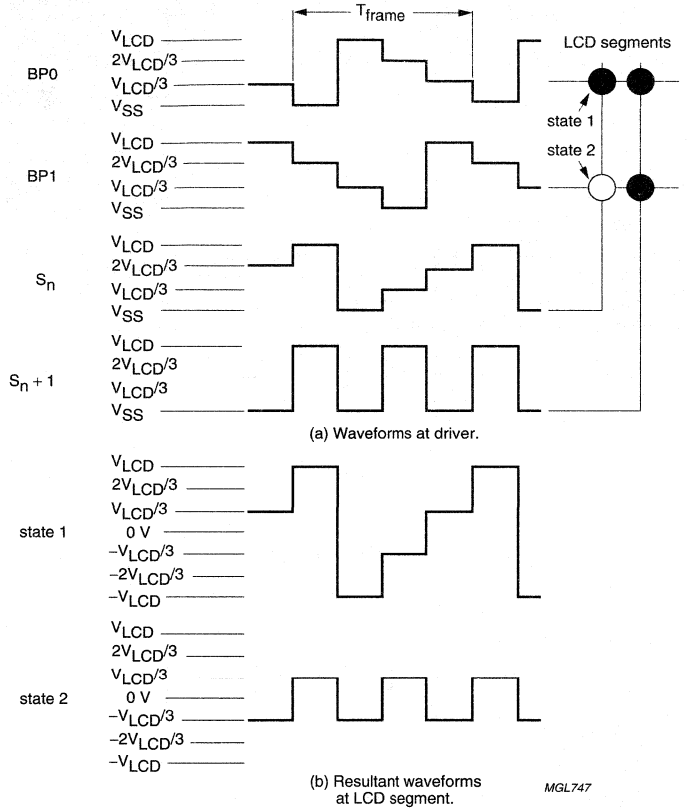
6.4.2 1 : 2 MULTIPLEX DRIVE MODE

When two backplanes are provided in the LCD, the 1 : 2 multiplex mode applies. The PCF8533 allows the use of ½bias or ⅓bias in this mode as shown in Figs 4 and 5.



$V_{state1}(t) = V_{sn}(t) - V_{BP0}(t)$.
$V_{on(rms)} = 0.791V_{LCD}$.
$V_{state2}(t) = V_{sn}(t) - V_{BP1}(t)$.
$V_{off(rms)} = 0.354V_{LCD}$.

Fig.4 Waveforms for the 1 : 2 multiplex drive mode with ½bias.

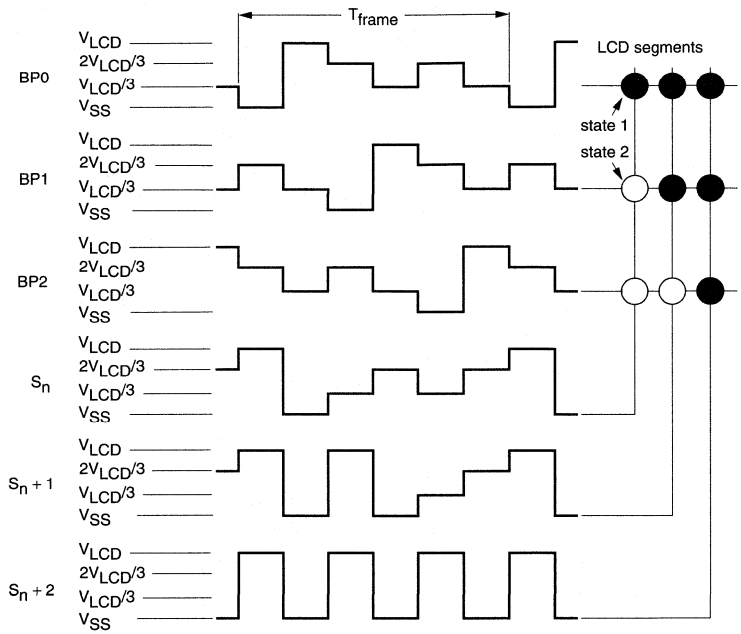


$V_{state1}(t) = V_{sn}(t) - V_{BP0}(t)$.
$V_{on(rms)} = 0.745V_{LCD}$.
$V_{state2}(t) = V_{sn}(t) - V_{BP1}(t)$.
$V_{off(rms)} = 0.333V_{LCD}$.

Fig.5 Waveforms for the 1 : 2 multiplex drive mode with 1/3 bias.

6.4.3 1 : 3 MULTIPLEX DRIVE MODE

When three backplanes are provided in the LCD, the 1 : 3 multiplex drive mode applies, as shown in Fig.6.

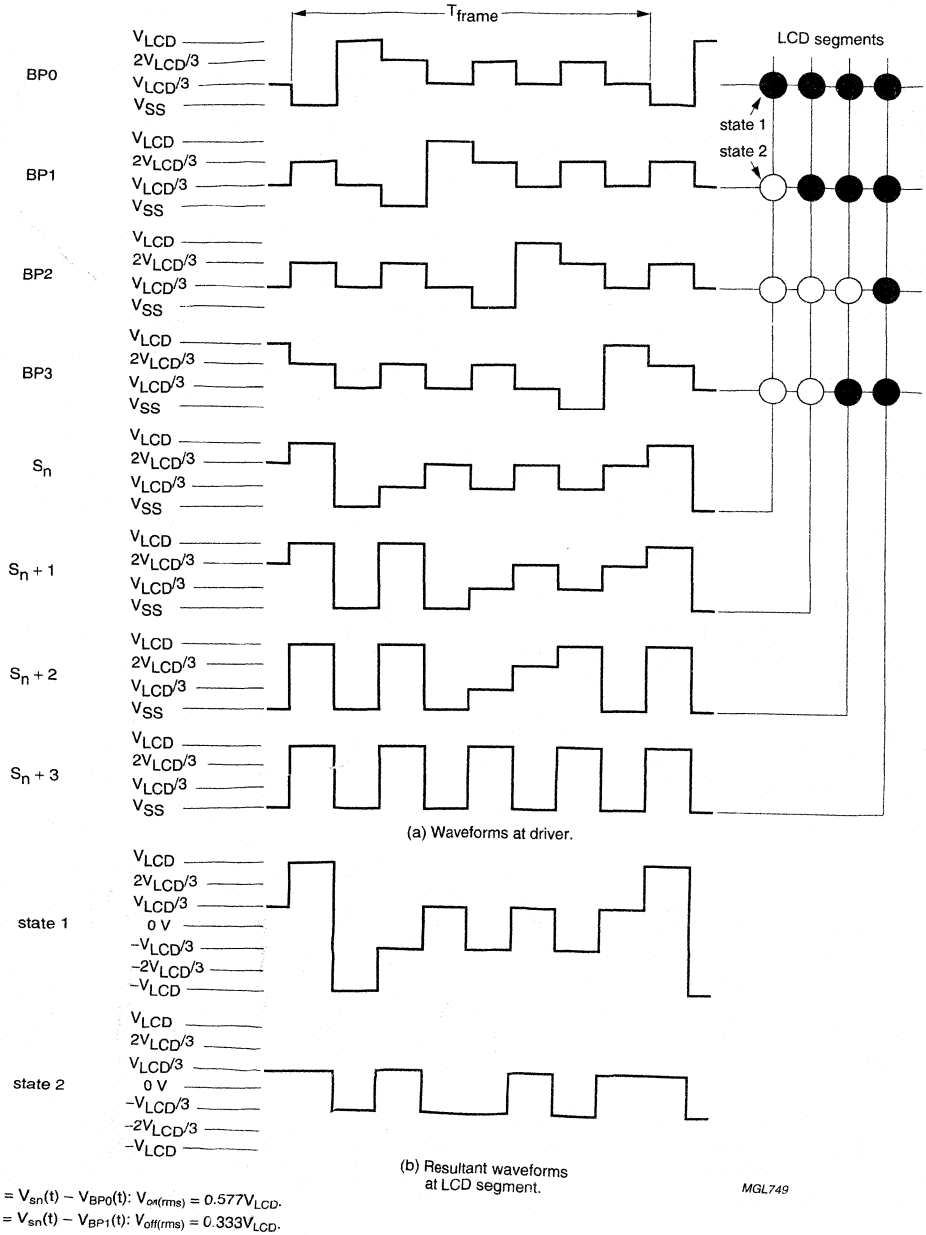


$V_{state1}(t) = V_{sn}(t) - V_{BP0}(t)$.
$V_{on(rms)} = 0.638V_{LCD}$.
$V_{state2}(t) = V_{sn}(t) - V_{BP1}(t)$.
$V_{off(rms)} = 0.333V_{LCD}$.

Fig.6 Waveforms for the 1 : 3 multiplex drive mode.

6.4.4 1 : 4 MULTIPLEX DRIVE MODE

When four backplanes are provided in the LCD, the 1 : 4 multiplex drive mode applies, as shown in Fig.7.



$V_{state1}(t) = V_{sn}(t) - V_{BP0}(t)$: $V_{on(rms)} = 0.577V_{LCD}$.
$V_{state2}(t) = V_{sn}(t) - V_{BP1}(t)$: $V_{off(rms)} = 0.333V_{LCD}$.

Fig.7 Waveforms for the 1 : 4 multiplex drive mode.

6.5 Oscillator

6.5.1 INTERNAL CLOCK

The internal logic and the LCD drive signals of the PCF8533 are timed either by the built-in oscillator or from an external clock. When the internal oscillator is used, pad OSC should be connected to V_{SS}. In this event, the output from pad CLK provides the clock signal for cascaded PCF8533s in the system. After power-up, SDA must be HIGH to guarantee that the clock starts.

6.5.2 EXTERNAL CLOCK

The condition for external clock is made by tying pad OSC to V_{DD}; pad CLK then becomes the external clock input.

The clock frequency (f_{CLK}) determines the LCD frame frequency.

A clock signal must always be supplied to the device; removing the clock may freeze the LCD in a DC state.

6.6 Timing

The timing of the PCF8533 organizes the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. In cascaded applications, the synchronization signal ($\overline{SYNC}$) maintains the correct timing relationship between the PCF8533s in the system. The timing also generates the LCD frame frequency which it derives as an integer division of the clock frequency (see Table 3). The frame frequency is a fixed division of the internal clock or of the frequency applied to pad CLK when an external clock is used.

6.7 Display register

The display latch holds the display data while the corresponding multiplex signals are generated. There is a one-to-one relationship between the data in the display latch, the LCD segment outputs and one column of the display RAM.

6.8 Segment outputs

The LCD drive section includes 80 segment outputs (S0 to S79) which should be connected directly to the LCD. The segment output signals are generated in accordance with the multiplexed backplane signals and with data resident in the display latch. When less than 80 segment outputs are required the unused segment outputs should be left open-circuit.

6.9 Backplane outputs

The LCD drive section includes four backplane outputs BP0 to BP3 which should be connected directly to the LCD. The backplane output signals are generated in accordance with the selected LCD drive mode. If less than four backplane outputs are required the unused outputs can be left open-circuit. In the 1 : 3 multiplex drive mode BP3 carries the same signal as BP1, therefore these two adjacent outputs can be tied together to give enhanced drive capabilities. In the 1 : 2 multiplex drive mode BP0 and BP2, BP1 and BP3 respectively carry the same signals and may also be paired to increase the drive capabilities. In the static drive mode the same signal is carried by all four backplane outputs and they can be connected in parallel for very high drive requirements.

6.10 Display RAM

The display RAM is a static 80 × 4-bit RAM which stores LCD data. A logic 1 in the RAM bit map indicates the on-state of the corresponding LCD segment; similarly, a logic 0 indicates the off-state. There is a one-to-one correspondence between the RAM addresses and the segment outputs, and between the individual bits of a RAM word and the backplane outputs. The first RAM column corresponds to the 80 segments operated with respect to backplane BP0 (see Fig.8). In multiplexed LCD applications the segment data of the second, third and fourth column of the display RAM are time-multiplexed with BP1, BP2 and BP3 respectively.

When display data is transmitted to the PCF8533 the display bytes received are stored in the display RAM in accordance with the selected LCD drive mode. The data is stored as it arrives and does not wait for the acknowledge cycle as with the commands. Depending on the current mux mode data is stored singularly, in pairs, triplets or quadruplets. e.g. in 1 : 2 mux mode the RAM data is stored every second bit. To illustrate the filling order, an example of a 7-segment numeric display showing all drive modes is given in Fig.9; the RAM filling organization depicted applies equally to other LCD types. With reference to Fig.9, in the static drive mode the eight transmitted data bits are placed in bit 0 of eight successive display RAM addresses. In the 1 : 2 multiplex drive mode the eight transmitted data bits are placed in bits 0 and 1 of four successive display RAM addresses.

In the 1 : 3 multiplex drive mode these bits are placed in bits 0, 1 and 2 of three successive addresses, with bit 2 of the third address left unchanged. This last bit may, if necessary, be controlled by an additional transfer to this address but care should be taken to avoid overriding adjacent data because full bytes are always transmitted. In the 1 : 4 multiplex drive mode the eight transmitted data bits are placed in bits 0, 1, 2 and 3 of two successive display RAM addresses.

Table 3 LCD frame frequencies

FRAME FREQUENCY	NOMINAL FRAME FREQUENCY (Hz)
$\frac{f_{CLK}}{24}$	64

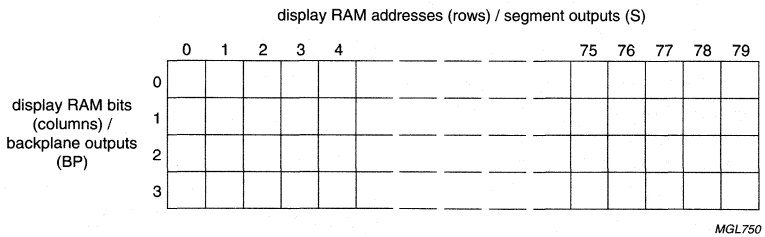


Fig.8 Display RAM bit map showing direct relationship between display RAM addresses and segment outputs, and between bits in a RAM word and backplane outputs.

6.11 Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the data pointer by the LOAD DATA POINTER command. Following this, an arriving data byte is stored starting at the display RAM address indicated by the data pointer thereby observing the filling order shown in Fig.9. The data pointer is automatically incremented in accordance with the chosen LCD configuration. That is, after each byte is stored, the contents of the data pointer are incremented by eight (static drive mode), by four (1 : 2 multiplex drive mode), by three (1 : 3 multiplex drive mode) or by two (1 : 4 multiplex drive mode). If an I²C-bus data access is terminated early then the state of the data pointer will be unknown. The data pointer should be re-written prior to further RAM accesses.

6.12 Subaddress counter

The storage of display data is conditioned by the contents of the subaddress counter. Storage is allowed to take place only when the contents of the subaddress counter agree with the hardware subaddress applied to A0, A1 and A2. The subaddress counter value is defined by the DEVICE SELECT command. If the contents of the subaddress counter and the hardware subaddress do not agree then data storage is inhibited but the data pointer is incremented as if data storage had taken place. The subaddress counter is also incremented when the data pointer overflows.

The storage arrangements described lead to extremely efficient data loading in cascaded applications. When a series of display bytes are sent to the display RAM, automatic wrap-over to the next PCF8533 occurs when the last RAM address is exceeded. Subaddressing across device boundaries is successful even if the change to the next device in the cascade occurs within a transmitted character (such as during the 27th display data byte transmitted in 1 : 3 multiplex mode).

The hardware subaddress should not be changed whilst the device is being accessed on the I²C-bus interface.

6.13 Output bank selector

The output bank selector selects one of the four bits per display RAM address for transfer to the display latch. The actual bit selected depends on the particular LCD drive mode in operation and on the instant in the multiplex sequence.

In 1 : 4 multiplex, all RAM addresses of bit 0 are selected, these are followed by the contents of bit 1, bit 2 and then bit 3. Similarly in 1 : 3 multiplex, bits 0, 1 and 2 are selected sequentially. In 1 : 2 multiplex, bits 0 and 1 are selected and, in the static mode, bit 0 is selected. The $\overline{\text{SYNC}}$ signal will reset these sequences to the following starting points; bit 3 for 1 : 4 multiplex, bit 2 for 1 : 3 multiplex, bit 1 for 1 : 2 multiplex and bit 0 for static mode.

The PCF8533 includes a RAM bank switching feature in the static and 1 : 2 multiplex drive modes. In the static drive mode, the BANK SELECT command may request the contents of bit 2 to be selected for display instead of the contents of bit 0. In the 1 : 2 drive mode, the contents of bits 2 and 3 may be selected instead of bits 0 and 1. This gives the provision for preparing display information in an alternative bank and to be able to switch to it once it is assembled.

6.14 Input bank selector

The input bank selector loads display data into the display RAM in accordance with the selected LCD drive configuration. Display data can be loaded in bit 2 in static drive mode or in bits 2 and 3 in 1 : 2 drive mode by using

the BANK SELECT command. The input bank selector functions independently to the output bank selector.

6.15 Blinker

The display blinking capabilities of the PCF8533 are very versatile. The whole display can be blinked at frequencies selected by the BLINK command. The blinking frequencies are integer multiples of the clock frequency. The ratios between the clock and blinking frequencies depend on the mode in which the device is operating, see Table 4.

An additional feature is for an arbitrary selection of LCD segments to be blinked. This applies to the static and 1 : 2 LCD drive modes and can be implemented without any communication overheads. By means of the output bank selector, the displayed RAM banks are exchanged with alternate RAM banks at the blinking frequency. This mode can also be specified by the BLINK command.

In the 1 : 3 and 1 : 4 multiplex modes, where no alternate RAM bank is available, groups of LCD segments can be blinked by selectively changing the display RAM data at fixed time intervals.

If the entire display is to be blinked at a frequency other than the nominal blinking frequency, this can be effectively performed by resetting and setting the display enable bit E at the required rate using the MODE SET command.

Table 4 Blinking frequencies

BLINKING MODE	NORMAL OPERATING MODE RATIO	NOMINAL BLINKING FREQUENCY
Off	–	blinking off
2 Hz	$\frac{f_{CLK}}{768}$	2 Hz
1 Hz	$\frac{f_{CLK}}{1536}$	1 Hz
0.5 Hz	$\frac{f_{CLK}}{3072}$	0.5 Hz

X = data bit unchanged.

Fig.9 Relationships between LCD layout, drive mode, display RAM filling order and display data transmitted over the I²C-bus.

7 CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a Serial Data line (SDA) and a Serial Clock Line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

By connecting SDAACK to SDA on the PCF8533, the SDA line becomes fully I²C-bus compatible. Having the acknowledge output separated from the serial data line is advantageous in Chip-On-Glass (COG) applications. In COG applications where the track resistance from the SDAACK pad to the system SDA line can be significant, a potential divider is generated by the bus pull-up resistor and the Indium Tin Oxide (ITO) track resistance. It is possible that during the acknowledge cycle the PCF8533 will not be able to create a valid logic 0 level. By splitting the SDA input from the output the device could be used in a mode that ignores the acknowledge bit. In COG applications where the acknowledge cycle is required, it is necessary to minimize the track resistance from the SDAACK pad to the system SDA line to guarantee a valid low level.

The following definition assumes SDA and SDAACK are connected and refers to the pair as SDA.

7.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal. Bit transfer is illustrated in Fig.10.

7.2 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P). The START and STOP conditions are illustrated in Fig.11.

7.3 System configuration

A device generating a message is a 'transmitter', a device receiving a message is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves'. The system configuration is illustrated in Fig.12.

7.4 Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition. Acknowledgement on the I²C-bus is illustrated in Fig.13.

7.5 PCF8533 I²C-bus controller

The PCF8533 acts as an I²C-bus slave receiver. It does not initiate I²C-bus transfers or transmit data to an I²C-bus master receiver. The only data output from the PCF8533 are the acknowledge signals of the selected devices. Device selection depends on the I²C-bus slave address, on the transferred command data and on the hardware subaddress.

In single device application, the hardware subaddress inputs A0, A1 and A2 are normally tied to V_{SS} which defines the hardware subaddress 0. In multiple device applications A0, A1 and A2 are tied to V_{SS} or V_{DD} in accordance with a binary coding scheme such that no two devices with a common I²C-bus slave address have the same hardware subaddress.

7.6 Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

7.7 I²C-bus protocol

Two I²C-bus slave addresses (01110000 and 01110010) are reserved for the PCF8533. The least significant bit of the slave address that a PCF8533 will respond to is defined by the level tied at its input SA0. The PCF8533 is a write only device and will not respond to a read access. Therefore, two types of PCF8533 can be distinguished on the same I²C-bus which allows:

1. Up to 16 PCF8533s on the same I²C-bus for very large LCD applications
2. The use of two types of LCD multiplex on the same I²C-bus.

The I²C-bus protocol is shown in Fig.14. The sequence is initiated with a START condition (S) from the I²C-bus master which is followed by one of the two PCF8533 slave addresses available. All PCF8533s with the corresponding SA0 level acknowledge in parallel to the slave address, but all PCF8533s with the alternative SA0 level ignore the whole I²C-bus transfer.

After acknowledgement, a control byte follows which defines if the next byte is RAM or command information. The control byte also defines if the next following byte is a control byte or further RAM/command data.

In this way it is possible to configure the device then fill the display RAM with little overhead.

The command bytes and control bytes are also acknowledged by all addressed PCF8533s connected to the bus.

The display bytes are stored in the display RAM at the address specified by the data pointer and the subaddress counter. Both data pointer and subaddress counter are automatically updated and the data is directed to the intended PCF8533 device.

The acknowledgement after each byte is made only by the (A0, A1 and A2) addressed PCF8533. After the last display byte, the I²C-bus master issues a STOP condition (P). Alternatively a START may be issued to RESTART an I²C-bus access.

7.8 Command decoder

The command decoder identifies command bytes that arrive on the I²C-bus. The five commands available to the PCF8533 are defined in Table 5.

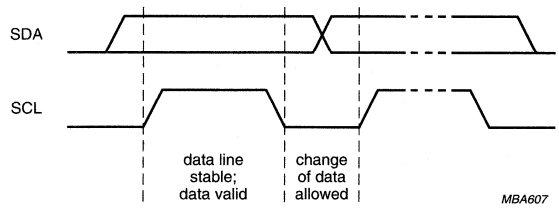


Fig.10 Bit transfer.

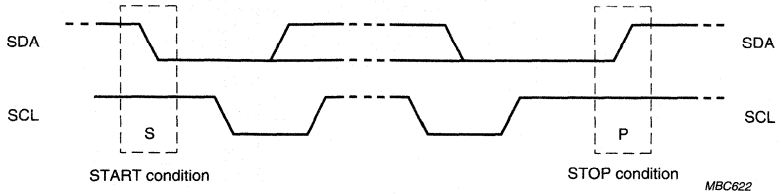


Fig.11 Definition of START and STOP conditions.

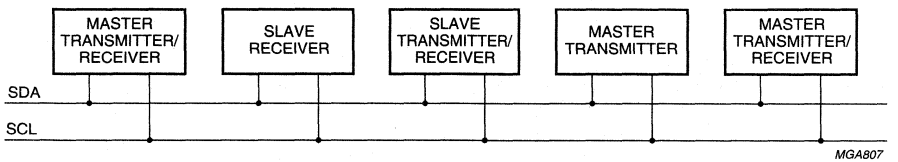


Fig.12 System configuration.

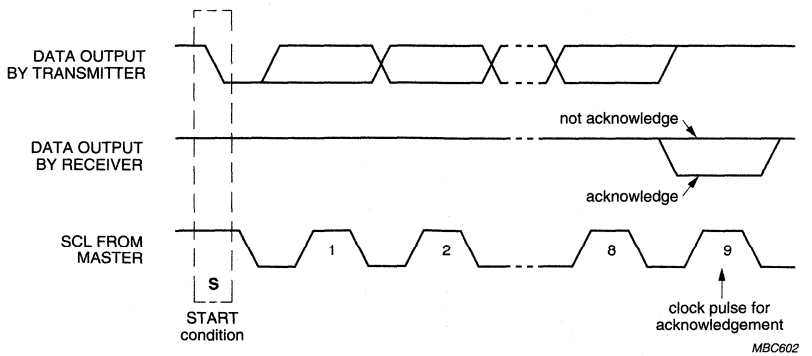


Fig.13 Acknowledgement on the I^2C-bus.

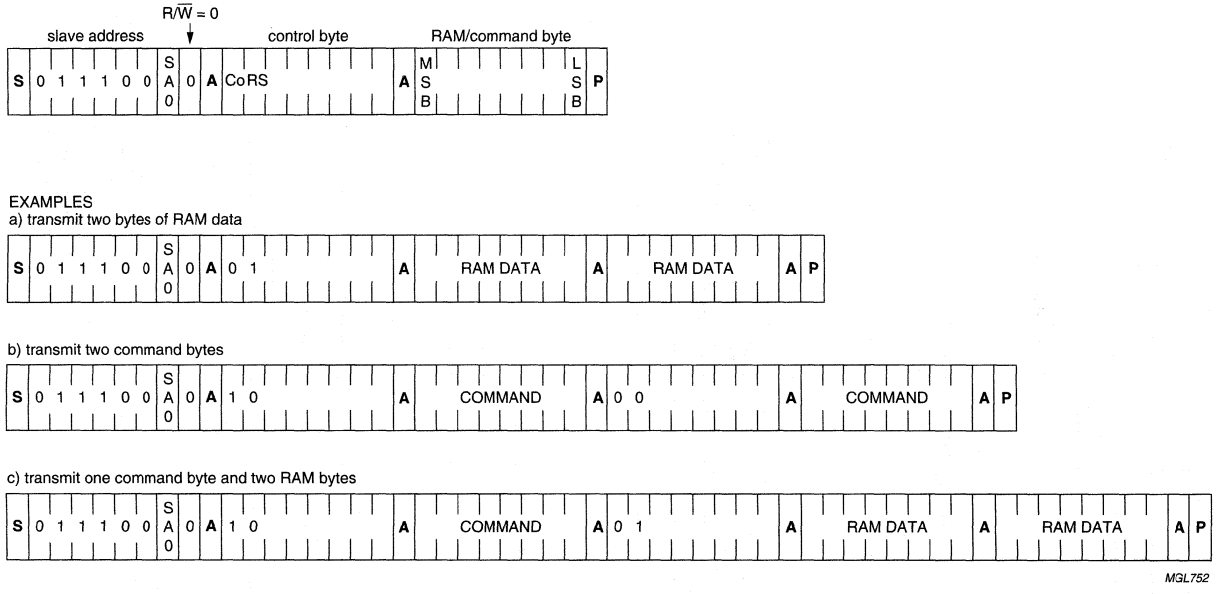
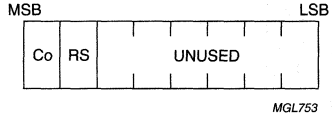


Fig.14 I²C-bus protocol.



Co = 0; last control byte.
Co = 1; control bytes continue.
RS = 0; data is a command byte
RS = 1; data is a display byte

Fig.15 Format of control byte.

Table 5 Definition of PCF8533 commands

COMMAND	OPCODE								OPTIONS	DESCRIPTION
MODE SET	1	1	0	0	E	B	M1	M0	Table 6	defines LCD drive mode
									Table 7	defines LCD bias configuration
									Table 8	defines display status; the possibility to disable the display allows implementation of blinking under external control
LOAD DATA POINTER	0	P6	P5	P4	P3	P2	P1	P0	Table 9	seven bits of immediate data, bits P6 to P0, are transferred to the data pointer to define one of eighty display RAM addresses
DEVICE SELECT	1	1	1	0	0	A2	A1	A0	Table 10	three bits of immediate data, bits A0 to A3, are transferred to the subaddress counter to define one of eight hardware subaddresses
BANK SELECT	1	1	1	1	1	0	I	O	Table 11	defines input bank selection (storage of arriving display data)
									Table 12	defines output bank selection (retrieval of LCD display data); the BANK SELECT command has no effect in 1 : 3 and 1 : 4 multiplex drive modes
BLINK	1	1	1	1	0	A	BF 1	BF 0	Table 13	defines the blinking frequency
									Table 14	selects the blinking mode; normal operation with frequency set by BF1, BF0 or blinking by alternation of display RAM banks. Alternation blinking does not apply in 1 : 3 and 1 : 4 multiplex drive modes

Table 6 Mode set option 1

LCD DRIVE MODE		BITS	
DRIVE MODE	BACKPLANE	M1	M0
Static	1 BP	0	1
1 : 2	MUX (2 BP)	1	0
1 : 3	MUX (3 BP)	1	1
1 : 4	MUX (4 BP)	0	0

Table 7 Mode set option 2

LCD BIAS	BIT B
1/3 bias	0
1/2 bias	1

Table 8 Mode set option 3

DISPLAY STATUS	BIT E
Disabled (blank)	0
Enabled	1

Table 9 Load data pointer option 1

DESCRIPTION	BITS						
7 bit binary value of 0 to 79	P6	P5	P4	P3	P2	P1	P0

Table 10 Device select option 1

DESCRIPTION	BITS		
3 bit binary value of 0 to 7	A2	A1	A0

Table 11 Bank select option 1 (Input)

STATIC	1 : 2 MUX	BIT I
RAM bit 0	RAM bits 0 and 1	0
RAM bit 2	RAM bits 2 and 3	1

Table 12 Bank select option 2 (Output)

STATIC	1 : 2 MUX	BIT O
RAM bit 0	RAM bits 0 and 1	0
RAM bit 2	RAM bits 2 and 3	1

Table 13 Blink option 1

BLINK FREQUENCY	BITS	
	BF1	BF0
Off	0	0
2 Hz	0	1
1 Hz	1	0
0.5 Hz	1	1

Table 14 Blink option 2

BLINK MODE	BIT A
Normal blinking(1)	0
Alternation blinking	1

Note

1. Normal blinking is assumed when multiplex rates 1 : 3 or 1 : 4 are selected.

7.9 Display controller

The display controller executes the commands identified by the command decoder. It contains the status registers of the PCF8533 and co-ordinates their effects.
The controller is also responsible for loading display data into the display RAM as required by the filling order.

7.10 Cascaded operation

In large display configurations, up to 16 PCF8533s can be distinguished on the same I²C-bus by using the 3-bit hardware subaddress (A0, A1 and A2) and the programmable I²C-bus slave address (SA0). When cascaded PCF8533s are synchronized they can share the backplane signals from one of the devices in the cascade. Such an arrangement is cost-effective in large LCD applications since the backplane outputs of only one device need to be through-plated to the backplane electrodes of the display. The other PCF8533s of the cascade contribute additional segment outputs but their backplane outputs are left open-circuit (see Fig.16).

The $\overline{\text{SYNC}}$ line is provided to maintain the correct synchronization between all cascaded PCF8533s. This synchronization is guaranteed after the Power-on reset. The only time that $\overline{\text{SYNC}}$ is likely to be needed is if synchronization is accidentally lost (e.g. by noise in adverse electrical environments, or by the definition of a multiplex mode when PCF8533s with different SA0 levels are cascaded). $\overline{\text{SYNC}}$ is organized as an input/output pad; the output selection being realized as an open-drain driver with an internal pull-up resistor. A PCF8533 asserts the $\overline{\text{SYNC}}$ line at the onset of its last active backplane signal and monitors the $\overline{\text{SYNC}}$ line at all other times. Should synchronization in the cascade be lost, it will be restored by the first PCF8533 to assert $\overline{\text{SYNC}}$. The timing relationship between the backplane waveforms and the $\overline{\text{SYNC}}$ signal for the various drive modes of the PCF8533 are shown in Fig.17.

The contact resistance between the $\overline{\text{SYNC}}$ pads of cascaded devices must be controlled. If the resistance is too high then the device will not be able to synchronize properly. This is particularly applicable to COG applications. Table 15 shows the limiting values for contact resistance.

Table 15 $\overline{\text{SYNC}}$ contact resistance

NUMBER OF DEVICES	MAXIMUM CONTACT RESISTANCE
2	6000 Ω
3 to 5	2200 Ω
6 to 10	1200 Ω
11 to 16	700 Ω

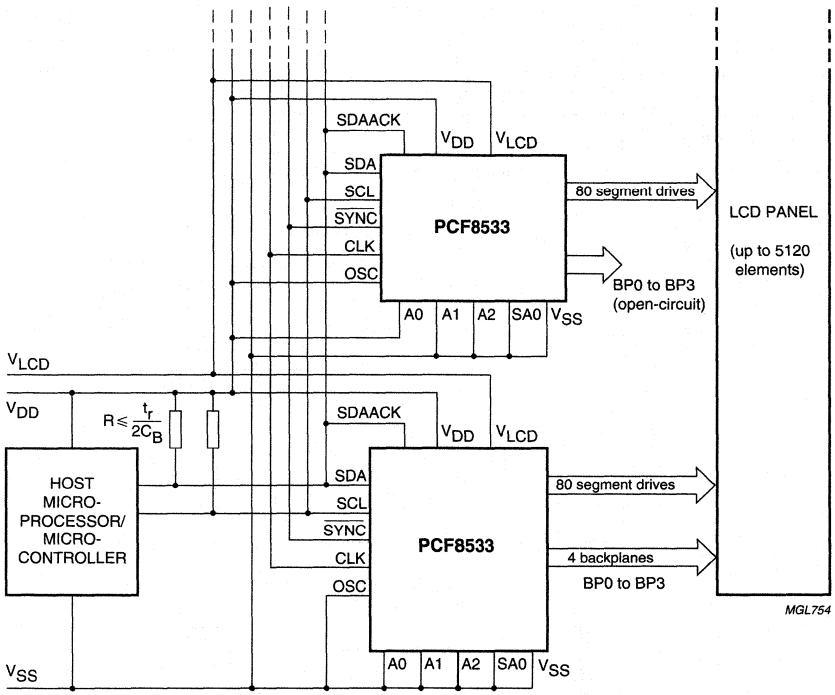


Fig.16 Cascaded PCF8533 configuration.

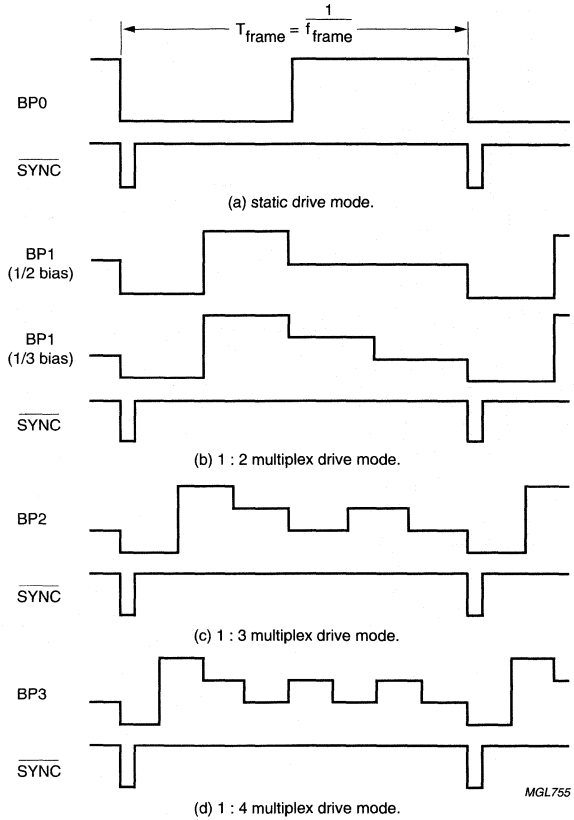


Fig.17 Synchronization of the cascade for the various PCF8533 drive modes.

8 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.5	+6.5	V
I_{DD}	supply current	−50	+50	mA
V_{LCD}	LCD supply voltage	V_{SS} − 0.5	+7.5	V
I_{LCD}	LCD supply current	−50	+50	mA
I_{SS}	negative supply current	−50	+50	mA
$V_{I(n)}$	input voltage on pads SDA, SCL, CLK, $\overline{SYNC}$, SA0, OSC and A0 to A2	V_{SS} − 0.5	V_{DD} + 0.5	V
$V_{O(n)}$	output voltage on pads S0 to S79 and BP0 to BP3	V_{SS} − 0.5	V_{LCD} + 0.5	V
I_I	DC input current	−10	+10	mA
I_O	DC output current	−10	+10	mA
P_{tot}	total power dissipation	−	400	mW
P/out	power dissipation per output	−	100	mW
T_{stg}	storage temperature	−65	+150	°C

9 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see *"Handling MOS Devices"*).

10 DC CHARACTERISTICS

V_{DD} = 1.8 to 5.5 V; V_{SS} = 0 V; V_{LCD} = 2.5 to 6.5 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage		1.8	–	5.5	V
V_{LCD}	LCD supply voltage		2.5	–	6.5	V
I_{DD}	supply current	f_{CLK} = 1536 Hz; note 1	–	8	20	μA
I_{LCD}	LCD supply current	f_{CLK} = 1536 Hz; note 1	–	24	60	μA
Logic						
V_{IL}	LOW-level input voltage		V_{SS}	–	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	–	V_{DD}	V
I_{OL1}	LOW-level output current on pads CLK and $\overline{SYNC}$	V_{OL} = 0.4 V; V_{DD} = 5 V	1	–	–	mA
I_{OH1}	HIGH-level output current pad CLK	V_{OH} = 4.6 V; V_{DD} = 5 V	−1	–	–	mA
I_{OL2}	LOW-level output current pad SDA	V_{OL} = 0.4 V; V_{DD} = 5 V	3	–	–	mA
I_{L1}	leakage current on pads SA0, A0 to A2, CLK, SDA and SCL	$V_I = V_{DD}$ or V_{SS}	−1	–	+1	μA
I_{L2}	leakage current pad OSC	$V_I = V_{DD}$	−1	–	+1	μA
V_{POR}	Power-on reset voltage level		1.0	1.3	1.6	V
C_I	input capacitance	note 2	–	–	7	pF
LCD outputs						
V_{BP}	DC voltage component on pads BP0 to BP3	C_{BP} = 35 nF	−100	–	+100	mV
V_S	DC voltage component on pads S0 to S79	C_S = 5 nF	−100	–	+100	mV
R_{BP}	output resistance at pads BP0 to BP3	V_{LCD} = 5 V; note 3	–	1.5	10	kΩ
R_S	output resistance at pads S0 to S79	V_{LCD} = 5 V; note 3	–	6.0	13.5	kΩ

Notes

1. LCD outputs are open-circuit; inputs at V_{SS} or V_{DD}; external clock with 50% duty factor; I^2C-bus inactive.
2. Not tested; given by design.
3. Outputs measured one at a time.

11 AC CHARACTERISTICS

V_{DD} = 1.8 to 5.5 V; V_{SS} = 0 V; V_{LCD} = 2.5 to 6.5 V; T_{amb} = −40 to + 85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{CLK}	oscillator frequency at pad CLK	V_{DD} = 5 V; note 1	797	1536	3046	Hz
t_{CLKH}	input CLK HIGH time		130	–	–	µs
t_{CLKL}	input CLK LOW time		130	–	–	µs
$t_{d(p)SYNC}$	$\overline{SYNC}$ propagation delay time		–	30	–	ns
t_{SYNCL}	$\overline{SYNC}$ LOW time		1	–	–	µs
$t_{d(PLCD)}$	driver delays with test loads	V_{LCD} = 5 V	–	–	30	µs
Timing characteristics: I²C-bus; note 2						
f_{SCL}	SCL clock frequency		–	–	400	kHz
t_{BUF}	bus free time between a STOP and START		1.3	–	–	µs
$t_{HD;STA}$	START condition hold time		0.6	–	–	µs
$t_{SU;STA}$	set-up time for a repeated START condition		0.6	–	–	µs
t_{LOW}	SCL LOW time		1.3	–	–	µs
t_{HIGH}	SCL HIGH time		0.6	–	–	µs
t_r	SCL and SDA rise time		–	–	0.3	µs
t_f	SCL and SDA fall time		–	–	0.3	µs
C_b	capacitive bus line load		–	–	400	pF
$t_{SU;DAT}$	data set-up time		100	–	–	ns
$t_{HD;DAT}$	data hold time		0	–	–	ns
$t_{SU;STO}$	set-up time for STOP condition		0.6	–	–	µs
t_{SW}	tolerable spike width on bus		–	–	50	ns

Notes

1. Typical output duty cycle of 50%.
2. All timing values are valid within the operating supply voltage and ambient temperature range and are referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

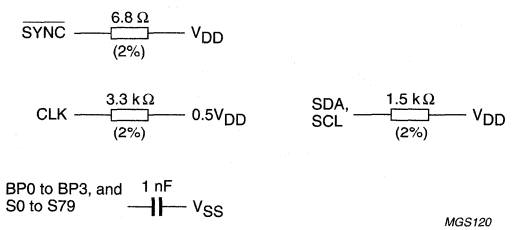


Fig.18 Test loads.

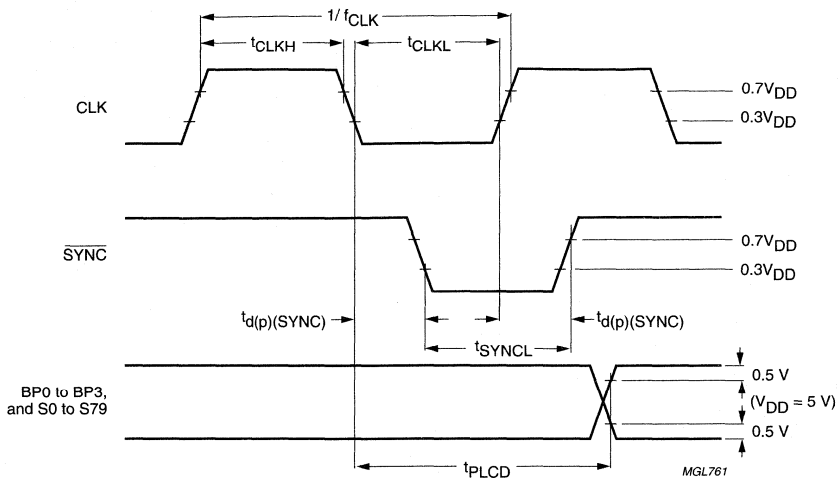


Fig.19 Driver timing waveforms.

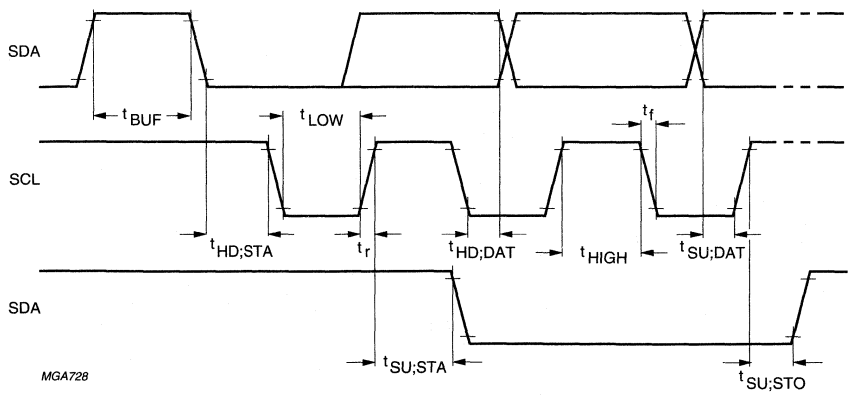


Fig.20 I²C-bus timing waveforms.

12 BONDING PAD LOCATIONS

Bonding pad locations (dimensions in μm)

All x and y coordinates are referenced to centre of chip (see Fig.22).

SYMBOL	PAD	x	y
SDAACK	1	−1079.20	−594.40
SDA	2	−839.20	−594.40
SDA	3	−759.20	−594.40
SCL	4	−599.20	−594.40
SCL	5	−519.20	−594.40
CLK	6	−414.80	−594.40
V_{DD}	7	−284.80	−594.40
$\overline{SYNC}$	8	+4.20	−594.40
OSC	9	+119.20	−594.40
A0	10	+249.20	−594.40
A1	11	+379.20	−594.40
A2	12	+581.20	−594.40
SA0	13	+711.20	−594.40
V_{SS}	14	+841.20	−594.40
V_{LCD}	15	+1099.60	−594.40
BP2	16	+1277.60	−594.40
BP0	17	+1357.60	−594.40
S0	18	+1437.60	−594.40
S1	19	+1517.60	−594.40
S2	20	+1597.60	−594.40
S3	21	+1677.60	−594.40
S4	22	+1757.60	−594.40
S5	23	+1837.60	−594.40
S6	24	+1917.60	−594.40
S7	25	+1997.60	−594.40
S8	26	+2077.60	−594.40
S9	27	+2157.60	−594.40
S10	28	+2237.60	−594.40
S11	29	+2317.60	−594.40
S12	30	+2357.60	+594.40
S13	31	+2277.60	+594.40
S14	32	+2197.60	+594.40
S15	33	+2117.60	+594.40
S16	34	+2037.60	+594.40
S17	35	+1957.60	+594.40
S18	36	+1877.60	+594.40
S19	37	+1797.60	+594.40

SYMBOL	PAD	x	y
S20	38	+1717.60	+594.40
S21	39	+1637.60	+594.40
S22	40	+1557.60	+594.40
S23	41	+1477.60	+594.40
S24	42	+1317.60	+594.40
S25	43	+1237.60	+594.40
S26	44	+1157.60	+594.40
S27	45	+1077.60	+594.40
S28	46	+997.60	+594.40
S29	47	+917.60	+594.40
S30	48	+837.60	+594.40
S31	49	+757.60	+594.40
S32	50	+677.60	+594.40
S33	51	+597.60	+594.40
S34	52	+437.60	+594.40
S35	53	+357.60	+594.40
S36	54	+277.60	+594.40
S37	55	+197.60	+594.40
S38	56	+117.60	+594.40
S39	57	+37.60	+594.40
S40	58	−42.40	+594.40
S41	59	−122.40	+594.40
S42	60	−202.40	+594.40
S43	61	−282.40	+594.40
S44	62	−362.40	+594.40
S45	63	−442.40	+594.40
S46	64	−602.40	+594.40
S47	65	−682.40	+594.40
S48	66	−762.40	+594.40
S49	67	−842.40	+594.40
S50	68	−922.40	+594.40
S51	69	−1002.40	+594.40
S52	70	−1082.40	+594.40
S53	71	−1162.40	+594.40
S54	72	−1242.40	+594.40
S55	73	−1322.40	+594.40
S56	74	−1402.40	+594.40

SYMBOL	PAD	x	y
S57	75	−1562.40	+594.40
S58	76	−1642.40	+594.40
S59	77	−1722.40	+594.40
S60	78	−1802.40	+594.40
S61	79	−1882.40	+594.40
S62	80	−1962.40	+594.40
S63	81	−2042.40	+594.40
S64	82	−2122.40	+594.40
S65	83	−2202.40	+594.40
S66	84	−2282.40	+594.40
S67	85	−2362.40	+594.40
S68	86	−2322.40	−594.40
S69	87	−2242.40	−594.40
S70	88	−2162.40	−594.40
S71	89	−2082.40	−594.40
S72	90	−2002.40	−594.40
S73	91	−1922.40	−594.40
S74	92	−1842.40	−594.40
S75	93	−1762.40	−594.40
S76	94	−1682.40	−594.40
S77	95	−1602.40	−594.40
S78	96	−1522.40	−594.40
S79	97	−1442.40	−594.40
BP3	98	−1362.40	−594.40
BP1	99	−1282.40	−594.40
Alignment marks			
C1	−	+2300.5	+55.0
C2	−	−2320.2	+107.0
F	−	−2208.3	−165.4
Dummy pads (connected to segments shown; note			
D1	(S11)	+2469.70	−594.40
D2	(S11)	+2549.70	−594.40
D3	(S12)	+2517.60	+594.40
D4	(S12)	+2437.60	+594.40
D5	(S67)	−2442.30	+594.40
D6	(S67)	−2522.30	+594.40
D7	(S68)	−2554.40	−594.40
D8	(S68)	−2474.40	−594.40
Chip corners (pre-sawing)			
Bottom left	−	−2695.00	−750.00
Top right	−	+2695.00	+750.00

Note

1. The dummy pads are not tested.

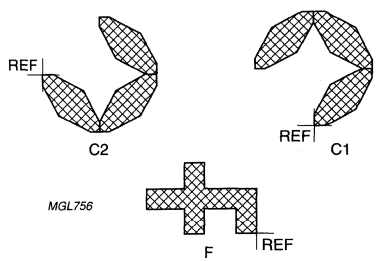


Fig.21 Alignment markers.

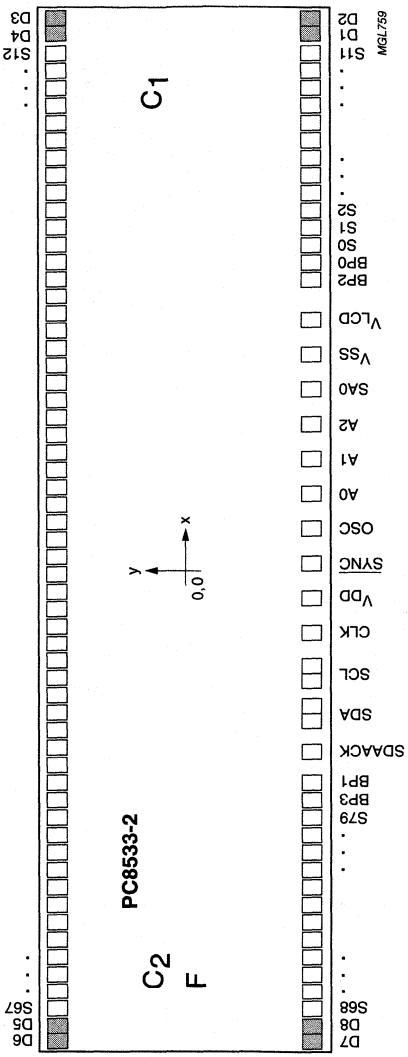


Fig.22 Bonding pad locations.

The position of the bonding pads is not to scale.
Chip dimensions: approximately 5.40 × 1.51 mm.
Bump dimensions: 90 × 50 × 17.5 µm.
Wafer thickness: 381 µm.

13 DEVICE PROTECTION

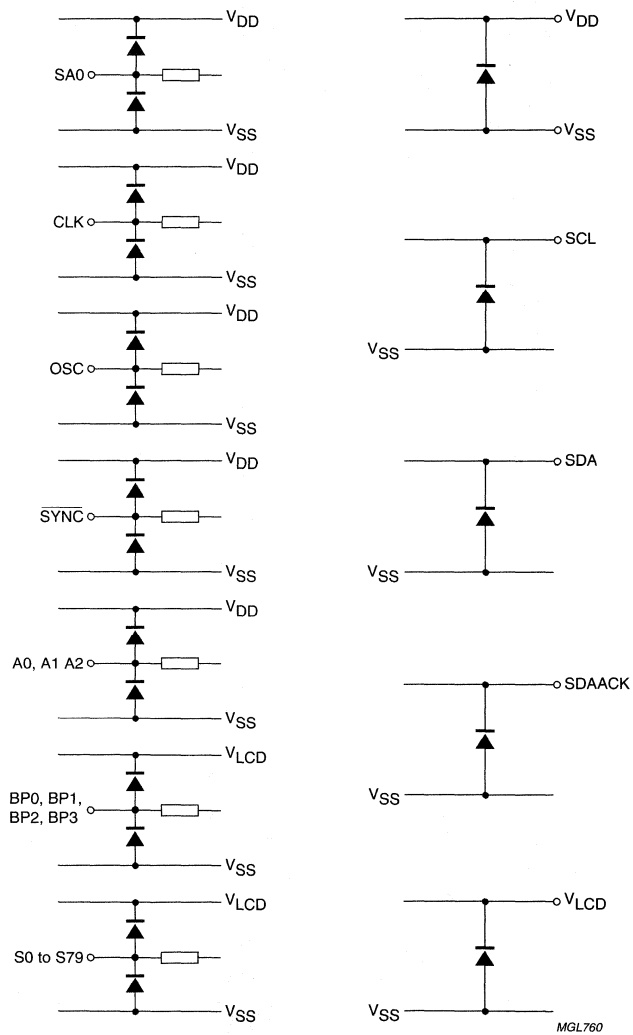
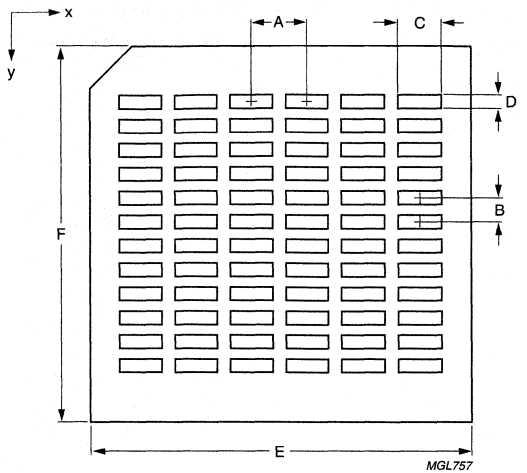


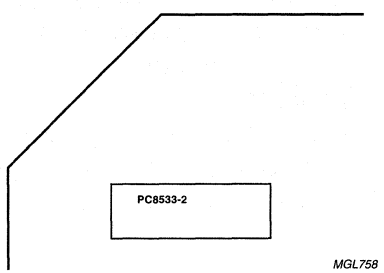
Fig.23 Device protection diagram.

14 TRAY INFORMATION



The dimensions are given in Table 16.

Fig.24 Tray details.



The orientation of the IC in a pocket is indicated by the position of the IC type name on the die surface with respect to the chamfer on the upper left corner of the tray. Refer to the bonding pad location diagram for the orientating and position of the type name on the die surface.

Fig.25 Tray alignment.

Table 16 Dimensions

DIM.	DESCRIPTION	VALUE
A	pocket pitch, x direction	7.37 mm
B	pocket pitch, y direction	3.68 mm
C	pocket width, x direction	5.50 mm
D	pocket width, y direction	1.60 mm
E	tray width, x direction	50.8 mm
F	tray width, y direction	50.8 mm
x	no. pockets in x direction	6
y	no. pockets in y direction	12

CONTENTS

65 × 133 pixel matrix driver PCF8535

1 FEATURES

- Single-chip LCD controller/driver
- 65 row, 133 column outputs
- Display data RAM 65 × 133 bits
- 133 icons (last row is used for icons)
- Fast mode I²C-bus interface (400 kbits/s)
- Software selectable multiplex rates: 1 : 17, 1 : 26, 1 : 34, 1 : 49 and 1 : 65
- On-chip:
  - Generation of intermediate LCD bias voltages
  - Oscillator requires no external components (external clock also possible)
  - Generation of V_{LCD}.
- CMOS compatible inputs
- Software selectable bias configuration
- Logic supply voltage range V_{DD1} to V_{SS1} 4.5 to 5.5 V
- Supply voltage range for high voltage part V_{DD2} and V_{DD3} to V_{SS2} and V_{SS3} 4.5 to 5.5 V
- Display supply voltage range V_{LCD} to V_{SS}:
  - Mux rate 1 : 65: 8 to 16 V.
- Low power consumption, suitable for battery operated systems
- Internal Power-on reset and/or external reset
- Temperature read back available
- Manufactured in N-well silicon gate CMOS process.

2 APPLICATIONS

- Automotive information systems
- Telecommunication systems
- Point-of-sale terminals
- Instrumentation.

3 GENERAL DESCRIPTION

The PCF8535 is a low power CMOS LCD row/column driver, designed to drive dot matrix graphic displays at multiplex rates of 1 : 17, 1 : 26, 1 : 34, 1 : 49 and 1 : 65. Furthermore, it can drive up to 133 icons. All necessary functions for the display are provided in a single chip, including on-chip generation of LCD bias voltages, resulting in a minimum of external components and low power consumption. The PCF8535 is compatible with most microcontrollers and communicates via an industry standard two-line bidirectional I²C-bus serial interface. All inputs are CMOS compatible.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8535U	–	chip with bumps in tray	–

5 BLOCK DIAGRAM

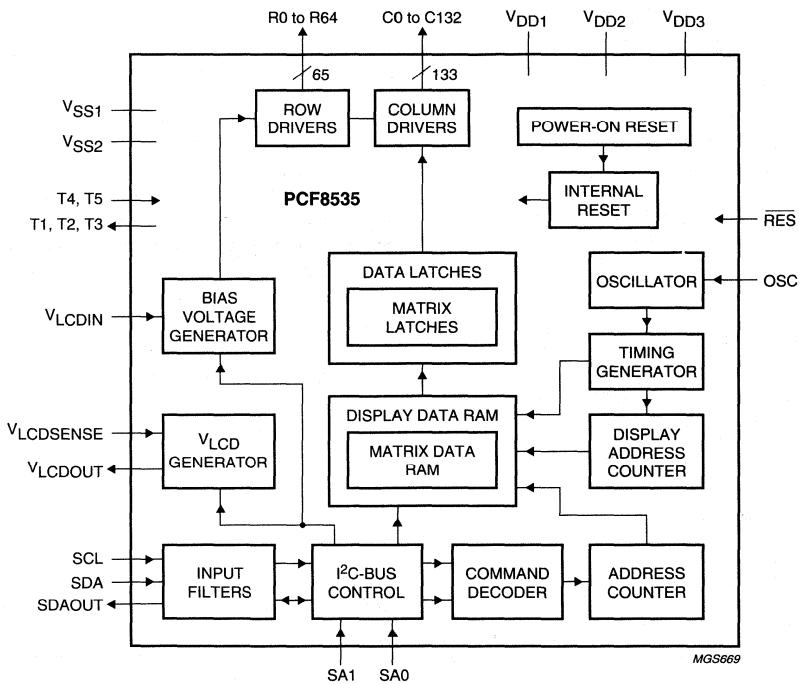


Fig.1 Block diagram.

5.1 Block diagram functions

5.1.1 Oscillator

The on-chip oscillator provides the display clock for the system; it requires no external components. Alternatively, an external display clock may be provided via the OSC input. The OSC input must be connected to V_{DD1} or V_{SS1} when not in use. During power-down additional current saving can be made if the external clock is disabled.

5.1.2 Power-on reset

The on-chip Power-on reset initializes the chip after power-on or power failure.

5.1.3 I²C-bus controller

The I²C-bus controller detects the I²C-bus protocol, slave address, commands and display data bytes. It performs the conversion of the data input (serial-to-parallel). The PCF8535 acts as an I²C-bus slave and therefore cannot initiate bus communication.

5.1.4 Input filters

Input filters are provided to enhance noise immunity in electrically adverse environments; RC low-pass filters are provided on the SDA, SCL and $\overline{RES}$ lines.

5.1.5 Display data RAM

The PCF8535 contains a 65 × 133 bit static RAM which stores the display data. The RAM is divided into 9 banks of 133 bytes. The last bank is used for icon data and is only one bit deep. During RAM access, data is transferred to the RAM via the I²C-bus interface. There is a direct correspondence between the X address and the column output number.

5.1.6 Timing generator

The timing generator produces the various signals required to drive the internal circuitry. Internal chip operation is not disturbed by operations on the data bus.

5.1.7 Address counter

The Address Counter (AC) sends addresses to the Display Data RAM (DDRAM) for writing.

5.1.8 Display address counter

The display is generated by continuously shifting rows of RAM data to the dot matrix LCD via the column outputs. The display status (all dots on or off, normal or inverse video) is set via the I²C-bus.

6 PINNING

SYMBOL	PAD	DESCRIPTION
	1	dummy pad
	2	bump/alignment mark 1
R0 to R15	3 to 18	LCD row driver outputs
C0 to C132	19 to 151	LCD column driver outputs
R47 to R33	152 to 166	LCD row driver outputs
	167	bump/alignment mark 2
	168	dummy pad
R48 to R64	169 to 185	LCD row driver outputs; R64 is icon row
	186	bump/alignment mark 3
	187 to 189	dummy pad
OSC	190	oscillator
V_{LCDIN}	191 to 196	LCD supply voltage
V_{LCDOUT}	197 to 203	voltage multiplier output
$V_{LCDSENSE}$	204	voltage multiplier regulation input (V_{LCD})
	205 and 206	dummy pad
$\overline{RES}$	207	external reset input (active LOW)
T3	208	test output 3
T2	209	test output 2
T1	210	test output 1
V_{DD2}	211 to 218	supply voltage 2
V_{DD3}	219 to 222	supply voltage 3
V_{DD1}	223 to 228	supply voltage 1
	229	dummy pad
SDA	230 and 231	I²C-bus serial data inputs
SDAOUT	232	I²C-bus serial data output
SA1	233	I²C-bus slave address input
SA0	234	I²C-bus slave address input
V_{SS2}	235 to 242	ground 2
V_{SS1}	243 to 250	ground 1
T5	251	test input 5
T4	252	test input 4
	253	dummy pad
SCL	254 and 255	I²C-bus serial clock inputs
	256	bump/alignment mark 4
R32 to R16	257 to 273	LCD row driver outputs

6.1 Pin functions

6.1.1 R0 TO R64

These pads output the display row signals.

6.1.2 C0 TO C132

These pads output the display column signals.

6.1.3 V_{SS1} AND V_{SS2}

V_{SS1} and V_{SS2} must be connected together.

6.1.4 V_{DD1} TO V_{DD3}

V_{DD1} is the logic supply. V_{DD2} and V_{DD3} are for the voltage multiplier. For split power supplies V_{DD2} and V_{DD3} must be connected together. If only one supply voltage is available, all three supplies must be connected together.

6.1.5 V_{LCDOUT}

If, in the application, an external V_{LCD} is used, V_{LCDOUT} must be left open-circuit; otherwise (if the internal voltage multiplier is enabled) the chip may be damaged. V_{LCDOUT} should not be driven when V_{DD1} is below its minimum allowed value otherwise a low impedance path between V_{LCDOUT} and V_{SS1} will exist.

6.1.6 V_{LCDIN}

This is the V_{LCD} supply for when an external V_{LCD} is used. If the internal V_{LCD} generator is used, then V_{LCDOUT} and V_{LCDIN} must be connected together. V_{LCDIN} should not be driven when V_{DD1} is below its minimum allowed value, otherwise a low impedance path between V_{LCDIN} and V_{SS1} will exist.

6.1.7 $V_{LCDSENSE}$

This is the input to the internal voltage multiplier regulator. It must be connected to V_{LCDOUT} when the internal voltage generator is used otherwise it may be left open-circuit. $V_{LCDSENCE}$ should not be driven when V_{DD1} is below its minimum allowed value, otherwise a low impedance path between $V_{LCDSENCE}$ and V_{SS1} will exist.

6.1.8 SDA

I²C-bus serial data input.

6.1.9 SDAOUT

SDAOUT is the serial data acknowledge for the I²C-bus. By connecting SDAOUT to SDA externally, the SDA line becomes fully I²C-bus compatible. Having the acknowledge output separated from the serial data line is advantageous in Chip-On-Glass (COG) applications. In COG applications where the track resistance from the SDAOUT pad to the system SDA line can be significant, a potential divider is generated by the bus pull-up resistor and the Indium Tin Oxide (ITO) track resistance. It is possible that during the acknowledge cycle the PCF8535 will not be able to create a valid logic 0 level. By splitting the SDA input from the SDAOUT output the device could be used in a mode that ignores the acknowledge bit. In COG applications where the acknowledge cycle is required or where read back is required, it is necessary to minimize the track resistance from the SDAOUT pad to the system SDA line to guarantee a valid LOW level.

6.1.10 SCL

I²C-bus serial clock input.

6.1.11 SA0 AND SA1

Least significant bits of the I²C-bus slave address.

Table 1 Slave address; see note 1

SA1 AND SA0	MODE	SLAVE ADDRESS
0 and 0	write	78H
	read	79H
0 and 1	write	7AH
	read	7BH
1 and 0	write	7CH
	read	7DH
1 and 1	write	7EH
	read	7FH

Note

1. The slave address is a concatination of the following bits {01111, SA1, SA0 and R/$\overline{W}$}.

6.1.12 OSC

If the on-chip oscillator is used this input must be connected to V_{DD1} or V_{SS1}.

6.1.13 $\overline{RES}$

External reset pad: when this pad is LOW the chip will be reset; see Section 7.1. If an external reset is not required, this pad must be tied to V_{DD1}. Timing for the $\overline{RES}$ pad is given in Chapter 12.

6.1.14 T1, T2, T3, T4 AND T5

In applications T4 and T5 must be connected to V_{SS}. T1, T2 and T3 are to be left open-circuit.

7 FUNCTIONAL DESCRIPTION

The PCF8535 is a low power LCD driver designed to interface with microprocessors/microcontrollers and a wide variety of LCDs.

The host microprocessor/microcontroller and the PCF8535 are both connected to the I²C-bus. The SDA and SCL lines must be connected to the positive power supply via pull-up resistors. The internal oscillator requires no external components. The appropriate intermediate biasing voltage for the multiplexed LCD waveforms are generated on-chip. The only other connections required to complete the system are to the power supplies (V_{DD}, V_{SS} and V_{LCD}) and suitable capacitors for decoupling V_{LCD} and V_{DD}.

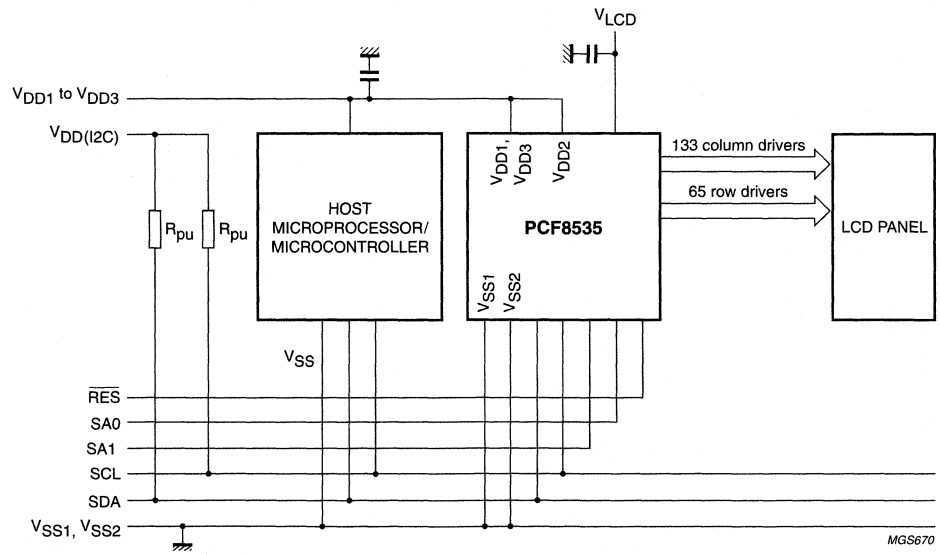


Fig.2 Typical system configuration.

7.1 Reset

The PCF8535 has two reset modes; internal Power-on reset or external reset. Reset initiated from either the $\overline{RES}$ pad or the internal Power-on reset block will initialize the chip to the following starting condition:

- Power-down mode (PD = 1)
- Horizontal addressing (V = 0); no mirror X or Y (MX = 0 and MY = 0)
- Display blank (D = 0 and E = 0)
- Address counter X[6:0] = 0, Y[2:0] = 0 and XM_0 = 0
- Bias system BS[2:0] = 0
- Multiplex rate M[2:0] = 0 (Mux rate 1 : 17)
- Temperature control mode TC[2:0] = 0
- HV-gen control, HVE = 0 the HV generator is switched off, PRS = 0 and S[1:0] = 00
- V_{LCDOUT} is equal to 0 V
- RAM data is unchanged (Note: RAM data is undefined after power-up)
- All row and column outputs are set to V_{SS} (display off)
- TRS and BRS are set to zero
- Direct mode is disabled (DM = 0)
- Internal oscillator is selected, but not running (EC = 0)
- Bias current set to low current mode (IB = 0).

7.2 Power-down

During power-down all static currents are switched off (no internal oscillator, no timing and no LCD segment drive system) and all LCD outputs are internally connected to V_{SS}. The serial bus function remains active.

7.3 LCD voltage selector

The practical value for V_{OP} is determined by equating $V_{off(rms)}$ with defined LCD threshold voltage (V_{th}), typically when the LCD exhibits approximately 10% contrast.

7.4 Oscillator

The internal logic operation and the multi-level drive signals of the PCF8535 are clocked by the built-in RC oscillator. No external components are required.

7.5 Timing

The timing of the PCF8535 organizes the internal data flow of the device. The timing also generates the LCD frame frequency which is derived from the clock frequency generated in the internal clock generator.

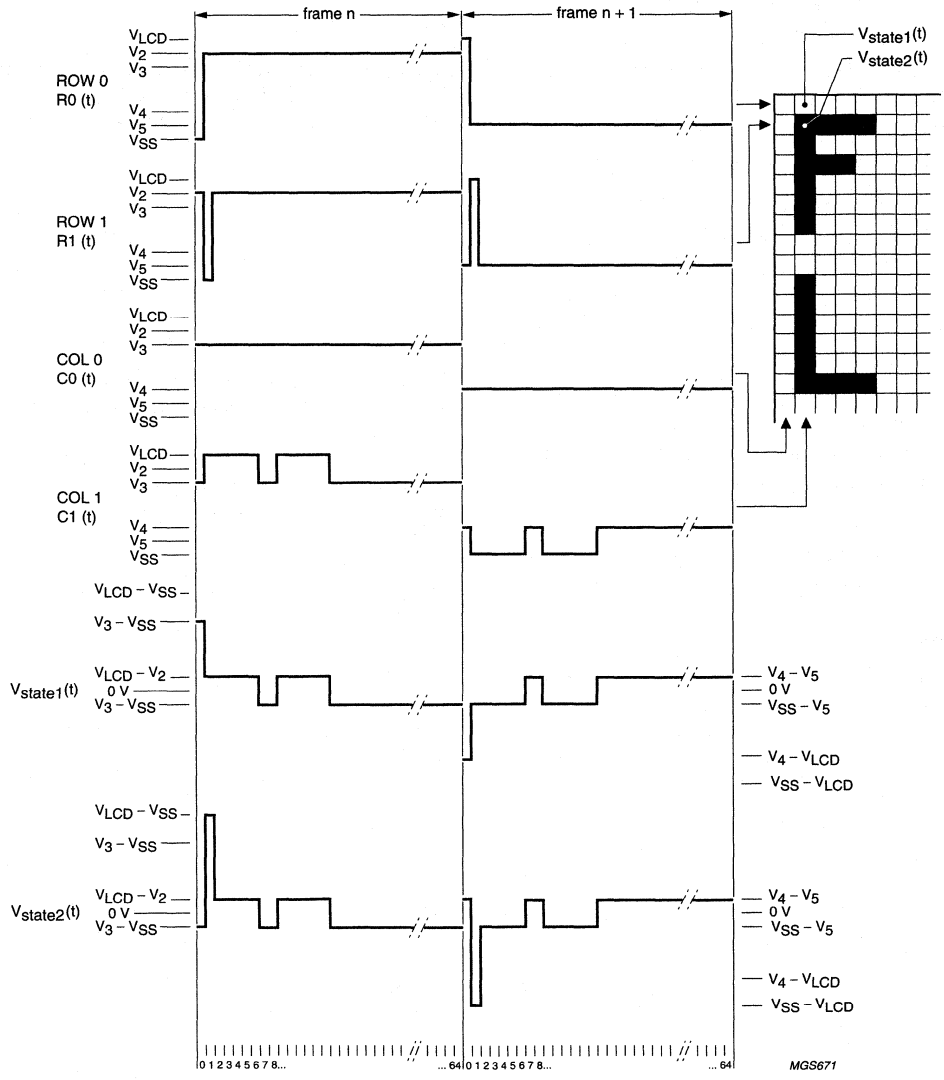
7.6 Column driver outputs

The LCD drive section includes 133 column outputs (C0 to C132) which should be connected directly to the LCD. The column output signals are generated in accordance with the multiplexed row signals and with the data in the display latch. When less than 133 columns are required the unused column outputs should be left open-circuit.

7.7 Row driver outputs

The LCD drive section includes 65 row outputs (R0 to R64) which should be connected directly to the LCD. The row output signals are generated in accordance with the selected LCD drive mode. If lower Mux rates or less than 65 rows are required, the unused outputs should be left open-circuit.

7.8 Drive waveforms



$V_{state1}(t) = C1(t) - R0(t)$.
$V_{state2}(t) = C1(t) - R1(t)$.

Fig.3 Typical LCD driver waveforms.

7.9 Set multiplex rate

The PCF8535 can be used to drive displays of varying sizes. The multiplex mode selected controls which rows are used. In all cases, the last row is always driven and is intended for icons. If Top Row Swap (TRS) is at logic 1 then the icon row will be output on pad R48. M[2:0] selects the multiplex rate (see Table 2).

Table 2 Multiplex rates

M[2]	M[1]	M[0]	MULTIPLEX RATE	ACTIVE ROWS
0	0	0	1 : 17	R0 to R15 and R64
0	0	1	1 : 26	R0 to R24 and R64
0	1	0	1 : 34	R0 to R32 and R64
0	1	1	1 : 49	R0 to R47 and R64
1	0	0	1 : 65	R0 to R64
101 – 111			do not use	–

7.10 Bias system

7.10.1 SET BIAS SYSTEM

The bias voltage levels are set in the ratio of R – R – nR – R – R. Different multiplex rates require different factors n. This is programmed by BS[2:0]. For optimum bias values, n can be calculated from: $n = \sqrt{\text{Mux rate}} - 3$.

Changing the bias system from the optimum will have a consequence on the contrast and viewing angle. One reason to come away from the optimum would be to reduce the required V_{OP}. A compromise between contrast and V_{OP} must be found for any particular application.

Table 3 Programming the required bias system

BS[2]	BS[1]	BS[0]	n	BIAS MODE	TYPICAL MUX RATES
0	0	0	7	$^1/_{11}$	1 : 100
0	0	1	6	$^1/_{10}$	1 : 80
0	1	0	5	$^1/_9$	1 : 65
0	1	1	4	$^1/_8$	1 : 49
1	0	0	3	$^1/_7$	1 : 33
1	0	1	2	$^1/_6$	1 : 26
1	1	0	1	$^1/_5$	1 : 17
1	1	1	0	$^1/_4$	1 : 9

Table 4 Example of LCD bias voltage for $^1/_7$bias, n = 3

SYMBOL	BIAS VOLTAGE FOR $^1/_7$BIAS
V1	V_{LCD}
V2	$^6/_7 \times V_{LCD}$
V3	$^5/_7 \times V_{LCD}$
V4	$^2/_7 \times V_{LCD}$
V5	$^1/_7 \times V_{LCD}$
V6	V_{SS}

7.11 Temperature measurement

7.11.1 Temperature read back

The PCF8535 has an in-built temperature sensor. For power saving, the sensor should only be enabled when a measurement is required. It will not operate in power-down mode. The temperature read back requires a clock to operate. Normally the internal clock is used but, if the device is operating from an external clock, then this must be present for the measurement to work. V_{DD2} and V_{DD3} must also be applied. A measurement is initialized by setting the SM bit. Once started the SM bit will be automatically cleared. An internal oscillator will be initialized and allowed to warm-up for approximately 2 frame periods. After this the measurement starts and lasts for a maximum of 2 frame periods.

Temperature data is returned via a status register. During the measurement the register will contain zero. Once the measurement is completed the register will be updated with the current temperature (non zero value). Because the I²C-bus interface is asynchronous to the temperature measurement, read back prior to the end of the measurement is not guaranteed. If this mode is required the register should be read twice to validate the data.

The ideal temperature read-out can be calculated as follows;

$$TR_{ideal} = 128 + (T - 27\ °C) \times \frac{1}{c} \quad (1)$$

where T is the on-chip temperature in °C and c is the conversion constant; c = 1.17 °C/lsb.

To improve the accuracy of the temperature measurement a calibration is recommended during the assembly of the final product.

For calibrating the temperature read-out a measurement must be taken at a defined temperature. The offset between the ideal read-out and the actual result has to be stored into a non-volatile register (e.g. EEPROM);

$$Offset = TR_{ideal} - TR_{meas} \quad (2)$$

where TR_{meas} is the actual temperature read-out of the PCF8535.

The calibrated temperature read-out can be calculated for each measurement as follows:

$$TR_{cal} = TR_{meas} + Offset \quad (3)$$

The accuracy after the calibration is ±6.7% (plus ±1 lsb) of the difference between the current temperature and the calibration temperature. For this reason a calibration at or near the most sensitive temperature for the display is recommended.

E.g. for a calibration at 25 °C with the current temperature at –20 °C, the absolute error may be calculated as:

Absolute error = 0.067 × (25 °C – –20 °C)
= ±3 °C + ±1 lsb = ±4.17 °C.

7.12 Temperature compensation

7.12.1 Temperature coefficients

Due to the temperature dependency of the liquid crystals viscosity the LCD controlling voltage, V must be increased at lower temperatures to maintain optimum contrast. Figure 4 shows V_{LCD} as a function of temperature for a typical high multiplex rate liquid.

In the PCF8535 the temperature coefficient of V_{LCD} can be selected from 8 values by setting bits TC[2:0], see Table 5.

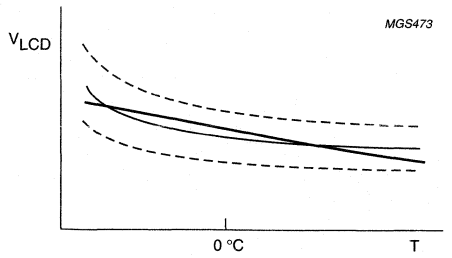


Fig.4 V_{LCD} as function of liquid crystal temperature (typical values).

Table 5 Selectable temperature coefficients

TC[2]	TC[1]	TC[0]	TC VALUE	UNIT
0	0	0	0	1/°C
0	0	1	-0.44×10^{-3}	1/°C
0	1	0	-1.10×10^{-3}	1/°C
0	1	1	-1.45×10^{-3}	1/°C
1	0	0	-1.91×10^{-3}	1/°C
1	0	1	-2.15×10^{-3}	1/°C
1	1	0	-2.32×10^{-3}	1/°C
1	1	1	-2.74×10^{-3}	1/°C

7.13 V_{OP}

7.13.1 SET V_{OP} VALUE

The voltage at the reference temperature can be calculated as: [V_{LCD} ($T = T_{cut}$)]

$$V_{LCD_{(Tcut)}} = (a + V_{OP} \times b) \quad (4)$$

The operating voltage, V_{OP}, can be set by software. The generated voltage is dependent on the temperature, programmed Temperature Coefficient (TC) and the programmed voltage at the reference temperature (T_{cut}):

$$V_{LCD} = (a + V_{OP} \times b) \times (1 + ((T - T_{cut}) \times TC)) \quad (5)$$

The values for T_{cut}, a and b are given in Table 6. The maximum voltage that can be generated is dependent on the voltage V_{DD2} and the display load current. Two overlapping V_{OP} ranges are selectable via the command page "Hv-gen control", see Fig.5.

The low range offers programming from 4.5 to 10.215 V, with the high range from 10.215 to 15.93 V at the cut point temperature, T_{cut}. Care must be taken, when using temperature coefficients, that the programmed voltage does not exceed the maximum allowed V_{LCD} voltage, see Chapter 10.

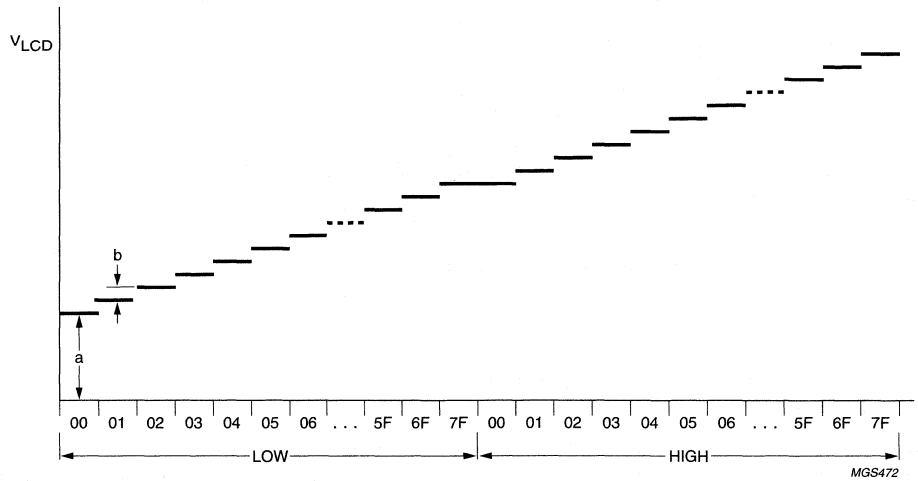
For a particular liquid, the optimum V_{LCD} can be calculated for a given multiplex rate. For a Mux rate of 1 : 65, the optimum operating voltage of the liquid can be calculated as:

$$V_{LCD} = \frac{1 + \sqrt{65}}{\sqrt{2 \times \left(1 - \frac{1}{\sqrt{65}}\right)}} \times V_{th} = 6.85 \times V_{th} \quad (6)$$

where V_{th} is the threshold voltage of the liquid crystal material used.

Table 6 Values for parameters of the HV generator programming

SYMBOL	BITS	VALUE	UNIT
a	PRS = 0	4.5	V
	PRS = 1	10.215	V
b		0.045	V
T_{cut}		27	°C



V_{OP}[6:0] programming (00H to 7FH, programming range LOW and HIGH).

Fig.5 V_{OP} programming of PCF8535.

7.14 Voltage multiplier control

7.14.1 S[1:0]

The PCF8535 incorporates a software configurable voltage multiplier. After reset ($\overline{RES}$) the voltage multiplier is set to 2 × V_{DD2}. Other voltage multiplier factors are set via the HV-gen command page. Before switching on the charge pump, the charge pump has to be pre-charged using the following sequence.

A starting state of HVE = 0, DOF = 0, PD = 1 and DM = 0 is assumed. A small delay between steps is indicated. The recommended wait period is 20 µs per 100 nF of capacitance on V_{LCD1}.

1. Set DM = 1 and PD = 0
2. Delay
3. Set the multiplication factor to 2 by setting S[1:0] = 00
4. Set the required V_{OP} and PRS.
5. Set HVE = 1 to switch-on the charge pump with a multiplication factor of 2
6. Delay
7. Increase the number of stages, one at a time, with a delay between each until the required level is achieved.

Table 7 HV generator multiplication factor

S[1]	S[0]	MULTIPLICATION FACTOR
0	0	2 × V_{DD2}
0	1	3 × V_{DD2}
1	0	4 × V_{DD2}
1	1	5 × V_{DD2}

7.15 Addressing

Addressing of the RAM can be split into two parts; input addressing and output addressing. Input addressing is concerned with writing data into the RAM. Output addressing is almost entirely automatic and taken care of by the device, however, it is possible to affect the output mode.

7.15.1 INPUT ADDRESSING

Data is down loaded byte wise into the RAM matrix of the PCF8535 as indicated in Figs 6 to 10.

The display RAM has a matrix of 65 × 133 bits. The columns are addressed by a combination of the X address pointer and the X-RAM page pointer, whilst the rows addressed in groups of 8 by the Y address pointer. The X address pointer has a range of 0 to 127 (7FH). Its range can be extended by the X-RAM page pointer, XM_0. The Y address pointer has a range of 0 to 8 (08H). The PCF8535 is limited to 133 columns by 65 rows, addressing the RAM outside of this area is not allowed.

Table 8 Effect of X-RAM page pointer

X ADDRESS POINTER	X-RAM PAGE POINTER XM_0	ADDRESSED COLUMN MX = 0	ADDRESSED COLUMN MX = 1
0	0	C0	C132
1	0	C1	C131
2	0	C2	C130
:	:	:	:
125	0	C125	C7
126	0	C126	C6
127	0	C127	C5
0	1	C128	C4
1	1	C129	C3
:	:	:	:
4	1	C132	C0

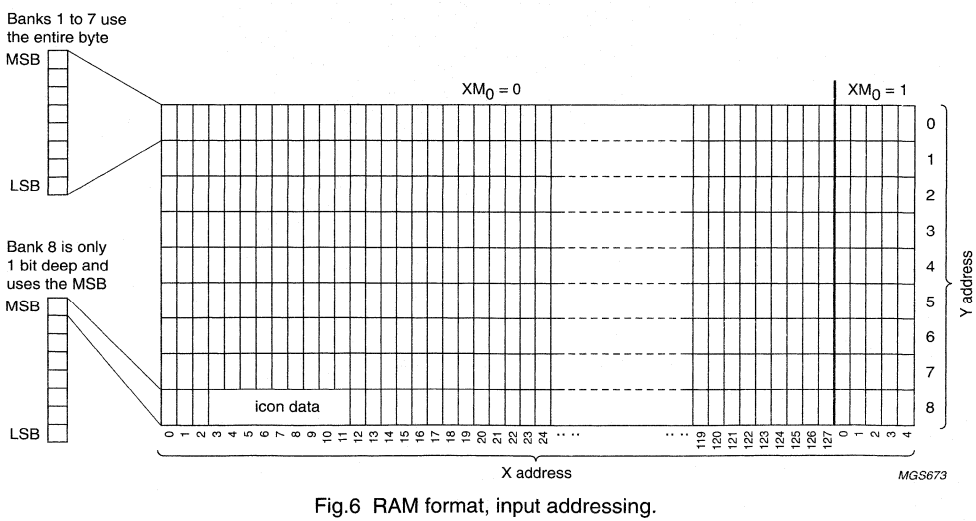


Fig.6 RAM format, input addressing.

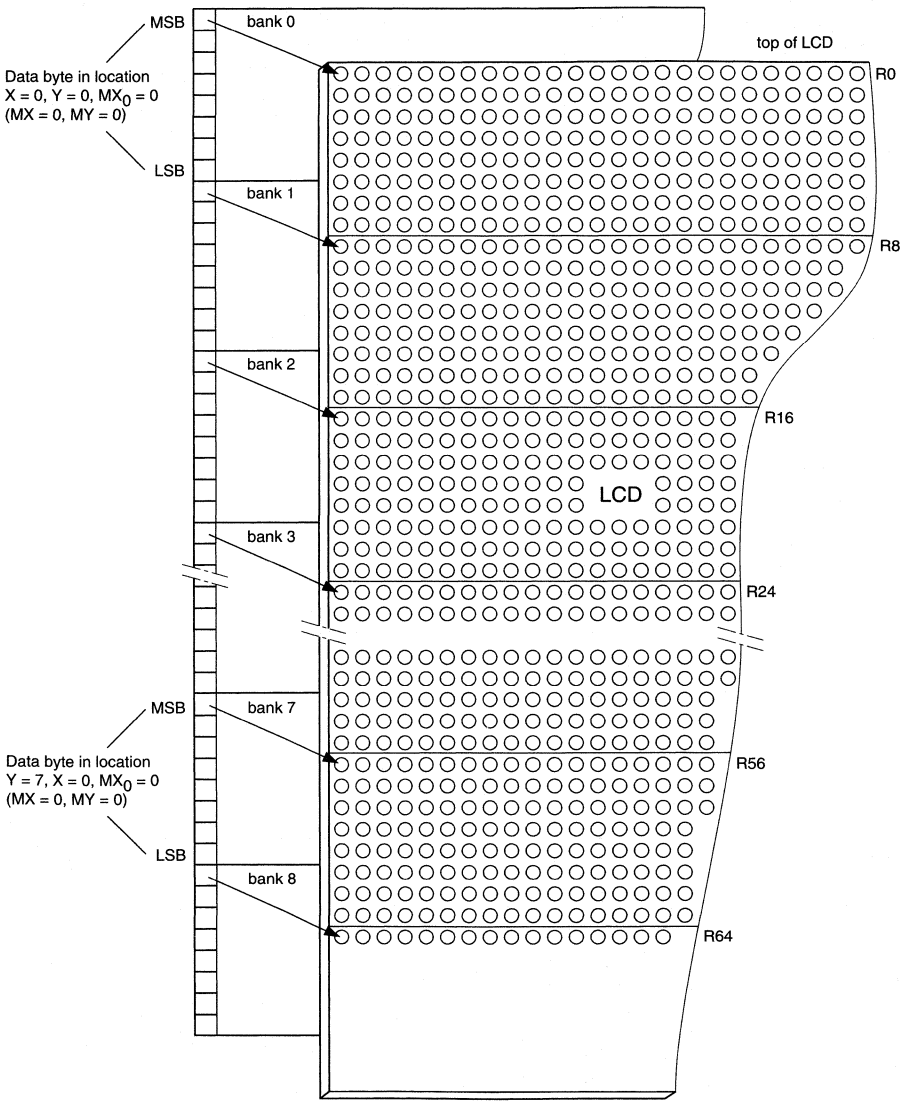


Fig.7 DDRAM to display mapping.

Two automated addressing modes are available; vertical addressing (V = 1) and horizontal addressing (V = 0). These modes change the way in which the auto-incrementing of the address pointers is handled and are independent of multiplex rate. The auto-incrementing works in a way so as to aid filling of the entire RAM. It is not a prerequisite of operation that the entire RAM is filled; in lower multiplex modes not all of the RAM will be needed. For these multiplex rates, use of horizontal addressing mode (V = 0) is recommended.

Addressing the icon row is a special case as these RAM locations are not automatically accessed. These locations must be explicitly addressed by setting the Y address pointer to 8.

The Y address pointer does not auto-increment when the X address over or underflows, it stays set to 8. Writing icon data is independent of the vertical and horizontal addressing mode, but is effected by the mirror X bit as described in Sections 7.15.1.2 and 7.15.1.3.

The addressing modes may be further modified by the mirror X bit MX. This bit causes the data to be written into the RAM from right to left instead of the normal left to right. This effectively flips the display about the Y axis. The MX bit affects the mode of writing into the RAM, changing the MX bit after RAM data is written will not flip the display.

7.15.1.1 Vertical addressing: non-mirrored; V = 1 and MX = 0

In the vertical addressing mode data is written top to bottom and left to right. Here, the Y counter will auto-increment from 0 to 7 and then wrap around to 0 (see Fig.8). On each wrap over, the X counter will increment to address the next column. When the X counter wraps over from 127 to 0, the XM_0 bit will be set. The last address accessible is Y = 7, X = 4 and XM_0 = 1; after this access the counter will wrap around to Y = 0, X = 0 and XM_0 = 0.

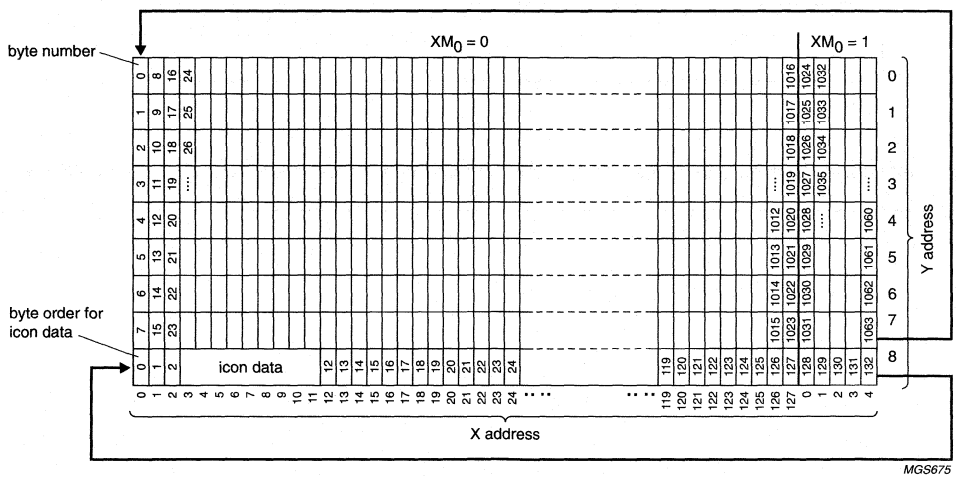


Fig.8 Sequence of writing data bytes into the RAM with normal vertical addressing (V = 1 and MX = 0).

7.15.1.2 Vertical addressing: mirrored; V = 1 and MX = 1

It is also possible to write data from right to left, instead of from the normal left to right, still going top to bottom. In the mirrored vertical addressing mode the Y counter will auto-increment from 0 to 7 and then wrap around to 0 (see Fig.9). On each wrap-over, the X counter will decrement to address the preceding column. The XM_0 bit will be automatically toggled each time the X address counter wraps over from 0. The last address accessible is Y = 7, X = 0 and XM_0 = 0; after this access the counter will wrap around to Y = 0, X = 4 and XM_0 = 1.

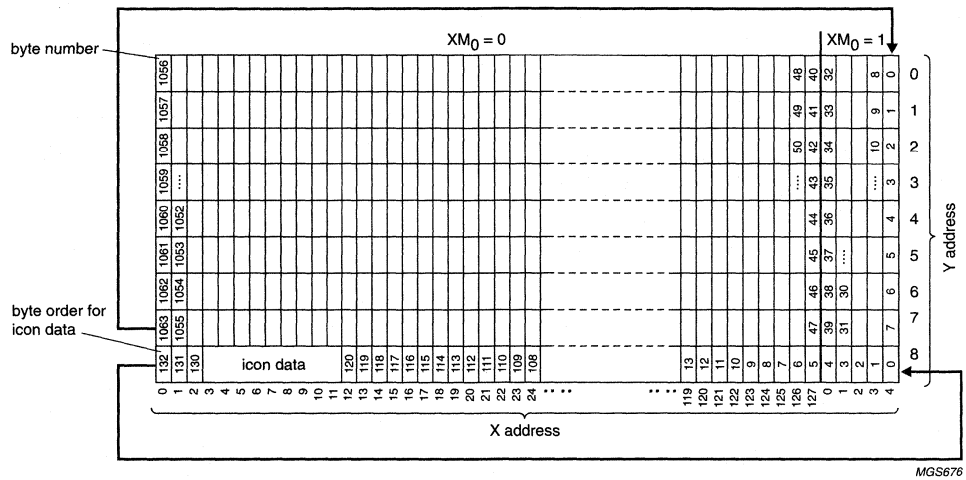


Fig.9 Sequence of writing data bytes into the RAM with mirrored vertical addressing (V = 1 and MX = 1).

7.15.1.3 Horizontal addressing: non-mirrored; V = 0 and MX = 0

In horizontal addressing mode data is written from left to right and top to bottom. Here, the X counter will auto-increment from 0 to 127, set the XM_0, then count 0 to 4 before wrapping around to 0 and clearing the XM_0 bit (see Fig.10). On each wrap-over, the Y counter will increment. The last address accessible is Y = 7, X = 4 and XM_0 = 1; after this access the counter will wrap around to Y = 0, X = 0 and XM_0 = 0.

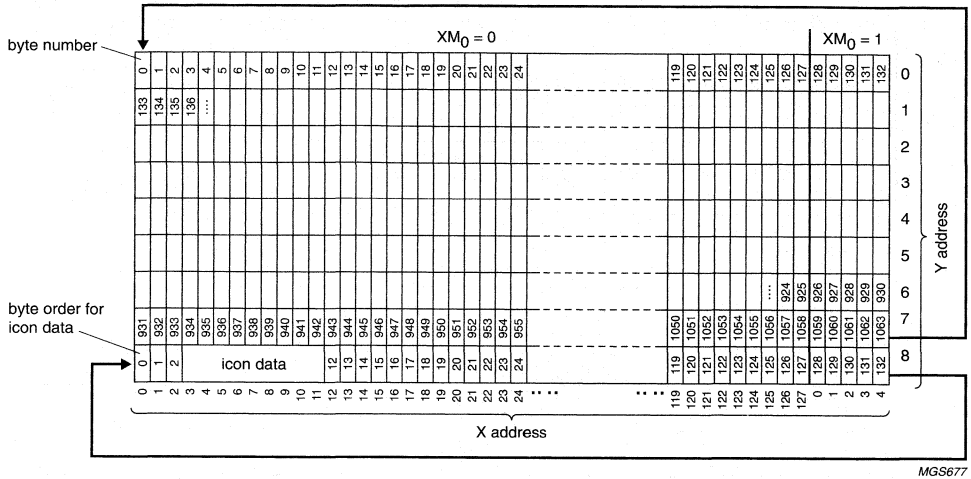


Fig.10 Sequence of writing data bytes into the RAM with normal horizontal addressing (V = 0 and MX = 0).

7.15.1.4 Horizontal addressing: mirrored; V = 0 and MX = 1

It is also possible to write data from right to left, instead of from the normal left to right, still going top to bottom. In the mirrored horizontal addressing mode the X counter will auto-decrement from 4 to 0, clear the XM_0, then count 127 to 0 before wrapping around to 4 and setting the XM_0 bit (see Fig.10). On each wrap-over, the Y counter will increment. The last address accessible is Y = 7, X = 0 and XM_0 = 0; after this access the counter will wrap around to Y = 0, X = 4 and XM_0 = 1.

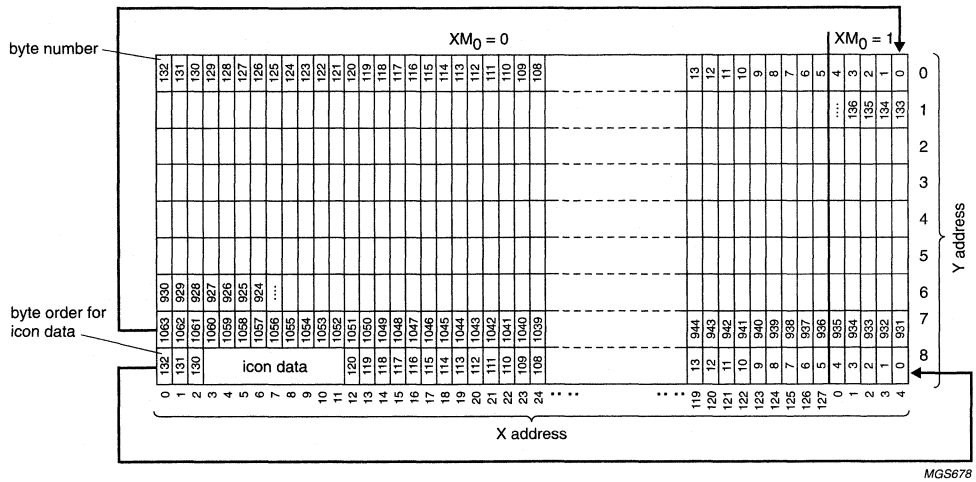


Fig.11 Sequence of writing data bytes into the RAM with mirrored horizontal addressing (V = 0 and MX = 1).

7.15.2 OUTPUT ADDRESSING

The output addressing of the RAM is done automatically in accordance with the currently selected multiplex rate. Normally the user would not need to make any alterations to the addressing. There are, however, circumstances pertaining to various connectivity of the device on a glass that would benefit from some in-built functionality. Three modes exist that enable the user to modify the output addressing, namely:

1. MY, mirror the Y axis. This mode effectively flips the display about the X axis, resulting in an upside down display. The effect is observable immediately the bit is modified. This is useful if the device is to be mounted above the display area instead of below.
2. Bottom Row Swap (BRS). This mode swaps the order of the rows on the bottom(1) edge of the chip. This is useful to aide routing to the display when it is not possible to pass tracks under the device; a typical example would be in tape carrier package. This mode is often used in conjunction with TRS.
3. Top Row Swap (TRS). As with BRS, but swaps the order of rows on the top(1) edge of the chip.

7.15.2.1 Mirror Y, MY

As described above, the Y axis is mirrored in the X axis.

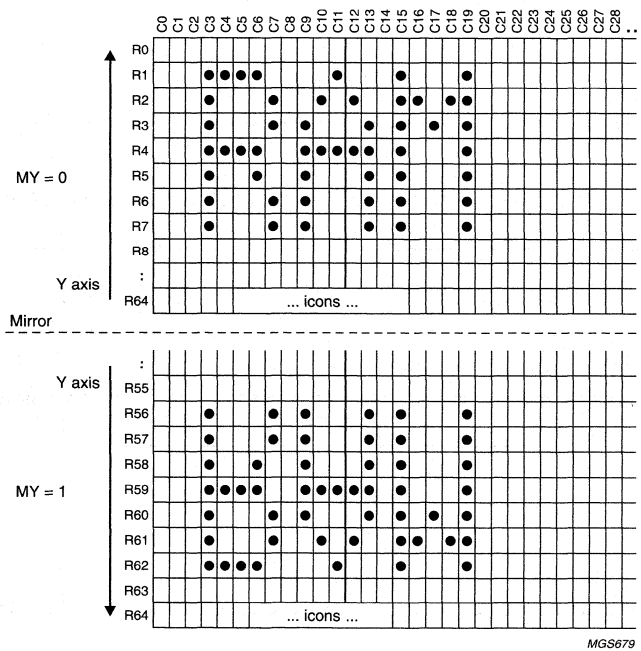


Fig.12 Mirror Y behaviour (Mux rate 1 : 65).

(1) The top edge is defined as the edge containing the user interface connections. The bottom edge is the opposing edge.

7.15.2.2 Bottom Row Swap

Here the order of the row pads is modified. Each block of rows is swapped about its local Y axis.

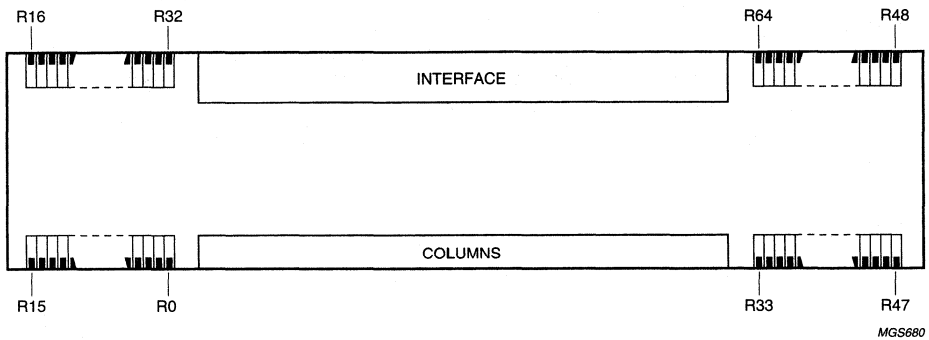


Fig.13 Bottom row swap.

7.15.2.3 Top Row Swap

Here the order of the row pads is modified. Each block of rows is swapped about its local Y axis.

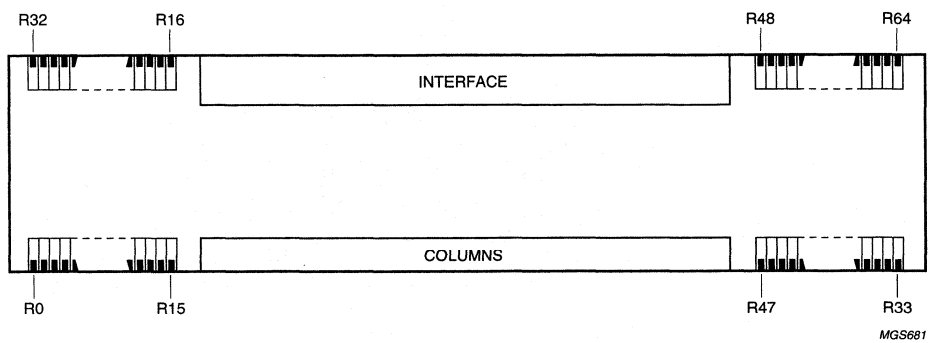


Fig.14 Top row swap.

7.15.2.4 Output row order

The order in which the rows are activated is a function of bits MY, TRS, BRS and the selected multiplex mode. Tables 9 to 12 give the order in which the rows are activated. In all cases, the RAM is accessed in a linear fashion, starting at zero with a jump to the last row for the icon data.

Table 9 Row order for BRS = 0 and TRS = 0

MULTIPLEX MODE	MY = 0	MY = 1
1 : 17	R0 to R15 and R64	R15 to R0 and R64
1 : 26	R0 to R24 and R64	R24 to R0 and R64
1 : 33	R0 to R31 and R64	R31 to R0 and R64
1 : 49	R0 to R47 and R64	R47 to R0 and R64
1 : 65	R0 to R64	R63 to R0 and R64

Table 10 Row order for BRS = 1 and TRS = 0

MULTIPLEX MODE	MY = 0	MY = 1
1 : 17	R15 to R0 and R64	R0 to R15 and R64
1 : 26	R15 to R0, R16 to R24 and R64	R24 to R16, R0 to R15 and R64
1 : 33	R15 to R0, R16 to R31 and R64	R31 to R16, R0 to R15 and R64
1 : 49	R15 to R0, R16 to R32, R47 to R33 and R64	R33 to R47, R32 to R16, R0 to R15 and R64
1 : 65	R15 to R0, R16 to R32, R47 to R33 and R48 to R64	R63 to R48, R33 to R47, R32 to R16, R0 to R15 and R64

Table 11 Row order for BRS = 0 and TRS = 1

MULTIPLEX MODE	MY = 0	MY = 1
1 : 17	R0 to R15 and R48	R15 to R0 and R48
1 : 26	R0 to R15, R32 to R24 and R48	R24 to R32, R15 to R0 and R48
1 : 33	R0 to R15, R32 to R17 and R48	R17 to R32, R15 to R0 and R48
1 : 49	R0 to R15, R32 to R16, R33 to R47 and R48	R47 to R33, R16 to R32, R15 to R0 and R48
1 : 65	R0 to R15, R32 to R16, R33 to R47 and R64 to R48	R49 to R64, R47 to R33, R16 to R32, R15 to R0 and R48

Table 12 Row order for BRS = 1 and TRS = 1

MULTIPLEX MODE	MY = 0	MY = 1
1 : 17	R15 to R0 and R48	R0 to R15 and R48
1 : 26	R15 to R0, R32 to R24 and R48	R0 to R15, R32 to R24 and R48
1 : 33	R15 to R0, R32 to R17 and R48	R0 to R15, R17 to R32 and R48
1 : 49	R15 to R0, R32 to R16, R47 to R33 and R48	R0 to R15, R16 to R32, R33 to R47 and R48
1 : 65	R15 to R0, R32 to R16, R47 to R33 and R64 to R48	R0 to R15, R16 to R32, R33 to R47, R47 to R64 and R48

7.16 Instruction set

Data accesses to the PCF8535 can be broken down into two areas, those that define the operating mode of the device and those that fill the display RAM; the distinction being the D/$\overline{C}$ bit. When the D/$\overline{C}$ bit is at logic 0, the chip will respond to instructions as defined in Table 16. When the D/$\overline{C}$ bit is at logic 1, the chip will store data into the RAM. Data may be written to the chip that is independent to the presence of the display clock.

There are 4 instruction types. Those which:

1. Define PCF8535 functions such as display configuration, etc.
2. Set internal RAM addresses
3. Perform data transfer with internal RAM
4. Others.

In normal use, category 3 instructions are the most frequently used. To lessen the MPU program load, automatic incrementing by one of the internal RAM address pointers after each data write is implemented.

The instruction set is broken down into several pages, each command page being individually addressed via the H[2:0] bits.

7.16.1 RAM READ/WRITE COMMAND PAGE

This page is special in that it is accessible independently of the H bits. This page is mainly used as a stepping stone to other pages. Sending the 'Default H[2:0]' command will cause an immediate step to the 'Function and RAM command page' which will allow the H[2:0] bits to be set.

7.16.2 FUNCTION AND RAM COMMAND PAGE

7.16.2.1 Command page

Setting H[2:0] will move the user immediately to the required command page. Pages not listed should not be accessed as the behaviour is not defined.

7.16.2.2 Function set

PD

When PD = 1, the LCD driver is in power-down mode:

- All LCD outputs at V_{SS}
- Oscillator off
- V_{LCDIN} may be disconnected
- I^2C-bus interface accesses are possible
- RAM contents are not cleared; RAM data can be written
- Register settings remain unchanged.

V

When V = 0, horizontal addressing is selected. When V = 1, vertical addressing is selected. The behaviour is described in Section 7.15.

7.16.2.3 RAM page

The XM_0 bit extends the RAM into a second page. The bit may be considered to be the Most Significant Bit (MSB) of an 8-bit X address. The behaviour is described in Section 7.15.

7.16.2.4 Set Y address

The Y address is used as a pointer to the RAM for RAM writing. The range is 0 to 8. Each bank corresponds to a set of 8 rows, the only exception being bank 8, which contains the icon data and is only 1-bit deep; see Table 13.

Table 13 Y address pointer

Y[3]	Y[2]	Y[1]	Y[0]	BANK	ROWS
0	0	0	0	bank 0	R0 to R7
0	0	0	1	bank 1	R8 to R15
0	0	1	0	bank 2	R16 to R23
0	0	1	1	bank 3	R24 to R31
0	1	0	0	bank 4	R32 to R39
0	1	0	1	bank 5	R40 to R47
0	1	1	0	bank 6	R48 to R55
0	1	1	1	bank 7	R56 to R63
1	0	0	0	bank 8 (icons)	R64

7.16.2.5 Set X address

The X address is used as a pointer to the RAM for RAM writing. The range of X is 0 to 127 (7FH) and may be extended by the XM_0 bit. The combined value of XM_0 and X address directly corresponds to the display column number when MX = 0 and corresponds to the inverse display column number when MX = 1; see Table 14.

Table 14 X address pointer

XM_0, X[6:0]	ADDRESSED COLUMN, MX = 0	ADDRESSED COLUMN, MX = 1
0	C0	C132
1	C1	C131
2	C2	C130
3	C3	C129
:	:	:
129	C129	C3
130	C130	C2
131	C131	C1
132	C132	C0

7.16.3 DISPLAY SETTING COMMAND PAGE

7.16.3.1 Display control

The D and E bits set the display mode as given in Table 15.

Table 15 Display control

D	E	MODE
0	0	display blank
1	0	normal mode
0	1	all display segments on
1	1	inverse video

7.16.3.2 External display control

Mirror X and mirror Y have the effect of flipping the display left to right or top to bottom respectively. MX works by changing the order data that is written into the RAM. As such, the effects of toggling MX will only be seen after data is written into the RAM. MY works by reversing the order that column data is accessed relative to the row outputs. The effect of toggling MY will be seen immediately. The behaviour of both of these bits is further described in Section 7.15.

7.16.3.3 Bias system

BS[2:0] sets the bias system; see Section 7.10.

7.16.3.4 Display size

Physically large displays require stronger drivers. Bit IB enables the user to select a stronger driving mode and should be used if suitable display quality can not be achieved with the default setting.

7.16.3.5 Multiplex rate

M[2:0] sets the multiplex rate; see Section 7.9.

7.16.4 HV-GEN COMMAND PAGE

7.16.4.1 HV-gen control

PRS

Programmable charge pump range select. This bit defines whether the programmed voltage for V_{OP} is in the low or the high range. The behaviour of this bit is further described in Section 7.13.

HVE

High voltage generator enable. When set to logic 0, the charge pump is disabled. When set to logic 1, the charge pump is enabled.

7.16.4.2 HV-gen stages

S[1:0] set the multiplication factor of the charge pump ranging from times 2 to times 5. The behaviour of these bits is further described in Section 7.14.

7.16.4.3 Temperature coefficients

TC[2:0] set the required temperature coefficient. The behaviour of these bits is further described in Section 7.12.

7.16.4.4 Temperature measurement control

The SM bit is used to initiate a temperature measurement. The SM bit is automatically cleared at the end of the measurement. The behaviour of this bit is further described in Section 7.11.

7.16.4.5 V_{LCD} control

V_{OP}[6:0] sets the required operating voltage for the display.

7.16.5 Special feature command page

7.16.5.1 State control

DM

Direct mode allows V_{LCDOUT} to be sourced directly from V_{DD2}. This may be useful in systems where V_{DD} is to be used for V_{LCD}.

DOF

Display off will turn off all internal analog circuitry that is not required for temperature measurement.
As a consequence the display will be turned off. This mode is only required if temperature measurements are required whilst in power-down mode.

7.16.5.2 Oscillator setting

The internal oscillator may be disabled and the source clock for the display derived from the OSC pad. It is important to remember that LCDs are damaged by DC voltages and that the clock, whether derived internally or externally, should never be disabled whilst the display is active. The internal oscillator is switched off during power-down mode.

When using an external clock and disabling it during power-down mode will further reduce the standby current. If it is not possible to disable it externally then it is worth noting that by selecting the internal clock, which is disabled during power-down mode, the same effect may be achieved.

7.16.5.3 COG/TCP

The chip may be mounted on either a glass, foil or tape carrier package. For these applications, different organizations of the row pads are required to negate the necessity of routing under the device. The TRS and BRS allow for this swapping. The behaviour of both of these bits is further described in Section 7.15.

7.16.6 Instruction set

Table 16 Instruction set

INSTRUCTION	D/$\overline{C}$	R/$\overline{W}$(1)	I²C-BUS COMMAND BYTE								I²C-BUS COMMANDS
			DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
H[2:0] = XXX; RAM read/write command page											
Write data	1	0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	writes data to display RAM
Read status	0	1	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	returns result of temperature measurement
NOP	0	0	0	0	0	0	0	0	0	0	no operation
Default H[2:0]	0	0	0	0	0	0	0	0	0	1	jump to H[2:0] = 111
H[2:0] = 111; function and RAM command page											
Command page	0	0	0	0	0	0	1	H_2	H_1	H_0	select command page
Function set	0	0	0	0	0	1	0	PD	V	0	power-down control, data entry mode
RAM page	0	0	0	0	1	0	0	XM_0	0	0	set RAM page for X address
Set Y address of RAM	0	0	0	1	0	0	Y_3	Y_2	Y_1	Y_0	sets Y address of RAM $0 \leq Y \leq 8$
Set X address of RAM	0	0	1	X_6	X_5	X_4	X_3	X_2	X_1	X_0	sets X address of RAM $0 \leq X \leq 127$

INSTRUCTION	D/$\overline{C}$	R/$\overline{W}$(1)	I²C-BUS COMMAND BYTE								I²C-BUS COMMANDS
			DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
H[2:0] = 110; display setting command page											
Display control	0	0	0	0	0	0	0	1	D	E	sets display mode
External display control	0	0	0	0	0	0	1	MX	MY	0	mirror X, mirror Y
Bias system	0	0	0	0	0	1	0	BS_2	BS_1	BS_0	set bias system
Display size	0	0	0	0	1	0	0	IB	0	0	set current for bias system
Multiplex rate	0	0	1	0	0	0	0	M_2	M_1	M_0	set multiplex rate
H[2:0] = 101; HV-gen command page											
HV-gen control	0	0	0	0	0	0	0	1	PRS	HVE	V_{LCD} range, enable/disable HV-gen
HV-gen stages	0	0	0	0	0	0	1	0	S_1	S_0	# of HV-gen voltage multiplication
Temperature coefficients	0	0	0	0	0	1	0	TC_2	TC_1	TC_0	set temperature coefficient
Temperature measurement control	0	0	0	0	1	0	0	0	0	SM	start temperature measurement
V_{LCD} control	0	0	1	V_{OP6}	V_{OP5}	V_{OP4}	V_{OP3}	V_{OP2}	V_{OP1}	V_{OP0}	set V_{LCD} register $0 \leq V_{LCD} \leq 127$
H[2:0] = 011; special feature command page											
State control	0	0	0	0	0	0	0	1	DOF	DM	display off, direct mode
Oscillator setting	0	0	0	0	0	0	1	0	EC	0	enable/disable the internal oscillator
COG/TCP	0	0	0	1	0	TRS	BRS	0	0	0	top row swap, bottom row swap

Note

1. R/$\overline{W}$ is set in the slave address.

Table 17 Description of the symbols used in Table 16

BIT	0	1
PD	chip is active	chip is in power-down mode
V	horizontal addressing	vertical addressing
HVE	voltage multiplier disabled	voltage multiplier enabled
PRS	V_{LCD} programming range LOW	V_{LCD} programming range HIGH
SM	no measurement	start measurement
MX	no X mirror	mirror X
MY	no Y mirror	mirror Y
TRS	top row swap inactive	top row swap active
BRS	bottom row swap inactive	bottom row swap active
EC	internal oscillator enabled; OSC pad ignored	internal oscillator disabled; OSC pad enabled for input
DM(1)	direct mode disabled	direct mode enabled
DOF(1)	display off mode disabled	display off mode enabled
IB	low current mode for smaller displays	high current mode for larger displays

Note

1. Conditional on other bits.

Table 18 Priority behaviour of bits PD, DOF, HVE and DM; note 1

PD	DOF	HVE	DM	MODE
1	X	X	X	chip is in power-down mode as defined under PD
0	1	X	X	all analog blocks except those required for temperature measurement are off
0	0	1	X	chip is active and using the internal V_{LCD} generator
0	0	0	1	chip is active and using V_{DD} as V_{LCD}
0	0	0	0	chip is active and using an external V_{LCD} generator attached to V_{LCDIN}

Note

1. X = don't care state.

7.17 I²C-bus interface

7.17.1 Characteristics of the I²C-bus

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

7.17.1.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal. Bit transfer is illustrated in Fig.15.

7.17.1.2 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P). The START and STOP conditions are illustrated in Fig.16.

7.17.1.3 System configuration

The system configuration is illustrated in Fig.17.

- Transmitter: the device which sends the data to the bus
- Receiver: the device which receives the data from the bus
- Master: the device which initiates a transfer, generates clock signals and terminates a transfer
- Slave: the device addressed by a master
- Multi-master: more than one master can attempt to control the bus at the same time without corrupting the message
- Arbitration: procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted
- Synchronization: procedure to synchronize the clock signals of two or more devices.

7.17.1.4 Acknowledge

Each byte of 8 bits is followed by an acknowledge bit. The acknowledge bit is a HIGH signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition. Acknowledgement on the I²C-bus is illustrated in Fig.18.

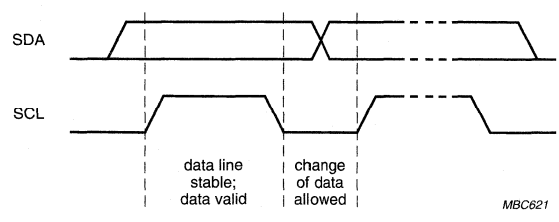


Fig.15 Bit transfer.

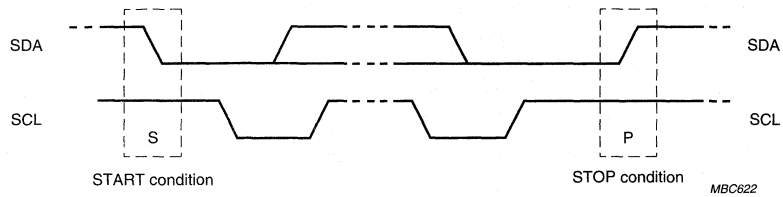


Fig.16 Definition of START and STOP conditions.

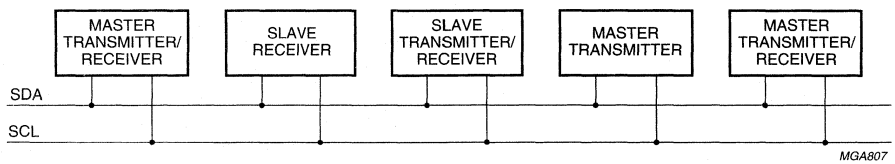


Fig.17 System configuration.

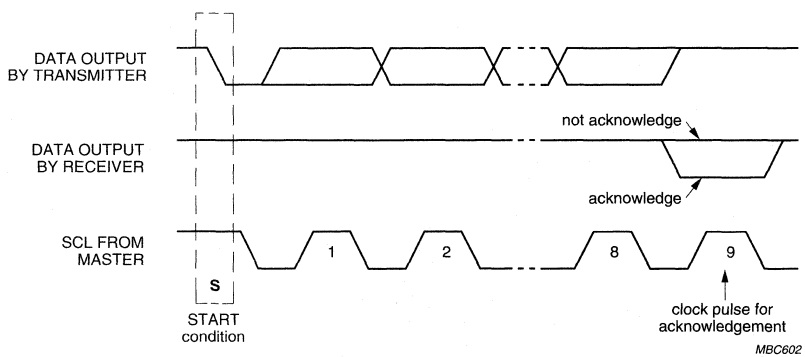


Fig.18 Acknowledgement on the I^2C-bus.

7.17.2 I²C-BUS PROTOCOL

The PCF8535 is a slave receiver/transmitter. If data is to be read from the device the SDAOUT pad must be connected, otherwise SDAOUT is unused.

Before any data is transmitted on the I²C-bus, the device which should respond is addressed. Four slave addresses, 0111100, 0111101, 0111110 and 0111111 are reserved for the PCF8535. The Least Significant Bits (LSBs) of the slave address is set by connecting SA1 and SA0 to either logic 0 (V_{SS}) or logic 1 (V_{DD}).

A sequence is initiated with a START condition (S) from the I²C-bus master which is followed by the slave address. All slaves with the corresponding address acknowledge in parallel, all the others will ignore the I²C-bus transfer.

After the acknowledgement cycle of a write, a control byte follows which defines the destination for the forthcoming data byte and the mode for subsequent bytes. For a read, the PCF8535 will immediately start to output the requested data until a NOT acknowledge is transmitted by the master. The sequence should be terminated by a STOP in the event that no further access is required for the time being, or by a RE-START, should further access be required.

For ease of operation a continuation bit, Co, has been included. This bit allows the user to set-up the chip configuration and transmit RAM data in one access. A data selection bit, D/$\overline{C}$, defines the destination for data. These bits are contained in the control byte. DB5 to DB0 should be set to logic 0. These bits are reserved for future expansion.

Table 19 Co and D/$\overline{C}$ definitions

BIT	0/1	R/$\overline{W}$	ACTION
Co	0	n.a.	last control byte to be sent: only a stream of data bytes are allowed to follow; this stream may only be terminated by a STOP or RE-START condition
	1		another control byte will follow the data byte unless a STOP or RE-START condition is received
D/$\overline{C}$	0	0	data byte will be decoded and used to set up the device
		1	data byte will return the contents of the currently selected status register
	1	0	data byte will be stored in the display RAM
		1	no provision for RAM read back is provided

An example of a write access is given in Fig.19. Here, multiple instruction data is sent, followed by multiple display bytes.

An example of a read access is given in Fig.20.

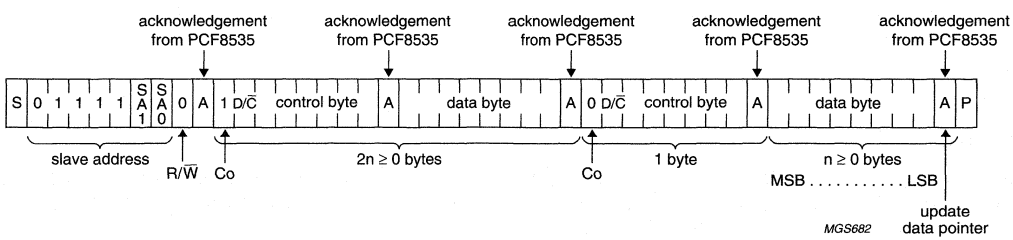


Fig.19 Master transmits to slave receiver; write mode.

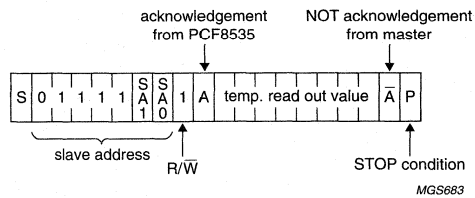


Fig.20 Master reads a slaves' status register.

8 LIMITING VALUES (PROVISIONAL)

In accordance with the Absolute Maximum Rating System (IEC 134); notes 1, 2 and 3.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.5	+7.0	V
I_{DD}	supply current	−50	+50	mA
V_{LCD}	LCD supply voltage	−0.5	+17.0	V
I_{LCD}	LCD supply current	−50	+50	mA
I_{SS}	negative supply current	−50	+50	mA
V_I/V_O	input/output voltage (any input/output)	−0.5	V_{DD} + 0.5	V
I_I	DC input current	−10	+10	mA
I_O	DC output current	−10	+10	mA
P_{tot}	total power dissipation per package	−	300	mW
P/out	power dissipation per output	−	30	mW
T_{amb}	ambient temperature	−40	+85	°C
T_{stg}	storage temperature	−65	+150	°C
$T_{j(max)}$	maximum junction temperature	−	150	°C

Notes

1. Stresses above these values listed may cause permanent damage to the device.
2. Parameters are valid over the operating temperature range unless otherwise specified. All voltages are referenced to V_{SS} unless otherwise specified.
3. V_{SS} = 0 V.

9 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is recommended to take normal precautions appropriate to handling MOS devices (see *"Handling MOS Devices"*).

10 DC CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; V_{SS} = 0 V; V_{LCD} = 4.5 to 16.0 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{LCDIN}	LCD supply voltage	Mux mode 1 : 65	8.0	–	16.0	V
		Mux mode 1 : 49	8.0	–	16.0	V
		Mux mode 1 : 34	–	–	16.0	V
		Mux mode 1 : 26	–	–	16.0	V
		Mux mode 1 : 17	–	–	16.0	V
I_{LCDIN}	LCD supply current	normal mode; notes 1 and 2	–	40	90	µA
		normal mode; notes 1 and 4	–	18	40	µA
V_{LCDOUT}	generated supply voltage	LCD voltage generator enabled	–	–	16.0	V
V_{DD1}, V_{DD2}, V_{DD3}	supply voltage		4.5	–	5.5	V
I_{DD}	supply current	power-down mode; notes 1, 3 and 5	–	2	10	µA
		display off mode; notes 1 and 5	–	–	–	µA
		normal mode; notes 1 and 6	–	160	350	µA
		normal mode; notes 1 and 2	–	40	90	µA
Logic						
V_{IL}	LOW-level input voltage		V_{SS}	–	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	–	V_{DD}	V
I_{OL}	LOW-level output current (SDA)	V_{OL} = 0.4 V; V_{DD} = 5 V	3.0	–	–	mA
I_L	leakage current	$V_I = V_{DD}$ or V_{SS}	−1	–	+1	µA
Column and row outputs						
$R_{o(col)}$	column output resistance C0 to C132	V_{LCD} = 12 V; note 7	–	–	10	kΩ
$R_{o(row)}$	row output resistance R0 to R33	V_{LCD} = 12 V; note 7	–	–	3.0	kΩ
$V_{bias(col)}$	bias tolerance C0 to C132		−100	0	+100	mV
$V_{bias(row)}$	bias tolerance R0 to R64		−100	0	+100	mV
Temperature coefficient						
t_{cut}	cut point temperature	T_{amb} = −20 to +70 °C	–	27	–	°C

Notes

1. LCD outputs are open-circuit, inputs at V_{DD} or V_{SS}, bus inactive, f_{OSC} = typical internal oscillator frequency.
2. Conditions are: V_{DD1} to V_{DD3} = 5.0 V, V_{LCD} = 12.0 V and external V_{LCD}.
3. Power-down mode. During power-down all static currents are switched off.
4. Conditions are: V_{DD1} to V_{DD3} = 5.0 V, $V_{LCD} = V_{DD2}$ and external V_{LCD}.
5. Internal V_{LCD} generation or external V_{LCD}.
6. Conditions are: V_{DD1} to V_{DD3} = 5.0 V, V_{LCD} = 12.0 V and voltage multiplier = $3V_{DD}$.
7. I_{LCD} = 10 µA. Outputs tested one at a time.

11 AC CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; V_{SS} = 0 V; V_{LCD} = 4.5 to 16.0 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$f_{fr(LCD)}$	LCD frame frequency (internal clock)		48	80	165	Hz
$f_{clk(ext)}$	external clock frequency	see Table 20	120	–	410	kHz
$t_{W(RESL)}$	reset LOW pulse width		1	–	–	µs
$t_{W(RESH)}$	reset HIGH pulse width		5	–	–	µs
$t_{SU;RESL}$	reset LOW pulse set-up time after power-on	notes 1 and 2	–	–	30	µs
$t_{R(op)}$	end of reset pulse to interface being operational		–	–	3	µs
Serial-bus interface; note 3						
f_{SCL}	SCL clock frequency		0	–	400	kHz
t_{LOW}	SCL clock LOW period		1.3	–	–	µs
t_{HIGH}	SCL clock HIGH period		0.6	–	–	µs
$t_{SU;DAT}$	data set-up time		100	–	–	ns
$t_{HD;DAT}$	data hold time		0	–	0.9	µs
t_r	SCL, SDA rise time	note 4	$20 + 0.1C_b$	–	300	ns
t_f	SCL, SDA fall time	note 4	$20 + 0.1C_b$	–	300	ns
C_b	capacitive load represented by each bus line		–	–	400	pF
$t_{SU;STA}$	set-up time for a repeated START condition		0.6	–	–	µs
$t_{HD;STA}$	START condition hold time		0.6	–	–	µs
$t_{SU;STO}$	set-up time for STOP condition		0.6	–	–	µs
t_{SP}	tolerable spike width on bus		–	–	50	ns
t_{BUF}	bus free time between a STOP and START condition		1.3	–	–	µs

Notes

1. V_{DD1} to V_{DD3} = 5 V.
2. Decoupling capacitor V_{LCD} and V_{SS} = 100 nF (higher capacitor size increases $t_{SU;RESL}$ and higher V_{DD1} to V_{DD3} reduces $t_{SU;RESL}$).
3. All timing values are valid within the operating supply voltage and ambient temperature range and are referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.
4. C_b = total capacitance of one bus line in pF.

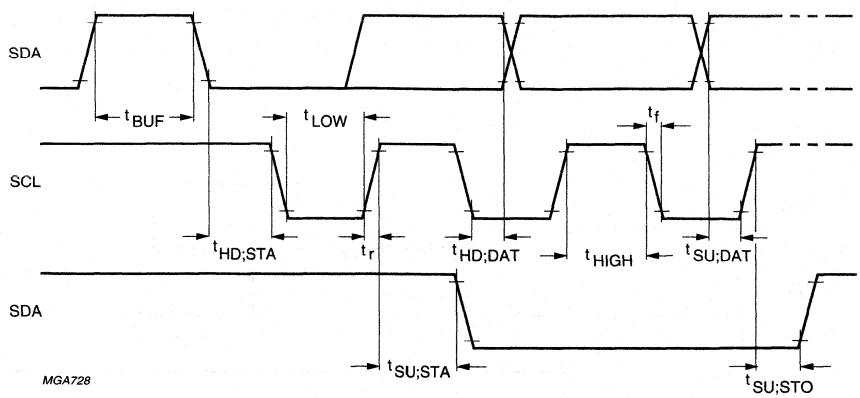


Fig.21 I^2C-bus timing diagram.

Table 20 External clock frequency

MUX MODE	DIVISION RATIO	EXTERNAL CLOCK FREQUENCY FOR AN 80 Hz FRAME FREQUENCY (DIVISION RATIO × 80 Hz)
1 : 65	3168	253 kHz
1 : 48	3136	251 kHz
1 : 33	2720	218 kHz
1 : 26	2592	207 kHz
1 : 17	2592	207 kHz

12 RESET TIMING

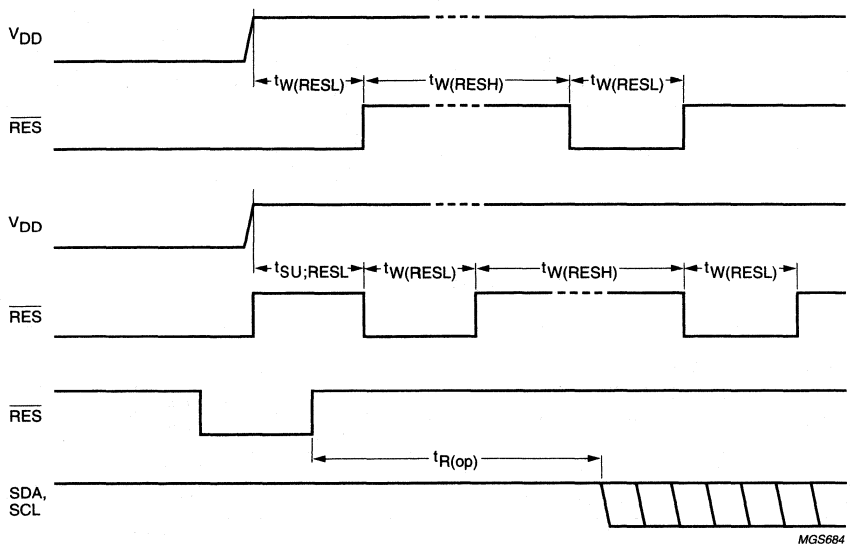
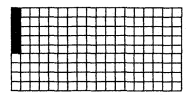
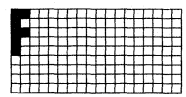
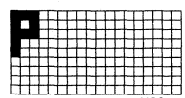
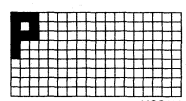
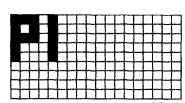
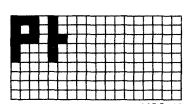
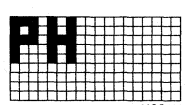
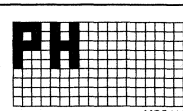


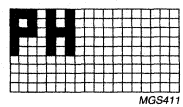
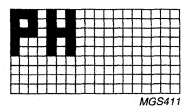
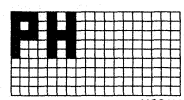
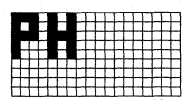
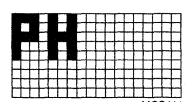
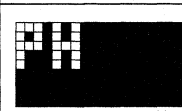
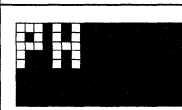
Fig.22 Reset timing.

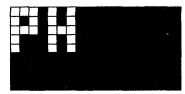
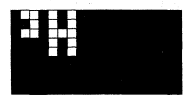
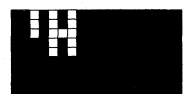
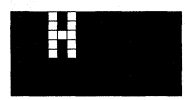
13 APPLICATION INFORMATION

Table 21 Programming example for PCF8535

STEP	SERIAL BUS BYTE								DISPLAY(1)	OPERATION
1	START condition								BLANK	start
2	DB7 0	DB6 1	DB5 1	DB4 1	DB3 1	DB2 SA1	DB1 SA0	DB0 0	BLANK	slave address, R/$\overline{W}$ = 0
3	DB7 0	DB6 0	DB5 0	DB4 0	DB3 0	DB2 0	DB1 0	DB0 0	BLANK	control byte, Co = 0, D/$\overline{C}$ = 0
4	DB7 0	DB6 0	DB5 0	DB4 0	DB3 0	DB2 0	DB1 0	DB0 1	BLANK	H[2:0] independent command; select function and RAM command page H[1:0] = 111
5	DB7 0	DB6 0	DB5 0	DB4 1	DB3 0	DB2 0	DB1 0	DB0 0	BLANK	function and RAM command page; PD = 0, V = 0
6	DB7 0	DB6 0	DB5 0	DB4 0	DB3 1	DB2 1	DB1 1	DB0 0	BLANK	function and RAM command page; select display setting command page H[1:0] = 110
7	DB7 0	DB6 0	DB5 0	DB4 1	DB3 0	DB2 0	DB1 1	DB0 0	BLANK	display setting command page; set bias system to $^1/_9$BS[2:0] = 010
8	DB7 0	DB6 0	DB5 0	DB4 0	DB3 0	DB2 1	DB1 1	DB0 0	BLANK	display setting command page; set normal mode (D = 1, E = 0)
9	DB7 1	DB6 0	DB5 0	DB4 0	DB3 0	DB2 1	DB1 0	DB0 0	BLANK	select Mux rate 1 : 65
10	DB7 0	DB6 0	DB5 0	DB4 0	DB3 0	DB2 0	DB1 0	DB0 1	BLANK	H[2:0] independent command; select function and RAM command page H[1:0] = 111
11	DB7 0	DB6 0	DB5 0	DB4 0	DB3 1	DB2 1	DB1 0	DB0 1	BLANK	function and RAM command page; select Hv-gen command page H[1:0] = 101
12	DB7 0	DB6 0	DB5 0	DB4 0	DB3 1	DB2 0	DB1 0	DB0 1	BLANK	Hv-gen command page; select voltage multiplication factor 3 S[1:0] = 01
13	DB7 0	DB6 0	DB5 0	DB4 1	DB3 0	DB2 0	DB1 1	DB0 0	BLANK	Hv-gen command page; select temperature coefficient 2 TC[2:0] = 010
14	DB7 1	DB6 0	DB5 1	DB4 0	DB3 1	DB2 0	DB1 0	DB0 0	BLANK	Hv-gen command page; set V_{LCD} = 12.02 V; V_{OP}[6:0] = 0101000
15	DB7 0	DB6 0	DB5 0	DB4 0	DB3 0	DB2 1	DB1 1	DB0 1	BLANK	Hv-gen command page; select high V_{LCD} programming range (PRS = 1), voltage multiplier on (HVE = 1)
16	START condition								BLANK	repeat start
17	DB7 0	DB6 1	DB5 1	DB4 1	DB3 1	DB2 SA1	DB1 SA0	DB0 0	BLANK	slave address, R/$\overline{W}$ = 0
18	DB7 0	DB6 1	DB5 0	DB4 0	DB3 0	DB2 0	DB1 0	DB0 0	BLANK	control byte, Co = 0, D/$\overline{C}$ = 1

STEP	SERIAL BUS BYTE								DISPLAY(1)	OPERATION
19	DB7 0	DB6 0	DB5 0	DB4 1	DB3 1	DB2 1	DB1 1	DB0 1	 MGS405	data write; Y, X are initialized to logic 0 by default, so they are not set here
20	DB7 0	DB6 0	DB5 0	DB4 0	DB3 0	DB2 1	DB1 0	DB0 1	 MGS406	data write
21	DB7 0	DB6 0	DB5 0	DB4 0	DB3 0	DB2 1	DB1 1	DB0 1	 MGS407	data write
22	DB7 0	DB6 0	DB5 0	DB4 0	DB3 0	DB2 0	DB1 0	DB0 0	 MGS408	data write
23	DB7 0	DB6 0	DB5 0	DB4 1	DB3 1	DB2 1	DB1 1	DB0 1	 MGS409	data write
24	DB7 0	DB6 0	DB5 0	DB4 0	DB3 0	DB2 1	DB1 0	DB0 0	 MGS410	data write
25	DB7 0	DB6 0	DB5 0	DB4 1	DB3 1	DB2 1	DB1 1	DB0 1	 MGS411	data write, last data, stop transmission
26	START condition									repeat start
27	DB7 0	DB6 1	DB5 1	DB4 1	DB3 1	DB2 SA1	DB1 SA0	DB0 0	 MGS411	slave address, R/$\overline{W}$ = 0

STEP	SERIAL BUS BYTE								DISPLAY(1)	OPERATION
28	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	 MGS411	control byte, Co = 1, D/$\overline{C}$ = 0
	1	0	0	0	0	0	0	0		
29	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	 MGS411	H[1:0] independent command; select function and RAM command page H[1:0] = 111
	0	0	0	0	0	0	0	1		
30	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	 MGS411	control byte, Co = 1, D/$\overline{C}$ = 0
	1	0	0	0	0	0	0	0		
31	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	 MGS411	function and RAM command page; select display setting command page H[1:0] = 110
	0	0	0	0	1	1	1	0		
32	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	 MGS411	control byte, Co = 1, D/$\overline{C}$ = 0
	1	0	0	0	0	0	0	0		
33	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	 MGS412	display control; set inverse video mode (D = 1, E = 1)
	0	0	0	0	1	1	0	1		
34	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	 MGS412	control byte, Co = 1, D/$\overline{C}$ = 0
	1	0	0	0	0	0	0	0		
35	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	 MGS412	set X address of RAM; set address to '0000000'
	1	0	0	0	0	0	0	0		

STEP	SERIAL BUS BYTE								DISPLAY(1)	OPERATION
36	DB7 0	DB6 1	DB5 0	DB4 0	DB3 0	DB2 0	DB1 0	DB0 0	 MGS412	control byte, Co = 0, D/$\overline{C}$ = 1
37	DB7 0	DB6 0	DB5 0	DB4 0	DB3 0	DB2 0	DB1 0	DB0 0	 MGS414	data write
38	DB7 0	DB6 0	DB5 0	DB4 0	DB3 0	DB2 0	DB1 0	DB0 0	 MGS685	data write
39	DB7 0	DB6 0	DB5 0	DB4 0	DB3 0	DB2 0	DB1 0	DB0 0	 MGS686	data write
40	STOP condition									end of transfer

Note

1. Assumes the display RAM was previously empty.

The pinning of the PCF8535 is optimized for single plane wiring e.g. for chip-on-glass display modules.

Display size: 65 × 133 pixels.

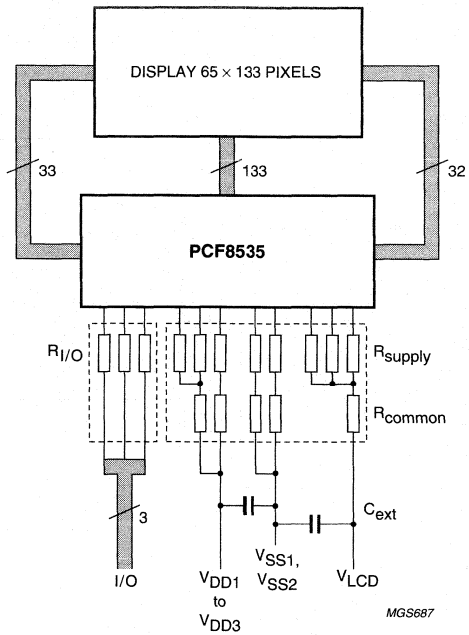


Fig.23 Application diagram (COG).

The required minimum value for the external capacitors in an application with the PCF8535 are:

C_{ext} for V_{LCD}, V_{SS1} and V_{SS2} = 100 nF (min.) (recommended 470 nF to 1 μF); C_{ext} for V_{DD1} to V_{DD3}, V_{SS1} and V_{SS2} = 470 nF (recommended capacitor larger than the capacitor for V_{LCD}, V_{SS1} and V_{SS2}).

Higher capacitor values are recommended for ripple reduction.

For COG applications the recommended ITO track resistance is to be minimized for the I/O and supply connections. Maximum values for supply tracks (R_{supply}) are 120 Ω. Maximum values for the common resistance to the source, (R_{common}) are 120 Ω. Higher track resistance reduces performance and increases current consumption.

Three I/O lines are required for the COG module; SDA, SCL and $\overline{RES}$ (optional). Other signals may be fixed on the module to appropriate levels. $R_{I/O}$ should also be minimized. In particular, if the I²C-bus acknowledge or temperature read back is required, the $R_{I/O}$ for the SDA line must be carefully considered in conjunction with the value of the external pull-up resistor.

14 BONDING PAD LOCATIONS

Table 22 Bonding pad locations

All x and y coordinates are referenced to the centre of the chip (dimensions in μm; see Fig.27).

SYMBOL	PAD	x	y
dummy	1	−1050	−6156
bump/align 1	2	+1050	−6081
R0	3	+1050	−5985
R1	4	+1050	−5915
R2	5	+1050	−5845
R3	6	+1050	−5775
R4	7	+1050	−5705
R5	8	+1050	−5635
R6	9	+1050	−5565
R7	10	+1050	−5495
R8	11	+1050	−5425
R9	12	+1050	−5355
R10	13	+1050	−5285
R11	14	+1050	−5215
R12	15	+1050	−5145
R13	16	+1050	−5075
R14	17	+1050	−5005
R15	18	+1050	−4935
C0	19	+1050	−4725
C1	20	+1050	−4655
C2	21	+1050	−4585
C3	22	+1050	−4515
C4	23	+1050	−4445
C5	24	+1050	−4305
C6	25	+1050	−4235
C7	26	+1050	−4165
C8	27	+1050	−4095
C9	28	+1050	−4025
C10	29	+1050	−3955
C11	30	+1050	−3885
C12	31	+1050	−3815
C13	32	+1050	−3745
C14	33	+1050	−3675
C15	34	+1050	−3605
C16	35	+1050	−3535
C17	36	+1050	−3465
C18	37	+1050	−3395
C19	38	+1050	−3325
C20	39	+1050	−3255
C21	40	+1050	−3185
C22	41	+1050	−3115
C23	42	+1050	−3045
C24	43	+1050	−2975
C25	44	+1050	−2905
C26	45	+1050	−2835
C27	46	+1050	−2765
C28	47	+1050	−2695
C29	48	+1050	−2625
C30	49	+1050	−2555
C31	50	+1050	−2485
C32	51	+1050	−2415
C33	52	+1050	−2345
C34	53	+1050	−2275
C35	54	+1050	−2205
C36	55	+1050	−2135
C37	56	+1050	−1995
C38	57	+1050	−1925
C39	58	+1050	−1855
C40	59	+1050	−1785
C41	60	+1050	−1715
C42	61	+1050	−1645
C43	62	+1050	−1575
C44	63	+1050	−1505
C45	64	+1050	−1435
C46	65	+1050	−1365
C47	66	+1050	−1295
C48	67	+1050	−1225
C49	68	+1050	−1155
C50	69	+1050	−1085
C51	70	+1050	−1015
C52	71	+1050	−945
C53	72	+1050	−875
C54	73	+1050	−805
C55	74	+1050	−735
C56	75	+1050	−665
C57	76	+1050	−595
C58	77	+1050	−525
C59	78	+1050	−455

SYMBOL	PAD	x	y
C60	79	+1050	−385
C61	80	+1050	−315
C62	81	+1050	−245
C63	82	+1050	−175
C64	83	+1050	−105
C65	84	+1050	−35
C66	85	+1050	+35
C67	86	+1050	+105
C68	87	+1050	+175
C69	88	+1050	+315
C70	89	+1050	+385
C71	90	+1050	+455
C72	91	+1050	+525
C73	92	+1050	+595
C74	93	+1050	+665
C75	94	+1050	+735
C76	95	+1050	+805
C77	96	+1050	+875
C78	97	+1050	+945
C79	98	+1050	+1015
C80	99	+1050	+1085
C81	100	+1050	+1155
C82	101	+1050	+1225
C83	102	+1050	+1295
C84	103	+1050	+1365
C85	104	+1050	+1435
C86	105	+1050	+1505
C87	106	+1050	+1575
C88	107	+1050	+1645
C89	108	+1050	+1715
C90	109	+1050	+1785
C91	110	+1050	+1855
C92	111	+1050	+1925
C93	112	+1050	+1995
C94	113	+1050	+2065
C95	114	+1050	+2135
C96	115	+1050	+2205
C97	116	+1050	+2275
C98	117	+1050	+2345
C99	118	+1050	+2415
C100	119	+1050	+2485

SYMBOL	PAD	x	y
C101	120	+1050	+2625
C102	121	+1050	+2695
C103	122	+1050	+2765
C104	123	+1050	+2835
C105	124	+1050	+2905
C106	125	+1050	+2975
C107	126	+1050	+3045
C108	127	+1050	+3115
C109	128	+1050	+3185
C110	129	+1050	+3255
C111	130	+1050	+3325
C112	131	+1050	+3395
C113	132	+1050	+3465
C114	133	+1050	+3535
C115	134	+1050	+3605
C116	135	+1050	+3675
C117	136	+1050	+3745
C118	137	+1050	+3815
C119	138	+1050	+3885
C120	139	+1050	+3955
C121	140	+1050	+4025
C122	141	+1050	+4095
C123	142	+1050	+4165
C124	143	+1050	+4235
C125	144	+1050	+4305
C126	145	+1050	+4375
C127	146	+1050	+4445
C128	147	+1050	+4515
C129	148	+1050	+4585
C130	149	+1050	+4655
C131	150	+1050	+4725
C132	151	+1050	+4795
R47	152	+1050	+5005
R46	153	+1050	+5075
R45	154	+1050	+5145
R44	155	+1050	+5215
R43	156	+1050	+5285
R42	157	+1050	+5355
R41	158	+1050	+5425
R40	159	+1050	+5495
R39	160	+1050	+5565

SYMBOL	PAD	x	y
R38	161	+1050	+5635
R37	162	+1050	+5705
R36	163	+1050	+5775
R35	164	+1050	+5845
R34	165	+1050	+5915
R33	166	+1050	+5985
bump/align 2	167	+1050	+6081
dummy	168	−1050	+6094
R48	169	−1050	+5954
R49	170	−1050	+5884
R50	171	−1050	+5814
R51	172	−1050	+5744
R52	173	−1050	+5674
R53	174	−1050	+5604
R54	175	−1050	+5534
R55	176	−1050	+5464
R56	177	−1050	+5394
R57	178	−1050	+5324
R58	179	−1050	+5254
R59	180	−1050	+5184
R60	181	−1050	+5114
R61	182	−1050	+5044
R62	183	−1050	+4974
R63	184	−1050	+4904
R64	185	−1050	+4834
bump/align 3	186	−1050	+4414
dummy	187	−1050	+4274
dummy	188	−1050	+3996
dummy	189	−1050	+3574
OSC	190	−1050	+3154
V_{LCDIN}	191	−1050	+2874
V_{LCDIN}	192	−1050	+2804
V_{LCDIN}	193	−1050	+2734
V_{LCDIN}	194	−1050	+2664
V_{LCDIN}	195	−1050	+2594
V_{LCDIN}	196	−1050	+2524
V_{LCDOUT}	197	−1050	+2384
V_{LCDOUT}	198	−1050	+2314
V_{LCDOUT}	199	−1050	+2244
V_{LCDOUT}	200	−1050	+2174
V_{LCDOUT}	201	−1050	+2104

SYMBOL	PAD	x	y
V_{LCDOUT}	202	−1050	+2034
V_{LCDOUT}	203	−1050	+1964
$V_{LCDSENCE}$	204	−1050	+1894
dummy	205	−1050	+1544
dummy	206	−1050	+1264
$\overline{RES}$	207	−1050	+914
T3	208	−1050	+704
T2	209	−1050	+494
T1	210	−1050	+284
V_{DD2}	211	−1050	+144
V_{DD2}	212	−1050	+74
V_{DD2}	213	−1050	+4
V_{DD2}	214	−1050	−66
V_{DD2}	215	−1050	−136
V_{DD2}	216	−1050	−206
V_{DD2}	217	−1050	−276
V_{DD2}	218	−1050	−346
V_{DD3}	219	−1050	−416
V_{DD3}	220	−1050	−486
V_{DD3}	221	−1050	−556
V_{DD3}	222	−1050	−626
V_{DD1}	223	−1050	−696
V_{DD1}	224	−1050	−766
V_{DD1}	225	−1050	−836
V_{DD1}	226	−1050	−906
V_{DD1}	227	−1050	−976
V_{DD1}	228	−1050	−1046
dummy	229	−1050	−1186
SDA	230	−1050	−1466
SDA	231	−1050	−1536
SDAOUT	232	−1050	−1886
SA1	233	−1050	−2166
SA0	234	−1050	−2376
V_{SS2}	235	−1050	−2586
V_{SS2}	236	−1050	−2656
V_{SS2}	237	−1050	−2726
V_{SS2}	238	−1050	−2796
V_{SS2}	239	−1050	−2866
V_{SS2}	240	−1050	−2936
V_{SS2}	241	−1050	−3006
V_{SS2}	242	−1050	−3076

SYMBOL	PAD	x	y
V_{SS1}	243	−1050	−3146
V_{SS1}	244	−1050	−3216
V_{SS1}	245	−1050	−3286
V_{SS1}	246	−1050	−3356
V_{SS1}	247	−1050	−3426
V_{SS1}	248	−1050	−3496
V_{SS1}	249	−1050	−3566
V_{SS1}	250	−1050	−3636
T5	251	−1050	−3846
T4	252	−1050	−4056
dummy	253	−1050	−4126
SCL	254	−1050	−4406
SCL	255	−1050	−4476
bump/align 4	256	−1050	−4605
R32	257	−1050	−4826
R31	258	−1050	−4896
R30	259	−1050	−4966
R29	260	−1050	−5036
R28	261	−1050	−5106
R27	262	−1050	−5176
R26	263	−1050	−5246
R25	264	−1050	−5316
R24	265	−1050	−5386
R23	266	−1050	−5456
R22	267	−1050	−5526
R21	268	−1050	−5596
R20	269	−1050	−5666
R19	270	−1050	−5736
R18	271	−1050	−5806
R17	272	−1050	−5876
R16	273	−1050	−5946

Table 23 Alignment marks

MARKS	x	y
Alignment mark 1	−1045	−4720
Alignment mark 2	−1045	+4620
Alignment mark 3	+1045	+6196
Alignment mark 4	+1045	−6196
Dummy bump/alignment mark 1	+1050	−6081
Dummy bump/alignment mark 2	+1050	+6081
Dummy bump/alignment mark 3	−1050	+4414
Dummy bump/alignment mark 4	−1050	−4605
Bottom left	−1180	−6330
Top right	+1180	+6330

Table 24 Bonding pads

PAD	SIZE	UNIT
Pad pitch	minimum 70	μm
Pad size; Al	62 × 100	μm
CBB opening	36 × 76	μm
Bump dimensions	50 × 90 × 17.5 (± 5)	μm
Wafer thickness (including bumps)	maximum 381	μm

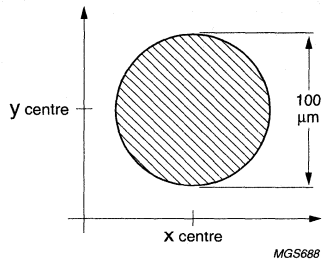


Fig.24 Shape of alignment mark.

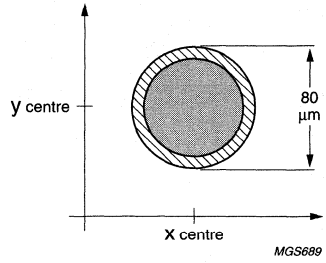


Fig.25 Shape of dummy bump/alignment mark.

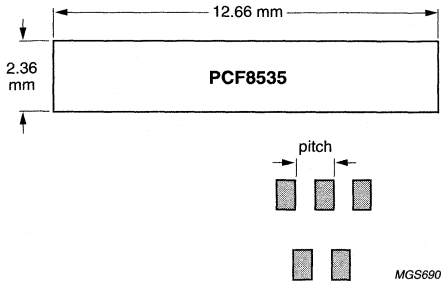
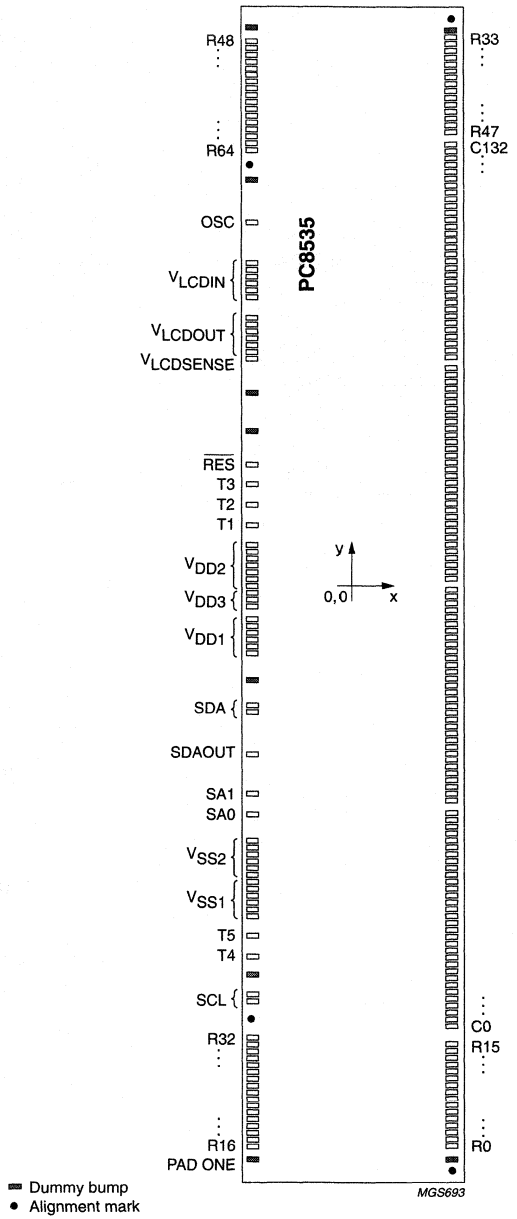


Fig.26 Bonding pads.



The position of the bonding pads is not to scale.

Fig.27 Bonding pad location (viewed from bump side).

15 DEVICE PROTECTION DIAGRAM

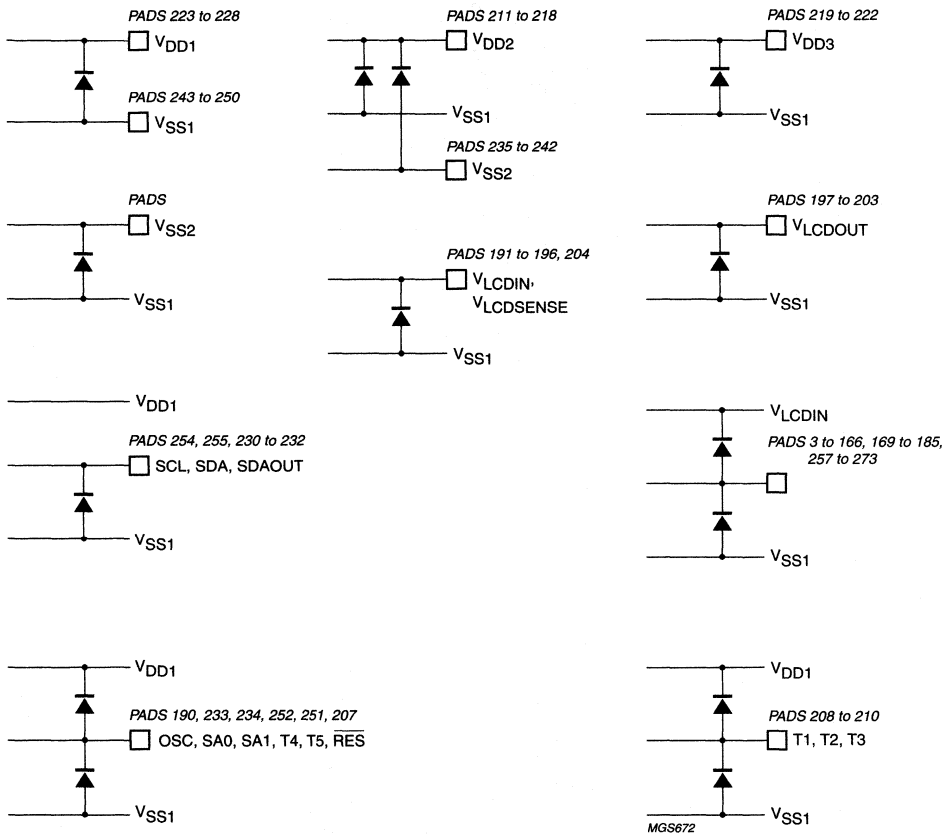
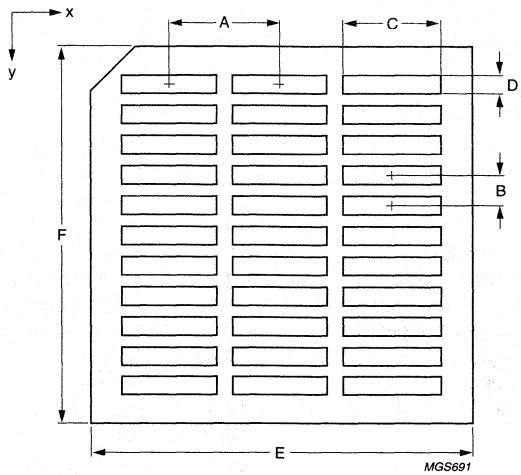


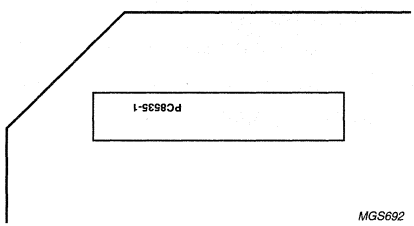
Fig.28 Device diode protection diagram.

16 TRAY INFORMATION



The dimensions are given in Table 25.

Fig.29 Tray details.



The orientation of the IC in a pocket is indicated by the position of the IC type name on the die surface with respect to the chamfer on the upper left corner of the tray. Refer to the bonding pad location diagram for the orientating and position of the type name on the die surface.

Fig.30 Tray alignment.

Table 25 Dimensions

DIM.	DESCRIPTION	VALUE
A	pocket pitch in x direction	14.88 mm
B	pocket pitch in y direction	4.06 mm
C	pocket width in x direction	12.76 mm
D	pocket width in y direction	2.46 mm
E	tray width in x direction	50.8 mm
F	tray width in y direction	50.8 mm
x	number of pockets in x direction	3
y	number of pockets in y direction	11

CONTENTS

65 × 102 pixels matrix LCD driver PCF8548

1 FEATURES

- Single-chip LCD controller/driver
- 65 row and 102 column outputs
- Display data RAM 65 × 102 bits
- On-chip:
  - Configurable 5 (4, 3 and 2) × voltage multiplier generating V_{LCD} (external V_{LCD} also possible)
  - Generation of intermediate LCD bias voltages
  - Oscillator requires no external components (external clock also possible).
- 400 kbits/s fast I²C-bus interface
- CMOS compatible inputs
- Mux rate: 1 : 65
- Logic supply voltage range V_{DD1} to V_{SS}:
  - 1.9 to 5.5 V.
- High voltage generator supply voltage range V_{DD2} to V_{SS} and V_{DD3} to V_{SS}:
  - 2.4 to 4.5 V with LCD voltage internally generated (voltage generator enabled).
- Display supply voltage range V_{LCD} to V_{SS}:
  - 4.5 to 9.0 V
- Low power consumption, suitable for battery operated systems
- Temperature compensation of V_{LCD}
- Slim chip layout, suitable for Chip-On-Glass (COG) applications
- Programmable bottom row pads mirroring and top row pads mirroring, for compatibility with both Tape Carrier Package (TCP) and COG applications.

2 APPLICATIONS

- Telecom equipment
- Portable instruments
- Point of sale terminals.

3 GENERAL DESCRIPTION

The PCF8548 is a low power CMOS LCD controller driver, designed to drive a graphic display of 65 rows and 102 columns. All necessary functions for the display are provided in a single chip, including on-chip generation of LCD supply and bias voltages, resulting in a minimum of external components and low power consumption.
The PCF8548 interfaces to most microcontrollers via an I²C-bus interface.

3.1 Packages

The PCF8548 is available as chip with bumps in tray; tape carrier package is available on request.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8548U/2	Tray	chip with bumps in tray	–
PCF8548U/9	Bumped wafer	quarter wafer	–

5 BLOCK DIAGRAM

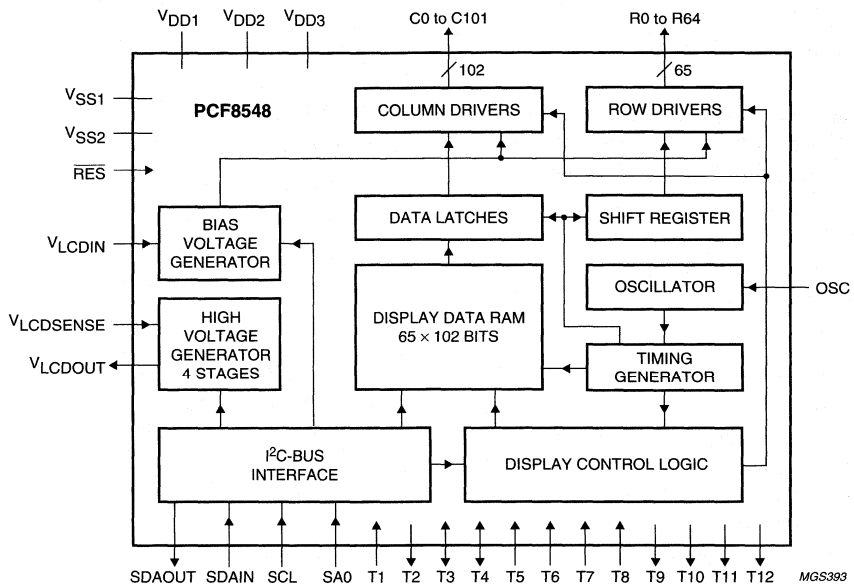


Fig.1 Block diagram.

6 PINNING

SYMBOL	PAD	DESCRIPTION
$\overline{RES}$	1	external reset input (active LOW)
SDAOUT	2	I²C-bus data output
SDAIN	3 and 4	I²C-bus data input
SCL	5 and 6	I²C-bus clock input
T2	7	test 2 output
SA0	8	least significant bit of slave address
T7 to T5	9 to 11	test inputs
T4 and T3	12 and 13	test input/output
T1	14	test input
V_{SS1}	15 to 20	negative power supply 1
V_{SS2}	21 to 26	negative power supply 2
V_{LCDOUT}	28 to 33	voltage multiplier output
$V_{LCDSENSE}$	34	voltage multiplier regulation input (V_{LCD})

SYMBOL	PAD	DESCRIPTION
V_{LCDIN}	35 to 40	LCD supply voltage
R32 to R19	41 to 54	LCD row driver outputs
R0 to R18	57 to 75	LCD row driver outputs
C0 to C101	76 to 177	LCD column driver outputs
R50 to R33	178 to 195	LCD row driver outputs
R51 to R64	198 to 211	LCD row driver outputs
T12 to T9	212 to 215	test outputs
OSC	216	oscillator
T8	217	test input
V_{DD1}	218 to 223	supply voltage 1
V_{DD3}	224 to 226	supply voltage 3
V_{DD2}	227 to 233	supply voltage 2
	27, 55, 56, 196 and 197	dummy pads

7 PIN FUNCTIONS

7.1 R0 to R64: row driver outputs

These pads output the row signals.

7.2 C0 to C101: column driver outputs

These pads output the column signals.

7.3 V_{SS1} and V_{SS2}: negative power supply rails

V_{SS2} is related to V_{DD2} and V_{DD3} and V_{SS1} is related to V_{DD1}.

7.4 V_{DD1} to V_{DD3}: positive power supply rails

V_{DD2} and V_{DD3} are the supply voltages for the internal voltage generator. Both have to be at the same voltage and must be connected together outside of the chip. If the internal voltage generator is not used, they should both be connected to power or to the V_{DD1} pad.

V_{DD1} is used as the power supply for the rest of the chip. This voltage can be a different voltage than V_{DD2} and V_{DD3}.

7.5 V_{LCDIN}: LCD power supply

Internally generated positive power supply for the liquid crystal display. An external LCD supply voltage can be supplied using the V_{LCDIN} pad. In this case, V_{LCDOUT} has to be connected to ground, and the internal voltage generator has to be programmed to zero. If the PCF8548 is in power-down mode, the external LCD supply voltage must be switched off.

7.6 V_{LCDOUT}: LCD power supply

Positive power supply for the liquid crystal display. If the internal voltage generator is used, the two supply rails V_{LCDIN} and V_{LCDOUT} must be connected together and an external capacitor must be connected (see Fig.19).

7.7 $V_{LCDSENSE}$: voltage multiplier regulation input (V_{LCD})

$V_{LCDSENSE}$ is the input voltage for the internal voltage multiplier regulation.

If the internal voltage generator is used then $V_{LCDSENSE}$ must be connected to V_{LCDOUT}. If an external supply voltage is used then $V_{LCDSENSE}$ must be connected to ground.

7.8 T1 to T12: test pads

T1 and T3 to T7 must be connected to V_{SS1}. T8 must be connected to V_{DD1}. T2 and T9 to T12 must be left open-circuit; not accessible to user.

7.9 SDAIN and SDAOUT: I²C-bus data lines

Serial data and acknowledge lines for the I²C-bus. By connecting SDAIN to SDAOUT, the SDA line becomes fully I²C-bus compatible. Having the acknowledge output (SDAOUT) separated from the serial data line is advantageous in Chip-On-Glass (COG) applications. In COG applications where the track resistance from the SDAOUT pad to the system SDA line can be significant, a potential divider is generated by the bus pull-up resistor and the Indium Tin Oxide (ITO) track resistance. It is possible that during the acknowledge cycle the PCF8548 will not be able to create a valid logic 0 level. By splitting the SDA input from the output the device could be used in a mode that ignores the acknowledge bit. In COG applications where the acknowledge cycle is required, it is necessary to minimize the track resistance from the SDACK pad to the system SDA line to guarantee a valid LOW level.

7.10 SCL: I²C-bus clock signal

I²C-bus serial clock signal input.

7.11 SA0: slave address

Two different slave addresses can be selected using the SA0 pad. This allows two PCF8548 LCD drivers to be connected to the same I²C-bus.

7.12 OSC: oscillator

When the on-chip oscillator is used this input must be connected to V_{DD1}. An external clock signal, if used, is connected to this input.

7.13 $\overline{RES}$: reset

This signal is used to reset the device. The signal is active LOW.

8 BLOCK DIAGRAM FUNCTIONS

8.1 Oscillator

The on-chip oscillator provides the clock signal for the display system. No external components are required and the OSC input must be connected to V_{DD1}. An external clock signal (if used), is connected to this input.

8.2 I²C-bus interface

The I²C-bus interface receives and executes the commands sent via the I²C-bus. It also receives RAM data and sends it to the RAM.

8.3 Display control logic

The display control logic generates the control signals to read from the RAM via the 102 bits parallel port. It also generates the control signals for the row and column drivers.

8.4 Display Data RAM (DDRAM)

The PCF8548 contains a 65 × 102 bit static RAM which stores the display data. The RAM is divided into 8 banks of 102 bytes and 1 bank of 102 bits [(8 × 8 + 1) × 102 bits]. During RAM access, data is transferred to the RAM via the I²C-bus interface. There is a direct correspondence between the X address and column output number.

8.5 Timing generator

The timing generator produces the various signals required to drive the internal circuitry. Internal chip operation is not disturbed by operations on the I²C-bus.

8.6 LCD row and column drivers

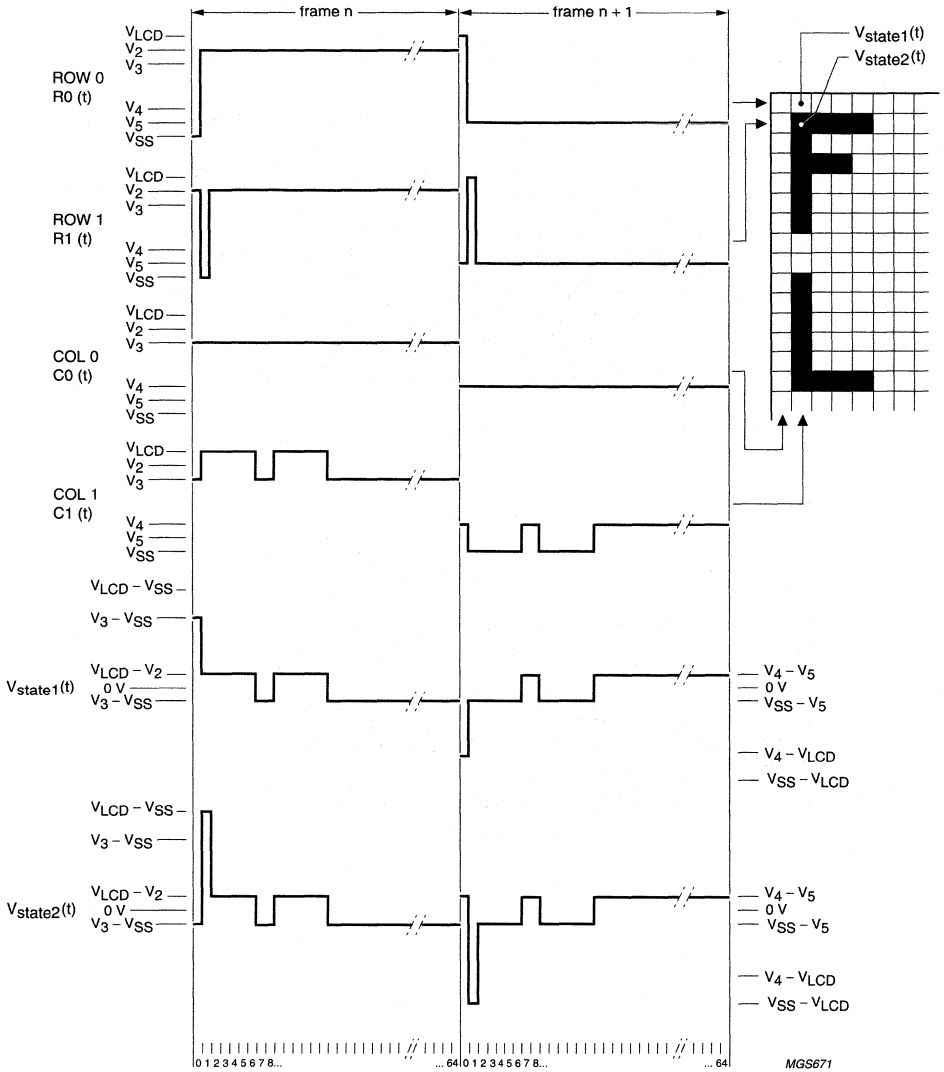
The PCF8548 contains 65 row and 102 column drivers, which connect the appropriate LCD bias voltages to the display in accordance with the data to be displayed. Figure 2 shows typical waveforms. Unused outputs should be left unconnected.

9 INITIALIZATION

Immediately following Power-on, all internal registers and the RAM content are undefined. A reset pulse must first be applied.

Reset is accomplished by applying an external $\overline{RES}$ pulse (active LOW). When reset occurs within the specified time all internal registers are initialized, however the RAM is still undefined. The state after reset is described in Section 12.1.

The $\overline{RES}$ input must be $\leq 0.3\ V_{DD}$ when V_{DD} reaches $V_{DD(min)}$ (or higher) within a maximum time t_{VHRL} after V_{DD} goes HIGH (see Fig.17).



$V_{state1}(t) = C1(t) - R0(t)$.
$V_{state2}(t) = C1(t) - R1(t)$.

Fig.2 Typical LCD driver waveforms.

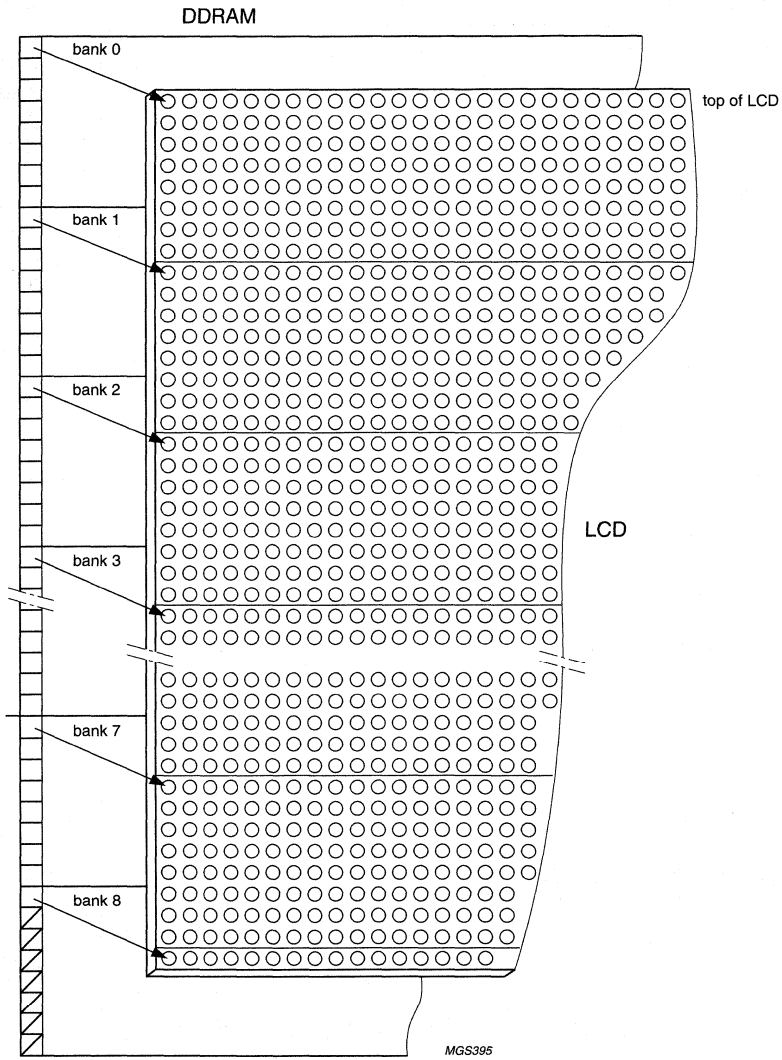


Fig.3 DDRAM to display mapping.

10 ADDRESSING

The Display Data RAM (DDRAM) of the PCF8548 is accessed as indicated in Figs 3, 6, 7, 8 and 9. The DDRAM has a matrix of 65 × 102 bits. The RAM cells are addressed by the X and Y address pointers. The address ranges are X0 to X101 (1100101b) and Y0 to Y8 (1000b). Addresses outside of these ranges are not allowed. In vertical addressing mode (V = 1) the Y address increments after each byte (see Fig.5). After the last Y address (Y = 8), Y wraps around to 0 and X increments to address the next column. In the horizontal addressing mode (V = 0) the X address increments after each byte (see Fig.4). After the last X address (X = 101), X wraps around to 0 and Y increments to address the next row. After the very last address (X = 101 and Y = 8) the address pointers wrap around to address X = 0 and Y = 0.

10.1 Display data RAM structure

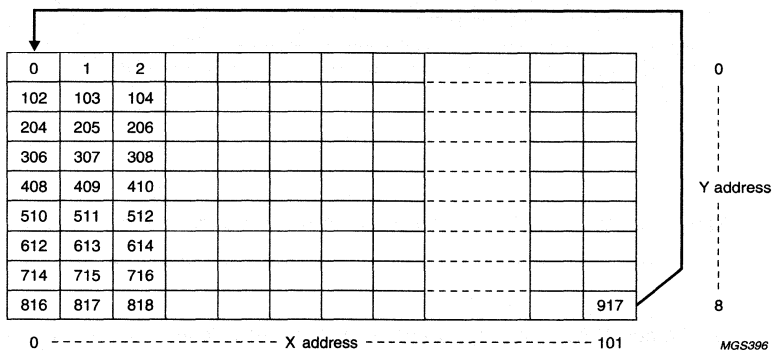


Fig.4 Sequence of writing data bytes into RAM with horizontal addressing (V = 0).

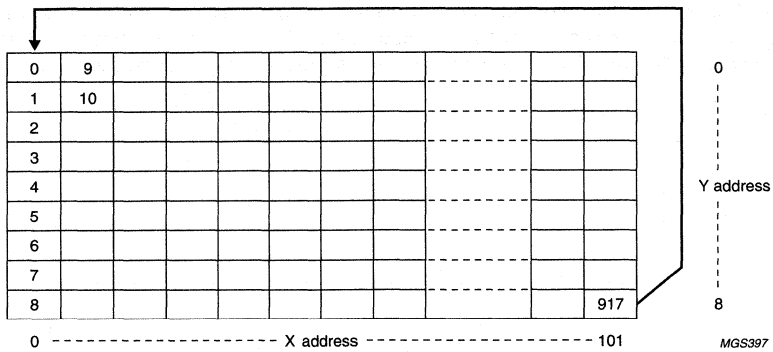


Fig.5 Sequence of writing data bytes into RAM with vertical addressing (V = 1).

The DO bit defines the bit order (MSB on top or MSB on bottom) for writing to the RAM (see Figs 6 and 7).

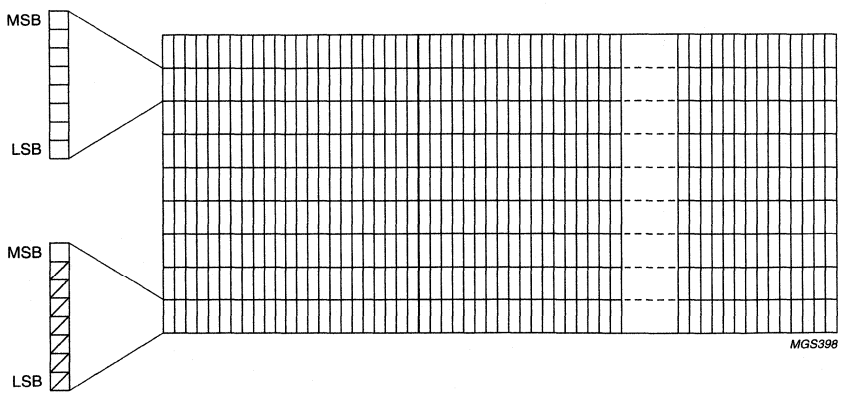


Fig.6 RAM byte organization, if DO = 0.

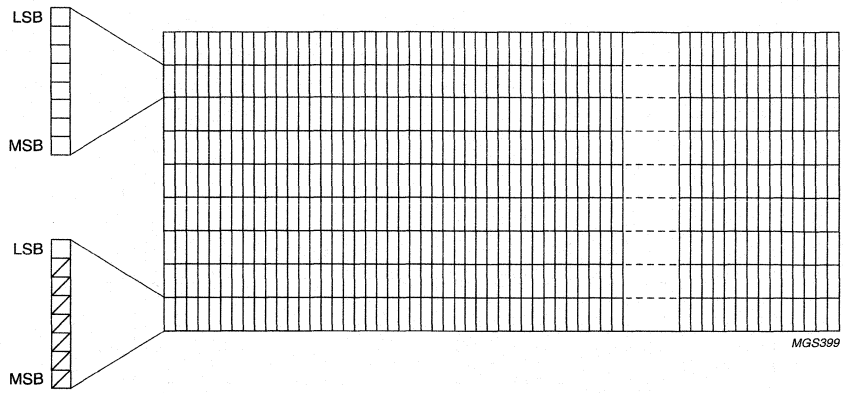


Fig.7 RAM byte organization, if DO = 1.

The MX bit allows a horizontal mirroring; when MX = 1, the X address space is mirrored. The address X = 0 is then located at the right side (column 101) of the display (see Fig.9). When MX = 0 the mirroring is disabled and the address X = 0 is located at the left side (column 0) of the display (see Fig.8).

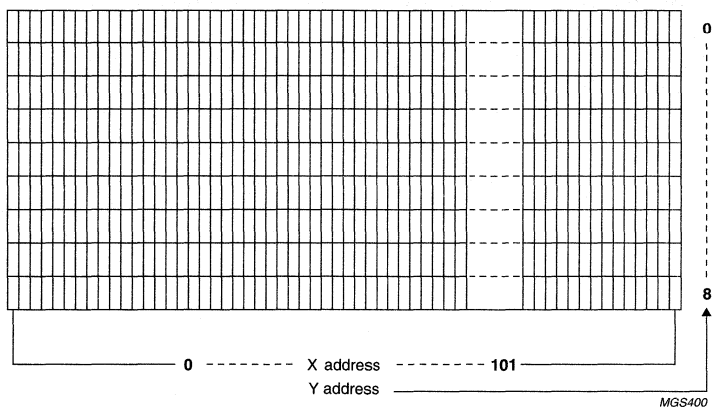


Fig.8 RAM format addressing (MX = 0).

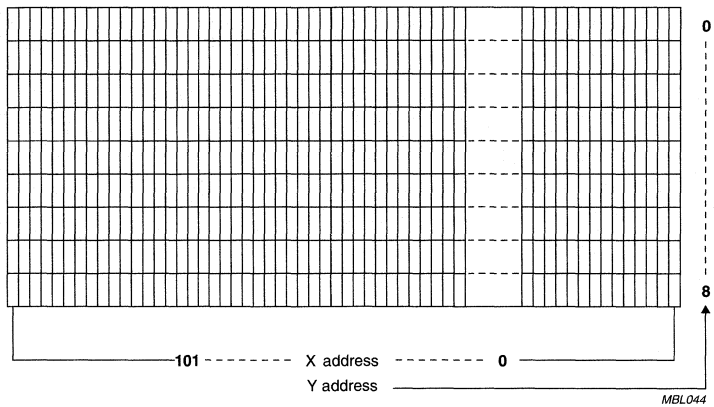


Fig.9 RAM format addressing (MX = 1).

10.2 RAM access

If the D/$\overline{C}$ bit is logic 1 the RAM can be written to. The data is written to the RAM during the acknowledge cycle.

11 I²C-BUS INTERFACE

11.1 Characteristics of the I²C-bus

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a Serial Data line (SDA) and a Serial Clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

11.1.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse because changes in the data line at this time will be interpreted as a control signal. Bit transfer is illustrated in Fig.10.

11.1.2 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P). The START and STOP conditions are illustrated in Fig.11.

11.1.3 System configuration

The system configuration is illustrated in Fig.12.

- Transmitter: the device which sends the data to the bus
- Receiver: the device which receives the data from the bus
- Master: the device which initiates a transfer, generates clock signals and terminates a transfer
- Slave: the device addressed by a master
- Multi-Master: more than one master can attempt to control the bus at the same time without corrupting the message
- Arbitration: procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted
- Synchronization: procedure to synchronize the clock signals of two or more devices.

11.1.4 Acknowledge

Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. A master receiver must also generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end-of-data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition. Acknowledgement on the I²C-bus is illustrated in Fig.13.

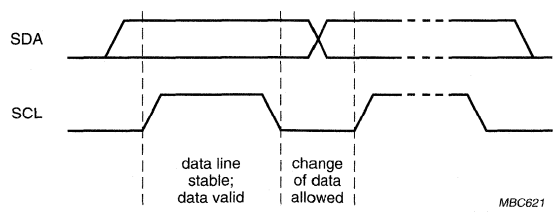


Fig.10 Bit transfer.

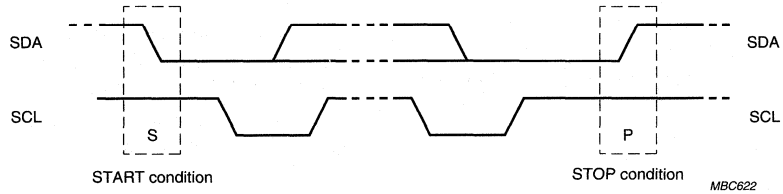


Fig.11 Definition of START and STOP conditions.

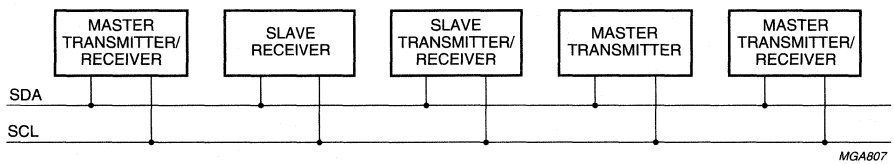


Fig.12 System configuration.

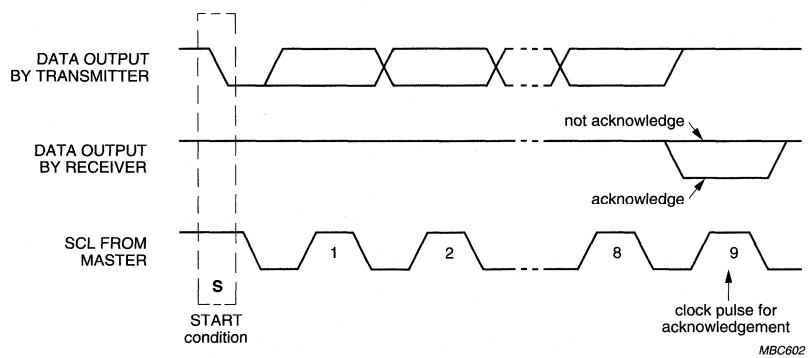


Fig.13 Acknowledgement on the I^2C-bus.

11.2 I²C-bus protocol

The PCF8548 supports command, data write and status read access.

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. Two 7-bit slave addresses (0111100 and 0111101) are reserved for the PCF8548. The least significant bit of the slave address is set by connecting the input SA0 to either logic 0 (V_{SS1}) or logic 1 (V_{DD1}).

The I²C-bus protocol is illustrated in Fig.14.

The sequence is initiated with a START condition (S) from the I²C-bus master which is followed by the slave address. All slaves with the corresponding address acknowledge in parallel, all the others will ignore the I²C-bus transfer. After acknowledgement, one or more command words follow which define the status of the addressed slaves.
A command word consists of a control byte, which defines Co and D/$\overline{C}$, plus a data byte (see Fig.14 and Table 1).

The last control byte is tagged with a cleared most significant bit (i.e. the continuation bit Co). After a control byte with a cleared Co bit, only data bytes will follow. The state of the D/$\overline{C}$ bit defines whether the data byte is interpreted as a command or as RAM data.

The control and data bytes are also acknowledged by all addressed slaves on the bus.

After the last control byte, depending on the D/$\overline{C}$ bit setting, either a series of display data bytes or command data bytes may follow. If the D/$\overline{C}$ bit is set to logic 1, these display bytes are stored in the display RAM at the address specified by the data pointer. The data pointer is automatically updated and the data is directed to the intended PCF8548 device. If the D/$\overline{C}$ bit of the last control byte is set to logic 0, these command bytes will be decoded and the setting of the device will be changed according to the received commands. The acknowledgement after each byte is made only by the addressed slave. At the end of the transmission the I²C-bus master issues a STOP condition (P).

If the R/$\overline{W}$ bit is set to logic 1 the chip will output data immediately after the slave address if the D/$\overline{C}$ bit, which was sent during the last write access, is set to logic 0. If no acknowledge is generated by the master after a byte, the driver stops transferring data to the master.

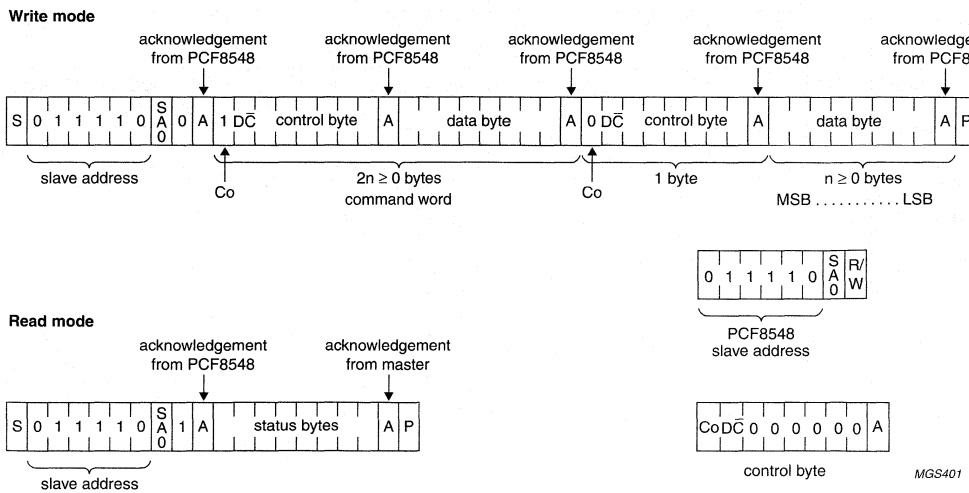


Fig.14 I²C-bus protocol.

12 INSTRUCTIONS

The instruction format is divided into two modes:

1. If D/$\overline{C}$ is set LOW, commands can be sent to the chip.
2. If D/$\overline{C}$ is set HIGH, the DDRAM will be accessed.

Every instruction can be sent in any order to the PCF8548.

Table 1 Instruction set

INSTRUCTION	D/$\overline{C}$	R/$\overline{W}$	COMMAND BYTE								DESCRIPTION
			B7	B6	B5	B4	B3	B2	B1	B0	
H = 0 or 1											
NOP	0	0	0	0	0	0	0	0	0	0	no operation
Reserved	0	0	0	0	0	0	0	0	0	1	do not use
Function set	0	0	0	0	1	MX	MY	PD	V	H	Power-down control; entry mode; extended instruction set control (H)
Read status byte	0	1	PD	TRS	BRS	D	E	MX	MY	DO	read status byte
Write data	1	0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	writes data to RAM
H = 0											
Reserved	0	0	0	0	0	0	0	0	1	X	do not use
Set V_{LCD} range	0	0	0	0	0	0	0	1	0	PRS	V_{LCD} programming range select
Display control	0	0	0	0	0	0	1	D	0	E	sets display configuration
Set HV-gen stages	0	0	0	0	0	1	0	0	S1	S0	# of HV-gen voltage multiplication
Set Y address of RAM	0	0	0	1	0	0	Y_3	Y_2	Y_1	Y_0	sets Y address of RAM: $0 \leq Y \leq 8$
Set X address of RAM	0	0	1	X_6	X_5	X_4	X_3	X_2	X_1	X_0	sets X address of RAM: $0 \leq X \leq 101$
H = 1											
Reserved	0	0	0	0	0	0	0	0	1	X	do not use
Temperature control	0	0	0	0	0	0	0	1	TC_1	TC_0	set temperature coefficient (TCx)
Display configuration	0	0	0	0	0	0	1	DO	TRS	BRS	top/bottom row mode set data order
Bias system	0	0	0	0	0	1	0	BS_2	BS_1	BS_0	set bias system (BSx)
Reserved	0	0	0	1	X	X	X	X	X	X	do not use (reserved for test)
Set V_{OP}	0	0	1	V_{OP6}	V_{OP5}	V_{OP4}	V_{OP3}	V_{OP2}	V_{OP1}	V_{OP0}	write V_{OP} to register

Table 2 Explanations of symbols in Table 1

BIT		0	1	RESET STATE
PD		chip is active	chip is in Power-down mode	1
V		horizontal addressing	vertical addressing	0
H		use basic instruction set	use extended instruction set	0
MX		normal X addressing	X address is mirrored	0
MY		display is not vertically mirrored	display is vertically mirrored	0
TRS		top rows are not mirrored	top rows are mirrored	0
BRS		bottom rows are not mirrored	bottom rows are mirrored	0
DO		MSB is on top	LSB is on top	0
PRS		V_{LCD} programming range LOW	V_{LCD} programming range HIGH	0
D and E	00	display blank		D = 0 E = 0
	10	normal mode		
	01	all display segments on		
	11	inverse video mode		
TC[1:0]	00	V_{LCD} temperature coefficient 0		TC[1:0] = 00
	01	V_{LCD} temperature coefficient 1		
	10	V_{LCD} temperature coefficient 2		
	11	V_{LCD} temperature coefficient 3		
S[1:0]	00	2 × voltage multiplier		S[1:0] = 00
	01	3 × voltage multiplier		
	10	4 × voltage multiplier		
	11	5 × voltage multiplier		
BS[2:0]		bias system		BS[2:0] = 000
V_{op}[6:0]		V_{LCD} programming		V_{op}[6:0] = 0000000

12.1 External reset ($\overline{RES}$)

After power-on a reset pulse must be applied immediately to the chip, as it is in an undefined state. A reset of the chip can be achieved using the external reset pad. After the reset the LCD driver is set to the following states:

- Power-down mode (PD = 1)
- All LCD outputs at V_{SS} (display off)
- Horizontal addressing (V = 0)
- Normal instruction set (H = 0)
- Normal display (MX = MY = TRS = BRS = 0)
- Display blank (E = D = 0)
- Address counter X[6:0] = 0 and Y[3:0] = 0
- Temperature coefficient (TC[1:0] = 0)
- Bias system (BS[2:0] = 0)
- V_{LCD} is equal to 0, the HV generator is switched off (V_{op}[6:0] = 0 and PRS = 0)
- After power-on (RAM data is undefined), the reset signal does not change the content of the RAM.

12.2 Function set

12.2.1 POWER-DOWN (PD)

- All LCD outputs at V_{SS} (display off)
- Bias generator and V_{LCD} generator off
- Oscillator off (external clock possible)
- V_{LCD} can be disconnected
- RAM contents not cleared (RAM data can be written)
- V_{LCD} output is discharged to V_{SS}.

12.2.2 V

When V = 0, the horizontal addressing is selected. The data is written to the RAM as shown in Fig.4. When V = 1, the vertical addressing is selected. The data is written to the RAM as shown in Fig.5.

12.2.3 H

When H = 0 the commands 'display control', 'set HV-gen stages', 'set Y address' and 'set X address' can be performed. When H = 1 the other commands can be executed. The commands 'write data' and 'function set' can be executed in both cases.

12.2.4 MX

When MX = 0, the display RAM is written from left to right (X = 0 is on the left side of the display, X = 100 is on the right side of the display). When MX = 1 the display RAM is written from right to left (X = 0 is on the right side of the display, X = 100 is on the left side of the display).

Thus, if a horizontally mirroring of the display is desired the RAM must first be rewritten.

12.2.5 MY

When MY = 1, the display is mirrored vertically.

A change of this bit has an immediate effect on the display.

12.3 Display control

12.3.1 D AND E

The bits D and E select the display mode (see Table 2).

12.4 Display configuration

12.4.1 TRS

Bit TRS enables the top row pad blocks to be mirrored. This is used to enable flexibility in the wiring of the row lines from the PCF8548 to the LCD cell (e.g. COG or TCP wiring). When TRS = 0 rows 19 to 32 and rows 51 to 64 are organized as illustrated in Fig.22. When TRS = 1 rows 19 to 32 and rows 51 to 64 are mirrored and organized as illustrated in Fig.23.

12.4.2 BRS

Bit BRS enables the bottom row pad blocks to be mirrored. This is used to enable flexibility in the wiring of the row lines from the PCF8548 to the LCD cell (e.g. COG or TCP wiring). When BRS = 0 rows 0 to 18 and rows 33 to 50 are organized as illustrated in Fig.22. When BRS = 1 rows 0 to 18 and rows 33 to 50 are mirrored and organized as illustrated in Fig.23.

12.5 Set Y address of RAM

Y[3 : 0] defines the Y address vector address of the RAM.

Table 3 X and Y address ranges

Y_3	Y_2	Y_1	Y_0	CONTENT	ALLOWED X RANGE
0	0	0	0	bank 0 (display RAM)	0 to 101
0	0	0	1	bank 1 (display RAM)	0 to 101
0	0	1	0	bank 2 (display RAM)	0 to 101
0	0	1	1	bank 3 (display RAM)	0 to 101
0	1	0	0	bank 4 (display RAM)	0 to 101
0	1	0	1	bank 5 (display RAM)	0 to 101
0	1	1	0	bank 6 (display RAM)	0 to 101
0	1	1	1	bank 7 (display RAM)	0 to 101
1	0	0	0	bank 8 (display RAM); note 1	0 to 101

Note

1. In bank 8 only the MSB is accessed.

12.6 Set X address of RAM

The X address points to the columns. The range of X is 0 to 101 (65H).

12.7 Set HV generator stages

12.7.1 S[1:0]

The PCF8548 incorporates a software configurable voltage multiplier. After reset the voltage multiplier is set to $2 \times V_{DD2}$. Other voltage multiplier factors are set via the command 'set HV-gen stages' (see Tables 1 and 2).

12.8 Temperature control

Due to the temperature dependency of the liquid crystals viscosity, the LCD controlling voltage V_{LCD} must be increased with lower temperature to maintain optimum contrast.

There are 4 different temperature coefficients available in the PCF8548 (see Fig.15). The coefficients are selected by the two bits TC[1:0]. Table 6 shows the typical values of the different temperature coefficients. The coefficients are proportional to the programmed V_{LCD}.

12.9 Bias system

The Bias voltage levels are set in the ratio of R – R – nR – R – R giving a $\frac{1}{n+4}$ bias system.

The resulting bias levels are shown in Table 5.

Different multiplex rates require different factors n (see Table 4); this is programmed by BS[2 : 0]. For Mux 1 : 65 the optimum bias value n is given by:

$n = \sqrt{m} - 3 = \sqrt{65} - 3 = 5.06 = 5$ resulting in 1/9 bias.

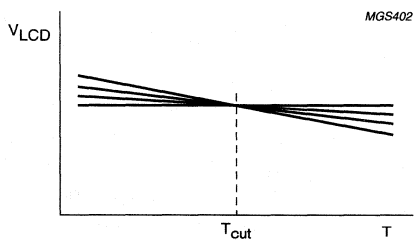


Fig.15 Temperature coefficients.

Table 4 Programming the required bias system

BS[2]	BS[1]	BS[0]	n	RECOMMENDED MUX RATE
0	0	0	7	1 : 100
0	0	1	6	1 : 81
0	1	0	5	1 : 64
0	1	1	4	1 : 49
1	0	0	3	1 : 36
1	0	1	2	1 : 24
1	1	0	1	1 : 16
1	1	1	0	1 : 9

Table 5 LCD bias voltage

SYMBOL	BIAS VOLTAGES	BIAS VOLTAGES FOR 1/9 BIAS
V1	V_{LCD}	V_{LCD}
V2	(n + 3)/(n + 4)	$^8/_9 \times V_{LCD}$
V3	(n + 2)/(n + 4)	$^7/_9 \times V_{LCD}$
V4	2/(n + 4)	$^2/_9 \times V_{LCD}$
V5	1/(n + 4)	$^1/_9 \times V_{LCD}$
V6	V_{SS}	V_{SS}

12.10 Set V_{OP} value

The voltage at reference temperature can be calculated as: [V_{LCD} (T = T_{cut})]

$$V_{LCD_{(Tcut)}} = (a + V_{OP} \times b) \quad (1)$$

The operating voltage V_{LCD} can be set by software. The generated voltage is dependent on the temperature, programmed Temperature Coefficient (TC) and the programmed voltage at reference temperature (T_{cut}).

$$V_{LCD} = (a + V_{OP} \times b) \times [1 + (T - T_{cut}) \times TC] \quad (2)$$

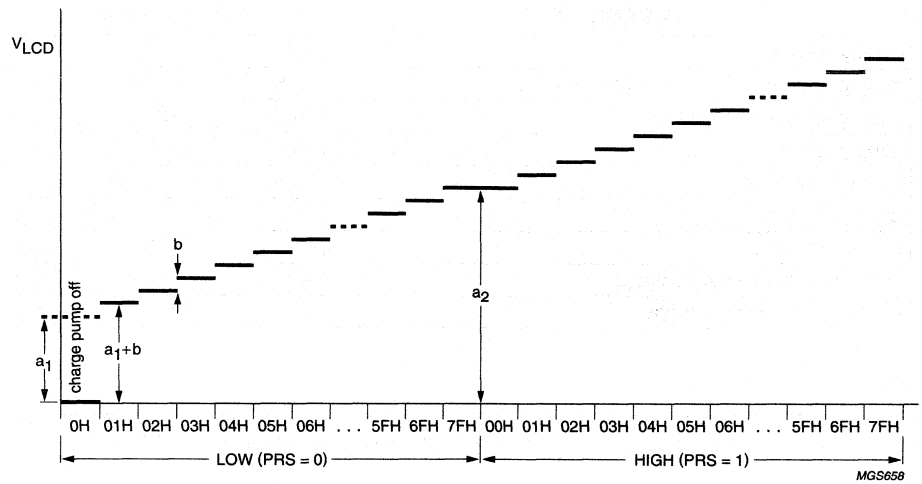
The parameters are explained in Fig.16 and Table 6. The maximum voltage that can be generated is dependent on the V_{DD2} voltage and the display load current. Two overlapping V_{LCD} ranges are selectable via the command 'HV-gen control'. For the LOW (PRS = 0) range a = a_1 and for the HIGH (PRS = 1) range a = a_2 with steps equal to b in both ranges. It should be noted that the charge pump is turned off if V_{OP}[6;0] and bit PRS are all set to zero. For Mux 1 : 65 the optimum operation voltage of the liquid can be calculated as follows:

$$V_{LCD} = \frac{1 + \sqrt{65}}{\sqrt{2 \times \left(1 - \frac{1}{\sqrt{65}}\right)}} \times V_{th} = 6.85 \times V_{th}$$

where V_{th} is the threshold voltage of the liquid crystal material used.

Table 6 Typical values for parameters for the HV-generator programming

SYMBOL	BITS	VALUE	UNIT
a_1		2.94 (PRS = 0)	V
a_2		6.75 (PRS = 1)	V
b		0.03	V
T_{cut}		27	°C



V_{OP}[6:0] (programmed); 00H to 7FH, programme range LOW and HIGH.

Fig.16 V_{OP} programming of PCF8548.

As the programming range for the internally generated V_{LCD} allows values above the maximum allowed V_{LCD} (9.0 V) the customer must ensure while setting the V_{OP} register and selecting the temperature coefficient, under all conditions and including all tolerances V_{LCD} remains below 9.0 V.

13 LIMITING VALUES

Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134); parameters are valid over operating temperature range unless otherwise specified; all voltages referenced to V_{SS} = 0 V. Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD1}	supply voltage	−0.5	+6.5	V
V_{DD2},V_{DD3}	supply voltage for internal voltage generator	−0.5	+4.5	V
V_{LCD}	supply voltage for the LCD	−0.5	+9.0	V
I_{SS}	supply current	−50	+50	mA
$V_{i(n)}$	all input voltages	−0.5	V_{DD} + 0.5	V
I_I	DC input current	−10	+10	mA
I_O	DC output current	−10	+10	mA
P_{pack}	power dissipation per package	−	300	mW
P/out	power dissipation per output	−	30	mW

14 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see "Handling MOS Devices").

15 DC CHARACTERISTICS

V_{DD1} = 1.9 to 5.5 V; V_{DD2} and V_{DD3} = 2.4 to 4.5 V; V_{SS1} and V_{SS2} = 0 V; V_{LCD} = 4.5 to 9.0 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD1}	supply voltage		1.9	−	5.5	V
		T_{amb} = −25 to +85 °C	1.8	−	5.5	V
V_{DD2},V_{DD3}	supply voltage for internal voltage generator	LCD voltage internally generated (voltage generator enabled)	2.4	−	4.5	V
V_{LCDIN}	LCD input supply voltage	LCD voltage externally supplied (voltage generator disabled)	4.5	−	9.0	V
V_{LCDOUT}	LCD output supply voltage	LCD voltage internally generated (voltage generator enabled); note 1	4.5	−	9.0	V
I_{DD1}	supply current	V_{DD1} = 2.8 V; V_{LCD} = 7.6 V; f_{sclk} = 0; T_{amb} = 25 °C; notes 2 and 3	−	20	−	µA
I_{DD2},I_{DD3}	supply current for internal voltage generator	with external V_{LCD}	−	0.5	−	µA
		with internal V_{LCD} generation; V_{DD1} = 2.8 V; V_{LCD} = 7.6 V; f_{sclk} = 0; T_{amb} = 25 °C; no display load; 4 × charge pump; notes 2 and 3	−	180	−	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{DD(tot)}$	total supply current	with internal V_{LCD} generation; V_{DD1} = 2.8 V; V_{LCD} = 7.6 V; f_{sclk} = 0; T_{amb} = 25 °C; no display load; 4 × charge pump; notes 2 and 3	–	200	350	μA
		(Power-down mode) with internal or external V_{LCD} generation; note 4	–	1.5	10	μA
I_{LCDIN}	supply current from external V_{LCD}	V_{DD1} = 2.8 V; V_{LCD} = 7.6 V; f_{sclk} = 0; T_{amb} = 25 °C; no display load; notes 2, 3 and 5	–	30	–	μA
Logic						
V_{IL}	LOW-level input voltage		V_{SS1}	–	$0.3V_{DD1}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD1}$	–	V_{DD1}	V
I_L	leakage current	$V_i = V_{DD1}$ or V_{SS1}	−1	–	+1	μA
Column and row outputs						
R_{row}	row output resistance R0 to R64	V_{DD1} to V_{DD3} = 5.0 V; V_{LCD} = 7.6 V; I_L = 10 μA; outputs tested one at a time	–	12	20	kΩ
R_{col}	column output resistance C0 to C101	V_{LCD} = 7.6 V	–	12	20	kΩ
$V_{bias(col)}$	column bias tolerance C0 to C101		−100	0	+100	mV
$V_{bias(row)}$	row bias tolerance R0 to R64		−100	0	+100	mV
LCD supply voltage generator						
V_{LCD}	V_{LCD} tolerance internally generated	V_{DD1} = 2.8 V; V_{LCD} = 7.6 V; f_{sclk} = 0; T_{amb} = 25 °C; no display load; notes 2, 3 6 and 7	−300	0	+300	mV
TC	temperature coefficient	00	–	-0.0×10^{-3}	–	1/°C
		01	–	-0.76×10^{-3}	–	1/°C
		10	–	-1.05×10^{-3}	–	1/°C
		11	–	-2.10×10^{-3}	–	1/°C

Notes

1. The maximum possible V_{LCD} voltage that can be generated is dependent on voltage, temperature and (display) load.
2. Internal clock.
3. When f_{sclk} = 0 there is no I^2C-bus clock.
4. Power-down mode. During power-down all static currents are switched off.
5. If external V_{LCD}, the display load current is not transmitted to I_{DD}.
6. Tolerance depends on the temperature; (typically zero at T_{amb} = 27 °C), maximum tolerance values are measured at the temperature range limit.
7. For TC0 to TC3.

16 AC CHARACTERISTICS

V_{DD1} = 1.9 to 5.5 V; V_{DD2} and V_{DD3} = 2.4 to 4.5 V; V_{SS1} and V_{SS2} = 0 V; V_{LCD} = 4.5 to 9 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{OSC}	oscillator frequency	V_{DD1} = 2.8 V; T_{amb} = −20 to +70 °C	20	38	70	kHz
$f_{clk(ext)}$	external clock frequency		20	38	100	kHz
f_{frame}	frame frequency	f_{OSC} or $f_{clk(ext)}$ = 38 kHz; note 1	–	73	–	Hz
t_{VHRL}	V_{DD1} to $\overline{RES}$ LOW	see Fig.17 and note 2	0	–	1	µs
$t_{W(RES)}$	$\overline{RES}$ LOW pulse width	see Fig.17 and note 3	100	–	–	ns
I²C-bus timing characteristics; see note 4						
f_{SCLK}	SCL clock frequency		0	–	400	kHz
t_{SCLL}	SCL clock LOW period		1.3	–	–	µs
t_{SCLH}	SCL clock HIGH period		0.6	–	–	µs
$t_{SU;DAT}$	data set-up time		100	–	–	ns
$t_{HD;DAT}$	data hold time		0	–	0.9	µs
t_r	SCL and SDA rise time	note 5	20 + 0.1C_b	–	300	ns
t_f	SCL and SDA fall time	note 5	20 + 0.1C_b	–	300	ns
$t_{f(SDA)(ro)}$	SDA fall time for read out	V_{DD1} = <3.6 V	20 + 0.1C_b	–	1000	ns
C_b	capacitive load represented by each bus line		–	–	400	pF
$t_{SU;STA}$	set-up time for a repeated START condition		0.6	–	–	µs
$t_{HD;STA}$	START condition hold time		0.6	–	–	µs
$t_{SU;STO}$	set-up time for STOP condition		0.6	–	–	µs
t_{SW}	tolerable spike width on bus	note 6	–	–	50	ns
t_{BUF}	bus free time between a STOP and START condition		1.3	–	–	µs

Notes

1. $f_{frame} = \frac{f_{clk(ext)}}{520}$
2. $\overline{RES}$ may be LOW before V_{DD1} goes HIGH.
3. If $t_{W(RES)}$ is longer than 3 ns (typical) a reset may be generated.
4. All timing values are valid within the operating supply voltage and ambient temperature ranges and are referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.
5. The rise and fall times specified here refer to the driver device (i.e. not PCF8548) and are part of the general fast I²C-bus specification. When PCF8548 asserts an acknowledge on SDA, the minimum fall time is 10 ns. C_b = capacitive load per bus line.
6. The device inputs SDA and SCL are filtered and will reject spikes on the bus lines of width $<t_{SW(max)}$.

17 RESET

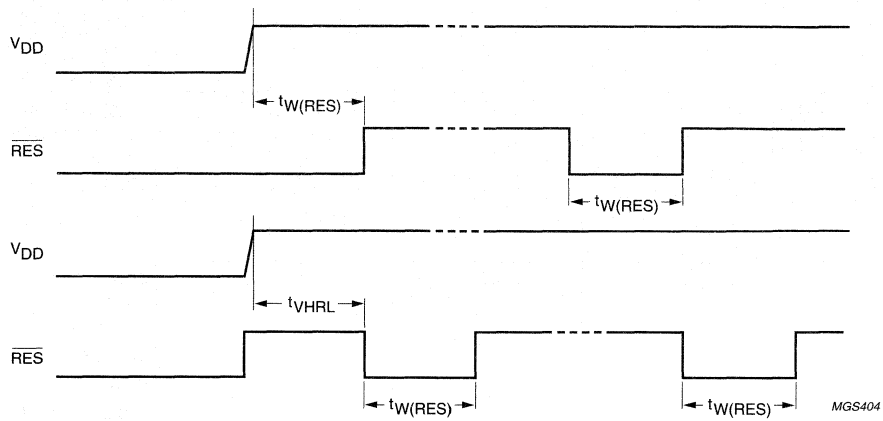
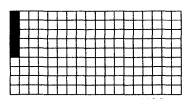
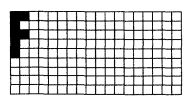
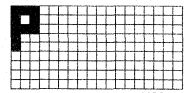
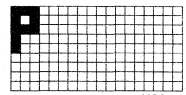
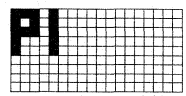
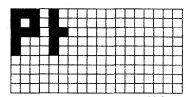
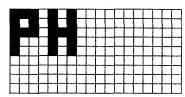


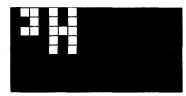
Fig.17 Reset timing.

18 APPLICATION INFORMATION

Table 7 Programming example for PCF8548

STEP	BITS								DISPLAY	OPERATION
	B7	B6	B5	B4	B3	B2	B1	B0		
1	I^2C-bus start									
2	0	1	1	1	1	0	0	0		slave address for write
3	0	0	0	0	0	0	0	0		control byte with cleared Co bit and D/$\overline{C}$ set to logic 0
4	0	0	1	0	0	0	0	1		function set; PD = 0; V = 0; select extended instruction set (H = 1 mode)
5	0	0	0	1	0	0	1	0		set bias system 2; this is the recommended bias system for a multiplex rate 1 : 65
6	1	1	1	0	1	0	1	0		set V_{OP}; V_{OP} is set to a +106 × b [V]; it should be noted that the required voltage is dependent on the liquid
7	0	0	1	0	0	0	0	0		function set; PD = 0; V = 0; select normal instruction set (H = 0 mode)
8	0	0	0	0	1	1	0	0		display control; set normal mode (D = 1; E = 0)
9	I^2C-bus start									restart; to write into the display RAM the D/$\overline{C}$ must be set to logic 1; therefore a control byte is needed
10	0	1	1	1	1	0	0	0		slave address for write
11	0	1	0	0	0	0	0	0		control byte with cleared Co bit and D/$\overline{C}$ set to logic 1
12	1	1	1	1	1	0	0	0	 MGS405	data write; Y and X are initialized to 0 by default, so they are not set here
13	1	0	1	0	0	0	0	0	 MGS406	data write

STEP	BITS								DISPLAY	OPERATION
	B7	B6	B5	B4	B3	B2	B1	B0		
14	1	1	1	0	0	0	0	0	 MGS407	data write
15	0	0	0	0	0	0	0	0	 MGS408	data write
16	1	1	1	1	1	0	0	0	 MGS409	data write
17	0	0	1	0	0	0	0	0	 MGS410	data write
18	1	1	1	1	1	0	0	0	 MGS411	data write
19	I^2C-bus start									restart
20	0	1	1	1	1	0	0	0		slave address for write
21	1	0	0	0	0	0	0	0		control byte with set Co bit and D/$\overline{C}$ set to logic 0
22	0	0	0	0	1	1	0	1	 MGS412	display control; set inverse video mode (D = 1; E = 1)
23	1	0	0	0	0	0	0	0		control byte with set Co bit and D/$\overline{C}$ set to logic 0
24	1	0	0	0	0	0	0	0	 MGS413	set X address of RAM; set address to '0000000'

STEP	BITS								DISPLAY	OPERATION
	B7	B6	B5	B4	B3	B2	B1	B0		
25	1	1	0	0	0	0	0	0		control byte with set Co bit and D/$\overline{C}$ set to logic 1
26	0	0	0	0	0	0	0	0	 MGS414	data write
27	0	0	0	0	0	0	0	0		control byte with cleared Co bit and D/$\overline{C}$ set to logic 0
28	1	0	0	0	0	0	0	0	 MGS415	set X address of RAM; set address to '0000000'
29	I^2C-bus start									restart
30	0	1	1	1	1	0	0	0		slave address for write
31	1	1	0	0	0	0	0	0		control byte with set Co bit and D/$\overline{C}$ set to logic 1
32	1	1	1	1	1	0	0	0	 MGS416	write data
33	1	0	0	0	0	0	0	0		control byte with set Co bit and D/$\overline{C}$ set to logic 0

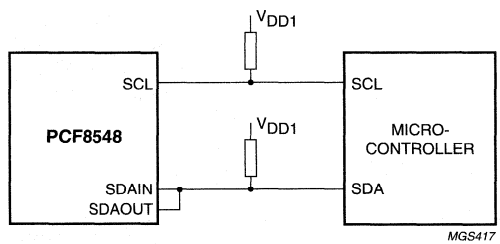
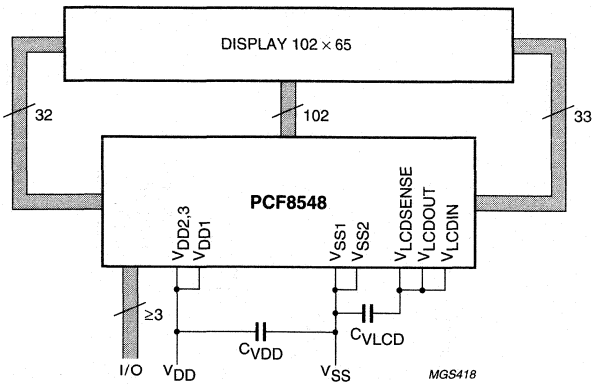
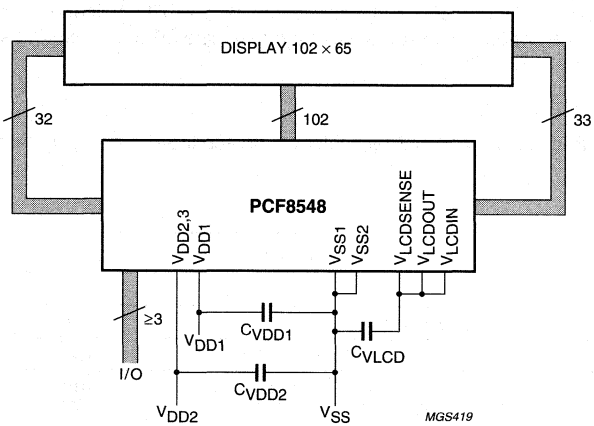


Fig.18 Connecting the I^2C-bus interface.



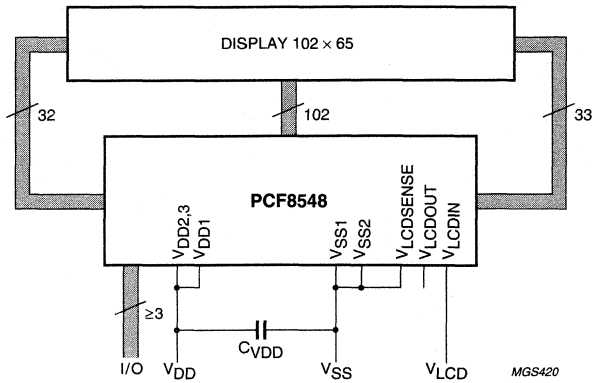
The number of I/Os depends on the application.

Fig.19 Internal charge pump is used and a single supply voltage.



The number of I/Os depends on the application.

Fig.20 Internal charge pump is used and two separate supply voltages.



The number of I/Os depends on the application.

Fig.21 External high voltage generation is used.

The pinning of the PCF8548 is optimized for single plane wiring e.g. for chip-on-glass display modules, or for TCP. Display size: 65 × 102 pixels. The required minimum value for the external capacitors in an application with the PCF8548 are: C_{VDD}, C_{VDD1}, C_{VDD2} and C_{VLCD} = 1.0 µF (min.). Higher capacitor values are recommended for ripple reduction.

To reduce the sensitivity of the reset to ESD/EMC disturbances for a COG application, it is strongly recommended to implement on the glass (ITO) a series input resistance in the reset line (The recommended minimum value is 8 kΩ).

19 CHIP INFORMATION

The PCF8548 is manufactured in n-well CMOS technology. The substrate is at V_{SS} potential.

20 PAD INFORMATION

PAD	VALUE	UNIT
Minimum bump pitch	70	µm
Pad size, alumin	62 × 100	µm
Bumps	50 (±6) × 90 (±6) × 17.5 (±5)	µm
Wafer thickness without bumps	U/2 = 381; U/9 = 525	µm

Table 8 Bonding pad location

All x and y coordinates are referenced to the centre of the chip (dimension in μm; see Fig.22).

SYMBOL	PAD	x	y
$\overline{RES}$	1	+1160	+899.4
SDAOUT	2	+840	+899.4
SDAIN	3	+600	+899.4
SDAIN	4	+520	+899.4
SCL	5	+200	+899.4
SCL	6	+120	+899.4
T2	7	−200	+899.4
SA0	8	−410	+899.4
T7	9	−620	+899.4
T6	10	−830	+899.4
T5	11	−1040	+899.4
T4	12	−1250	+899.4
T3	13	−1460	+899.4
T1	14	−1670	+899.4
V_{SS1}	15	−1750	+899.4
V_{SS1}	16	−1830	+899.4
V_{SS1}	17	−1910	+899.4
V_{SS1}	18	−1990	+899.4
V_{SS1}	19	−2070	+899.4
V_{SS1}	20	−2150	+899.4
V_{SS2}	21	−2310	+899.4
V_{SS2}	22	−2390	+899.4
V_{SS2}	23	−2470	+899.4
V_{SS2}	24	−2550	+899.4
V_{SS2}	25	−2630	+899.4
V_{SS2}	26	−2710	+899.4
dummy pad	27	−2790	+899.4
V_{LCDOUT}	28	−2950	+899.4
V_{LCDOUT}	29	−3030	+899.4
V_{LCDOUT}	30	−3110	+899.4
V_{LCDOUT}	31	−3190	+899.4
V_{LCDOUT}	32	−3270	+899.4
V_{LCDOUT}	33	−3350	+899.4
$V_{LCDSENSE}$	34	−3430	+899.4
V_{LCDIN}	35	−3510	+899.4
V_{LCDIN}	36	−3590	+899.4
V_{LCDIN}	37	−3670	+899.4
V_{LCDIN}	38	−3750	+899.4
V_{LCDIN}	39	−3830	+899.4
V_{LCDIN}	40	−3910	+899.4

SYMBOL	PAD	x	y
R32	41	−4235	+899.4
R31	42	−4305	+899.4
R30	43	−4375	+899.4
R29	44	−4445	+899.4
R28	45	−4515	+899.4
R27	46	−4585	+899.4
R26	47	−4655	+899.4
R25	48	−4725	+899.4
R24	49	−4795	+899.4
R23	50	−4865	+899.4
R22	51	−4935	+899.4
R21	52	−5005	+899.4
R20	53	−5075	+899.4
R19	54	−5145	+899.4
dummy pad	55	−5355	+899.4
dummy pad	56	−5320	−899.4
R0	57	−5040	−899.4
R1	58	−4970	−899.4
R2	59	−4900	−899.4
R3	60	−4830	−899.4
R4	61	−4760	−899.4
R5	62	−4690	−899.4
R6	63	−4620	−899.4
R7	64	−4550	−899.4
R8	65	−4480	−899.4
R9	66	−4410	−899.4
R10	67	−4340	−899.4
R11	68	−4270	−899.4
R12	69	−4200	−899.4
R13	70	−4130	−899.4
R14	71	−4060	−899.4
R15	72	−3990	−899.4
R16	73	−3920	−899.4
R17	74	−3850	−899.4
R18	75	−3780	−899.4
C0	76	−3570	−899.4
C1	77	−3500	−899.4
C2	78	−3430	−899.4
C3	79	−3360	−899.4
C4	80	−3290	−899.4

SYMBOL	PAD	x	y
C5	81	−3220	−899.4
C6	82	−3150	−899.4
C7	83	−3080	−899.4
C8	84	−3010	−899.4
C9	85	−2940	−899.4
C10	86	−2870	−899.4
C11	87	−2800	−899.4
C12	88	−2730	−899.4
C13	89	−2660	−899.4
C14	90	−2590	−899.4
C15	91	−2520	−899.4
C16	92	−2450	−899.4
C17	93	−2380	−899.4
C18	94	−2310	−899.4
C19	95	−2240	−899.4
C20	96	−2170	−899.4
C21	97	−2100	−899.4
C22	98	−2030	−899.4
C23	99	−1960	−899.4
C24	100	−1890	−899.4
C25	101	−1750	−899.4
C26	102	−1680	−899.4
C27	103	−1610	−899.4
C28	104	−1540	−899.4
C29	105	−1470	−899.4
C30	106	−1400	−899.4
C31	107	−1330	−899.4
C32	108	−1260	−899.4
C33	109	−1190	−899.4
C34	110	−1120	−899.4
C35	111	−1050	−899.4
C36	112	−980	−899.4
C37	113	−910	−899.4
C38	114	−840	−899.4
C39	115	−770	−899.4
C40	116	−700	−899.4
C41	117	−630	−899.4
C42	118	−560	−899.4
C43	119	−490	−899.4
C44	120	−420	−899.4
C45	121	−350	−899.4
C46	122	−280	−899.4

SYMBOL	PAD	x	y
C47	123	−210	−899.4
C48	124	−140	−899.4
C49	125	−70	−899.4
C50	126	+0	−899.4
C51	127	+140	−899.4
C52	128	+210	−899.4
C53	129	+280	−899.4
C54	130	+350	−899.4
C55	131	+420	−899.4
C56	132	+490	−899.4
C57	133	+560	−899.4
C58	134	+630	−899.4
C59	135	+700	−899.4
C60	136	+770	−899.4
C61	137	+840	−899.4
C62	138	+910	−899.4
C63	139	+980	−899.4
C64	140	+1050	−899.4
C65	141	+1120	−899.4
C66	142	+1190	−899.4
C67	143	+1260	−899.4
C68	144	+1330	−899.4
C69	145	+1400	−899.4
C70	146	+1470	−899.4
C71	147	+1540	−899.4
C72	148	+1610	−899.4
C73	149	+1680	−899.4
C74	150	+1750	−899.4
C75	151	+1820	−899.4
C76	152	+1890	−899.4
C77	153	+2030	−899.4
C78	154	+2100	−899.4
C79	155	+2170	−899.4
C80	156	+2240	−899.4
C81	157	+2310	−899.4
C82	158	+2380	−899.4
C83	159	+2450	−899.4
C84	160	+2520	−899.4
C85	161	+2590	−899.4
C86	162	+2660	−899.4
C87	163	+2730	−899.4
C88	164	+2800	−899.4

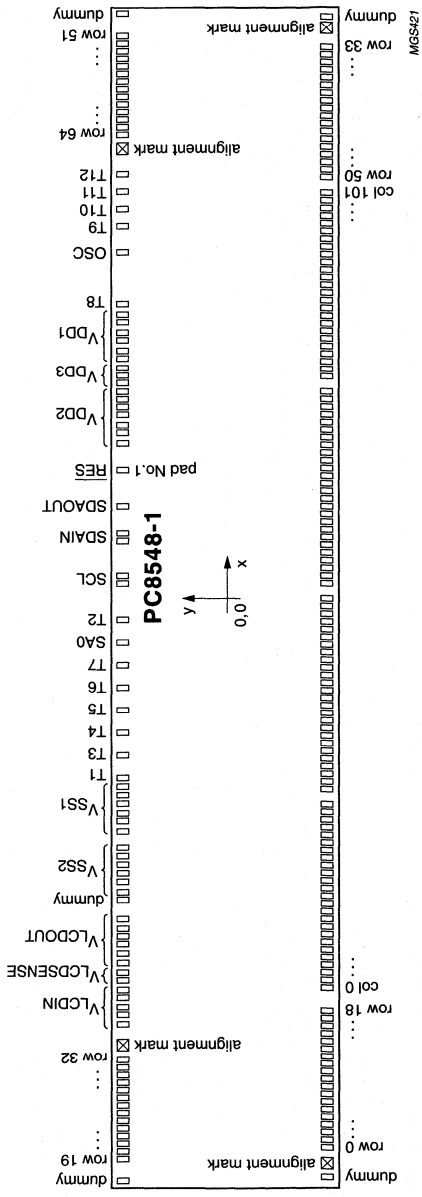
SYMBOL	PAD	x	y
C89	165	+2870	−899.4
C90	166	+2940	−899.4
C91	167	+3010	−899.4
C92	168	+3080	−899.4
C93	169	+3150	−899.4
C94	170	+3220	−899.4
C95	171	+3290	−899.4
C96	172	+3360	−899.4
C97	173	+3430	−899.4
C98	174	+3500	−899.4
C99	175	+3570	−899.4
C100	176	+3640	−899.4
C101	177	+3710	−899.4
R50	178	+3850	−899.4
R49	179	+3920	−899.4
R48	180	+3990	−899.4
R47	181	+4060	−899.4
R46	182	+4130	−899.4
R45	183	+4200	−899.4
R44	184	+4270	−899.4
R43	185	+4340	−899.4
R42	186	+4410	−899.4
R41	187	+4480	−899.4
R40	188	+4550	−899.4
R39	189	+4620	−899.4
R38	190	+4690	−899.4
R37	191	+4760	−899.4
R36	192	+4830	−899.4
R35	193	+4900	−899.4
R34	194	+4970	−899.4
R33	195	+5040	−899.4
dummy pad	196	+5320	−899.4
dummy pad	197	+5355	+899.4
R51	198	+5145	+899.4
R52	199	+5075	+899.4
R53	200	+5005	+899.4
R54	201	+4935	+899.4
R55	202	+4865	+899.4
R56	203	+4795	+899.4
R57	204	+4725	+899.4
R58	205	+4655	+899.4
R59	206	+4585	+899.4

SYMBOL	PAD	x	y
R60	207	+4515	+899.4
R61	208	+4445	+899.4
R62	209	+4375	+899.4
R63	210	+4305	+899.4
R64	211	+4235	+899.4
T12	212	+3880	+899.4
T11	213	+3720	+899.4
T10	214	+3560	+899.4
T9	215	+3400	+899.4
OSC	216	+3160	+899.4
T8	217	+2680	+899.4
V_{DD1}	218	+2600	+899.4
V_{DD1}	219	+2520	+899.4
V_{DD1}	220	+2440	+899.4
V_{DD1}	221	+2360	+899.4
V_{DD1}	222	+2280	+899.4
V_{DD1}	223	+2200	+899.4
V_{DD3}	224	+2120	+899.4
V_{DD3}	225	+2040	+899.4
V_{DD3}	226	+1960	+899.4
V_{DD2}	227	+1880	+899.4
V_{DD2}	228	+1800	+899.4
V_{DD2}	229	+1720	+899.4
V_{DD2}	230	+1640	+899.4
V_{DD2}	231	+1560	+899.4
V_{DD2}	232	+1480	+899.4
V_{DD2}	233	+1400	+899.4

Table 9 Alignment marks

x	y	MARKS
+5214	−899.4	mark 1
−5214	−899.4	mark 2
+4099	+899.4	mark 3
−4099	+899.4	mark 4

The alignment marks are circular with a diameter of 100 µm.



Maximum chip size: 2.12 mm × 10.99 mm.

Fig.22 Bonding pad location.

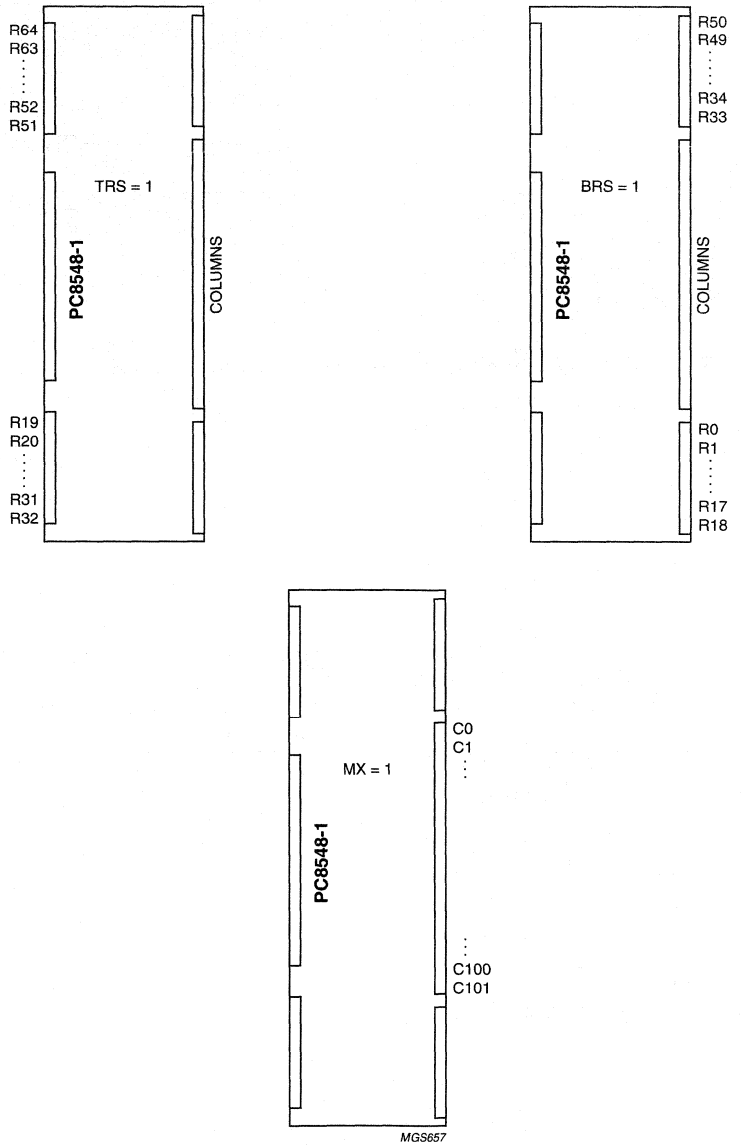


Fig.23 Pad layout for BRS, TRS and MX.

21 DEVICE PROTECTION DIAGRAM

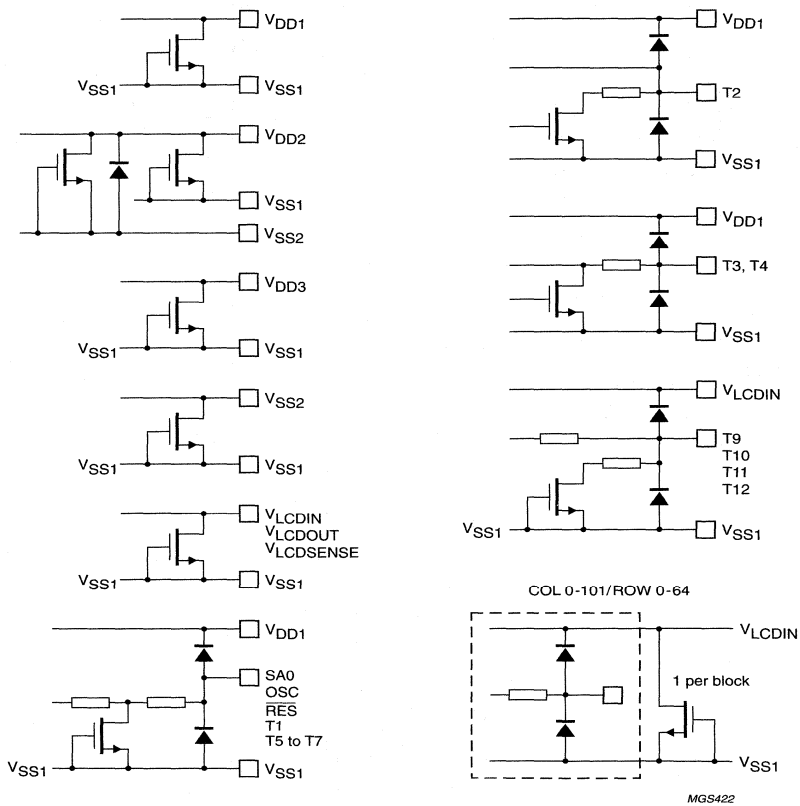
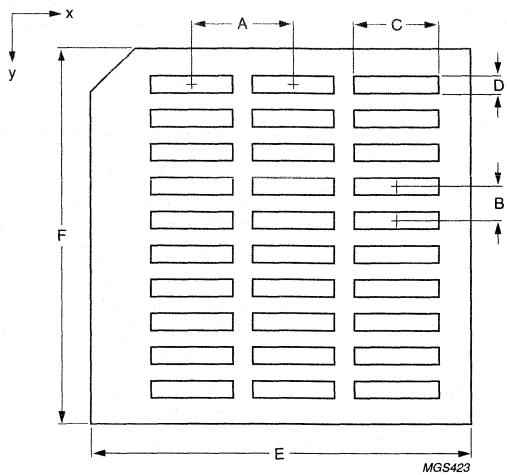


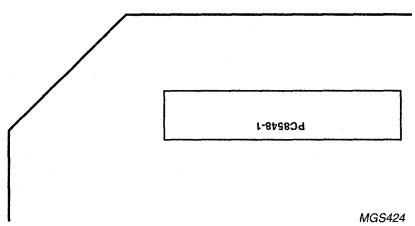
Fig.24 Device protection diagram.

22 TRAY INFORMATION



The dimensions are given in Table 10.

Fig.25 Tray details.



The orientation of the IC in a pocket is indicated by the position of the IC type name on the die surface with respect to the chamfer on the upper left corner of the tray. Refer to the bonding pad location diagram for the orientating and position of the type name on the die surface.

Fig.26 Tray alignment.

Table 10 Dimensions

DIM.	DESCRIPTION	VALUE
A	pocket pitch, x direction	13.77 mm
B	pocket pitch, y direction	4.45 mm
C	pocket width, x direction	11.09 mm
D	pocket width, y direction	2.3 mm
E	tray width, x direction	50.8 mm
F	tray width, x direction	50.8 mm
x	number of pockets in x direction	3
y	number of pockets in y direction	10

65 × 102 pixels matrix LCD driver PCF8549

FEATURES

- Single chip LCD controller/driver
- 65 row and 102 column outputs
- Display data RAM 65 × 102 bits
- On-chip:
  - Generation of LCD supply voltage
  - Generation of intermediate LCD bias voltages
  - Oscillator requires no external components (external clock also possible)
- 400 kHz Fast I²C Interface
- CMOS compatible inputs
- Mux rate: 65
- Logic supply voltage range $V_{DD1} - V_{SS}$: 1.5 to 6 V
- Voltage generator voltage range $V_{DD2/2\_HV} - V_{SS}$: 2.4 to 5 V
- Display supply voltage range $V_{LCD} - V_{SS}$: 7.0 to 16 V
- Low power consumption, suitable for battery operated systems
- Temperature compensation of V_{LCD}
- Interlacing for better display quality
- Slim chip layout, suited for chip-on-glass applications.

APPLICATIONS

- Telecom equipment
- Portable instruments
- Point of sale terminals.

GENERAL DESCRIPTION

The PCF8549 is a low power CMOS LCD controller driver, designed to drive a graphic display of 65 rows and 102 columns. All necessary functions for the display are provided in a single chip, including on-chip generation of LCD supply and bias voltages, resulting in a minimum of external components and low power consumption. The PCF8549 interfaces to most microcontrollers via an I²C interface.

Packages

The PCF8549U/2 is available as bumped die. Sawn wafer as chip sorted in chip tray. For further details see Section "Bonding pads".

Customized TCP upon request.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8549U/2/F1	TRAY	chip with bumps in tray	

BLOCK DIAGRAM

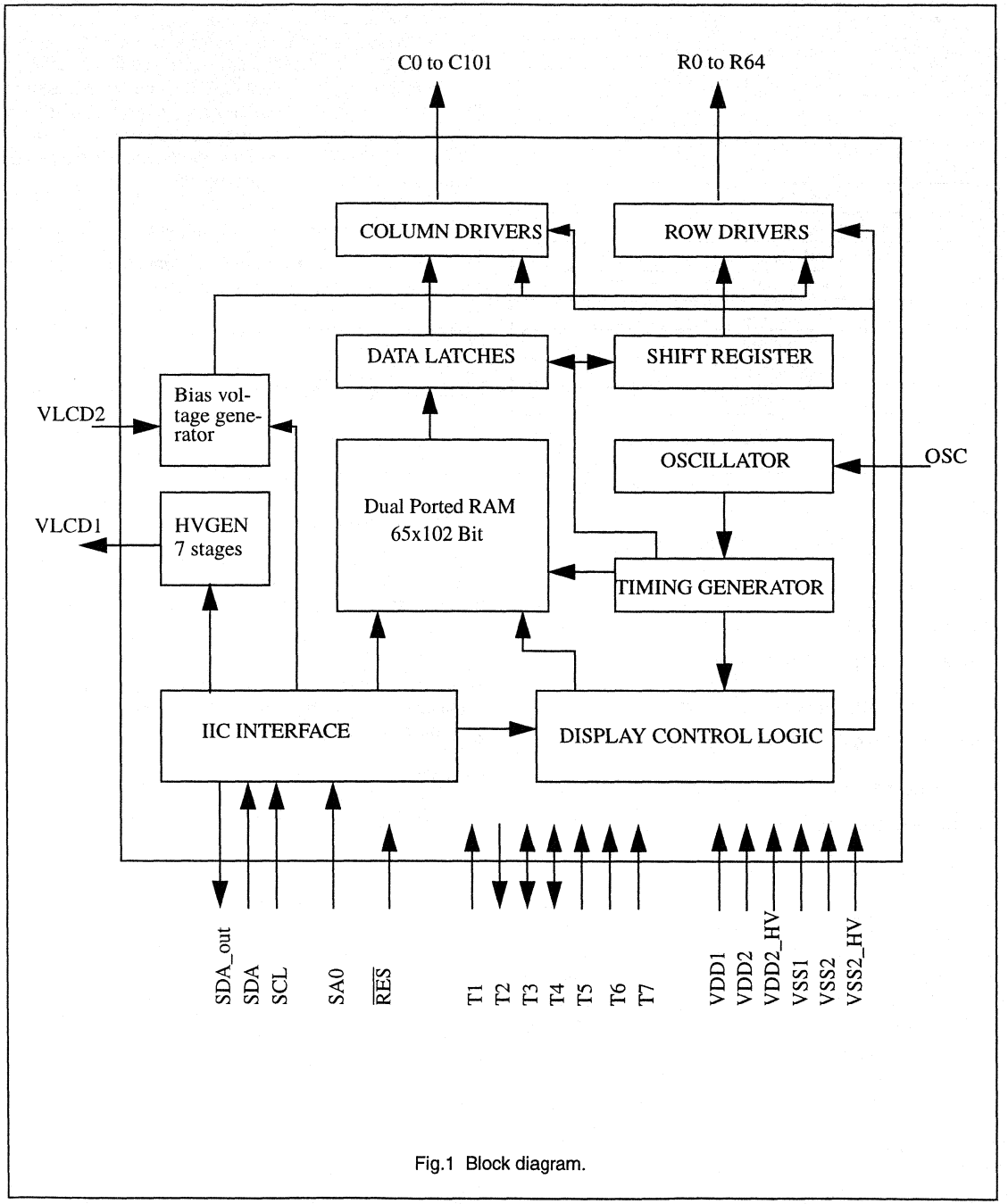


Fig.1 Block diagram.

PINNING

SYMBOL	DESCRIPTION
R0 to R64	LCD row driver outputs
C0 to C101	LCD column driver outputs
$V_{SS1,2,2\_HV}$	negative power supply
$V_{DD1,2,2\_HV}$	supply voltage
$V_{LCD1,2}$	LCD supply voltage
T1	test 1 input
T2	test 2 output
T3	test 3 I/O
T4	test 4 I/O
T5	test 5 input
T6	test 6 input
T7	test 7 input
SDA	I^2C data input
SCL	I^2C clock line
SDA_OUT	I^2C output
SA0	least significant bit of slave address
OSC	oscillator
$\overline{RES}$	external reset input, low active

Pin functions

R0 TO R64: ROW DRIVER OUTPUTS

These pads output the row signals.

C0 TO C101: COLUMN DRIVER OUTPUTS

These pads output the column signals.

$V_{SS1,2,2\_HV}$: NEGATIVE POWER SUPPLY RAILS

Negative power supplies.

$V_{DD1,2,2\_HV}$: POSITIVE POWER SUPPLY RAILS

V_{DD2} and V_{DD2_HV} are the supply voltages for the internal voltage generator. Both have to be on the same voltage and may be connected together outside of the chip. If the internal voltage generator is not used, they should be both connected to ground. V_{DD1} is used as power supply for the rest of the chip. This voltage can be a different voltage than V_{DD2} and V_{DD2_HV}.

$V_{LCD1,2}$: LCD POWER SUPPLY

Positive power supply for the liquid crystal display. If the internal voltage generator is used, the two supply rails V_{LCD1} and V_{LCD2} must be connected together. An external LCD supply voltage can be supplied using the V pad. In this case, V_{LCD1} has to be connected to ground, and the internal voltage generator has to be programmed to zero. If the PCF8549 is in power-down mode, the external LCD supply voltage has to be switched off.

T1, T2, T3, T4, T5, T6 AND T7: TEST PADS

T1, T3, T4, T5, T6 and T7 must be connected to V_{SS1}, T2 is to be left open. Not accessible to user.

SDA/SDA_OUT: I^2C DATA LINES

Output and input are separated. If both pads are connected together they behave like a standard I^2C pad.

SCL: I^2C CLOCK SIGNAL

Input for the I^2C-bus clock signal.

SA0: SLAVE ADDRESS

With the SA0 pin two different slave addresses can be selected. That allows to connect two PCF8549 LCD drivers to the same I^2C-bus.

OSC: OSCILLATOR

When the on-chip oscillator is used this input must be connected to V_{DD1}. An external clock signal, if used, is connected to this input.

$\overline{RES}$: RESET

This signal will reset the device. Signal is active low.

FUNCTIONAL DESCRIPTION

Block diagram functions

OSCILLATOR

The on-chip oscillator provides the clock signal for the display system. No external components are required and the OSC input must be connected to V_{DD1}. An external clock signal, if used, is connected to this input.

I²C INTERFACE

The I²C interface receives and executes the commands sent via the I²C-bus. It also receives RAM-data and sends them to the RAM. During read access the 8-bit parallel data or the status register content is converted to a serial data stream and output via the I²C-bus.

DISPLAY CONTROL LOGIC

The display control logic generates the control signals to read out the RAM via the 101 bit parallel port. It also generates the control signals for the row, and column drivers.

DISPLAY DATA RAM (DDRAM)

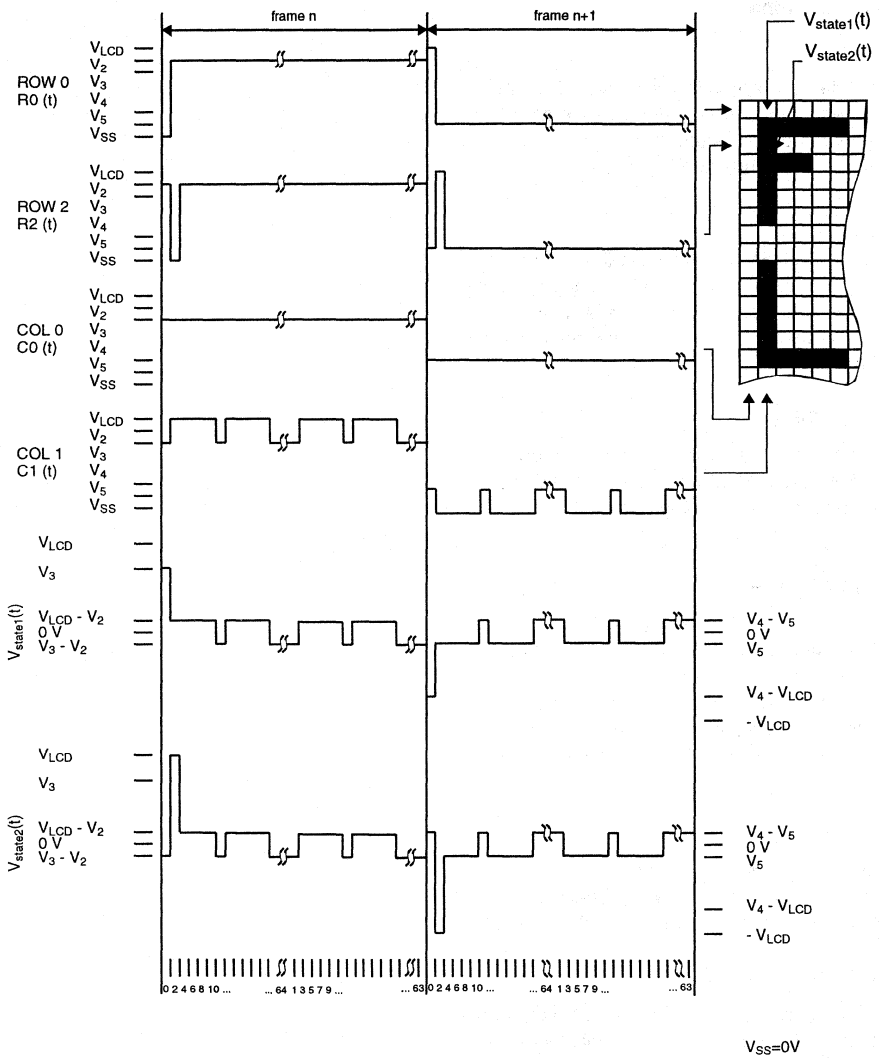
The PCF8549 contains a 65 × 102 bit static RAM which stores the display data. The RAM is divided into 8 banks of 102 bytes and one bank of 102 bits ((8 × 8 + 1) × 102 bits). During RAM access, data is transferred to the RAM via the I²C interface. There is a direct correspondence between X-address and column output number.

TIMING GENERATOR

The timing generator produces the various signals required to drive the internal circuitry. Internal chip operation is not disturbed by operations on the I²C-bus.

LCD ROW AND COLUMN DRIVERS

The PCF8549 contains 65 row and 102 column drivers, which connect the appropriate LCD bias voltages to the display in accordance with the data to be displayed. Figure 2 shows typical waveforms. Unused outputs should be left unconnected.



$V_{state1}(t) = C1(t) - R0(t)$
$V_{state2}(t) = C1(t) - R2(t)$

Fig.2 Typical LCD driver waveforms.

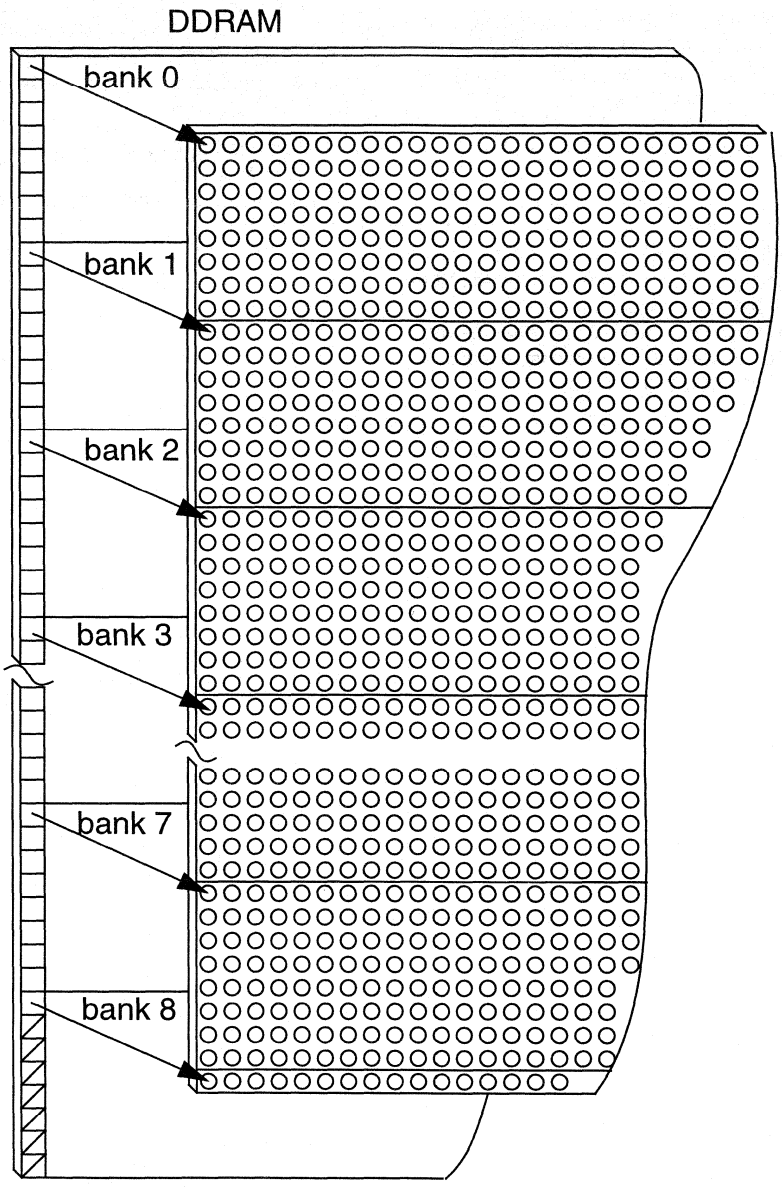


Fig.3 DDRAM to display mapping.

Addressing

The Display data RAM of the PCF8549 is accessed as indicated in Figs 3, 4, 4, 6 and 7. The display RAM has a matrix of 65 × 102 bits. The columns are addressed by the address pointer. The address ranges are:
X 0 to 101 (1100101b) and Y 0 to 8 (1000b). Addresses outside these ranges are not allowed. In vertical addressing mode (V = 1) the Y address increments (see Fig.7) after each byte. After the last Y address (Y = 8) Y wraps around to 0 and X increments to address the next column. In horizontal addressing mode (V = 0) the X address increments (see Fig.6) after each byte. After the last X address (X = 101) X wraps around to 0 and Y increments to address the next row. After the very last address (X = 101 and Y = 8) the address pointers wrap around to address (X = 0 and Y = 0).

The MX bit allows a horizontal mirroring: When MX = 1, the X address space is mirrored: The address X = 0 is then located at the right side (column 101) of the display (see Fig.4). When MX = 0 the mirroring is disabled and the address X = 0 is located at the left side (column 0) of the display (see Fig.4).

If the RM-bit (read-modify-write mode) is set, the address is only incremented after a write, otherwise the address is incremented after both read and write access to the display data RAM.

DISPLAY DATA RAM STRUCTURE

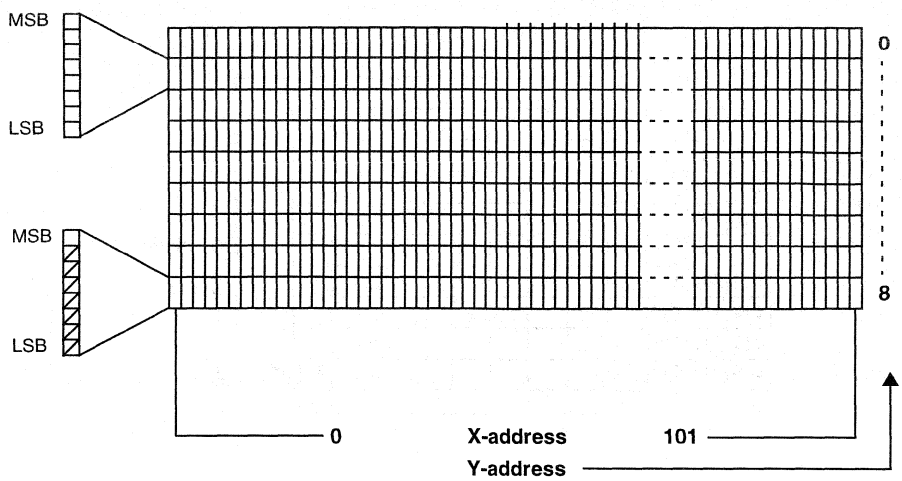


Fig.4 RAM format, addressing (MX = 0).

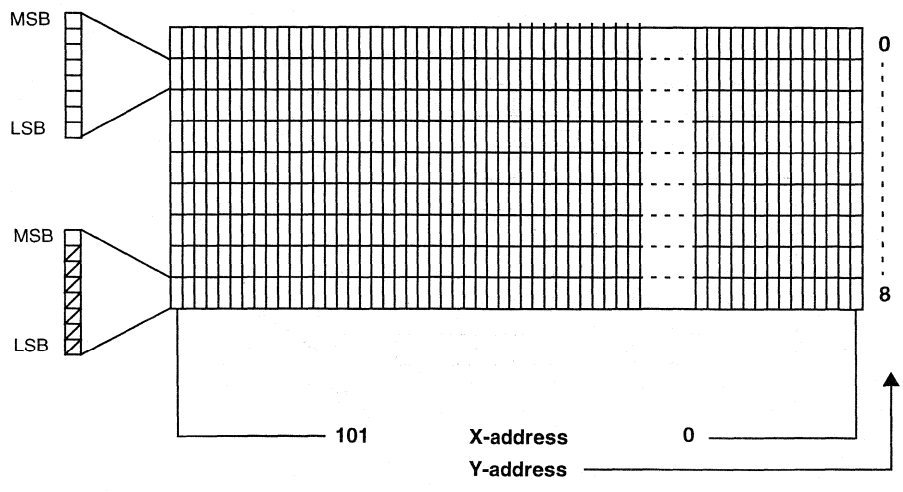


Fig.5 RAM format, addressing (MX = 1).

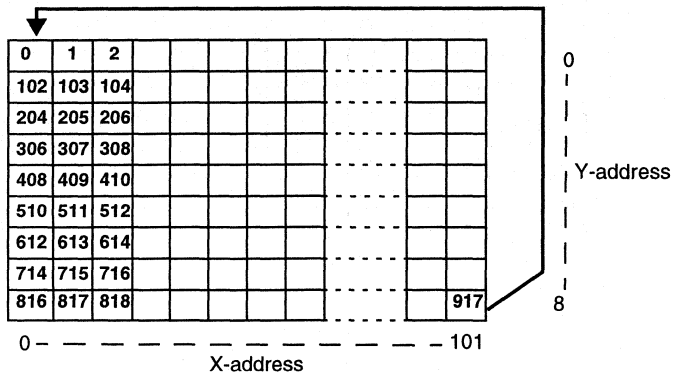


Fig.6 Sequence of writing data bytes into RAM with horizontal addressing (V = 0).

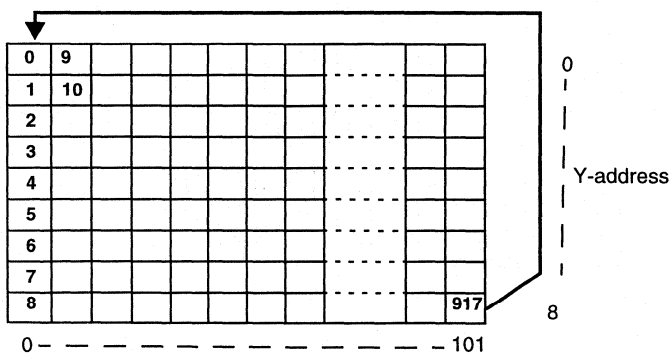


Fig.7 Sequence of writing data bytes into RAM with vertical addressing (V = 1).

RAM access

If the D/$\overline{C}$ bit is 1 the RAM can be accessed in both read and write access mode, depending on the R/$\overline{W}$ bit. The data is written to the RAM during the acknowledge cycle.

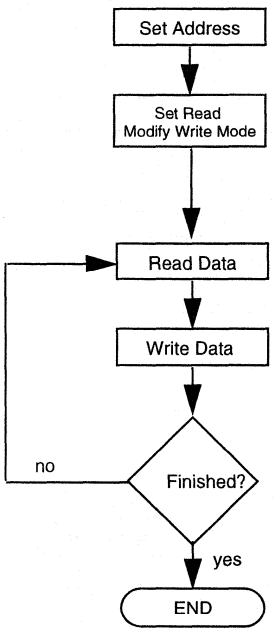


Fig.8 Read modify write access.

I²C-BUS INTERFACE

Characteristics of the I²C-bus

The I²C-bus is for bi-directional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

BIT TRANSFER (see Fig.9)

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

START AND STOP CONDITIONS (see Fig.10)

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P).

SYSTEM CONFIGURATION (see Fig.11)

- Transmitter: The device which sends the data to the bus
- Receiver: The device which receives the data from the bus
- Master: The device which initiates a transfer, generates clock signals and terminates a transfer
- Slave: The device addressed by a master
- Multi-Master: More than one master can attempt to control the bus at the same time without corrupting the message
- Arbitration: Procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted
- Synchronisation: Procedure to synchronize the clock signals of two or more devices.

ACKNOWLEDGE (see Fig.12)

Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

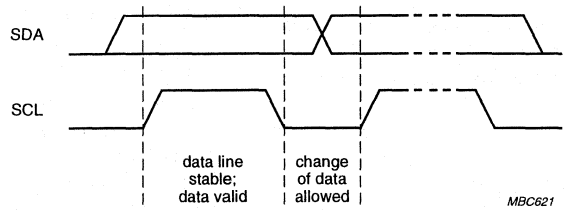


Fig.9 Bit transfer.

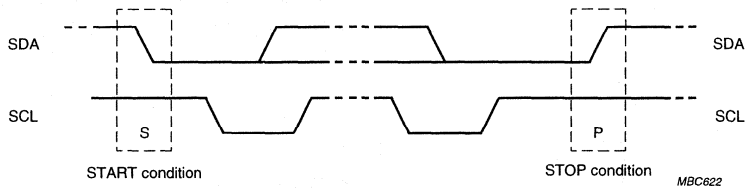


Fig.10 Definition of start and stop conditions.

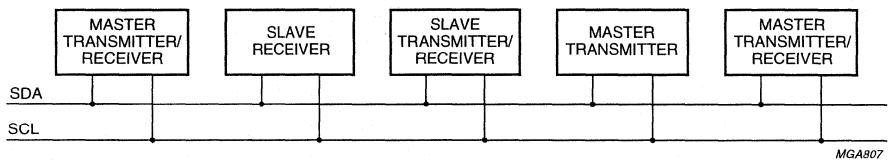


Fig.11 System configuration.

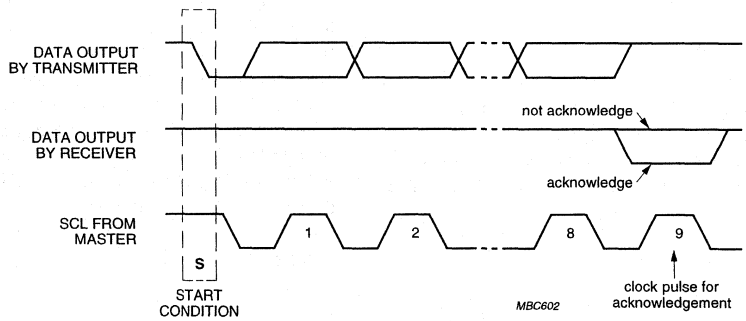


Fig.12 Acknowledgement on the I²C-bus.

I²C-bus protocol

The PCF8549 supports both read and write access. The R/$\overline{W}$ bit is part of the slave address.

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. Two 7-bit slave addresses (0111100 and 0111101) are reserved for the PCF8549. The least significant bit of the slave address is set by connecting the input SA0 to either logic 0 (V_{SS1}) or 1 (V_{DD1}).

The I²C-bus protocol is illustrated in Fig.13.

The sequence is initiated with a START condition (S) from the I²C-bus master which is followed by the slave address. All slaves with the corresponding address acknowledge in parallel, all the others will ignore the I²C-bus transfer. After acknowledgement, one or more command words follow which define the status of the addressed slaves. A command word consists of a control byte, which defines Co and D/$\overline{C}$, plus a data byte (see Fig.13 and Table 1).

The last control byte is tagged with a cleared most significant bit, the continuation bit Co. After a control byte with a cleared Co-bit, only data bytes will follow. The state of the D/$\overline{C}$-bit defines whether the data-byte is interpreted as a command or as RAM-data.The control and data bytes are also acknowledged by all addressed slaves on the bus.

After the last control byte, depending on the D/$\overline{C}$ bit setting, either a series of display data bytes or command data bytes may follow. If the D/$\overline{C}$ bit was set to '1', these display bytes are stored in the display RAM at the address specified by the data pointer. The data pointer is automatically updated and the data is directed to the intended PCF8549 device. If the D/$\overline{C}$ bit of the last control byte was set to '0', these command bytes will be decoded and the setting of the device will be changed according to the received commands. The acknowledgement after each byte is made only by the addressed slave. At the end of the transmission the I²C-bus master issues a stop condition (P).

If the R/$\overline{W}$ bit is set to one in the slave-address, the chip will output data immediately after the slave-address according to the D/$\overline{C}$ bit, which was sent during the last write access. If no acknowledge is generated by the master after a byte, the driver stops transferring data to the master.

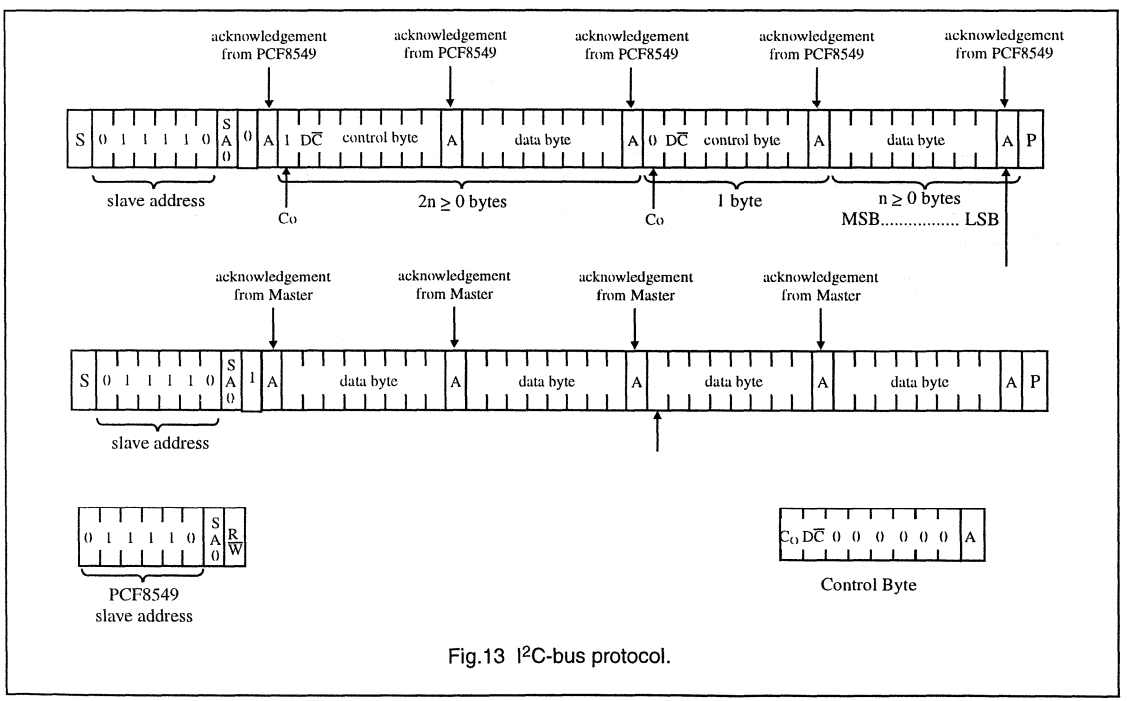


Fig.13 I²C-bus protocol.

INSTRUCTIONS

The instruction format is divided into two modes: If D/$\overline{C}$ is set low, the status byte can be read or commands can be sent to the chip, depending on the R/$\overline{W}$ signal. If D/$\overline{C}$ is set high, the DDRAM will be accessed. Every instruction can be sent in any order to the PCF8549.

Table 1 Instruction set

INSTRUCTION	D/$\overline{C}$	R/$\overline{W}$	COMMAND BYTE								DESCRIPTION
			DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
H = 0 or 1											
NOP	0	0	0	0	0	0	0	0	0	0	no operation
Function Set	0	0	0	0	1	MX	MY	PD	V	H	power down control; entry mode; Extended Instruction Set control (H)
Read Status Byte	0	1	PD	X	X	D	E	MX	MY	X	reads status byte
Write Data	1	0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	writes data to RAM
Read Data	1	1	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	reads data from RAM
H = 0											
Set Read Modify Write	0	0	0	0	0	0	0	0	1	RM	sets the read-modify-write mode
Reserved	0	0	0	0	0	0	0	1	X	X	do not use
Display Control	0	0	0	0	0	0	1	D	0	E	sets display configuration
Reserved	0	0	0	0	0	1	X	X	X	X	do not use
Set Y address of RAM	0	0	0	1	0	0	Y_3	Y_2	Y_1	Y_0	sets Y-address of RAM: $0 \leq Y \leq 8$
Set X address of RAM.	0	0	1	X_6	X_5	X_4	X_3	X_2	X_1	X_0	sets X-address of RAM: $0 \leq X \leq 101$
H = 1											
Reserved	0	0	0	0	0	0	0	0	0	1	do not use
Reserved	0	0	0	0	0	0	0	0	1	X	do not use
Temperature Control	0	0	0	0	0	0	0	1	TC_1	TC_0	set temperature coefficient (TCx)
Reserved	0	0	0	0	0	0	1	X	X	X	do not use
Bias System	0	0	0	0	0	1	0	BS_2	BS_1	BS_0	Set Bias System(BSx)
Reserved	0	0	0	1	X	X	X	X	X	X	do not use (reserved for test...)
Set V_{OP}	0	0	1	V_{OP6}	V_{OP5}	V_{OP4}	V_{OP3}	V_{OP2}	V_{OP1}	V_{OP0}	write V_{OP} to register

Table 2 Explanations for symbols in Table 1

BIT		0	1	RESET STATE
PD		chip is active	chip is in power down mode	1
V		horizontal addressing	vertical addressing	0
H		use basic instruction set	use extended instruction set	0
MX		normal X-addressing	X-address is mirrored	0
MY		display is not vertically mirrored	display is vertically mirrored	0
RM		read-modify-write mode is disabled	read-modify-write mode is enabled	0
D and E	00	display blank		D = 0 E = 0
	10	normal mode		
	01	all display segments on		
	11	inverse video mode		
TC[1 : 0]	00	V_{LCD} temperature coefficient 0		TC[1 : 0] = 00
	01	V_{LCD} temperature coefficient 1		
	10	V_{LCD} temperature coefficient 2		
	11	V_{LCD} temperature coefficient 3		
BS[2 : 0]		bias system		BS[2 : 0] = 000

External reset ($\overline{RES}$)

After power-on a reset pulse has to be applied immediately to the chip, as it is in an undefined state. A reset of the chip can be achieved with the external reset pin. After the reset the LCD driver is set to the following status:

- Power down mode (PD = 1)
- All LCD-outputs at V_{SS} (display off)
- Read-modify-write mode is disabled (RM = 0)
- Horizontal addressing (V = 0)
- Normal instruction set (H = 0)
- Normal display (MX = MY = 0)
- Display blank (E = D = 0)
- Address counter X[6 : 0] = 0 and Y[3 : 0] = 0
- Temperature coefficient (TC[1 : 0] = 0)
- Bias system (BS[2 : 0] = 0)
- Read-modify-write mode disabled (RM = 0)
- V_{LCD} is equal to 0, the HV generator is switched off (V_{OP}[6 : 0] = 0)
- After power-on, RAM data are undefined; The reset signal does not change the content of the RAM.

Set read-modify-write

When RM = 0, the read-modify-write mode is disabled. The X/Y-address counter is incremented after every read or write access to the display data RAM.

When RM = 1, the read-modify-write mode is enabled. In this mode the X/Y-address is incremented only after a write access to the display data RAM. The X/Y-address will not be incremented after a read access to the RAM.

Function Set

PD (POWER DOWN)

- All LCD outputs at V_{SS} (display off)
- Bias generator and V_{LCD} generator off
- Oscillator off (external clock possible)
- V_{LCD} can be disconnected
- Parallel bus, command, etc. function
- RAM contents not cleared; RAM data can be written.

V

When V = 0, the horizontal addressing is selected. The data is written into the RAM as shown in Fig.6. When V = 1, the vertical addressing is selected. The data is written into the RAM as shown in Fig.7.

H

When H = 0 the commands 'display control', 'set Y address' and 'set X address' can be performed, when H = 1 the other commands can be executed. The commands 'write data' and 'function set' can be executed in both cases.

MX

When MX = 0, the display is written from left to right (X = 0 is on the left side, X = 100 is on the right side of the display). When MX = 1 the display is written from right to left (X = 0 is on the right side, X = 100 is on the left side of the display).

MY

When MY = 1, the display is mirrored vertically.

Display Control

D AND E

The bits D and E select the display mode (see Table 2).

Set Y address of RAM

Y[3 : 0] defines the Y address vector address of the RAM.

Table 3 X-/Y-Address range

Y Y Y Y 3 2 1 0	CONTENT	ALLOWED X-RANGE
0 0 0 0	bank 0 (display RAM)	0 to 101
0 0 0 1	bank 1 (display RAM)	0 to 101
0 0 1 0	bank 2 (display RAM)	0 to 101
0 0 1 1	bank 3 (display RAM)	0 to 101
0 1 0 0	bank 4 (display RAM)	0 to 101
0 1 0 1	bank 5 (display RAM)	0 to 101
0 1 1 0	bank 6 (display RAM)	0 to 101
0 1 1 1	bank 7 (display RAM)	0 to 101
1 0 0 0	bank 8 (display RAM)	0 to 101

In bank 8 only the MSB is accessed.

Set X address of RAM

The X address points to the columns. The range of X is 0 to 101(65 hex).

Temperature Control

Due to the temperature dependency of the liquid crystals viscosity the LCD controlling voltage V_{LCD} must be increased with lower temperature to maintain optimal contrast. There are 4 different temperature coefficients available in the

PCF8549 (see Fig.14). The coefficients are selected by the two bits TC[1 : 0]. Table 6 shows the typical values of the different temperature coefficients. The coefficients are proportional to the programmed V_{LCD}.

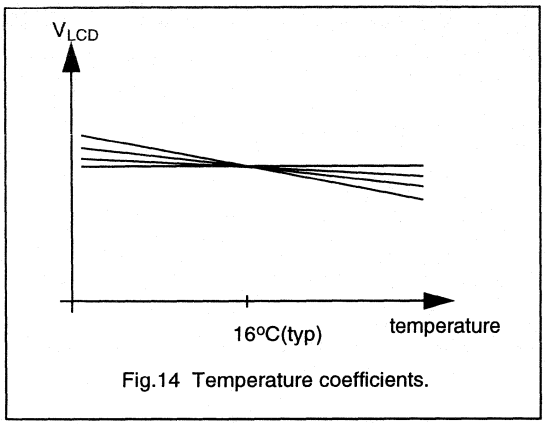


Fig.14 Temperature coefficients.

Bias value:

The bias voltage levels are set in the ratio of R – R – nR – R – R giving a $\frac{1}{n+4}$ bias system. The resulting bias levels are shown in table 5.

Different multiplex rates require different factors n (see Table 4). This is programmed by BS[2 : 0]. For MUX 1 : 65 the optimum bias value n is given by: $n = \sqrt{m} - 3 = \sqrt{65} - 3 = 5.06 = 5$

resulting in ⅕bias.

Table 4 Programming the required Bias system

BS[2]	BS[1]	BS[0]	n	b (RES. COUNT)	MUX RATE
0	0	0	7	11	1 : 100
0	0	1	6	10	1 : 81
0	1	0	5	9	1 : 64
0	1	1	4	8	1 : 49
1	0	0	3	7	1 : 36

BS[2]	BS[1]	BS[0]	n	b (RES. COUNT)	MUX RATE
1	0	1	2	6	1 : 24
1	1	0	1	5	1 : 16
1	1	1	0	4	1 : 9

Table 5 LCD bias voltage

SYMBOL	BIAS VOLTAGES
V1	V_{LCD}
V2	(b-1)/b × V_{LCD}
V3	(b-2)/b × V_{LCD}
V4	2/b × V_{LCD}
V5	1/b × V_{LCD}
V6	V_{SS}

Set V_{OP} value:

The operation voltage V_{LCD} can be set by software. The generated voltage is dependent of the temperature, the programmed temperature coefficient (TC), and the programmed voltage at reference temperature (T_{CUT}).

(1)

$$V_{LCD} = (a + VOP \cdot b) + (T - T_{CUT}) \cdot TC$$

The voltage at reference temperature ($V_{LCD}(T=T_{CUT})$) can be calculated as:

(2)

$$V_{LCD} = (a + VOP \cdot b)$$

The parameters are explained in table 6.

The maximum voltage that can be generated is depending on the $V_{DD2/2\_HV}$ Voltage and the display load current. The relation ship is shown in Fig.16.

The charge pump is turned off if Vop[6 : 0] is set to zero.

For Mux 1 : 65 the optimum operation voltage of the liquid can be calculated as:

$$V_{LCD} = \frac{1 + \sqrt{65}}{\sqrt{2 \cdot \left(1 - \frac{1}{\sqrt{65}}\right)}} \cdot V_{th} = 6.85 \cdot V_{th}$$

where V_{th} is the threshold voltage of the liquid crystal material used.

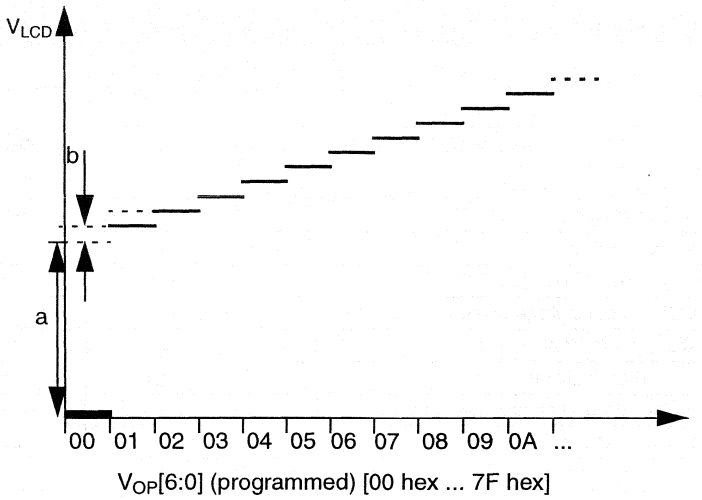


Fig.15 V_{OP} programming of PCF8549.

Table 6 Typical values for parameters for the HV-Generator programming

SYMBOL		VALUE	UNIT
a		7.06	V
b		0.06	V
T_{CUT}		16	°C
TC	00	$-0.142 \cdot 10^{-3} \cdot V_{LCD}(T = T_{CUT})$	V/°C
	01	$-1.3 \cdot 10^{-3} \cdot V_{LCD}(T = T_{CUT})$	V/°C
	10	$-2.467 \cdot 10^{-3} \cdot V_{LCD}(T = T_{CUT})$	V/°C
	11	$-3.483 \cdot 10^{-3} \cdot V_{LCD}(T = T_{CUT})$	V/°C

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134); all voltages referred to V_{SS} = 0V unless otherwise specified.

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{DD}	supply voltage range	-0.5	+7	V
V_{LCD}	supply voltage range LCD	-0.5	+17	V
I_{SS}	supply current	-50	50	mA
V_I/V_O	input/output voltage range	-0.5	V_{DD}+0.5	V
V_{OLCD}	LCD output voltage range	-0.5	V_{LCD}+0.5	V
I_I	DC input current	-10	10	mA
I_o	DC output current	-10	10	mA
P_{TOT}	power dissipation per package	-	300	mW
P_O	power dissipation per output	-	50	mW
T_{AMB}	operating ambient temperature. range	-40	+85	℃
T_{STG}	storage temperature range	-65	+150	°C

Notes

1. Stresses above those listed under Limiting Values may cause permanent damage to the device.
2. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.
3. with external LCD supply voltage external supplied **(voltage generator disabled)**. V_{DDmax} (V_{DD2},V_{DD2_HV}) is **5V** if LCD supply voltage is internally generated (voltage generator enabled).

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see "Handling MOS Devices"). The PCF8549 withstands the following stress:

- approximately 1.0kV Human Body Model
- approximately 150V Machine Model

DC CHARACTERISTICS

Table 7 V_{DD1} = 1.5 to 6 V; $V_{DD2/2\_HV}$ = 2.4 to 5.0 V; V_{DD2} = V_{DD2_HV}; V_{SS1} = V_{SS2} = V_{SS2_HV} = 0 V; V_{LCD} = 7 to 16 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD1}	Logic supply voltage range		1.5	3	6	V
V_{DD2}, V_{DD2_HV}	HV Generator supply range		2.4		5	V
I_{VDD1}	supply current internal V_{LCD}	V_{LCD} = 10.0V; f_{scl} = 0; display load = 0;		30	80	µA
$I_{VDD2/2\_HV}$	supply current internal V_{LCD}	VLCD = 10.0V; fscl = 0; display load = 0; (1)(5)		600	1200	µA
I_{VDD1}	supply current external V_{LCD}	V_{LCD} = 10.0V; f_{scl} = 0; display load = 0;		30	80	µA
$I_{VDD2/2\_HV}$	supply current external V_{LCD}	VLCD = 10.0V; fscl = 0; display load = 0; (2)(5)		0	10	µA
I_{VDD1}	supply current	power-down mode; V_{LCD} = 0V; fscl = 0; display load = 0		0.5	10	µA
I_{LCD}	supply current external V_{LCD}	V_{LCD} = 10 V; f_{SCL}= 0, display load = 0; (2)		50	130	µA
$V_{LCD(tol)}$	V_{LCD} tolerance internal generated	V_{DD} = 2.7V; VLCD = 10V; fSCL = 0; display load = 0;(3)(4)(6)			+/- 500	mV
V_{IL}	LOW level input voltage		V_{SS}		0.3V_{DD}	V
V_{IH}	HIGH level input voltage		0.7 V_{DD}		V_{DD}	V
I_{OL}	LOW level output current (SDA)	V_{OL} = 0.4V; V_{DD1} = 5 V		3.0		mA
I_L	leakage current	V_I = V_{DD1} or V_{SS1}	-1		+1	µA
R_{ROW}	Row output resistance R0 to R64			12	20	kOhm
R_{COL}	Column output resistance C0 to C101			12	20	kOhm

Notes

1. When a display is connected the I_{VDD2_HV} increases with 7 x display load current due to 7 stage charge pump.
2. With external V_{LCD}, the display load current does not translate into increased I_{VDD2_HV}.
3. For TC1, TC2 and TC3
4. The maximum possible VLCD voltage that may be generated is dependent on voltage ($V_{DD2/2\_HV}$), temperature and (display) load.
5. V_{DD2} V_{DD2_HV} connected together
6. Difference to the theoretical value given by equation 1

AC CHARACTERISTICS

Table 8 V_{DD1} = 1.5 to 6 V; $V_{DD2/2\_HV}$ = 2.4 to 5.0 V; V_{DD2} = V_{DD2_HV}; V_{SS1} = V_{SS2} = V_{SS2_HV} = 0 V; V_{LCD} = 7 to 16 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{OSC}	oscillator frequency		19	32	64	kHz
f_{EXT}	external clock frequency	(2)	10	32	64	kHz
t_{start}	oscillator start up time	(5)	–	450	1600	us
f_{FRAME}	frame frequency	f_{EXT} = 32 kHz;(1)	–	62	–	Hz
t_{VHRL}	VDD to $\overline{RES}$ Low	(5)			1	ms
t_{PWRES}	reset low pulse width		400	–	–	ns
I²C timing characteristics						
f_{SCLK}	SCL clock frequency	(6)	DC	–	400	kHz
t_{LOW}	SCL clock low period		1.3	–	–	us
t_{HIGH}	SCL clock high period		0.6	–	–	us
$t_{SU;Data}$	Data set-up time		100	–	–	ns
$t_{HD;Data}$	Data hold time		0	–	0.9	us
t_R	SCL and SDA rise time	(3)	20 + 0.1 Cb	–	300	ns
t_F	SCL and SDA fall time	(3)	20 + 0.1 Cb	–	300	ns
c_b	Capacitive load represented by each bus line		–	–	400	pF
$t_{SU;STA}$	setup time for a repeated START condition		0.6	–	–	us
$t_{HD;STA}$	start condition hold time		0.6	–	–	us
$t_{SU;DAT}$	data set-up time		100	–	–	ns
$t_{HD;DAT}$	data hold-time		0	–	–	ns
$t_{SU;STO}$	setup time for STOP condition		0.6	–	–	us
t_{SW}	tolerable spike width on bus	(4)	–	–	50	ns
t_{BUF}	BUS free time between a STOP and START condition		1.3	–	–	us

Notes

1. $f_{FRAME} = \frac{f_{EXT}}{520}$
2. Duty cycle of 50 +/-5%.
3. The rise and fall times specified here refer to the driver device (i.e. not PCF8549) and are part of the general fast I²C-bus specification. When PCF8549 asserts an acknowledge on SDA, the minimum fall time is 10ns. C_b= capacitive load per bus line.
4. The device inputs SDA and SCL are filtered and will reject spikes on the bus lines of width < $t_{SW(max)}$.
5. Not tested in production
6. Only for VDD1= 2V to 6V

TYPICAL CHARACTERISTICS

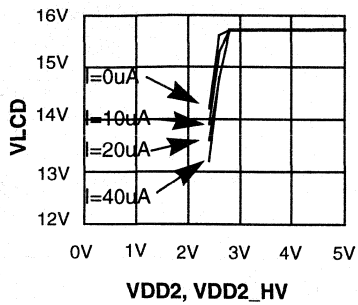


Fig.16 VLCD dependency of VDD2, VDD2_HV and load current. Programmed VLCD=15.8V (@ Room Temperature in special Test mode)

RESET

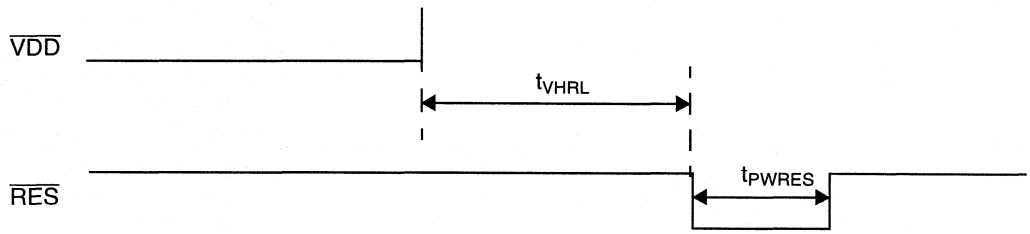
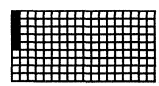
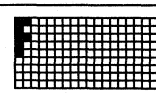
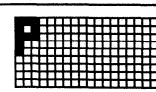
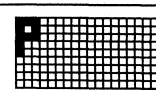
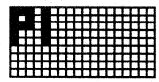
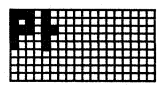
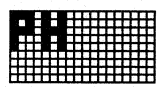
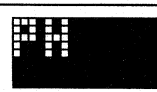
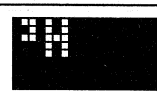
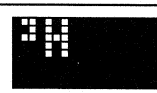
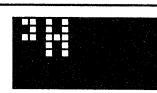


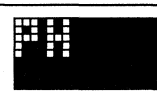
Fig.17 Reset timing.

APPLICATION INFORMATION

Table 9 programming example for PCF8549

STEP	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DISPLAY	OPERATION
1	I^2C start									
2	0	1	1	1	1	0	0	0		Slave address for write
3	0	0	0	0	0	0	0	0		Control byte with cleared C_O bit and D/$\overline{C}$ set to 0.
4	0	0	1	0	0	0	0	1		Function Set PD = 0; V = 0; select extended instruction set (H = 1 mode)
5	0	0	0	1	0	0	1	0		Set Bias System 2. This is the recommended Bias System for a multiplex rate 1:65
6	1	1	1	0	1	0	1	0		set V_{OP} V_{OP} is set to a +16 × b [V]. Please note: The required voltage is depending on the liquid.
7	0	0	1	0	0	0	0	0		Function Set PD = 0; V = 0; select normal instruction set (H = 0 mode)
8	0	0	0	0	1	1	0	0		Display Control set normal mode (D = 1 and E = 0)
9	I^2C start									Restart: To write into the Display RAM the D/$\overline{C}$ must be set to 1; therefore a control byte is needed.
10	0	1	1	1	1	0	0	0		Slave address for write
11	0	1	0	0	0	0	0	0		Control byte with cleared C_O bit and D/$\overline{C}$ set to 1.
12	1	1	1	1	1	0	0	0		Data Write Y and X are initialized to 0 by default, so they aren't set here
13	1	0	1	0	0	0	0	0		Data Write
14	1	1	1	0	0	0	0	0		Data Write
15	0	0	0	0	0	0	0	0		Data Write

STEP	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DISPLAY	OPERATION
16	1	1	1	1	1	0	0	0		Data Write
17	0	0	1	0	0	0	0	0		Data Write
18	1	1	1	1	1	0	0	0		Data Write
19	I^2C start									Restart
20	0	1	1	1	1	0	0	0		Slave address for write
21	1	0	0	0	0	0	0	0		Control byte with set C_O bit and D/$\overline{C}$ set to 0.
22	0	0	0	0	1	1	0	1		Display Control Set inverse video mode (D = 1 and E = 1)
23	1	0	0	0	0	0	0	0		Control byte with set C_O bit and D/$\overline{C}$ set to 0.
24	1	0	0	0	0	0	0	0		Set X address of RAM set address to '0000000'
25	1	1	0	0	0	0	0	0		Control byte with set C_O bit and D/$\overline{C}$ set to 1.
26	0	0	0	0	0	0	0	0		Data Write
27	0	0	0	0	0	0	0	0		Control byte with cleared C_O bit and D/$\overline{C}$ set to 0.
28	1	0	0	0	0	0	0	0		Set X address of RAM Set address to '0000000'
29	0	0	0	0	0	0	0	1		Set Read Modify Write Mode
30	I^2C start									Restart
31	0	1	1	1	1	0	0	0		Slave address for write

STEP	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DISPLAY	OPERATION
32	1	1	0	0	0	0	0	0		Control byte with set C_O bit and D/$\overline{C}$ set to 1.
33	I^2C start									Restart
34	0	1	1	1	1	0	0	1		Slave address for read
35	1	0	0	0	0	0	0	0		Read Data From Address '0000000'
36	1	0	0	0	0	0	0	0		Read Data From Address '0000000' again. Master does not send an acknowledge to stop the read access.
37	I^2C start									Restart
38	0	1	1	1	1	0	0	0		Slave address for write
39	1	1	0	0	0	0	0	0		Control byte with set C_O bit and D/$\overline{C}$ set to 1.
40	1	1	1	1	1	0	0	0		Write Data
41	1	0	0	0	0	0	0	0		Control byte with set C_O bit and D/$\overline{C}$ set to 0.
42	I^2C start									Restart
43	0	1	1	1	1	0	0	1		Slave address for read
44	1	0	0	0	0	0	0	0		Read Status Byte

APPLICATION INFORMATION

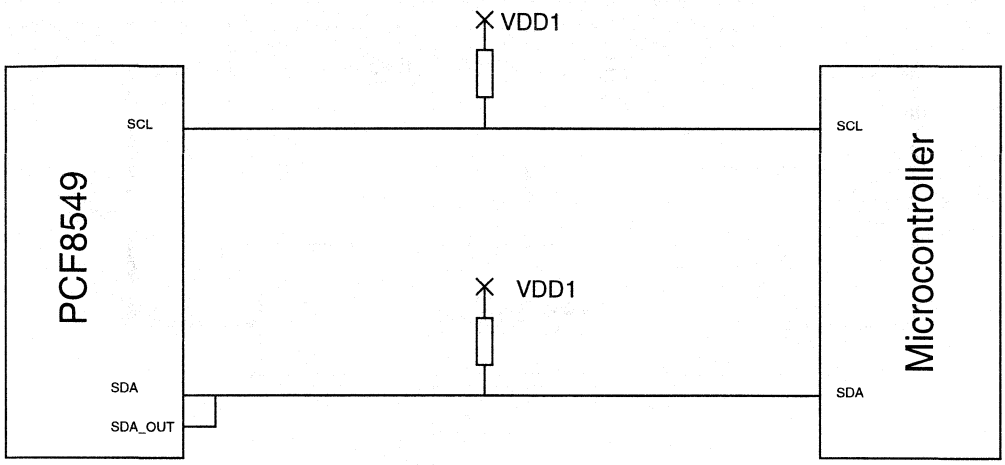


Fig.18 Application diagram: Connecting the I2C Interface

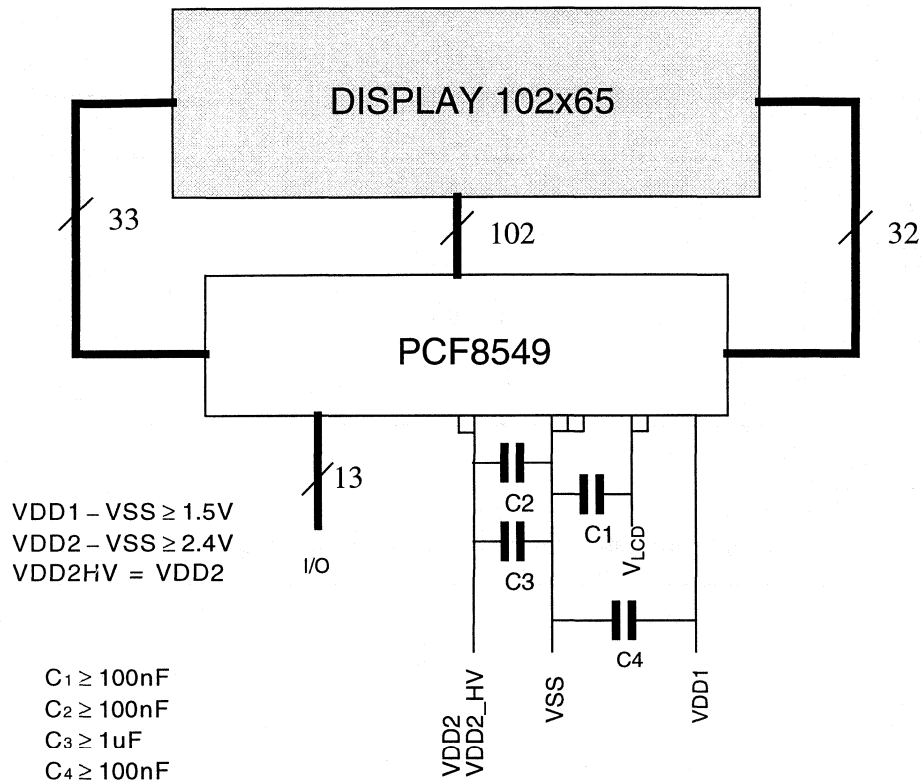


Fig.19 Application diagram: Connecting the power supplies

The pinning of the PCF8549 is optimized for single plane wiring e.g. for chip-on-glass display modules. Display size: 65 × 102 pixels.

CHIP INFORMATION

The PCF8549 is manufactured in n-well CMOS technology.

The substrate is on V_{SS} potential.

BONDING PADS

	VALUE	UNIT
Pad pitch	min. 100	μm
Pad size, alumin.	80 × 100	μm
Passivation.	48 × 78	μm
Bumps	60 (±6) × 90 (±6) × 17.5 (±5)	μm
Wafer thickness	380 (±25)	μm

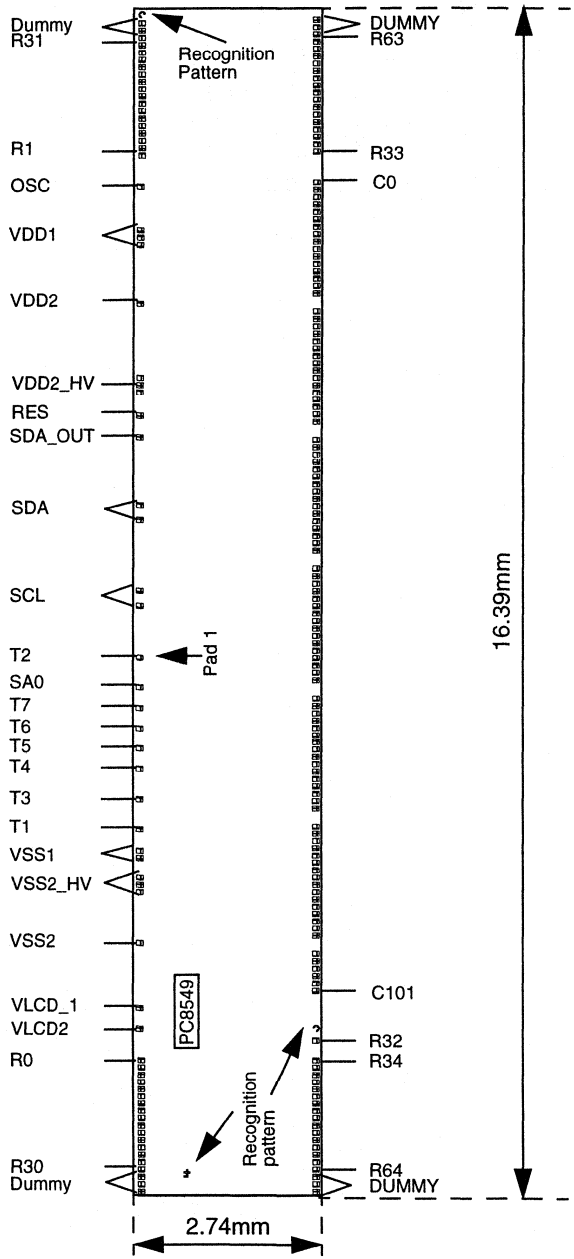

Dummy
R31
Recognition
Pattern
DUMMY
R63
R1
R33
OSC
C0
VDD1
VDD2
VDD2_HV
RES
SDA_OUT
SDA
SCL
T2
Pad 1
SA0
T7
T6
T5
T4
T3
T1
VSS1
VSS2_HV
VSS2
PC8549
VLCD_1
VLCD2
R0
C101
R32
R34
Recognition
pattern
R30
Dummy
R64
DUMMY
16.39mm
2.74mm

Fig.20 Pads.

Table 10 Bonding pad locations (dimensions in um).

Pad	Pad name	X	Y
1	T2	7359.5	2462
2	SA0	6958	2462
3	T7	6679	2462
4	T6	6400	2462
5	T5	6121	2462
6	T4	5841.5	2462
7	T3	5431.5	2462
8	T1	5022	2462
9	VSS1	4724	2458
10	VSS1	4624	2458
11	VSS2_HV	4359	2458
12	VSS2_HV	4259	2458
13	VSS2_HV	4159	2458
14	VSS2	3458.5	2458
15	VLCD1	2580	2462
16	VLCD2	2294	2462
17	ROW<0>	1870	2437
18	ROW<2>	1770	2437
19	ROW<4>	1670	2437
20	ROW<6>	1570	2437
21	ROW<8>	1470	2437
22	ROW<10>	1370	2437
23	ROW<12>	1270	2437
24	ROW<14>	1170	2437
25	ROW<16>	1070	2437
26	ROW<18>	970	2437
27	ROW<20>	870	2437
28	ROW<22>	770	2437
29	ROW<24>	670	2437
30	ROW<26>	570	2437
31	ROW<28>	470	2437
32	ROW<30>	370	2437
33	Dummy 4	270	2437
34	Dummy 5	170	2437
35	Dummy 6	70	2437
36	Dummy 3	70	84
37	Dummy 2	170	84
38	Dummy 1	270	84
39	ROW<64>	370	84
40	ROW<62>	470	84
41	ROW<60>	570	84
42	ROW<58>	670	84
43	ROW<56>	770	84
44	ROW<54>	870	84
45	ROW<52>	970	84
46	ROW<50>	1070	84
47	ROW<48>	1170	84
48	ROW<46>	1270	84
49	ROW<44>	1370	84
50	ROW<42>	1470	84
51	ROW<40>	1570	84
52	ROW<38>	1670	84
53	ROW<36>	1770	84
54	ROW<34>	1870	84
55	ROW<32>	2137	84
56	COL<101>	2812	84
57	COL<100>	2914	84
58	COL<99>	3014	84
59	COL<98>	3114	84
60	COL<97>	3214	84
61	COL<96>	3314	84
62	COL<95>	3560	84
63	COL<94>	3660	84
64	COL<93>	3760	84
65	COL<92>	3860	84
66	COL<91>	3960	84
67	COL<90>	4060	84
68	COL<89>	4160	84
69	COL<88>	4260	84
70	COL<87>	4360	84
71	COL<86>	4460	84
72	COL<85>	4560	84
73	COL<84>	4660	84
74	COL<83>	4760	84
75	COL<82>	4860	84
76	COL<81>	4960	84
77	COL<80>	5060	84
78	COL<79>	5306	84
79	COL<78>	5406	84
80	COL<77>	5506	84

Pad	Pad name	X	Y
81	COL<76>	5606	84
82	COL<75>	5706	84
83	COL<74>	5806	84
84	COL<73>	5906	84
85	COL<72>	6006	84
86	COL<71>	6106	84
87	COL<70>	6206	84
88	COL<69>	6306	84
89	COL<68>	6406	84
90	COL<67>	6506	84
91	COL<66>	6606	84
92	COL<65>	6706	84
93	COL<64>	6806	84
94	COL<63>	7052	84
95	COL<62>	7152	84
96	COL<61>	7252	84
97	COL<60>	7352	84
98	COL<59>	7452	84
99	COL<58>	7552	84
100	COL<57>	7652	84
101	COL<56>	7752	84
102	COL<55>	7852	84
103	COL<54>	7952	84
104	COL<53>	8052	84
105	COL<52>	8152	84
106	COL<51>	8252	84
107	COL<50>	8352	84
108	COL<49>	8452	84
109	COL<48>	8552	84
110	COL<47>	8798	84
111	COL<46>	8898	84
112	COL<45>	8998	84
113	COL<44>	9098	84
114	COL<43>	9198	84
115	COL<42>	9298	84
116	COL<41>	9398	84
117	COL<40>	9498	84
118	COL<39>	9598	84
119	COL<38>	9698	84
120	COL<37>	9798	84

Pad	Pad name	X	Y
121	COL<36	989	8
12	COL<35	999	8
12	COL<34	1009	8
12	COL<33	1019	8
12	COL<32>	1029	8
12	COL<31	1054	8
12	COL<30	1064	8
12	COL<29	1074	8
12	COL<28	10844	8
13	COL<27	1094	8
13	COL<26	1104	8
13	COL<25	1114	8
13	COL<24	1124	84
13	COL<23	1134	8
13	COL<22	1144	8
13	COL<21	1154	8
13	COL<20	1164	8
138	COL<19	1174	8
13	COL<18	1184	8
14	COL<17	1194	8
14	COL<16	1204	8
14	COL<15>	1229	8
14	COL<14	1239	8
14	COL<13	1249	8
14	COL<12	1259	8
14	COL<11	12690	8
14	COL<10	1279	8
14	COL<9	1289	8
14	COL<8	1299	8
15	COL<7	1309	84
15	COL<6	1319	8
15	COL<5	1329	8
15	COL<4	1339	8
15	COL<3	1349	8
155	COL<2	1359	8
15	COL<1	1369	8
15	COL<0	1379	8
15	ROW<33	1420	8
15	ROW<35>	1430	8
16	ROW<37	1440	8

Pad	Pad name	X	Y
16	ROW<39	1450	8
16	ROW<41	1460	8
16	ROW<43	14704	8
16	ROW<45	1480	8
16	ROW<47	1490	8
16	ROW<49	1500	8
16	ROW<51	1510	84
16	ROW<53	1520	8
16	ROW<55	1530	8
17	ROW<57	1540	8
17	ROW<59	1550	8
172	ROW<61	1560	8
17	ROW<63	1570	8
17	Dummy	1580	8
17	Dummy	1590	8
17	Dummy 9	1600	8
17	Dummy 1	1596	243
17	Dummy 1	1586	243
17	Dummy 1	1576	243
18	ROW<31	15661	243
18	ROW<29	1556	243
18	ROW<27	1546	243
18	ROW<25	1536	243
18	ROW<23	1526	2437
18	ROW<21	1516	243
18	ROW<19	1506	243
18	ROW<17	1496	243
18	ROW<15	1486	243
189	ROW<13	1476	243
19	ROW<11	1466	243
19	ROW<9	1456	243
19	ROW<7	1446	243
19	ROW<5>	1436	243
19	ROW<3	1426	243
19	ROW<1	1416	243
19	OS	1373	246
19	VDD	13147	246
19	VDD	1304	246
19	VDD	1294	246
20	VDD	1214	246

Pad	Pad name	X	Y
20	VDD2_HV_I	1114	2461
20	VDD2_HV_I	1104	246
20	VDD2_HV_I	1094	246
20	RES_B_I	1062	246
20	SDA_OU	10333.5	246
206	SDA_I	9412.	246
20	SDA_I	9212.	246
20	SCL_I	8256.	246
20	SCL_I	8056.	246
	Recpat C1	16275	2437
	Recpat C2	2301	80
	Recpat F	304	1824

Universal LCD driver for small graphic panels

PCF8558

FEATURES

- Single-chip LCD controller/driver
- 40 row and 101 column outputs
- Display data RAM
  40 × 101 bits = 505 bytes = 4040 bits
- On-chip:
  - Generation of intermediate LCD bias voltages
  - Oscillator requires no external components (external clock also possible)
- 400 kHz fast I²C-bus interface
- CMOS compatible
- MUX rate 1 : 40
- Logic supply voltage range $V_{DD} - V_{SS}$ = 2.5 to 6 V
- Display supply voltage range $V_{DD} - V_{LCD}$ = 3.5 to 9 V
- Low power consumption, suitable for battery operated systems.

GENERAL DESCRIPTION

The PCF8558 is a low power CMOS LCD controller driver, designed to drive a graphic display of 40 rows and 101 columns. All necessary functions for the display are provided in a single chip, including on-chip generation of LCD bias voltages, resulting in a minimum of external components and lower power consumption.

The PCF8558 interfaces to most microcontrollers via a I²C-bus interface.

APPLICATIONS

- Telecom equipment
- Portable instruments
- Point of sale terminals
- Alarm systems.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE[1]		
	NAME	DESCRIPTION	VERSION
PCF8558U/10	–	chip on FFC	–
PCF8558U/12	–	chip with bumps on FFC	–

Note

1. For further details see Chapter "Bonding pad locations".

BLOCK DIAGRAM

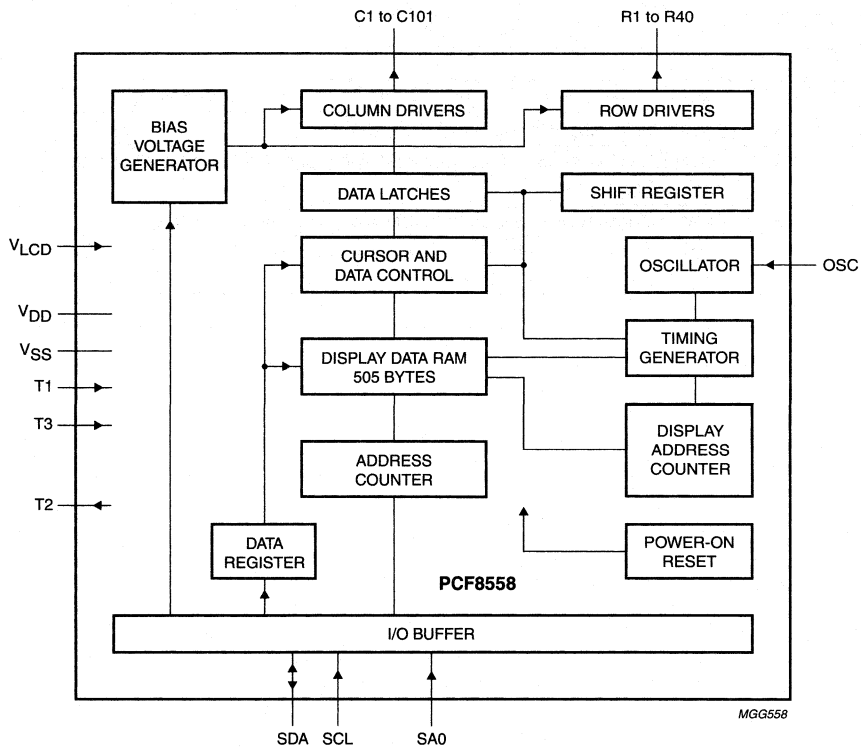


Fig.1 Block diagram.

PINNING

SYMBOL	PAD	DESCRIPTION
SCL	1	I^2C-bus serial clock input
R20 to R1	2 to 21	LCD row driver data outputs
C101 to C1	22 to 122	LCD column driver data outputs
R21 to R40	123 to 142	LCD row driver data outputs
T2	143	test pad output, must be left unconnected (not user accessible)
SDA	144	I^2C-bus serial data input/output
V_{SS}	145	ground
T1	146	test pad input, must be connected to V_{SS} (not user accessible)
V_{LCD}	147	negative supply voltage input
SA0	148	the LSB bit of the I^2C-bus slave address input is set by connecting this pin to either 0 (V_{SS}) or 1 (V_{DD})
T3	149	test pad input, must be connected to V_{DD} (not user accessible)
OSC	150	when the on-chip oscillator is used this pin must be connected to V_{DD}; an external clock signal, if used, is input at this pin
V_{DD}	151	positive supply voltage

FUNCTIONAL DESCRIPTION

LCD bias voltage generator

The intermediate bias voltages for the LCD display are generated and buffered on-chip. This removes the need for an external resistor bias chain and significantly reduces the system power consumption.

Oscillator

The on-chip oscillator provides the clock signal for the display system. No external components are required and the OSC pin must be connected to V_{DD}.

External clock

If an external clock is to be used it is input at the OSC pin. The resulting display frame frequency is given by

$$f_{frame} = \frac{f_{osc}}{3072}.$$

Only in the power-down state is the clock allowed to be stopped (OSC connected to V_{SS}), otherwise the LCD will be frozen in a state where a DC voltage is applied to it.

Power-on reset

The on-chip power-on reset block initializes the chip after power-on or power failure. This is a synchronous reset and requires 2 oscillator cycles to execute. These oscillator cycles must be provided from the external clock source if the internal oscillator is not used. If this is not done, the device may not respond to command sequences transmitted via the I^2C-bus interface.

Power-down

The chip can be put into power-down mode where all static currents are switched off (no internal oscillator, no internal power-on reset, no bias level generation and all LCD outputs are internally connected to V_{DD}) when PD = logic 1.

During power-down the information in the RAMs and the internal chip states are preserved. Instruction execution during power-down is possible if an externally clock signal is applied to pad OSC.

Registers

The PCF8558 has one 8-bit register, time shared as a Command Register (CR) and a Data Register (DR). The command register stores the command code such as display on or display off and address information for the Display Data RAM (DDRAM). Both registers can be written to but not read from by the system controller.

Address Counter (AC)

The address counter assigns addresses to the DDRAM for writing and is set by Y2 to Y0 in the command and X6 to X0 in the address. After a write operation the address counter is automatically incremented by 1 in accordance with the V flag.

Display Data RAM (DDRAM)

The PCF8558 contains a 40×101-bit static RAM which stores the display data. The RAM is divided into 5 banks of 101 bytes ($5 \times 8 \times 101$ bits). During RAM access, data is transferred to the RAM via the I^2C-bus. There is a direct correspondence between the X address and the column output number.

Timing generator

The timing generator produces the various signals required to drive the internal circuitry. Internal chip operation is not disturbed by operations on the data buses.

Display control

The display is generated by continuously shifting rows of RAM data to the dot matrix LCD via the column outputs.

The display status (all dots on/off and normal/inverse video) is set by bits E and D in the command word.

LCD row and column drivers

The PCF8558 contains 40 row and 101 column drivers, which connect the appropriate LCD bias voltages in sequence to the display in accordance with the data to be displayed. Figure 3 illustrates typical waveforms. Unused outputs should be left unconnected.

The bias voltage levels, V2 to V5, are chosen to give optimum display contrast for a multiplex rate of 1 : 40.

Table 1 Voltage bias levels

LEVEL	VOLTAGE
V2	$0.8635 \times (V_{DD} - V_{LCD})$
V3	$0.7270 \times (V_{DD} - V_{LCD})$
V4	$0.2730 \times (V_{DD} - V_{LCD})$
V5	$0.1365 \times (V_{DD} - V_{LCD})$

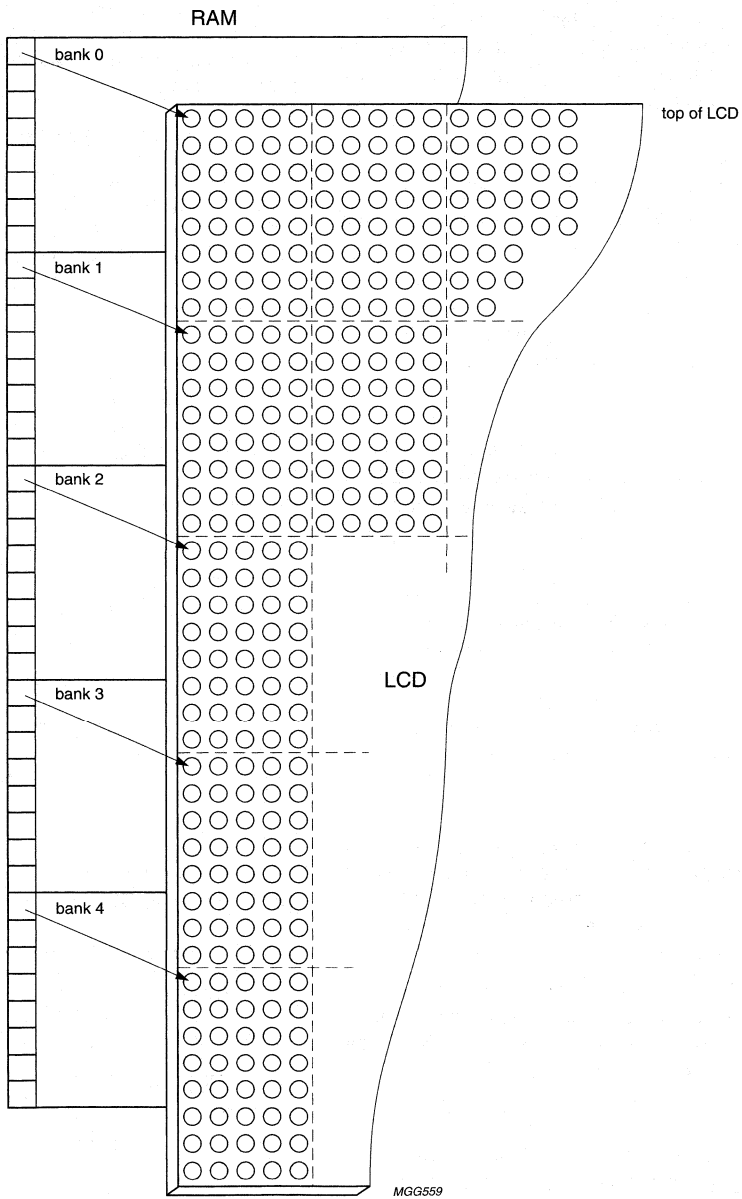
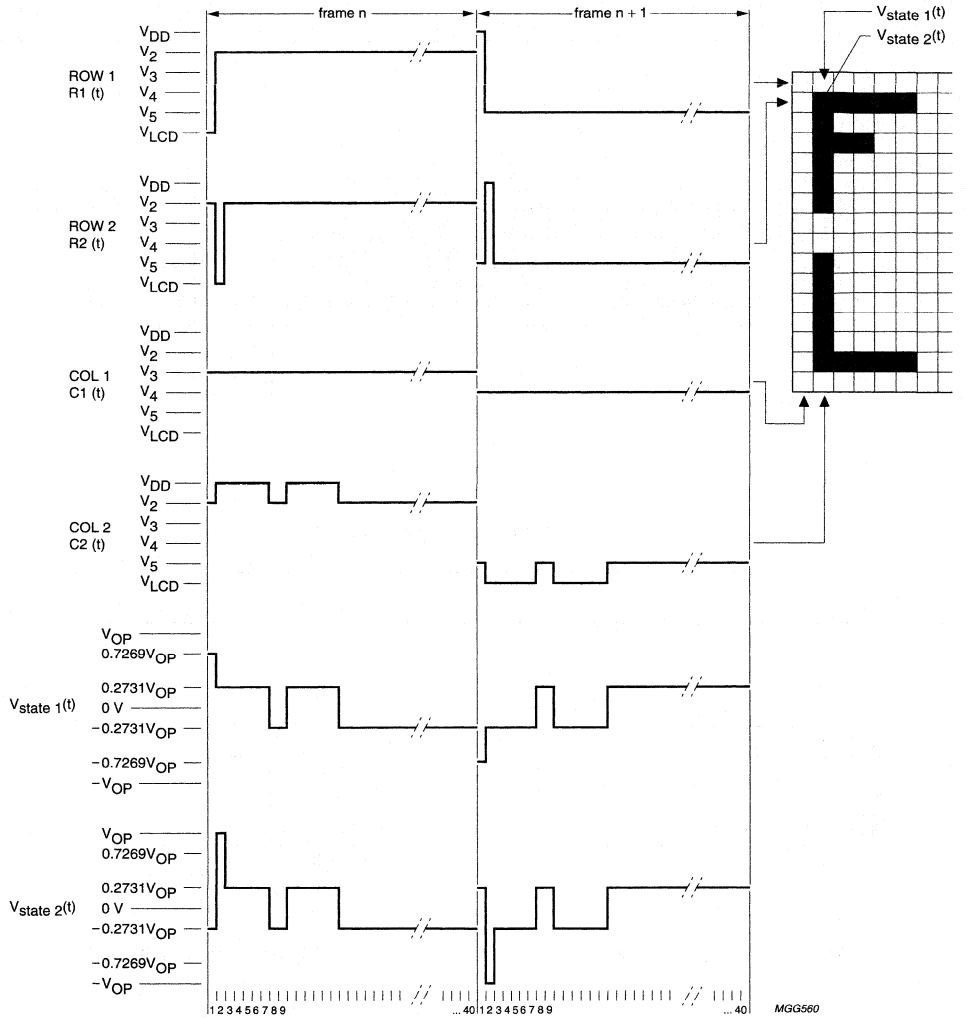


Fig.2 DDRAM to display mapping.



$V_{state1}(t) = C2(t) - R1(t)$; $V_{state2}(t) = C2(t) - R2(t)$.

Fig.3 Typical LCD driver waveforms (MUX rate 1 : 40).

ADDRESSING

The data is downloaded into the matrix of the PCF8558 as indicated in Figs 4 and 5.

The display RAM has a matrix of 40 by 101 bits (5 by 101 bytes). The columns are addressed by the address pointer. After writing one byte the pointer is set to the next byte. Control of address increment, horizontal or vertical, is by bit V in the command byte.

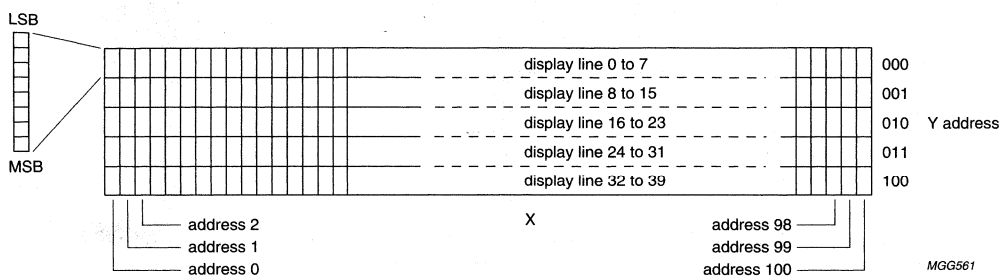
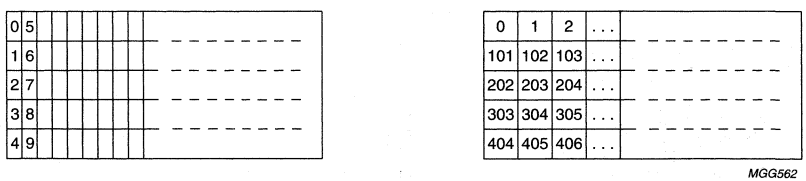


Fig.4 RAM format, addressing.

DATA STRUCTURE



a. Order of writing data bytes into RAM (V = 1).

b. Order of writing data bytes into RAM (V = 0).

Fig.5 Order of writing data bytes into RAM.

I²C-BUS PROTOCOL

Two 7-bit slave addresses (0111100 and 0111101) are reserved for both the PCF8558. The least-significant bit of the slave address is set by connecting input SA0 to either 0 (V_{SS}) or 1 (V_{DD}). Therefore, two PCF8558 can be used on the same I²C-bus allowing displays of up to 80 × 101 or 40 × 202 dots to be driven.

The I²C-bus protocol is shown in Fig.6.
All communications are initiated with a START condition (S) from the I²C-bus master, which is followed by the desired slave address and write bit. All devices with this slave address acknowledge in parallel. All other devices ignore the bus transfer.

In write mode (indicated by setting the read/write bit LOW) one or more commands follow the slave address acknowledgement. The commands are also acknowledged by all addressed devices on the bus. The last command must clear the continuation bit C. After the last command a series of data bytes may follow. The acknowledgement after each byte is made only by the addressed device. After the last data byte has been acknowledged, the I²C-bus master issues a STOP condition (P).

For PCF8558, no read mode is provided.

Display bytes are written into the RAM at the address specified by the data pointer and subaddress counter. Both the data pointer and subaddress counter are automatically incremented, enabling a stream of data to be transferred to the DDRAM.

The instruction format is composed of I²C-bus slave address followed by one command byte, one X address pointer, followed by any number of data bytes.

Command execution/storing of data takes place during the acknowledge cycle.

Definitions

- Transmitter: the device which sends the data to the bus
- Receiver: the device which receives the data from the bus
- Master: the device which initiates a transfer, generates clock signals and terminates a transfer
- Slave: the device addressed by a master
- Multi-master: more than one master can attempt to control the bus at the same time. The I²C-bus can accommodate this without data los/contention.
- Arbitration: procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted
- Synchronization: procedure to synchronize the clock signals of two or more devices.

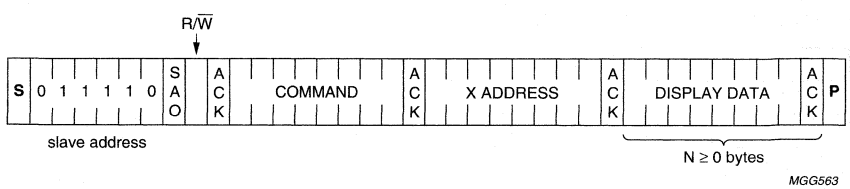


Fig.6 I²C-bus protocol.

COMMANDS

Display Control

BIT	LOGIC 0	LOGIC 1
PD	normal	power-down
V	horizontal addressing	vertical addressing

Table 2 Display status

DISPLAY STATUS	BITS	
	E	D
Blank	0	0
Normal	1	1
All segments on	1	0
Inverse video	0	1

PD: POWER-DOWN

- All LCD outputs at V_{DD} (display off)
- Bias generator off
- Power-on reset on, oscillator off (external clock still possible)
- V_{LCD} can be disconnected
- I^2C-bus, RAM, commands, etc. still function in power-down mode.

Set Address

Table 3 Y0, Y1 and Y2 define the Y address vector address of the display RAM

Y2	Y1	Y0	LINE
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4

Set X address

The X address points to the columns. The range of X is 0 to 100 (64H).

Reset function

After power-on the chip has the following state:

- Power-down mode (PD = 1)
- RAM undefined
- RAM X and Y address undefined
- Display control bits (except PD) undefined
- I^2C-bus interface reset.

Note

If the chip is used with an external clock source, after power-on, the chip requires at least 2 clock pulses to ensure that an internal synchronous reset is carried out. After the internal reset, the chip goes into power-down mode (PD = 1). If the clock pulses are not supplied, and the reset is not cleared, the chip cannot respond to commands in the I^2C bus.

In applications where the internal oscillator is used (pin OSC = V_{DD}), the oscillator starts after power-on. As soon as the synchronous reset is cleared, the chip goes into power-down mode, and the oscillator is stopped.

Table 4 Instructions: control byte, address

INSTRUCTION	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DESCRIPTION
Display control	0	E	D	PD	V	Y2	Y1	Y0	Y address vector, display control
X address	0	X address							set column address

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL) which must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this moment will be interpreted as control signals.

START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH, is defined as the STOP condition (P).

System configuration

A device transmitting a message is a 'transmitter', a device receiving a message is the 'receiver'. The device that controls the message flow is the 'master' and the devices which are controlled by the master are the 'slaves'.

Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each data byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal the end of a data transmission to the transmitter by **not** generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

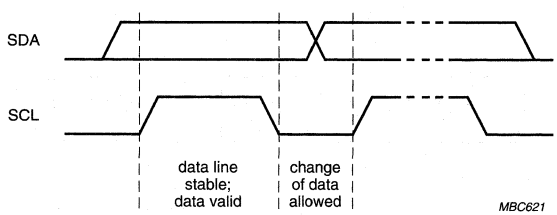


Fig.7 Bit transfer.

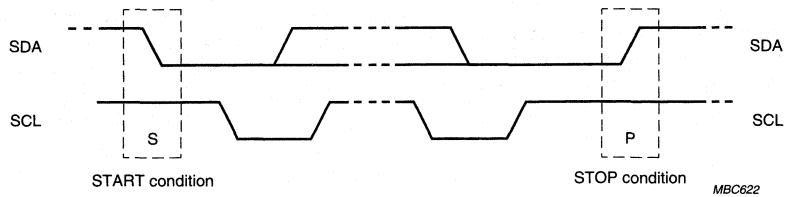


Fig.8 Definition of START and STOP condition.

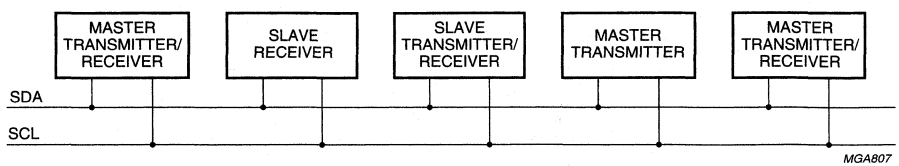
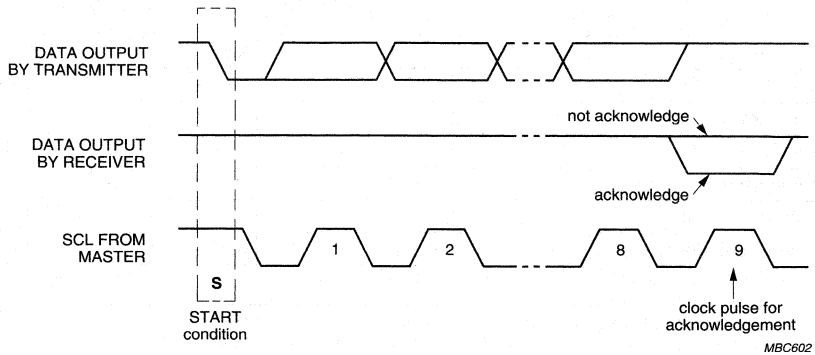


Fig.9 System configuration.



The general characteristics and detailed specification of the I²C-bus are available on request (order number 9398 393 40011).

Fig.10 Acknowledgment on the I²C-bus.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.5	+8.0	V
V_{LCD}	LCD supply voltage	V_{DD} − 11	V_{DD}	V
V_{i1}	input voltage T1, T3, SA0 and OSC	V_{SS} − 0.5	V_{DD} + 0.5	V
V_{i2}	input voltage SDA and SCL	V_{SS} − 0.5	8.0	V
V_{o1}	output voltage T2 and SDA	V_{SS} − 0.5	V_{DD} + 0.5	V
V_{o2}	output voltage R1 to R40 and C1 to C101	V_{LCD} − 0.5	V_{DD} + 0.5	V
I_I	DC input current	−10	+10	mA
I_O	DC output current	−10	+10	mA
I_{DD}, I_{SS}, I_{LCD}	V_{DD}, V_{SS} or V_{LCD} current	−50	+50	mA
P_{tot}	power dissipation per package	−	400	mW
P_o	power dissipation per output	−	100	mW
T_{stg}	storage temperature	−65	+150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe it is desirable to take normal precautions appropriate to handling MOS devices.

DC CHARACTERISTICS

V_{DD} = 2.5 to 6 V; V_{SS} = 0 V; V_{LCD} = V_{DD} − 3.5 V to V_{DD} − 9 V; T_{amb} = −40 to +85 °C; unless otherwise specified, note 1.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage		2.5	–	6.0	V
V_{LCD}	LCD supply voltage		V_{DD} − 9	–	V_{DD} − 3.5	V
$I_{DD(PD)}$	supply current in power-down mode		–	5	10	μA
I_{DD1}	supply current external clock		–	120	180	μA
I_{DD2}	supply current internal clock		–	130	200	μA
I_{LCD}	LCD input current		–	50	100	μA
V_{POR}	power-on reset level	note 2	0.6	1.3	1.8	V
Logic						
V_{IL1}	LOW level input voltage (all inputs except OSC)		V_{SS}	–	$0.3V_{DD}$	V
V_{IH1}	HIGH level input voltage (all inputs except OSC)		$0.7V_{DD}$	–	V_{DD}	V
V_{IL2}	LOW level input voltage (pin OSC)		V_{SS}	–	V_{DD} − 1.5	V
V_{IH2}	HIGH level input voltage (pin OSC)		V_{DD} − 0.1	–	V_{DD}	V
I_{L1}	leakage current at T1, T3 OSC and SA0	$V_I = V_{DD}$ or V_{SS}	−1	–	+1	mA
C_{I1}	input capacitance at T1, T3 OSC and SA0	note 3	–	–	5	pF
LCD outputs						
V_{DC}	DC component of LCD drivers R1 to R40 and C1 to C101		–	±20	–	mV
R_{ROW}	output resistance R1 to R40	note 4	–	1.5	6	kΩ
R_{COL}	output resistance C1 to C101	note 4	–	3	10	kΩ
I²C-bus; SDA and SCL						
V_{IL3}	LOW level input voltage	note 5	V_{SS}	–	$0.3V_{DD}$	V
V_{IH3}	HIGH level input voltage	note 5	$0.7V_{DD}$	–	6	V
I_{L2}	leakage current	$V_I = V_{DD}$ or V_{SS}	−1	–	+1	mA
C_{I2}	input capacitance	note 3	–	–	7	pF
I_{OL}	LOW level output current at SDA	V_{OL} = 0.4 V; V_{DD} = 5 V	3.0	–	–	mA

Notes

1. Outputs are open-circuit; inputs at V_{DD} or V_{SS}; I²C-bus inactive; external clock with 50% duty factor.
2. Resets all logic when $V_{DD} < V_{POR}$.
3. Periodically sampled, not 100% tested.
4. Resistance of output terminals (R1 to R40 and C1 to C101) with I_L = 20 μA; $V_{OP} = V_{DD} - V_{LCD}$ = 9 V; outputs measured one at a time.
5. When the voltages are above or below the supply voltages V_{DD} or V_{SS}, an input current may flow. This current must not exceed ±0.5 mA.

AC CHARACTERISTICS

All timing values are referenced to V_{IH} and V_{IL} levels with an input voltage swing of V_{SS} to V_{DD}. V_{DD} = 2.5 to 6 V; V_{SS} = 0 V; V_{LCD} = V_{DD} − 3.5 V to V_{DD} − 9 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$f_{FR)}$	LCD frame frequency (internal oscillator)		37	62.5	94	Hz
$f_{OSC(ext)}$	external clock frequency		90	150	225	kHz
t_{PLCD}	driver delays	V_{DD} − V_{LCD} = 9 V; with test loads	–	–	100	µs
I²C-bus (see Fig.12)						
f_{SCL}	SCL clock frequency		–	–	400	kHz
t_{CLKL}	SCL LOW time		1.3	–	–	µs
t_{CLKH}	SCL HIGH time		0.6	–	–	µs
t_{BUF}	bus free time	between successive STOP and START conditions	1.3	–	–	µs
t_r	SCL and SDA rise time	note 1	–	–	300	ns
t_f	SCL and SDA fall time	note 1	20 + 0.1C_b	–	300	ns
$t_{SU;STA}$	START condition set-up time	repeated start codes only	0.6	–	–	µs
$t_{HD;STA}$	START condition hold time		0.6	–	–	µs
$t_{SU;DAT}$	data set-up time		100	–	–	ns
$t_{HD;DAT}$	data hold time		0	–	–	ns
$t_{SU;STO}$	STOP condition set-up time		0.6	–	–	µs
t_{SW}	tolerable spike width on bus	note 2	–	–	50	ns
C_b	capacitive load per bus line		–	–	400	pF

Notes

1. The rise and fall times specified here refer to the driver device (i.e. not PCF8558) and are part of the general fast I²C-bus specification. However, when PCF8558 asserts an acknowledge on SDA, the fall time is given by parameter t_f. C_b = capacitive load per bus line.
2. The device inputs SDA and SCL are filtered and will reject spikes on the bus lines of width $<t_{SW(max)}$.

Fig.11 AC test loads.

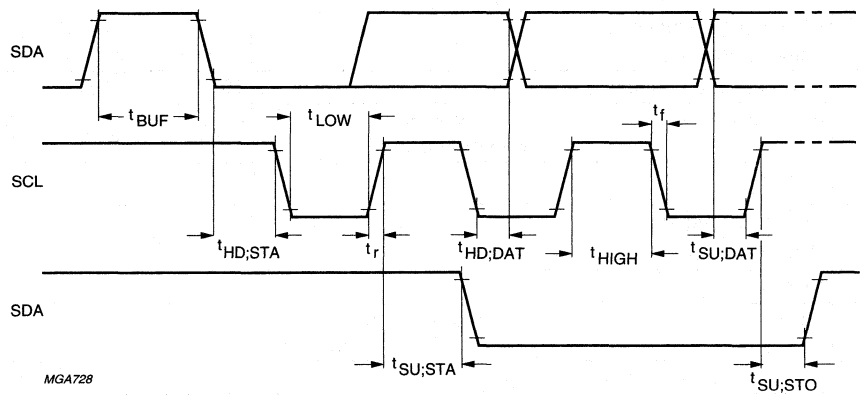


Fig.12 I²C-bus timing waveforms.

APPLICATION INFORMATION

The pinning of the PCF8558 is optimized for single plane wiring e.g. for Chip-on-glass display modules.

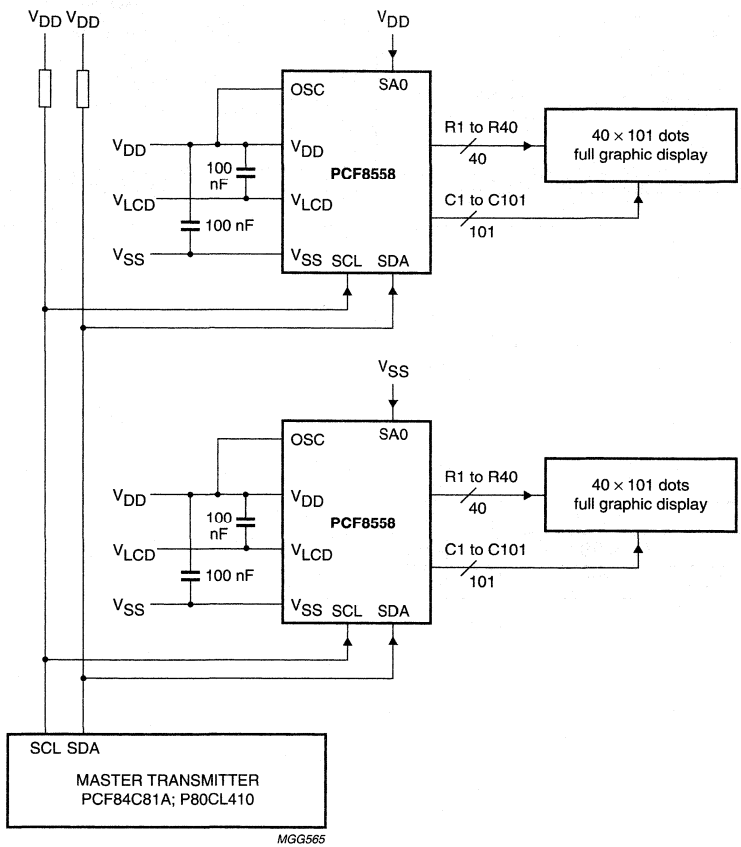


Fig.13 Application using I²C-bus interface.

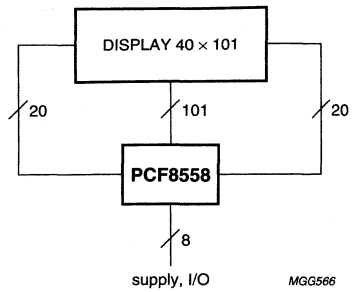


Fig.14 Application, display size 40 × 101 pixels.

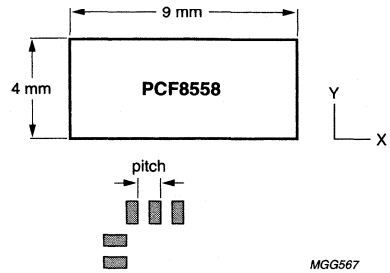


Fig.15 Bonding pads.

CHIP INFORMATION

The PCF8558 is manufactured in p-well CMOS technology. $V_{DD} - V_{LCD}$ is positive. The chip substrate is connected to V_{DD}.

Bonding pads

Pad pitch	100	μm
Pad size, aluminium	80 × 120	μm
Bump dimensions	59 × 99 × 15	μm
Wafer thickness	381	μm

BONDING PAD LOCATIONS

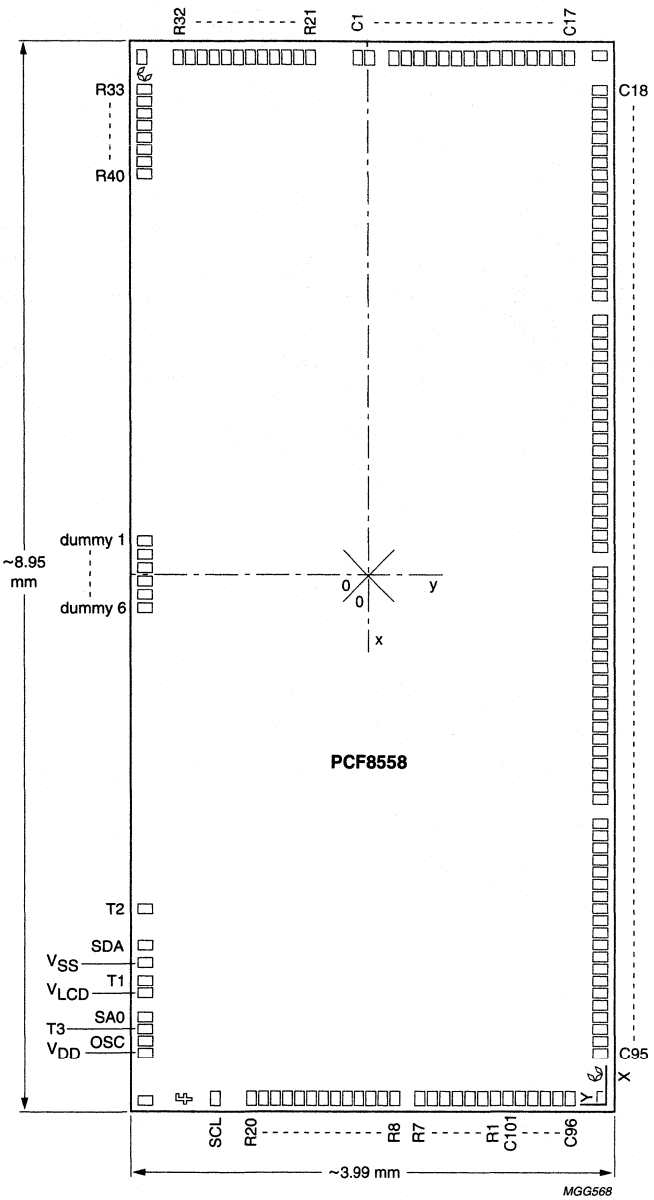


Fig.16 Bonding pad locations.

Table 5 Bonding pad locations (dimensions in μm). All x/y coordinates are referenced to the centre of the chip, see Fig.16.

SYMBOL	PAD	x	y
SCL	1	−4303.6	1280.0
R20	2	−4303.6	1005.8
R19	3	−4303.6	905.8
R18	4	−4303.6	805.8
R17	5	−4303.6	705.8
R16	6	−4303.6	605.8
R15	7	−4303.6	505.8
R14	8	−4303.6	405.8
R13	9	−4303.6	305.8
R12	10	−4303.6	205.8
R11	11	−4303.6	105.8
R10	12	−4303.6	5.8
R9	13	−4303.6	−94.3
R8	14	−4303.6	−194.3
R7	15	−4303.6	−383.3
R6	16	−4303.6	−483.3
R5	17	−4303.6	−583.3
R4	18	−4303.6	−683.3
R3	19	−4303.6	−783.3
R2	20	−4303.6	−883.3
R1	21	−4303.6	−983.3
C101	22	−4303.6	−1083.3
C100	23	−4303.6	−1183.3
C99	24	−4303.6	−1283.3
C98	25	−4303.6	−1383.3
C97	26	−4303.6	−1483.3
C96	27	−4303.6	−1583.3
C95	28	−3903.6	−1823.5
C94	29	−3803.6	−1823.5
C93	30	−3703.6	−1823.5
C92	31	−3603.6	−1823.5
C91	32	−3503.6	−1823.5
C90	33	−3403.6	−1823.5
C89	34	−3303.6	−1823.5
C88	35	−3203.6	−1823.5
C87	36	−3103.6	−1823.5
C86	37	−3003.6	−1823.5
C85	38	−2903.6	−1823.5
C84	39	−2803.6	−1823.5
C83	40	−2703.6	−1823.5
C82	41	−2603.6	−1823.5

SYMBOL	PAD	x	y
C81	42	−2503.6	−1823.5
C80	43	−2403.6	−1823.5
C79	44	−2303.6	−1823.5
C78	45	−2203.6	−1823.5
C77	46	−2103.6	−1823.5
C76	47	−2003.6	−1823.5
C75	48	−1814.6	−1823.5
C74	49	−1714.6	−1823.5
C73	50	−1614.6	−1823.5
C72	51	−1514.6	−1823.5
C71	52	−1414.6	−1823.5
C70	53	−1314.6	−1823.5
C69	54	−1214.6	−1823.5
C68	55	−1114.6	−1823.5
C67	56	−1014.6	−1823.5
C66	57	−914.6	−1823.5
C65	58	−814.6	−1823.5
C64	59	−714.6	−1823.5
C63	60	−614.6	−1823.5
C62	61	−514.6	−1823.5
C61	62	−414.6	−1823.5
C60	63	−314.6	−1823.5
C59	64	−214.6	−1823.5
C58	65	−114.6	−1823.5
C57	66	−14.6	−1823.5
C56	67	85.4	−1823.5
C55	68	274.4	−1823.5
C54	69	374.4	−1823.5
C53	70	474.4	−1823.5
C52	71	574.4	−1823.5
C51	72	674.4	−1823.5
C50	73	774.4	−1823.5
C49	74	874.4	−1823.5
C48	75	974.4	−1823.5
C47	76	1074.4	−1823.5
C46	77	1174.4	−1823.5
C45	78	1274.4	−1823.5
C44	79	1374.4	−1823.5
C43	80	1474.4	−1823.5
C42	81	1574.4	−1823.5
C41	82	1674.4	−1823.5

SYMBOL	PAD	x	y
C40	83	1774.4	−1823.5
C39	84	1874.4	−1823.5
C38	85	1974.4	−1823.5
C37	86	2074.4	−1823.5
C36	87	2174.4	−1823.5
C35	88	2363.4	−1823.5
C34	89	2463.4	−1823.5
C33	90	2563.4	−1823.5
C32	91	2663.4	−1823.5
C31	92	2763.4	−1823.5
C30	93	2863.4	−1823.5
C29	94	2963.4	−1823.5
C28	95	3063.4	−1823.5
C27	96	3163.4	−1823.5
C26	97	3263.4	−1823.5
C25	98	3363.4	−1823.5
C24	99	3463.4	−1823.5
C23	100	3563.4	−1823.5
C22	101	3663.4	−1823.5
C21	102	3763.4	−1823.5
C20	103	3863.4	−1823.5
C19	104	3963.4	−1823.5
C18	105	4063.4	−1823.5
C17	106	4303.6	−1583
C16	107	4303.6	−1483
C15	108	4303.6	−1383
C14	109	4303.6	−1283
C13	110	4303.6	−1183
C12	111	4303.6	−1083
C11	112	4303.6	−983
C10	113	4303.6	−883
C9	114	4303.6	−783
C8	115	4303.6	−683
C7	116	4303.6	−583
C6	117	4303.6	−483
C5	118	4303.6	−383
C4	119	4303.6	−283
C3	120	4303.6	−183
C2	121	4303.6	5.8
C1	122	4303.6	105.8
R21	123	4303.6	483
R22	124	4303.6	583
R23	125	4303.6	683
R24	126	4303.6	783

SYMBOL	PAD	x	y
R25	127	4303.6	883
R26	128	4303.6	983
R27	129	4303.6	1083
R28	130	4303.6	1183
R29	131	4303.6	1283
R30	132	4303.6	1383
R31	133	4303.6	1483
R32	134	4303.6	1583
R33	135	4017.1	1823.5
R34	136	3917.1	1823.5
R35	137	3817.1	1823.5
R36	138	3717.1	1823.5
R37	139	3617.1	1823.5
R38	140	3517.1	1823.5
R39	141	3417.1	1823.5
R40	142	3317.1	1823.5
T2	143	−2695.6	1823.5
SDA	144	−3044.1	1823.5
V_{SS}	145	−3190.6	1823.5
T1	146	−3362.1	1823.5
V_{LCD}	147	−3463.6	1823.5
SA0	148	−3635.1	1823.5
T3	149	−3735.1	1823.5
OSC	150	−3839.1	1823.5
V_{DD}	151	−3939.6	1823.5
Dummy pads			
dummy 1	–	−257.1	1790.4
dummy 2	–	−155.6	1790.4
dummy 3	–	−54.1	1790.4
dummy 4	–	47.4	1790.4
dummy 5	–	148.9	1790.4
dummy 6	–	250.4	1790.4
dummy 7	–	−4223.6	1823.4
dummy 8	–	4303.5	1843.5
dummy 9	–	−4303.6	−1843.5
dummy 10	–	4323.6	−1843.5
Alignment marks			
Sign C	–	−4082.6	−1782.5
Sign C	–	4147.4	1807.5
Sign F	–	−4262.6	1417.5

PCF8563

Real-time clock/calendar

16 April 1999 **Product specification**

1. General description

The PCF8563 is a CMOS real-time clock/calendar optimized for low power consumption. A programmable clock output, interrupt output and voltage-low detector are also provided. All address and data are transferred serially via a two-line bidirectional I²C-bus. Maximum bus speed is 400 kbits/s. The built-in word address register is incremented automatically after each written or read data byte.

2. Features

- Provides year, month, day, weekday, hours, minutes and seconds based on 32.768 kHz quartz crystal
- Century flag
- Wide operating supply voltage range: 1.0 to 5.5 V
- Low back-up current; typical 0.25 μA at V_{DD} = 3.0 V and T_{amb} = 25 °C
- 400 kHz two-wire I²C-bus interface (at V_{DD} = 1.8 to 5.5 V)
- Programmable clock output for peripheral devices: 32.768 kHz, 1024 Hz, 32 Hz and 1 Hz
- Alarm and timer functions
- Voltage-low detector
- Integrated oscillator capacitor
- Internal power-on reset
- I²C-bus slave address: read A3H; write A2H
- Open drain interrupt pin.

3. Applications

- Mobile telephones
- Portable instruments
- Fax machines
- Battery powered products.

4. Quick reference data

Table 1: Quick reference data

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage operating mode	I^2C-bus inactive; T_{amb} = 25 °C	1.0	5.5	V
		I^2C-bus active; f_{SCL} = 400 kHz; T_{amb} = −40 to +85 °C	1.8	5.5	V
I_{DD}	supply current; timer and CLKOUT disabled	f_{SCL} = 400 kHz	-	800	µA
		f_{SCL} = 100 kHz	-	200	µA
		f_{SCL} = 0 Hz; T_{amb} = 25 °C			
		V_{DD} = 5 V	-	550	nA
		V_{DD} = 2 V	-	450	nA
T_{amb}	operating ambient temperature		−40	+85	°C
T_{stg}	storage temperature		−65	+150	°C

5. Ordering information

Table 2: Ordering information

Type number	Package		
	Name	Description	Version
PCF8563P	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1
PCF8563T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1
PCF8563TS	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3.0 mm	SOT505-1

6. Block diagram

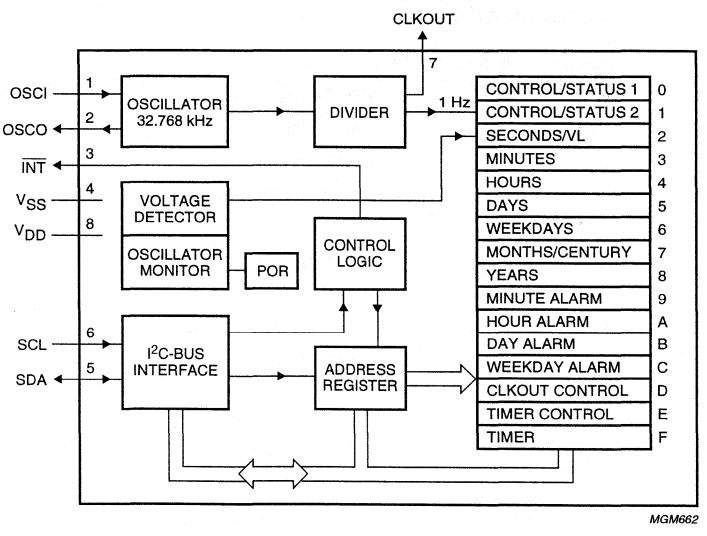


Fig 1. Block diagram.

7. Pinning information

7.1 Pinning

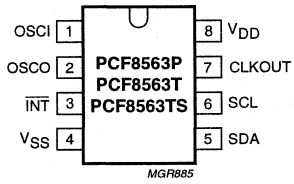


Fig 2. Pin configuration.

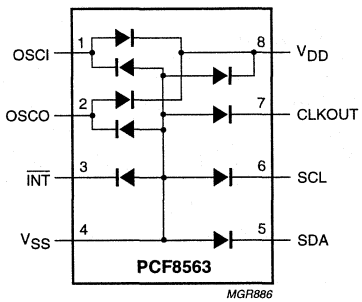


Fig 3. Device diode protection diagram.

7.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
OSCI	1	oscillator input
OSCO	2	oscillator output
$\overline{INT}$	3	interrupt output (open-drain; active LOW)
V_{SS}	4	ground
SDA	5	serial data I/O
SCL	6	serial clock input
CLKOUT	7	clock output (open-drain)
V_{DD}	8	positive supply

8. Functional description

The PCF8563 contains sixteen 8-bit registers with an auto-incrementing address register, an on-chip 32.768 kHz oscillator with an integrated capacitor, a frequency divider which provides the source clock for the Real-Time Clock (RTC), a programmable clock output, a timer, an alarm, a voltage-low detector and a 400 kHz I^2C-bus interface.

All 16 registers are designed as addressable 8-bit parallel registers although not all bits are implemented. The first two registers (memory address 00H and 01H) are used as control and/or status registers. The memory addresses 02H through 08H are used as counters for the clock function (seconds up to year counters). Address locations 09H through 0CH contain alarm registers which define the conditions for an alarm. Address 0DH controls the CLKOUT output frequency. 0EH and 0FH are the timer control and timer registers, respectively.

The Seconds, Minutes, Hours, Days, Months, Years as well as the Minute alarm, Hour alarm and Day alarm registers are all coded in BCD format. The Weekdays and Weekday alarm register are not coded in BCD format.

When one of the RTC registers is read the contents of all counters are frozen. Therefore, faulty reading of the clock/calendar during a carry condition is prevented.

8.1 Alarm function modes

By clearing the MSB (bit AE = Alarm Enable) of one or more of the alarm registers, the corresponding alarm condition(s) will be active. In this way an alarm can be generated from once per minute up to once per week. The alarm condition sets the alarm flag, AF (bit 3 of Control/Status 2 register). The asserted AF can be used to generate an interrupt ($\overline{INT}$). Bit AF can only be cleared by software.

8.2 Timer

The 8-bit countdown timer (address 0FH) is controlled by the Timer Control register (address 0EH; see Table 25). The Timer Control register selects one of 4 source clock frequencies for the timer (4096, 64, 1, or $1/60$ Hz), and enables/disables the timer. The timer counts down from a software-loaded 8-bit binary value. At the end of every countdown, the timer sets the timer flag TF (see Table 7). The timer flag TF can only be cleared by software. The asserted timer flag TF can be used to generate an interrupt ($\overline{INT}$). The interrupt may be generated as a pulsed signal every countdown period or as a permanently active signal which follows the condition of TF. TI/TP (see Table 7) is used to control this mode selection. When reading the timer, the current countdown value is returned.

8.3 CLKOUT output

A programmable square wave is available at the CLKOUT pin. Operation is controlled by the CLKOUT frequency register (address 0DH; see Table 23). Frequencies of 32.768 kHz (default), 1024, 32 and 1 Hz can be generated for use as a system clock, microcontroller clock, input to a charge pump, or for calibration of the oscillator. CLKOUT is an open-drain output and enabled at power-on. If disabled it becomes high-impedance.

8.4 Reset

The PCF8563 includes an internal reset circuit which is active whenever the oscillator is stopped. In the reset state the I^2C-bus logic is initialized and all registers, including the address pointer, are cleared with the exception of bits FE, VL, TD1, TD0, TESTC and AE which are set to logic 1.

8.5 Voltage-low detector and clock monitor

The PCF8563 has an on-chip voltage-low detector. When V_{DD} drops below V_{low} the VL bit (Voltage Low, bit 7 in the Seconds register) is set to indicate that reliable clock/calendar information is no longer guaranteed. The VL flag can only be cleared by software.

The VL bit is intended to detect the situation when V_{DD} is decreasing slowly for example under battery operation. Should V_{DD} reach V_{low} before power is re-asserted then the VL bit will be set. This will indicate that the time may be corrupted.

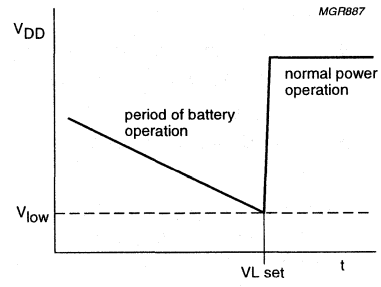


Fig 4. Voltage-low detection.

8.6 Register organization

Table 4: Registers overview

Bit positions labelled as '–' are not implemented; those labelled with '0' should always be written with logic 0.

Address	Register name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00H	Control/Status 1	TEST1	0	STOP	0	TESTC	0	0	0
01H	Control/Status 2	0	0	0	TI/TP	AF	TF	AIE	TIE
0DH	CLKOUT frequency	FE	–	–	–	–	–	FD1	FD0
0EH	Timer control	TE	–	–	–	–	–	TD1	TD0
0FH	Timer countdown value	<timer countdown value>							

Table 5: BCD formatted registers overview
Bit positions labelled as '–' are not implemented.

Address	Register name	BCD format tens nibble				BCD format units nibble			
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		2^3	2^2	2^1	2^0	2^3	2^2	2^1	2^0
02H	Seconds	VL	<seconds 00 to 59 coded in BCD>						
03H	Minutes	–	<minutes 00 to 59 coded in BCD>						
04H	Hours	–	–	<hours 00 to 23 coded in BCD>					
05H	Days	–	–	<days 01 to 31 coded in BCD>					
06H	Weekdays	–	–	–	–	–	<weekdays 0 to 6 > [1]		
07H	Months/Century	C	–	–	<months 01 to 12 coded in BCD>				
08H	Years	<years 00 to 99 coded in BCD>							
09H	Minute alarm	AE	<minute alarm 00 to 59 coded in BCD>						
0AH	Hour alarm	AE	–	<hour alarm 00 to 23 coded in BCD>					
0BH	Day alarm	AE	–	<day alarm 01 to 31 coded in BCD>					
0CH	Weekday alarm	AE	–	–	–	–	<weekday alarm 0 to 6 > [1]		

[1] Not coded in BCD.

8.6.1 Control/Status 1 register

Table 6: Control/Status 1 register bits description (address 00H)

Bit	Symbol	Description
7	TEST1	TEST1 = 0; normal mode. TEST1 = 1; EXT_CLK test mode; see Section 8.7.
5	STOP	STOP = 0; RTC source clock runs. STOP = 1; all RTC divider chain flip-flops are asynchronously set to logic 0; the RTC clock is stopped (CLKOUT at 32.768 kHz is still available).
3	TESTC	TESTC = 0; power-on reset override facility is disabled (set to logic 0 for normal operation). TESTC = 1; power-on reset override is enabled.
6, 4, 2 to 0	0	By default set to logic 0.

8.6.2 Control/Status 2 register

Table 7: Description of Control/Status 2 register bits description (address 01H)

Bit	Symbol	Description
7 to 5	0	By default set to logic 0.
4	TI/TP	TI/TP = 0: INT is active when TF is active (subject to the status of TIE). TI/TP = 1: INT pulses active according to Table 8 (subject to the status of TIE). Note that if AF and AIE are active then INT will be permanently active.
3	AF	When an alarm occurs, AF is set to logic 1. Similarly, at the end of a timer countdown, TF is set to logic 1. These bits maintain their value until overwritten by software. If both timer and alarm interrupts are required in the application, the source of the interrupt can be determined by reading these bits. To prevent one flag being overwritten while clearing another, a logic AND is performed during a write access. See Table 9 for the value descriptions of bits AF and TF.
2	TF	
1	AIE	Bits AIE and TIE activate or deactivate the generation of an interrupt when AF or TF is asserted, respectively. The interrupt is the logical OR of these two conditions when both AIE and TIE are set. AIE = 0: alarm interrupt disabled; AIE = 1: alarm interrupt enabled. TIE = 0: timer interrupt disabled; TIE = 1: timer interrupt enabled.
0	TIE	

Table 8: $\overline{INT}$ operation (bit TI/TP = 1)

Source clock (Hz)	$\overline{INT}$ [1] period (s)	
	n [2] = 1	n > 1
4 096	$1/8192$	$1/4096$
64	$1/128$	$1/64$
1	$1/64$	$1/64$
$1/60$	$1/64$	$1/64$

[1] TF and $\overline{INT}$ become active simultaneously.

[2] n = loaded countdown timer value. Timer stopped when n = 0.

Table 9: Value descriptions for bits AF and TF

R/W	Bit: AF		Bit: TF	
	Value	Description	Value	Description
Read	0	alarm flag inactive	0	timer flag inactive
	1	alarm flag active	1	timer flag active
Write	0	alarm flag is cleared	0	timer flag is cleared
	1	alarm flag remains unchanged	1	timer flag remains unchanged

8.6.3 Seconds, Minutes and Hours registers

Table 10: Seconds/VL register bits description (address 02H)

Bit	Symbol	Description
7	VL	VL = 0: reliable clock/calendar information is guaranteed; VL = 1: reliable clock/calendar information is no longer guaranteed.
6 to 0	<seconds>	These bits represent the current seconds value coded in BCD format; value = 00 to 59. Example: <seconds> = 101 1001, represents the value 59 s.

Table 11: Minutes register bits description (address 03H)

Bit	Symbol	Description
7	–	not implemented
6 to 0	<minutes>	These bits represent the current minutes value coded in BCD format; value = 00 to 59.

Table 12: Hours register bits description (address 04H)

Bit	Symbol	Description
7 to 6	–	not implemented
5 to 0	<hours>	These bits represent the current hours value coded in BCD format; value = 00 to 23.

8.6.4 Days, Weekdays, Months/Century and Years registers

Table 13: Days register bits description (address 05H)

Bit	Symbol	Description
7 to 6	–	not implemented
5 to 0	<days>	These bits represent the current day value coded in BCD format; value = 01 to 31. The PCF8563 compensates for leap years by adding a 29th day to February if the year counter contains a value which is exactly divisible by 4, including the year '00'.

Table 14: Weekdays register bits description (address 06H)

Bit	Symbol	Description
7 to 3	–	not implemented
2 to 0	<weekdays>	These bits represent the current weekday value 0 to 6; see Table 15. These bits may be re-assigned by the user.

Table 15: Weekday assignments

Day	Bit 2	Bit 1	Bit 0
Sunday	0	0	0
Monday	0	0	1
Tuesday	0	1	0
Wednesday	0	1	1
Thursday	1	0	0
Friday	1	0	1
Saturday	1	1	0

Table 16: Months/Century register bits description (address 07H)

Bit	Symbol	Description
7	C	Century bit. C = 0; indicates the century is 20xx. C = 1; indicates the century is 19xx. 'xx' indicates the value held in the Years register; see Table 18. This bit is toggled when the Years register overflows from 99 to 00.
6 to 5	–	These bits may be re-assigned by the user. not implemented
4 to 0	<months>	These bits represents the current month value coded in BCD format; value = 01 to 12; see Table 17.

Table 17: Month assignments

Month	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
January	0	0	0	0	1
February	0	0	0	1	0
March	0	0	0	1	1
April	0	0	1	0	0
May	0	0	1	0	1
June	0	0	1	1	0
July	0	0	1	1	1
August	0	1	0	0	0
September	0	1	0	0	1
October	1	0	0	0	0
November	1	0	0	0	1
December	1	0	0	1	0

Table 18: Years register bits description (address 08H)

Bit	Symbol	Description
7 to 0	<years>	This register represents the current year value coded in BCD format; value = 00 to 99.

8.6.5 Alarm registers

When one or more of the alarm registers are loaded with a valid minute, hour, day or weekday and its corresponding AE (Alarm Enable) bit is a logic 0, then that information will be compared with the current minute, hour, day and weekday. When all enabled comparisons first match, the bit AF (Alarm Flag) is set.

AF will remain set until cleared by software. Once AF has been cleared it will only be set again when the time increments to match the alarm condition once more. Alarm registers which have their AE bit set at logic 1 will be ignored.

Table 19: Minute alarm register bits description (address 09H)

Bit	Symbol	Description
7	AE	AE = 0; minute alarm is enabled. AE = 1; minute alarm is disabled.
6 to 0	<minute alarm>	These bits represents the minute alarm information coded in BCD format; value = 00 to 59.

Table 20: Hour alarm register bits description (address 0AH)

Bit	Symbol	Description
7	AE	AE = 0; hour alarm is enabled. AE = 1; hour alarm is disabled.
6 to 0	<hour alarm>	These bits represents the hour alarm information coded in BCD format; value = 00 to 23.

Table 21: Day alarm register bits description (address 0BH)

Bit	Symbol	Description
7	AE	AE = 0; day alarm is enabled. AE = 1; day alarm is disabled.
6 to 0	<day alarm>	These bits represents the day alarm information coded in BCD format; value = 01 to 31.

Table 22: Weekday alarm register bits description (address 0CH)

Bit	Symbol	Description
7	AE	AE = 0; weekday alarm is enabled. AE = 1; weekday alarm is disabled.
6 to 0	<weekday alarm>	These bits represents the weekday alarm information value 0 to 6.

8.6.6 CLKOUT frequency register

Table 23: CLKOUT frequency register bits description (address 0DH)

Bit	Symbol	Description
7	FE	FE = 0; the CLKOUT output is inhibited and the CLKOUT output is set to high-impedance. FE = 1; the CLKOUT output is activated.
6 to 2	–	not implemented
1	FD1	These bits control the frequency output (f_{CLKOUT}) on the CLKOUT pin; see Table 24.
0	FD0	

Table 24: CLKOUT frequency selection

FD1	FD0	f_{CLKOUT}
0	0	32.768 kHz
0	1	1 024 Hz
1	0	32 Hz
1	1	1 Hz

8.6.7 Countdown timer registers

The Timer register is an 8-bit binary countdown timer. It is enabled and disabled via the Timer control register bit TE. The source clock for the timer is also selected by the Timer control register. Other timer properties, e.g. interrupt generation, are controlled via the Control/status 2 register. For accurate read back of the countdown value, the I^2C-bus clock SCL must be operating at a frequency of at least twice the selected timer clock.

Table 25: Timer control register bits description (address 0EH)

Bit	Symbol	Description
7	TE	TE = 0; timer is disabled. TE = 1; timer is enabled.
6 to 2	–	not implemented
1	TD1	Timer source clock frequency selection bits. These bits determine the source clock for the countdown timer, see Table 26. When not in use, TD1 and TD0 should be set to '11' ($1/60$ Hz) for power saving.
0	TD0	

Table 26: Timer source clock frequency selection

TD1	TD0	Timer source clock frequency (Hz)
0	0	4096
0	1	64
1	0	1
1	1	$1/60$

Table 27: Timer countdown value register bits description (address 0FH)

Bit	Symbol	Description
7 to 0	<timer countdown value>	This register holds the loaded countdown value 'n'.

$$\text{Countdown period} = \frac{n}{\text{Source clock frequency}}$$

8.7 EXT_CLK test mode

A test mode is available which allows for on-board testing. In this mode it is possible to set up test conditions and control the operation of the RTC.

The test mode is entered by setting bit TEST1 in the Control/Status1 register. The CLKOUT pin then becomes an input. The test mode replaces the internal 64 Hz signal with the signal that is applied to the CLKOUT pin. Every 64 positive edges applied to CLKOUT will then generate an increment of one second.

The signal applied to the CLKOUT pin should have a minimum pulse width of 300 ns and a minimum period of 1000 ns. The internal 64 Hz clock, now sourced from CLKOUT, is divided down to 1 Hz by a 2^6 divide chain called a pre-scaler. The pre-scaler can be set into a known state by using the STOP bit. When the STOP bit is set, the pre-scaler is reset to 0. STOP must be cleared before the pre-scaler can operate again. From a STOP condition, the first 1 s increment will take place after 32 positive edges on CLKOUT. Thereafter, every 64 positive edges will cause a 1 s increment.

Remark: Entry into EXT_CLK test mode is not synchronized to the internal 64 Hz clock. When entering the test mode, no assumption as to the state of the pre-scaler can be made.

8.7.1 Operation example

1. Enter the EXT_CLK test mode; set bit 7 of Control/Status 1 register (TEST = 1)
2. Set bit 5 of Control/Status 1 register (STOP = 1)
3. Clear bit 5 of Control/Status 1 register (STOP = 0)
4. Set time registers (Seconds, Minutes, Hours, Days, Weekdays, Months/Century and Years) to desired value
5. Apply 32 clock pulses to CLKOUT
6. Read time registers to see the first change
7. Apply 64 clock pulses to CLKOUT
8. Read time registers to see the second change.

Repeat steps 7 and 8 for additional increments.

8.8 Power-On Reset (POR) override mode

The POR duration is directly related to the crystal oscillator start-up time. Due to the long start-up times experienced by these types of circuits, a mechanism has been built in to disable the POR and hence speed up on-board test of the device. The setting of this mode requires that the I^2C-bus pins, SDA and SCL, be toggled in a specific order as shown in Figure 5. All timing values are required minimum.

Once the override mode has been entered, the chip immediately stops being reset and normal operation starts i.e. entry into the EXT_CLK test mode via I^2C-bus access. The override mode is cleared by writing a logic 0 to bit TESTC. Re-entry into the override mode is only possible after TESTC is set to logic 1. Setting TESTC to logic 0 during normal operation has no effect except to prevent entry into the POR override mode.

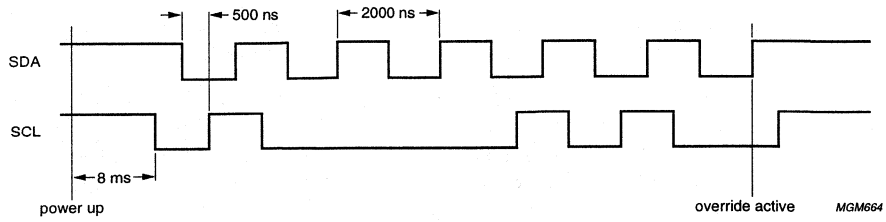


Fig 5. POR override sequence.

8.9 Serial interface

The serial interface of the PCF8563 is the I²C-bus. A detailed description of the I²C-bus specification, including applications, is given in the brochure: *The I²C-bus and how to use it*, order no. 9398 393 40011 or *I²C Peripherals Data Handbook IC12.*

8.9.1 Characteristics of the I²C-bus

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

The I²C-bus system configuration is shown in Figure 6. A device generating a message is a 'transmitter', a device receiving a message is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves'.

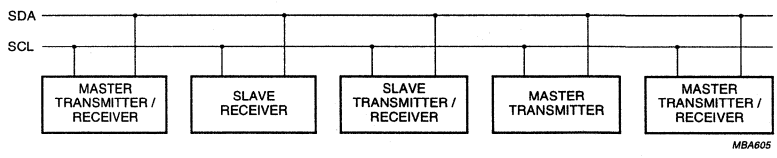


Fig 6. I²C-bus system configuration.

8.9.2 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P); see Figure 7.

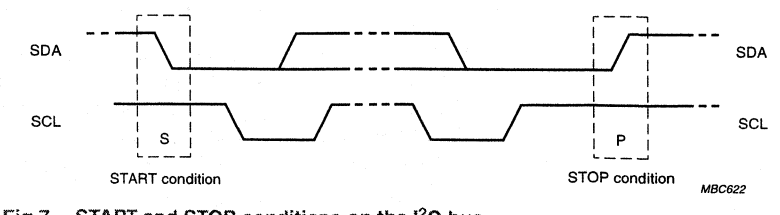


Fig 7. START and STOP conditions on the I²C-bus.

8.9.3 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal; see Figure 8.

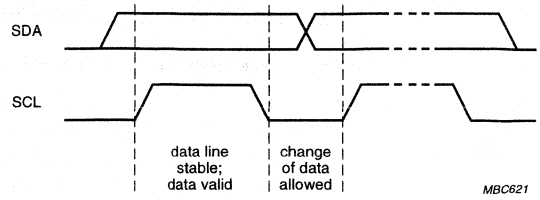


Fig 8. Bit transfer on the I²C-bus.

8.9.4 Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration).

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

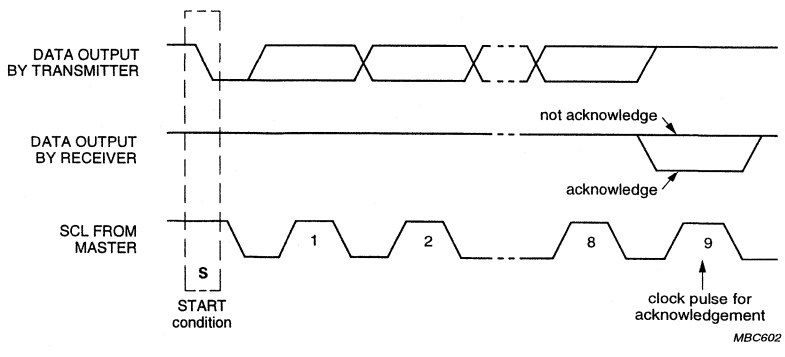


Fig 9. Acknowledge on the I²C-bus.

8.9.5 I²C-bus protocol

Addressing: Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always carried out with the first byte transmitted after the start procedure.

The PCF8563 acts as a slave receiver or slave transmitter. Therefore the clock signal SCL is only an input signal, but the data signal SDA is a bidirectional line.

The PCF8563 slave address is shown in Figure 10.

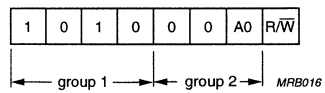


Fig 10. Slave address.

Clock/calendar read/write cycles: The I²C-bus configuration for the different PCF8563 read and write cycles are shown in Figure 11, 12 and 13. The word address is a four bit value that defines which register is to be accessed next. The upper four bits of the word address are not used.

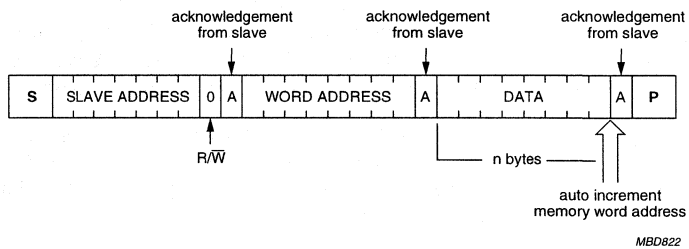


Fig 11. Master transmits to slave receiver (write mode).

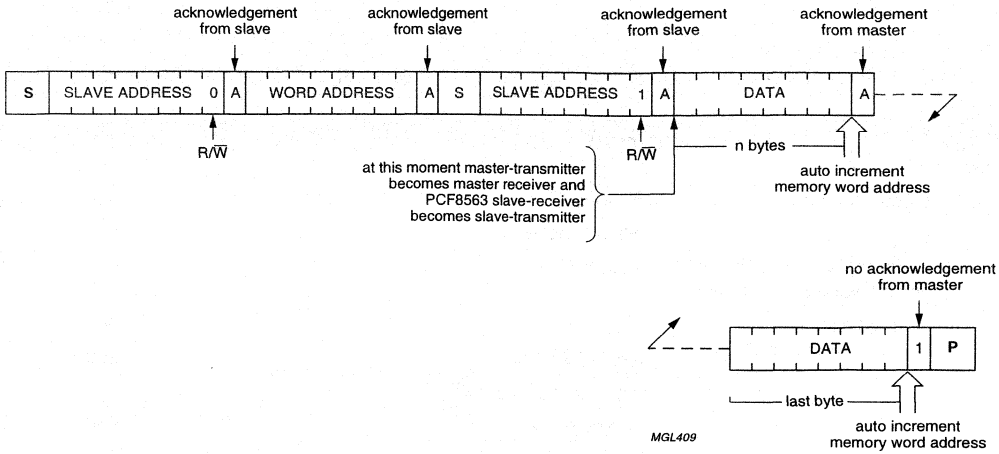


Fig 12. Master reads after setting word address (write word address; read data).

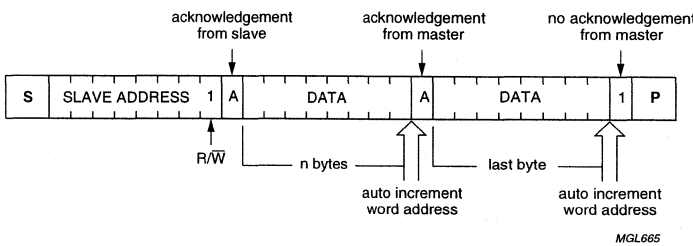


Fig 13. Master reads slave immediately after first byte (read mode).

9. Limiting values

Table 28: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		−0.5	+6.5	V
I_{DD}	supply current		−50	+50	mA
V_I	input voltage on inputs SCL and SDA		−0.5	6.5	V
	input voltage on input OSCI		−0.5	V_{DD} + 0.5	V
V_O	output voltage on outputs CLKOUT and $\overline{INT}$		−0.5	6.5	V
I_I	DC input current at any input		−10	+10	mA
I_O	DC output current at any output		−10	+10	mA
P_{tot}	total power dissipation		−	300	mW
T_{amb}	operating ambient temperature		−40	+85	°C
T_{stg}	storage temperature		−65	+150	°C

10. Static characteristics

Table 29: Static characteristics

V_{DD} = 1.8 to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 to 85 °C; f_{OSC} = 32.768 kHz; quartz R_s = 40 kΩ; C_L = 8 pF; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supplies							
V_{DD}	supply voltage	I²C-bus inactive; T_{amb} = 25 °C		1.0 [1]	–	5.5	V
		I²C-bus active; f_{SCL} = 400 kHz		1.8 [1]	–	5.5	V
	supply voltage for reliable clock/calendar information	T_{amb} = 25 °C		V_{low}	–	5.5	V
I_{DD1}	supply current; CLKOUT disabled (FE = 0)	f_{SCL} = 400 kHz	[2]	–	–	800	µA
		f_{SCL} = 100 kHz		–	–	200	µA
		f_{SCL} = 0 Hz; T_{amb} = 25 °C	[2]				
		V_{DD} = 5 V		–	275	550	nA
		V_{DD} = 3 V		–	250	500	nA
		V_{DD} = 2 V		–	225	450	nA
		f_{SCL} = 0 Hz	[2]				
		V_{DD} = 5 V		–	500	750	nA
		V_{DD} = 3 V		–	400	650	nA
		V_{DD} = 2 V		–	400	600	nA
I_{DD2}	supply current; CLKOUT enabled (f_{CLKOUT} = 32 kHz; FE = 1)	f_{SCL} = 0 Hz; T_{amb} = 25 °C	[2]				
		V_{DD} = 5 V		–	825	1600	nA
		V_{DD} = 3 V		–	550	1000	nA
		V_{DD} = 2 V		–	425	800	nA
		f_{SCL} = 0 Hz	[2]				
		V_{DD} = 5 V		–	950	1700	nA
		V_{DD} = 3 V		–	650	1100	nA
		V_{DD} = 2 V		–	500	900	nA
Inputs							
V_{IL}	LOW-level input voltage			V_{SS}	–	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	–	V_{DD}	V
I_{LI}	input leakage current	V_I = V_{DD} or V_{SS}		−1	–	+1	µA
C_i	input capacitance		[3]	–	–	7	pF
Outputs							
$I_{OL(SDA)}$	LOW-level output current; pin SDA	V_{OL} = 0.4 V; V_{DD} = 5 V		−3	–	–	mA
$I_{OL(\overline{INT})}$	LOW-level output current; pin $\overline{INT}$			−1	–	–	mA
$I_{OL(CLKOUT)}$	LOW-level output current; pin CLKOUT			−1	–	–	mA

Table 29: Static characteristics *...continued*

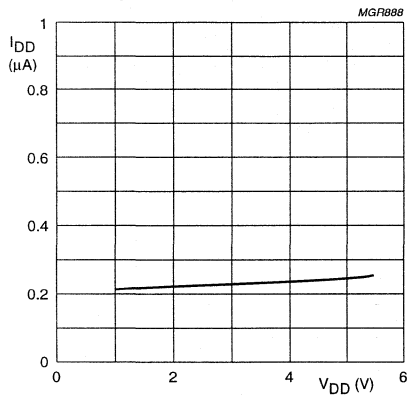
V_{DD} = 1.8 to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 to 85 °C; f_{OSC} = 32.768 kHz; quartz R_s = 40 kΩ; C_L = 8 pF; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{OH(CLKOUT)}$	HIGH-level output current; pin CLKOUT	V_{OH} = 4.6 V; V_{DD} = 5 V	1	–	–	mA
I_{LO}	output leakage current	$V_O = V_{DD}$ or V_{SS}	−1	–	+1	µA
Voltage detector						
V_{low}	voltage-low detection level	T_{amb} = 25 °C	–	0.9	1.0	V

[1] For reliable oscillator start-up at power-up: $V_{DD(min)power\text{-}up} = V_{DD(min)} + 0.3$ V.

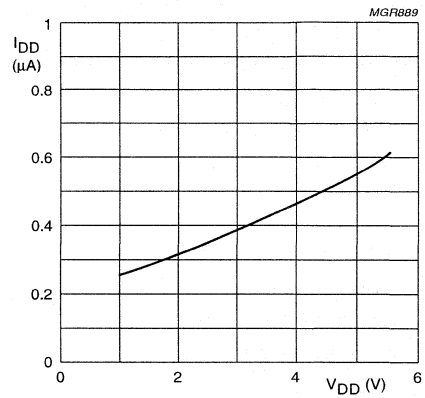
[2] Timer source clock = $1/60$ Hz; SCL and SDA = V_{DD}.

[3] Tested on sample basis.



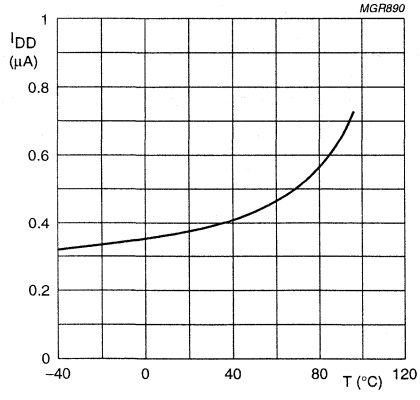
T_{amb} = 25 °C; Timer = 1 minute.

Fig 14. I_{DD} as a function of V_{DD}; CLKOUT disabled.



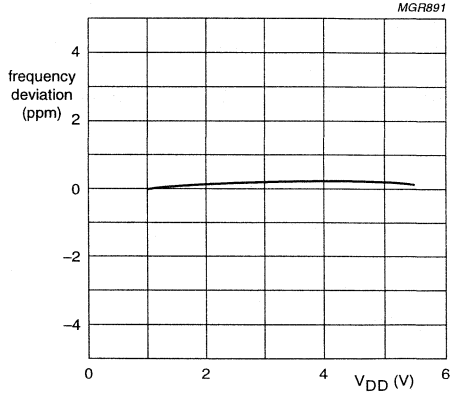
T_{amb} = 25 °C; Timer = 1 minute.

Fig 15. I_{DD} as a function of V_{DD}; CLKOUT = 32 kHz.



V_{DD} = 3 V; Timer = 1 minute.

Fig 16. I_{DD} as a function of T_{amb}; CLKOUT = 32 kHz.



T_{amb} = 25 °C; normalized to V_{DD} = 3 V.

Fig 17. Frequency deviation as function of V_{DD}.

11. Dynamic characteristics

Table 30: Dynamic characteristics

V_{DD} = 1.8 to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; f_{OSC} = 32.768 kHz; quartz R_s = 40 kΩ; C_L = 8 pF; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Oscillator							
$C_{L(integrated)}$	integrated load capacitance			15	25	35	pF
$\Delta f_{OSC}/f_{OSC}$	oscillator stability	ΔV_{DD} = 200 mV; T_{amb} = 25 °C		–	2×10^{-7}	–	
Quartz crystal parameters (f_{OSC} = 32.768 kHz)							
R_s	series resistance			–	–	40	kΩ
C_L	parallel load capacitance			–	10	–	pF
C_T	trimmer capacitance			5	–	25	pF
CLKOUT output							
δ_{CLKOUT}	CLKOUT duty factor		[1]	–	50	–	%
I^2C-bus timing characteristics [2]							
f_{SCL}	SCL clock frequency		[3]	–	–	400	kHz
$t_{HD;STA}$	START condition hold time			0.6	–	–	µs
$t_{SU;STA}$	set-up time for a repeated START condition			0.6	–	–	µs
t_{LOW}	SCL LOW time			1.3	–	–	µs
t_{HIGH}	SCL HIGH time			0.6	–	–	µs
t_r	SCL and SDA rise time			–	–	0.3	µs
t_f	SCL and SDA fall time			–	–	0.3	µs
C_b	capacitive bus line load			–	–	400	pF
$t_{SU;DAT}$	data set-up time			100	–	–	ns
$t_{HD;DAT}$	data hold time			0	–	–	ns
$t_{SU;STO}$	set-up time for STOP condition			4.0	–	–	µs
t_{SW}	tolerable spike width on bus			–	–	50	ns

[1] Unspecified for f_{CLKOUT} = 32.768 kHz.

[2] All timing values are valid within the operating supply voltage range at T_{amb} and referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

[3] I^2C-bus access time between two STARTs or between a START and a STOP condition to this device must be less than one second.

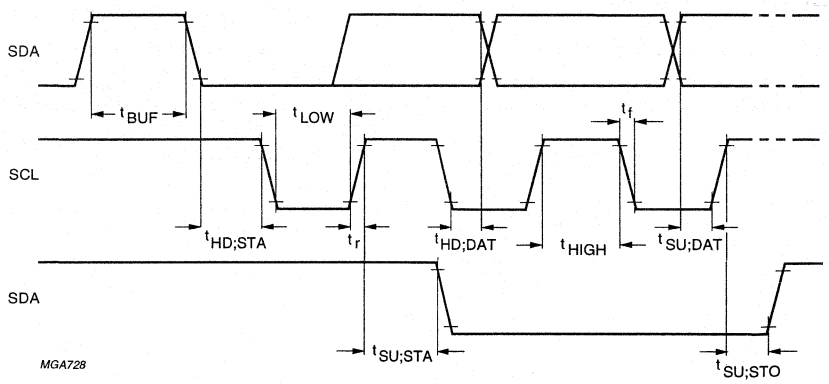


Fig 18. I²C-bus timing waveforms.

12. Application information

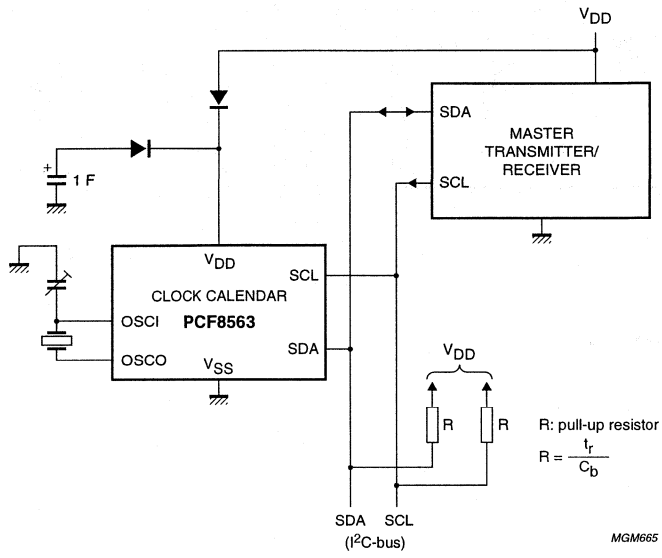


Fig 19. Application diagram.

12.1 Quartz crystal frequency adjustment

Method 1: Fixed OSCI capacitor — By evaluating the average capacitance necessary for the application layout a fixed capacitor can be used. The frequency is best measured via the 32.768 kHz signal available after power-on at the CLKOUT pin. The frequency tolerance depends on the quartz crystal tolerance, the capacitor tolerance and the device-to-device tolerance (on average $\pm 5 \times 10^{-6}$).

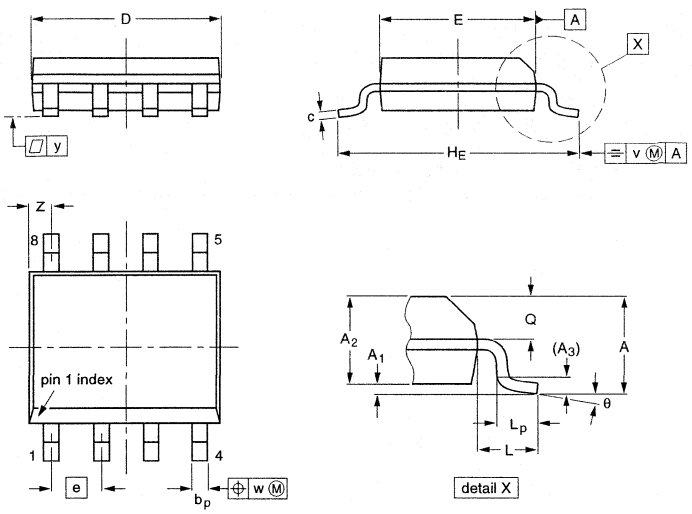
Average deviations of ±5 minutes per year can be easily achieved.

Method 2: OSCI trimmer — The oscillator is tuned to the required accuracy by adjusting a trimmer capacitor on pin OSCI and measuring the 32.768 kHz signal available after power-on at the CLKOUT pin.

Method 3: OSCO output — Direct output measurement on pin OSCO (accounting for test probe capacitance).

13. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

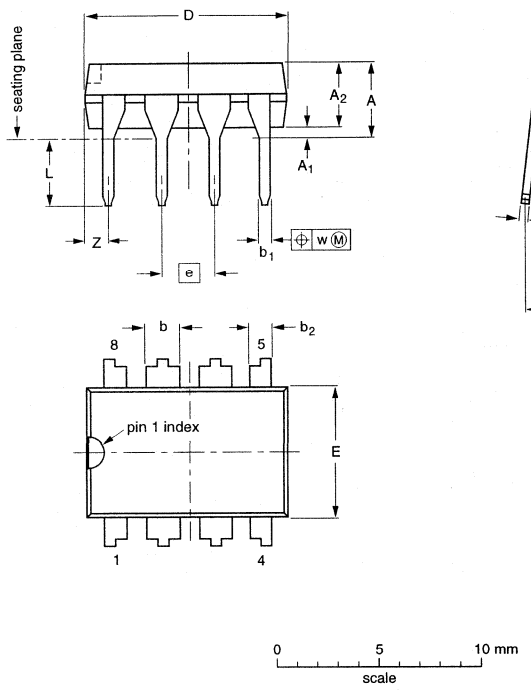
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03S	MS-012AA				~~95-02-04~~ 97-05-22

Fig 20. SOT96-1.

DIP8: plastic dual in-line package; 8 leads (300 mil) **SOT97-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	$D^{(1)}$	$E^{(1)}$	e	e_1	L	M_E	M_H	w	$Z^{(1)}$ max.
mm	4.2	0.51	3.2	1.73 1.14	0.53 0.38	1.07 0.89	0.36 0.23	9.8 9.2	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	1.15
inches	0.17	0.020	0.13	0.068 0.045	0.021 0.015	0.042 0.035	0.014 0.009	0.39 0.36	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.045

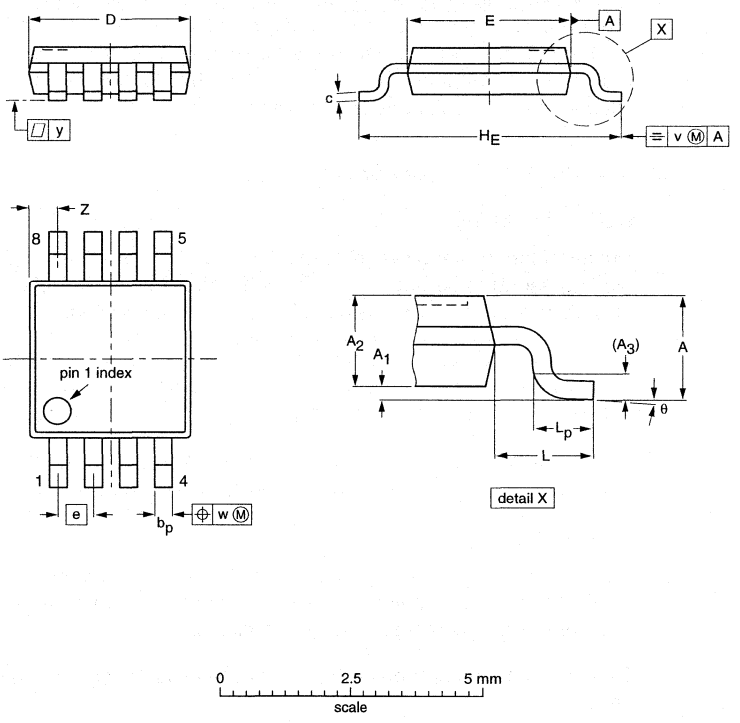
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT97-1	050G01	MO-001AN				~~92-11-17~~ 95-02-04

Fig 21. SOT97-1.

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm **SOT505-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.45 0.25	0.28 0.15	3.10 2.90	3.10 2.90	0.65	5.10 4.70	0.94	0.70 0.40	0.1	0.1	0.1	0.70 0.35	6° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT505-1						99-04-09

Fig 22. SOT505-1.

14. Soldering

14.1 Introduction

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mount components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

14.2 Surface mount packages

14.2.1 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

14.2.2 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C. A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

14.2.3 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

14.3 Through-hole mount packages

14.3.1 Soldering by dipping or by solder wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joints for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

14.3.2 Manual soldering

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

14.4 Package related soldering information

Table 31: Suitability of IC packages for wave, reflow and dipping soldering methods

Mounting	Package	Soldering method		
		Wave	Reflow [1]	Dipping
Through-hole mount	DBS, DIP, HDIP, SDIP, SIL	suitable [2]	–	suitable
Surface mount	BGA, SQFP	not suitable	suitable	–
	HLQFP, HSQFP, HSOP, HTSSOP, SMS	not suitable [3]	suitable	–
	PLCC [4], SO, SOJ	suitable	suitable	–
	LQFP, QFP, TQFP	not recommended [4] [5]	suitable	–
	SSOP, TSSOP, VSO	not recommended [6]	suitable	–

[1] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods.*

[2] For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.

[3] These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).

[4] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[5] Wave soldering is only suitable for LQFP, QFP and TQFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[6] Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

15. Revision history

Rev	Date	CPCN	Description
01	990416	-	**This data sheet supersedes the version of 1998 Mar 25 (9397 750 03282):** • The format of this specification has been redesigned to comply with Philips Semiconductors' new presentation and information standard • Added Figure 3 "Device diode protection diagram." on page 3 • Added Figure 4 "Voltage-low detection." on page 5 • Added paragraph in Section 8.5 "Voltage-low detector and clock monitor" on page 5 • Added Figure 14 to 17 on page 18 in Section 10.

16. Data sheet status

Datasheet status	Product status	Definition[1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued data sheet before initiating or completing a design.

17. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

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Malaysia: Tel. +60 37 50 5214, Fax. +60 37 57 4880
Mexico: Tel. +9-5 800 234 7381
Middle East: see Italy
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For all other countries apply to: Philips Semiconductors,
Marketing & Sales Communications,
Building BE, P.O. Box 218, 5600 MD EINDHOVEN,
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Contents

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Universal LCD driver for low multiplex rates

PCF8566

CONTENTS

Universal LCD driver for low multiplex rates PCF8566

1 FEATURES

- Single-chip LCD controller/driver
- Selectable backplane drive configuration: static or 2, 3 or 4 backplane multiplexing
- Selectable display bias configuration: static, ½ or ⅓
- Internal LCD bias generation with voltage-follower buffers
- 24 segment drives: up to twelve 8-segment numeric characters; up to six 15-segment alphanumeric characters; or any graphics of up to 96 elements
- 24 × 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- LCD and logic supplies may be separated
- 2.5 to 6 V power supply range
- Low power consumption
- Power saving mode for extremely low power consumption in battery-operated and telephone applications
- I²C-bus interface
- TTL/CMOS compatible
- Compatible with any 4-bit, 8-bit or 16-bit microprocessors/microcontrollers
- May be cascaded for large LCD applications (up to 1536 segments possible)
- Cascadable with the 40 segment LCD driver PCF8576C
- Optimized pinning for single plane wiring in both single and multiple PCF8566 applications
- Space-saving 40 lead plastic very small outline package (VSO40; SOT158-1)
- No external components required (even in multiple device applications)
- Manufactured in silicon gate CMOS process.

2 GENERAL DESCRIPTION

The PCF8566 is a peripheral device which interfaces to almost any Liquid Crystal Display (LCD) having low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 24 segments and can easily be cascaded for larger LCD applications. The PCF8566 is compatible with most microprocessors/microcontrollers and communicates via a two-line bidirectional I²C-bus. Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8566P	DIP40	plastic dual in-line package; 40 leads (600 mil)	SOT129-1
PCF8566T	VSO40	plastic very small outline package; 40 leads	SOT158-1

4 BLOCK DIAGRAM

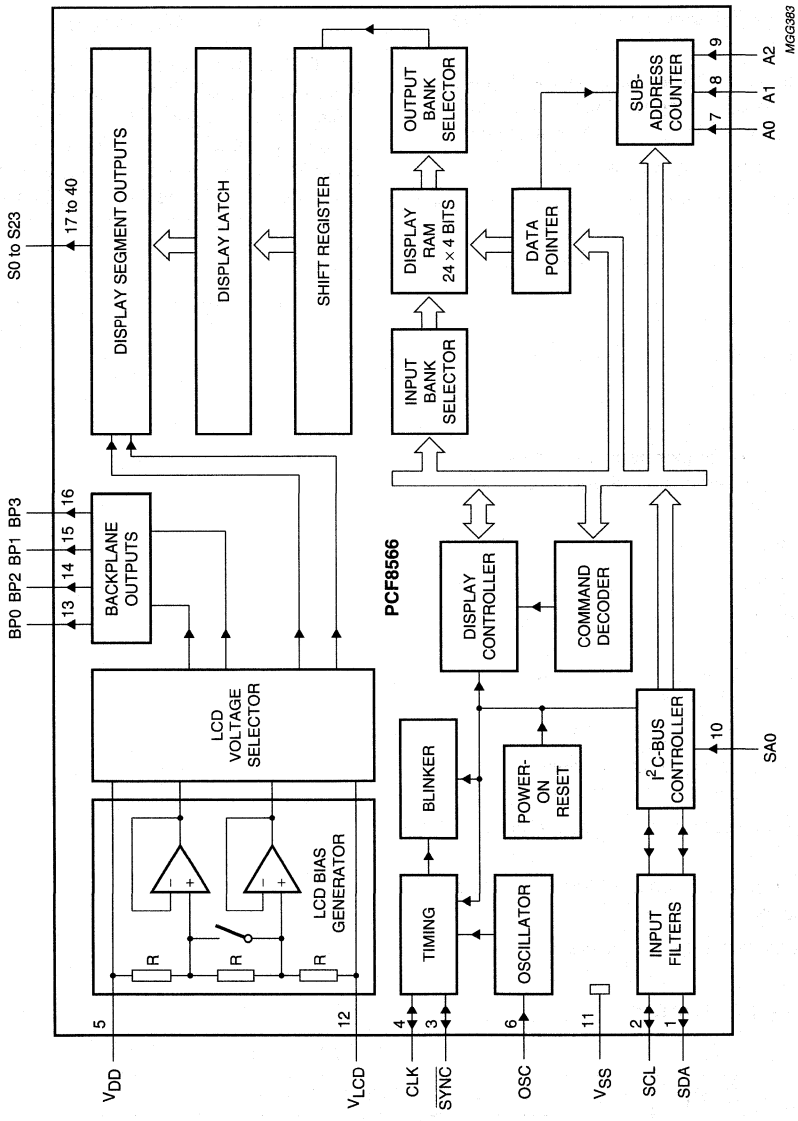


Fig.1 Block diagram.

5 PINNING

SYMBOL	PIN	DESCRIPTION
SDA	1	I²C-bus data input/output
SCL	2	I²C-bus clock input/output
$\overline{SYNC}$	3	cascade synchronization input/output
CLK	4	external clock input/output
V_{DD}	5	positive supply voltage
OSC	6	oscillator input
A0	7	I²C-bus subaddress inputs
A1	8	
A2	9	
SA0	10	I²C-bus slave address bit 0 input
V_{SS}	11	logic ground
V_{LCD}	12	LCD supply voltage
BP0	13	LCD backplane outputs
BP2	14	
BP1	15	
BP3	16	
S0 to S23	17 to 40	LCD segment outputs

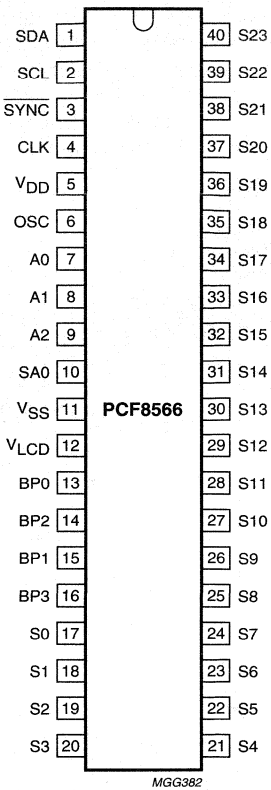


Fig.2 Pin configuration.

6 FUNCTIONAL DESCRIPTION

The PCF8566 is a versatile peripheral device designed to interface any microprocessor to a wide variety of LCDs. It can directly drive any static or multiplexed LCD containing up to 4 backplanes and up to 24 segments. The display configurations possible with the PCF8566 depend on the number of active backplane outputs required; a selection of display configurations is given in Table 1.

All of the display configurations given in Table 1 can be implemented in the typical system shown in Fig.3. The host microprocessor/microcontroller maintains the two-line I²C-bus communication channel with the PCF8566. The internal oscillator is selected by tying OSC (pin 6) to V_{SS}. The appropriate biasing voltages for the multiplexed LCD waveforms are generated internally. The only other connections required to complete the system are to the power supplies (V_{DD}, V_{SS} and V_{LCD}) and to the LCD panel chosen for the application.

Table 1 Selection of display configurations

ACTIVE BACKPLANE OUTPUTS	NUMBER OF SEGMENTS	7-SEGMENT NUMERIC	14-SEGMENT ALPHANUMERIC	DOT MATRIX
4	96	12 digits + 12 indicator symbols	6 characters + 12 indicator symbols	96 dots (4 × 24)
3	72	9 digits + 9 indicator symbols	4 characters + 16 indicator symbols	72 dots (3 × 24)
2	48	6 digits + 6 indicator symbols	3 characters + 6 indicator symbols	48 dots (2 × 24)
1	24	3 digits + 3 indicator symbols	1 character + 10 indicator symbols	24 dots

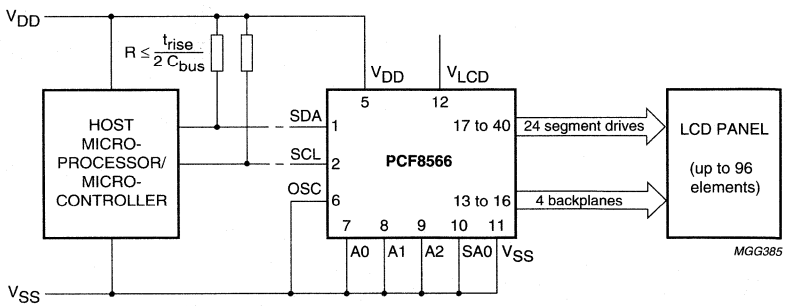


Fig.3 Typical system configuration.

6.1 Power-on reset

At power-on the PCF8566 resets to a defined starting condition as follows:

1. All backplane outputs are set to V_{DD}
2. All segment outputs are set to V_{DD}
3. The drive mode '1 : 4 multiplex with $\frac{1}{3}$bias' is selected
4. Blinking is switched off
5. Input and output bank selectors are reset (as defined in Table 5)
6. The I²C-bus interface is initialized
7. The data pointer and the subaddress counter are cleared.

Data transfers on the I²C-bus should be avoided for 1 ms following power-on to allow completion of the reset action.

6.2 LCD bias generator

The full-scale LCD voltage (V_{op}) is obtained from $V_{DD} - V_{LCD}$. The LCD voltage may be temperature compensated externally through the V_{LCD} supply to pin 12. Fractional LCD biasing voltages are obtained from an internal voltage divider of three series resistors connected between V_{DD} and V_{LCD}. The centre resistor can be switched out of circuit to provide a $\frac{1}{2}$bias voltage level for the 1 : 2 multiplex configuration.

6.3 LCD voltage selector

The LCD voltage selector coordinates the multiplexing of the LCD according to the selected LCD drive configuration. The operation of the voltage selector is controlled by MODE SET commands from the command decoder. The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of $V_{op} = V_{DD} - V_{LCD}$ and the resulting discrimination ratios (D), are given in Table 2.

A practical value of V_{op} is determined by equating $V_{off(rms)}$ with a defined LCD threshold voltage (V_{th}), typically when the LCD exhibits approximately 10% contrast. In the static drive mode a suitable choice is $V_{op} \geq 3\ V_{th}$. Multiplex drive ratios of 1 : 3 and 1 : 4 with $\frac{1}{2}$ bias are possible but the discrimination and hence the contrast ratios are smaller ($\sqrt{3} = 1.732$ for 1 : 3 multiplex or $\sqrt{21}/3 = 1.528$ for 1 : 4 multiplex). The advantage of these modes is a reduction of the LCD full scale voltage V_{op} as follows:

1 : 3 multiplex ($\frac{1}{2}$bias):

$$V_{op} = \sqrt{6}V_{op(mrs)} = 2.449V_{off(rms)}$$

1 : 4 multiplex ($\frac{1}{2}$bias):

$$V_{op} = \sqrt[4]{3}/3V_{off(rms)} = 2.309V_{off(rms)}$$

These compare with $V_{op} = 3\ V_{off(rms)}$ when $\frac{1}{3}$bias is used.

Table 2 Preferred LCD drive modes: summary of characteristics

LCD DRIVE MODE	LCD BIAS CONFIGURATION	$\frac{V_{off(rms)}}{V_{op}}$	$\frac{V_{on(rms)}}{V_{op}}$	$D = \frac{V_{on(rms)}}{V_{off(rms)}}$
Static (1 BP)	static (2 levels)	0	1	∞
1 : 2 MUX (2 BP)	$\frac{1}{2}$ (3 levels)	$\sqrt{2}/4 = 0.354$	$\sqrt{10}/4 = 0.791$	$\sqrt{5} = 2.236$
1 : 2 MUX (2 BP)	$\frac{1}{3}$ (4 levels)	$\frac{1}{3} = 0.333$	$\sqrt{5}/3 = 0.745$	$\sqrt{5} = 2.236$
1 : 3 MUX (3 BP)	$\frac{1}{3}$ (4 levels)	$\frac{1}{3} = 0.333$	$\sqrt{33}/9 = 0.638$	$\sqrt{33}/3 = 1.915$
1 : 4 MUX (4 BP)	$\frac{1}{3}$ (4 levels)	$\frac{1}{3} = 0.333$	$\sqrt{3}/3 = 0.577$	$\sqrt{3} = 1.732$

6.4 LCD drive mode waveforms

The static LCD drive mode is used when a single backplane is provided in the LCD. Backplane and segment drive waveforms for this mode are shown in Fig.4.

When two backplanes are provided in the LCD the 1 : 2 multiplex drive mode applies. The PCF8566 allows use of $\frac{1}{2}$ or $\frac{1}{3}$ bias in this mode as shown in Figs 5 and 6.

The backplane and segment drive waveforms for the 1 : 3 multiplex drive mode (three LCD backplanes) and for the 1 : 4 multiplex drive mode (four LCD backplanes) are shown in Figs 7 and 8 respectively.

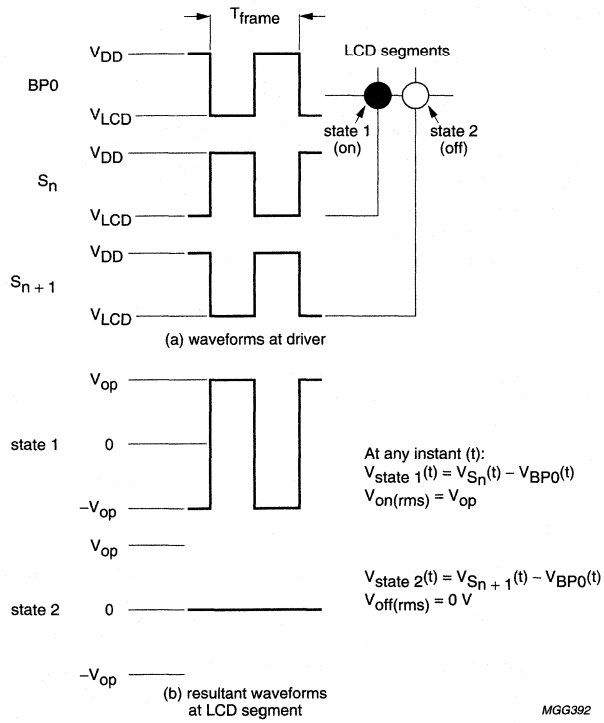


Fig.4 Static drive mode waveforms: $V_{op} = V_{DD} - V_{LCD}$.

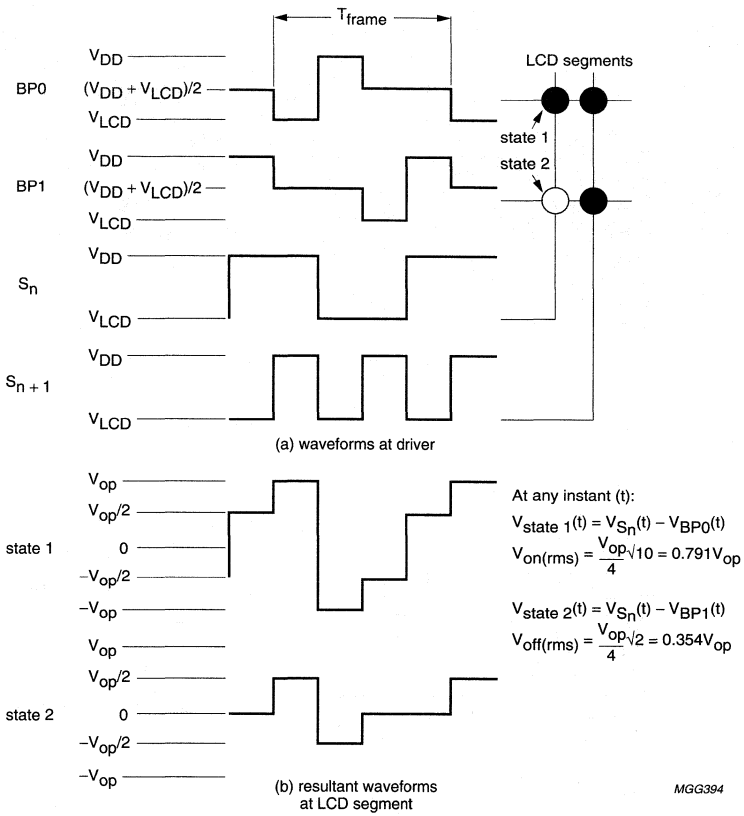


Fig.5 Waveforms for 1 : 2 multiplex drive mode with ½ bias: $V_{op} = V_{DD} - V_{LCD}$.

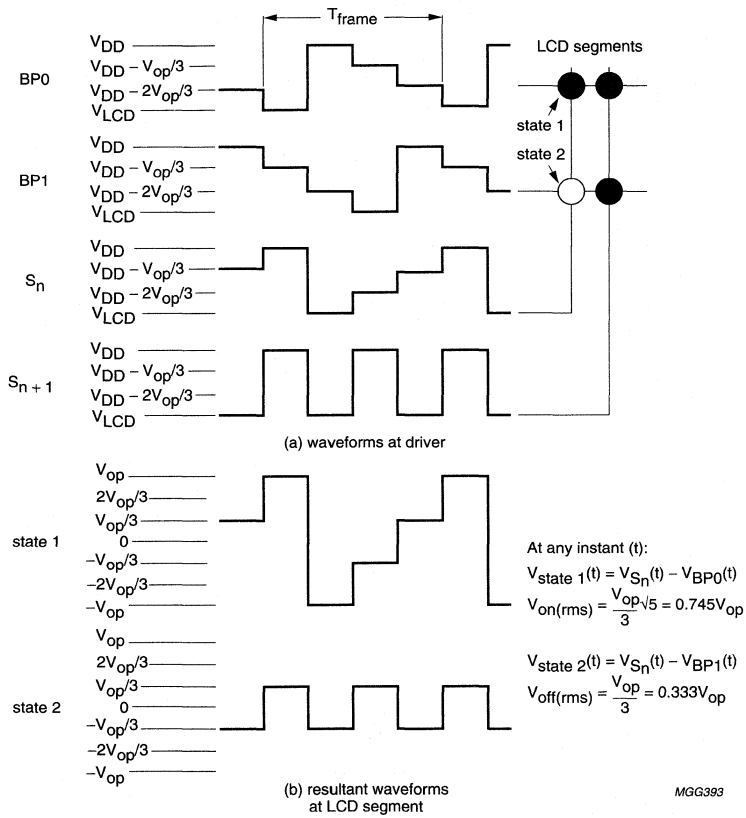


Fig.6 Waveforms for 1 : 2 multiplex drive mode with 1/3 bias: $V_{op} = V_{DD} - V_{LCD}$.

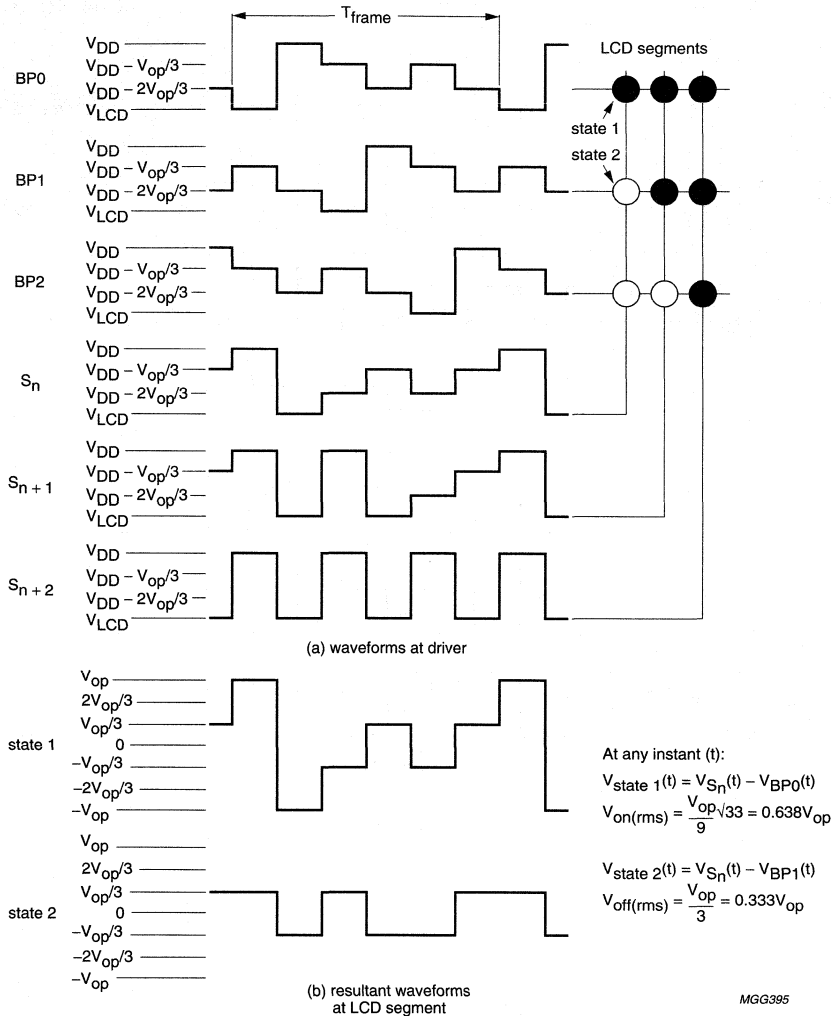


Fig.7 Waveforms for 1 : 3 multiplex drive mode: $V_{op} = V_{DD} - V_{LCD}$.

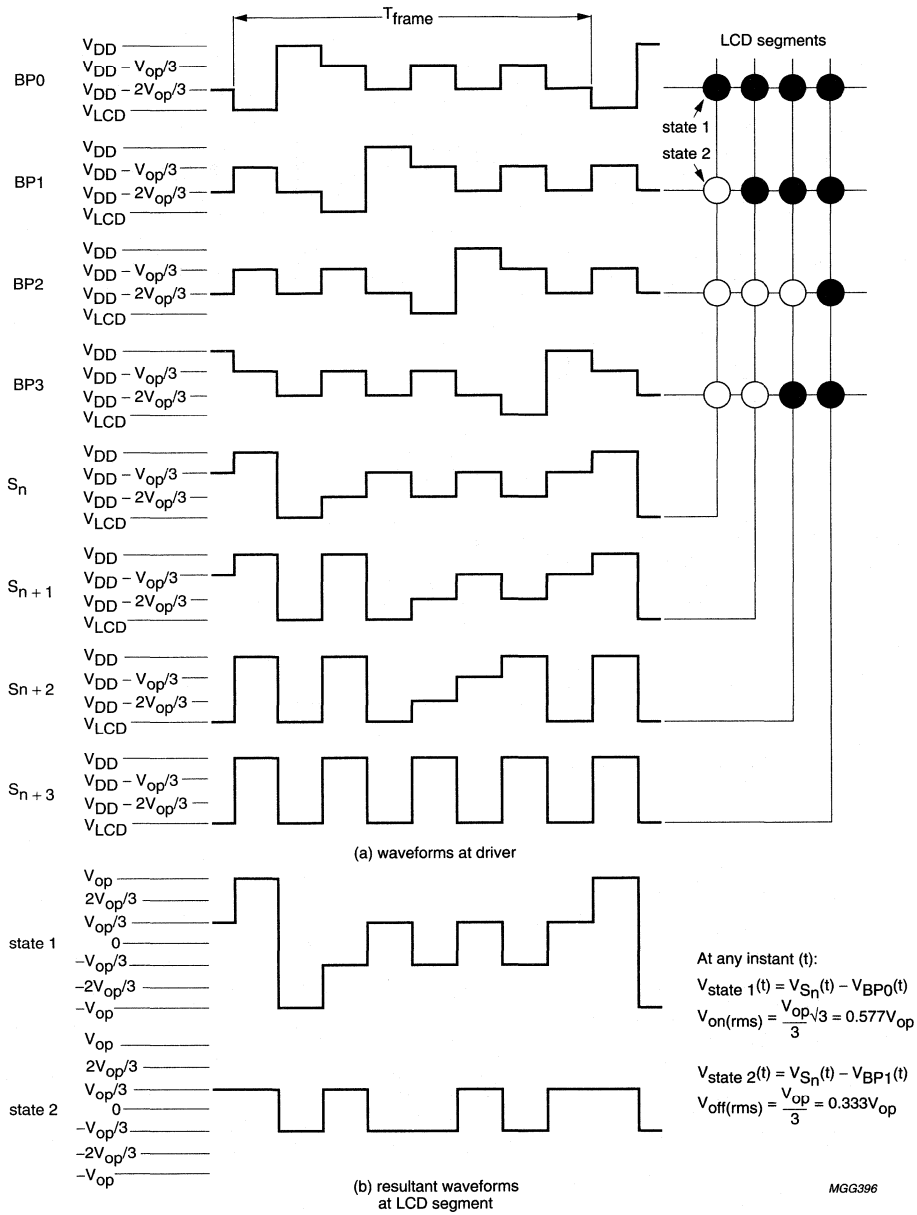


Fig.8 Waveforms for 1 : 4 multiplex drive mode: $V_{op} = V_{DD} - V_{LCD}$.

6.5 Oscillator

The internal logic and the LCD drive signals of the PCF8566 or PCF8576 are timed either by the built-in oscillator or from an external clock.

The clock frequency (f_{CLK}) determines the LCD frame frequency and the maximum rate for data reception from the I²C-bus. To allow I²C-bus transmissions at their maximum data rate of 100 kHz, f_{CLK} should be chosen to be above 125 kHz.

A clock signal must always be supplied to the device; removing the clock may freeze the LCD in a DC state.

6.6 Internal clock

When the internal oscillator is used, OSC (pin 6) should be tied to V_{SS}. In this case, the output from CLK (pin 4) provides the clock signal for cascaded PCF8566s and PCF8576s in the system.

6.7 External clock

The condition for external clock is made by tying OSC (pin 6) to V_{DD}; CLK (pin 4) then becomes the external clock input.

6.8 Timing

The timing of the PCF8566 organizes the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. In cascaded applications, the synchronization signal $\overline{SYNC}$ maintains the correct timing relationship between the PCF8566s in the system. The timing also generates the LCD frame frequency which it derives as an integer multiple of the clock frequency (Table 3). The frame frequency is set by MODE SET commands when internal clock is used, or by the frequency applied to pin 4 when external clock is used.

Table 3 LCD frame frequencies

PCF8566 MODE	f_{frame}	NOMINAL f_{frame} (Hz)
Normal mode	$f_{CLK}/2880$	64
Power saving mode	$f_{CLK}/480$	64

The ratio between the clock frequency and the LCD frame frequency depends on the mode in which the device is operating. In the power saving mode the reduction ratio is six times smaller; this allows the clock frequency to be reduced by a factor of six. The reduced clock frequency results in a significant reduction in power dissipation.

The lower clock frequency has the disadvantage of increasing the response time when large amounts of display data are transmitted on the I²C-bus. When a device is unable to 'digest' a display data byte before the next one arrives, it holds the SCL line LOW until the first display data byte is stored. This slows down the transmission rate of the I²C-bus but no data loss occurs.

6.9 Display latch

The display latch holds the display data while the corresponding multiplex signals are generated. There is a one-to-one relationship between the data in the display latch, the LCD segment outputs and one column of the display RAM.

6.10 Shift register

The shift register serves to transfer display information from the display RAM to the display latch while previous data are displayed.

6.11 Segment outputs

The LCD drive section includes 24 segment outputs S0 to S23 (pins 17 to 40) which should be connected directly to the LCD. The segment output signals are generated in accordance with the multiplexed backplane signals and with the data resident in the display latch. When less than 24 segment outputs are required the unused segment outputs should be left open-circuit.

6.12 Backplane outputs

The LCD drive section includes four backplane outputs BP0 to BP3 which should be connected directly to the LCD. The backplane output signals are generated in accordance with the selected LCD drive mode. If less than four backplane outputs are required the unused outputs can be left open. In the 1 : 3 multiplex drive mode BP3 carries the same signal as BP1, therefore these two adjacent outputs can be tied together to give enhanced drive capabilities. In the 1 : 2 multiplex drive mode BP0 and BP2, BP1 and BP3 respectively carry the same signals and may also be paired to increase the drive capabilities. In the static drive mode the same signal is carried by all four backplane outputs and they can be connected in parallel for very high drive requirements.

6.13 Display RAM

The display RAM is a static 24 × 4-bit RAM which stores LCD data. A logic 1 in the RAM bit-map indicates the 'on' state of the corresponding LCD segment; similarly, a logic 0 indicates the 'off' state.

There is a one-to-one correspondence between the RAM addresses and the segment outputs, and between the individual bits of a RAM word and the backplane outputs. The first RAM column corresponds to the 24 segments operated with respect to backplane BP0 (see Fig.9). In multiplexed LCD applications the segment data of the second, third and fourth column of the display RAM are time-multiplexed with BP1, BP2 and BP3 respectively.

When display data are transmitted to the PCF8566 the display bytes received are stored in the display RAM according to the selected LCD drive mode. To illustrate the filling order, an example of a 7-segment numeric display showing all drive modes is given in Fig.10; the RAM filling organization depicted applies equally to other LCD types.

With reference to Fig.10, in the static drive mode the eight transmitted data bits are placed in bit 0 of eight successive display RAM addresses. In the 1 : 2 multiplex drive mode the eight transmitted data bits are placed in bits 0 and 1 of four successive display RAM addresses. In the 1 : 3 multiplex drive mode these bits are placed in bits 0, 1 and 2 of three successive addresses, with bit 2 of the third address left unchanged. This last bit may, if necessary, be controlled by an additional transfer to this address but care should be taken to avoid overriding adjacent data because full bytes are always transmitted. In the 1 : 4 multiplex drive mode the eight transmitted data bits are placed in bits 0, 1, 2 and 3 of two successive display RAM addresses.

6.14 Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM.

The sequence commences with the initialization of the data pointer by the LOAD DATA POINTER command. Following this, an arriving data byte is stored starting at the display RAM address indicated by the data pointer thereby observing the filling order shown in Fig.10. The data pointer is automatically incremented according to the LCD configuration chosen. That is, after each byte is stored, the contents of the data pointer are incremented by eight (static drive mode), by four (1 : 2 multiplex drive mode), by three (1 : 3 multiplex drive mode) or by two (1 : 4 multiplex drive mode).

6.15 Subaddress counter

The storage of display data is conditioned by the contents of the subaddress counter. Storage is allowed to take place only when the contents of the subaddress counter agree with the hardware subaddress applied to A0, A1 and A2 (pins 7, 8, and 9). A0, A1 and A2 should be tied to V_{SS} or V_{DD}. The subaddress counter value is defined by the DEVICE SELECT command. If the contents of the subaddress counter and the hardware subaddress do not agree then data storage is inhibited but the data pointer is incremented as if data storage had taken place. The subaddress counter is also incremented when the data pointer overflows.

The storage arrangements described lead to extremely efficient data loading in cascaded applications. When a series of display bytes are being sent to the display RAM, automatic wrap-over to the next PCF8566 occurs when the last RAM address is exceeded. Subaddressing across device boundaries is successful even if the change to the next device in the cascade occurs within a transmitted character.

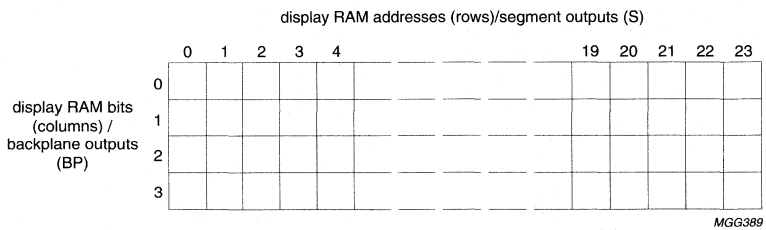


Fig.9 Display RAM bit-map showing direct relationship between display RAM addresses and segment outputs, and between bits in a RAM word and backplane outputs.

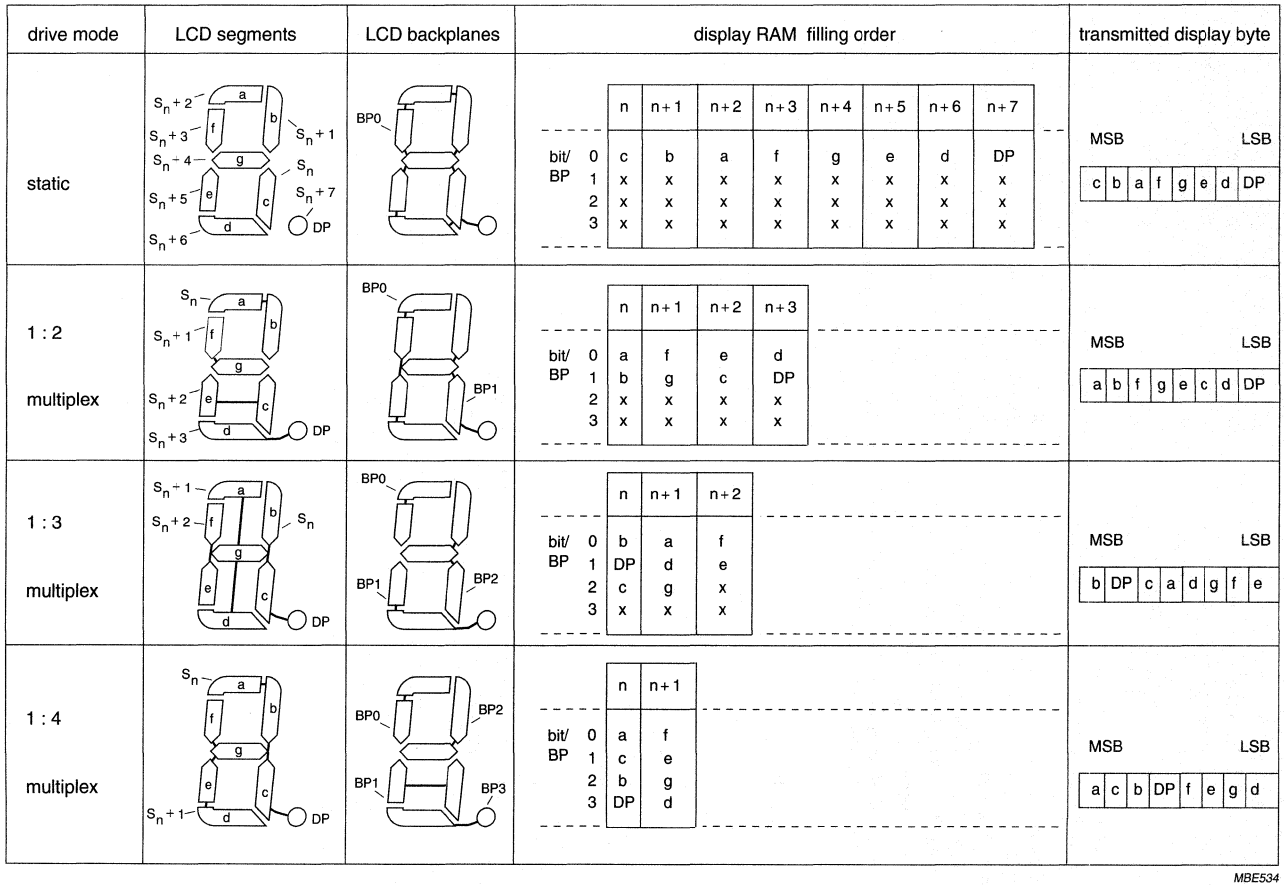


Fig.10 Relationships between LCD layout, drive mode, display RAM filling order and display data transmitted over the I²C-bus (X = data bit unchanged).

6.16 Output bank selector

This selects one of the four bits per display RAM address for transfer to the display latch. The actual bit chosen depends on the particular LCD drive mode in operation and on the instant in the multiplex sequence. In 1 : 4 multiplex, all RAM addresses of bit 0 are the first to be selected, these are followed by the contents of bit 1, bit 2 and then bit 3. Similarly in 1 : 3 multiplex, bits 0, 1 and 2 are selected sequentially. In 1 : 2 multiplex, bits 0 then 1 are selected and, in the static mode, bit 0 is selected.

The PCF8566 includes a RAM bank switching feature in the static and 1 : 2 multiplex drive modes. In the static drive mode, the BANK SELECT command may request the contents of bit 2 to be selected for display instead of bit 0 contents. In the 1 : 2 drive mode, the contents of bits 2 and 3 may be selected instead of bits 0 and 1. This gives the provision for preparing display information in an alternative bank and to be able to switch to it once it is assembled.

6.17 Input bank selector

The input bank selector loads display data into the display RAM according to the selected LCD drive configuration. Display data can be loaded in bit 2 in static drive mode or in bits 2 and 3 in 1 : 2 drive mode by using the BANK SELECT command. The input bank selector functions independently of the output bank selector.

6.18 Blinker

The display blinking capabilities of the PCF8566 are very versatile. The whole display can be blinked at frequencies selected by the BLINK command. The blinking frequencies are integer multiples of the clock frequency; the ratios between the clock and blinking frequencies depend on the mode in which the device is operating, as shown in Table 4.

An additional feature is for an arbitrary selection of LCD segments to be blinked. This applies to the static and 1 : 2 LCD drive modes and can be implemented without any communication overheads. By means of the output bank selector, the displayed RAM banks are exchanged with alternate RAM banks at the blinking frequency. This mode can also be specified by the BLINK command.

In the 1 : 3 and 1 : 4 multiplex modes, where no alternate RAM bank is available, groups of LCD segments can be blinked by selectively changing the display RAM data at fixed time intervals.

If the entire display is to be blinked at a frequency other than the nominal blinking frequency, this can be effectively performed by resetting and setting the display enable bit E at the required rate using the MODE SET command.

Table 4 Blinking frequencies

BLINKING MODE	NORMAL OPERATING MODE RATIO	POWER-SAVING MODE RATIO	NOMINAL BLINKING FREQUENCY f_{blink} (Hz)
Off	–	–	blinking off
2 Hz	$f_{CLK}/92160$	$f_{CLK}/15360$	2
1 Hz	$f_{CLK}/184320$	$f_{CLK}/30720$	1
0.5 Hz	$f_{CLK}/368640$	$f_{CLK}/61440$	0.5

7 I²C-BUS DESCRIPTION

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

7.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

7.2 Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P).

7.3 System configuration

A device generating a message is a 'transmitter', a device receiving a message is a 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves'.

7.4 Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is not limited. Each byte is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

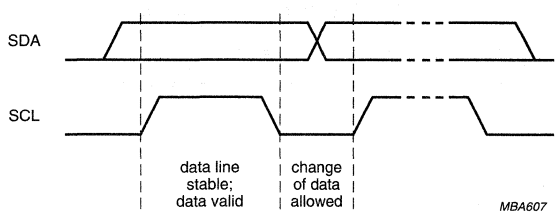


Fig.11 Bit transfer.

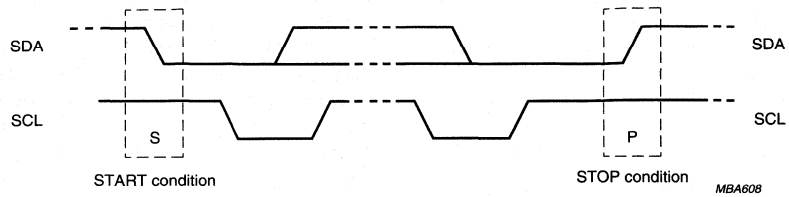


Fig.12 Definition of START and STOP conditions.

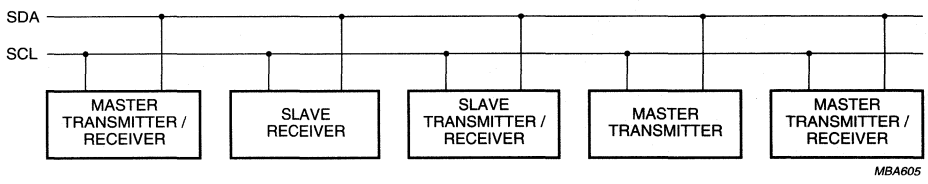


Fig.13 System configuration.

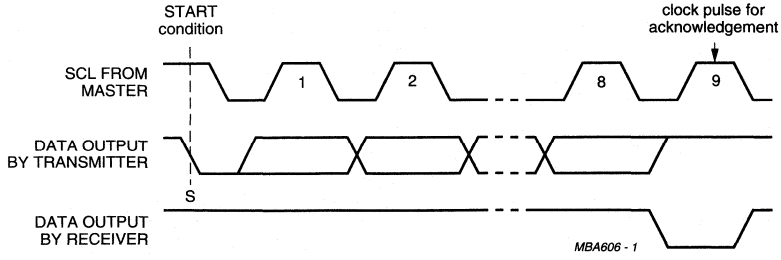


Fig.14 Acknowledgement on the I^2C-bus.

7.5 PCF8566 I²C-bus controller

The PCF8566 acts as an I²C-bus slave receiver. It does not initiate I²C-bus transfers or transmit data to an I²C-bus master receiver. The only data output from the PCF8566 are the acknowledge signals of the selected devices. Device selection depends on the I²C-bus slave address, on the transferred command data and on the hardware subaddress.

In single device applications, the hardware subaddress inputs A0, A1 and A2 are normally left open-circuit or tied to V_{SS} which defines the hardware subaddress 0.
In multiple device applications A0, A1 and A2 are left open-circuit or tied to V_{SS} or V_{DD} according to a binary coding scheme such that no two devices with a common I²C-bus slave address have the same hardware subaddress.

In the power-saving mode it is possible that the PCF8566 is not able to keep up with the highest transmission rates when large amounts of display data are transmitted. If this situation occurs, the PCF8566 forces the SCL line LOW until its internal operations are completed. This is known as the 'clock synchronization feature' of the I²C-bus and serves to slow down fast transmitters. Data loss does not occur.

7.6 Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

7.7 I²C-bus protocol

Two I²C-bus slave addresses (0111110 and 0111111) are reserved for PCF8566. The least-significant bit of the slave address that a PCF8566 will respond to is defined by the level tied at its input SA0 (pin 10). Therefore, two types of PCF8566 can be distinguished on the same I²C-bus which allows:

1. Up to 16 PCF8566s on the same I²C-bus for very large LCD applications
2. The use of two types of LCD multiplex on the same I²C-bus.

The I²C-bus protocol is shown in Fig.15. The sequence is initiated with a START condition (S) from the I²C-bus master which is followed by one of the two PCF8566 slave addresses available. All PCF8566s with the corresponding SA0 level acknowledge in parallel the slave address but all PCF8566s with the alternative SA0 level ignore the whole I²C-bus transfer. After acknowledgement, one or more command bytes (m) follow which define the status of the addressed PCF8566s. The last command byte is tagged with a cleared most-significant bit, the continuation bit C. The command bytes are also acknowledged by all addressed PCF8566s on the bus.

After the last command byte, a series of display data bytes (n) may follow. These display data bytes are stored in the display RAM at the address specified by the data pointer and the subaddress counter. Both data pointer and subaddress counter are automatically updated and the data are directed to the intended PCF8566 device.
The acknowledgement after each byte is made only by the (A0, A1, A2) addressed PCF8566. After the last display byte, the I²C-bus master issues a STOP condition (P).

7.8 Command decoder

The command decoder identifies command bytes that arrive on the I²C-bus. All available commands carry a continuation bit C in their most-significant bit position (see Fig.16). When this bit is set, it indicates that the next byte of the transfer to arrive will also represent a command.
If the bit is reset, it indicates the last command byte of the transfer. Further bytes will be regarded as display data.

The five commands available to the PCF8566 are defined in Table 5.

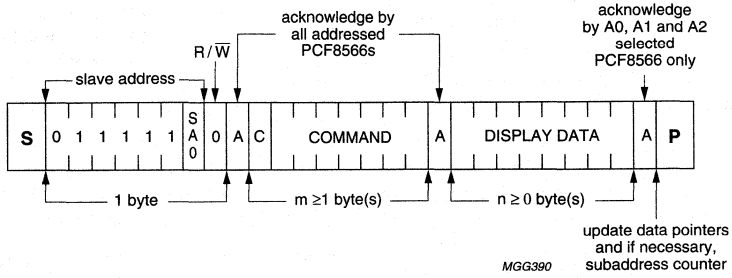


Fig.15 I²C-bus protocol.

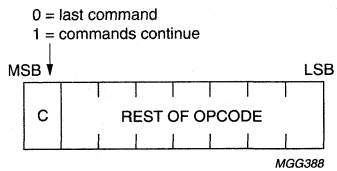


Fig.16 General format of command byte.

Table 5 Definition of PCF8566 commands

COMMAND/OPCODE								OPTIONS	DESCRIPTION
Mode set									
C	1	0	LP	E	B	M1	M0	see Table 6	defines LCD drive mode
								see Table 7	defines LCD bias configuration
								see Table 8	defines display status; the possibility to disable the display allows implementation of blinking under external control
								see Table 9	defines power dissipation mode
Load data pointer									
C	0	0	P4	P3	P2	P1	P0	see Table 10	five bits of immediate data, bits P4 to P0, are transferred to the data pointer to define one of twenty-four display RAM addresses
Device select									
C	1	1	0	0	A2	A1	A0	see Table 11	three bits of immediate data, bits A0 to A2, are transferred to the subaddress counter to define one of eight hardware subaddresses
Bank select									
C	1	1	1	1	0	I	O	see Table 12	defines input bank selection (storage of arriving display data)
								see Table 13	defines output bank selection (retrieval of LCD display data)
									the BANK SELECT command has no effect in 1 : 3 and 1 : 4 multiplex drive modes
Blink									
C	1	1	1	0	A	BF1	BF0	see Table 14	defines the blinking frequency
								see Table 15	selects the blinking mode; normal operation with frequency set by bits BF1 and BF0, or blinking by alternation of display RAM banks. Alternation blinking does not apply in 1 : 3 and 1 : 4 multiplex drive modes

Table 6 LCD drive mode

LCD DRIVE MODE	BIT M1	BIT M0
Static (1 BP)	0	1
1 : 2 MUX (2 BP)	1	0
1 : 3 MUX (3 BP)	1	1
1 : 4 MUX (4 BP)	0	0

Table 7 LCD bias configuration

LCD BIAS	BIT B
1/3bias	0
1/2bias	1

Table 8 Display status

DISPLAY STATUS	BIT E
Disabled (blank)	0
Enabled	1

Table 9 Power dissipation mode

MODE	BIT LP
Normal mode	0
Power-saving mode	1

Table 10 Load data pointer

BITS	P4	P3	P2	P1	P0
5-bit binary value of 0 to 23					

Table 11 Device select

BITS	A0	A1	A2
3-bit binary value of 0 to 7			

Table 12 Input bank selection

STATIC	1 : 2 MUX	BIT 1
RAM bit 0	RAM bits 0, 1	0
RAM bit 2	RAM bits 2, 3	1

Table 13 Output bank selection

STATIC	1 : 2 MUX	BIT 0
RAM bit 0	RAM bits 0, 1	0
RAM bit 2	RAM bits 2, 3	1

Table 14 Blinking frequency

BLINK FREQUENCY	BIT BF1	BIT BF0
Off	0	0
2 Hz	0	1
1 Hz	1	0
0.5 Hz	1	1

Table 15 Blink mode selection

BLINK MODE	BIT A
Normal blinking	0
Alternation blinking	1

7.9 Display controller

The display controller executes the commands identified by the command decoder. It contains the status registers of the PCF8566 and coordinates their effects.

The controller is also responsible for loading display data into the display RAM as required by the filling order.

7.10 Cascaded operation

In large display configurations, up to 16 PCF8566s can be distinguished on the same I²C-bus by using the 3-bit hardware subaddress (A0, A1 and A2) and the programmable I²C-bus slave address (SA0). It is also possible to cascade up to 16 PCF8566s. When cascaded, several PCF8566s are synchronized so that they can share the backplane signals from one of the devices in the cascade. Such an arrangement is cost-effective in large LCD applications since the outputs of only one device need to be through-plated to the backplane electrodes of the display. The other PCF8566s of the cascade contribute additional segment outputs but their backplane outputs are left open-circuit (Fig.17).

The $\overline{\text{SYNC}}$ line is provided to maintain the correct synchronization between all cascaded PCF8566s. This synchronization is guaranteed after the power-on reset. The only time that $\overline{\text{SYNC}}$ is likely to be needed is if synchronization is accidentally lost (e.g. by noise in adverse electrical environments; or by the definition of a multiplex mode when PCF8566s with differing SA0 levels are cascaded). $\overline{\text{SYNC}}$ is organized as an input/output pin; the output section being realized as an open-drain driver with an internal pull-up resistor. A PCF8566 asserts the $\overline{\text{SYNC}}$ line at the onset of its last active backplane signal and monitors the $\overline{\text{SYNC}}$ line at all other times. Should synchronization in the cascade be lost, it will be restored by the first PCF8566 to assert $\overline{\text{SYNC}}$. The timing relationships between the backplane waveforms and the $\overline{\text{SYNC}}$ signal for the various drive modes of the PCF8576 are shown in Fig.18. The waveforms are identical with the parent device PCF8576. Cascade ability between PCF8566s and PCF8576s is possible, giving cost effective LCD applications.

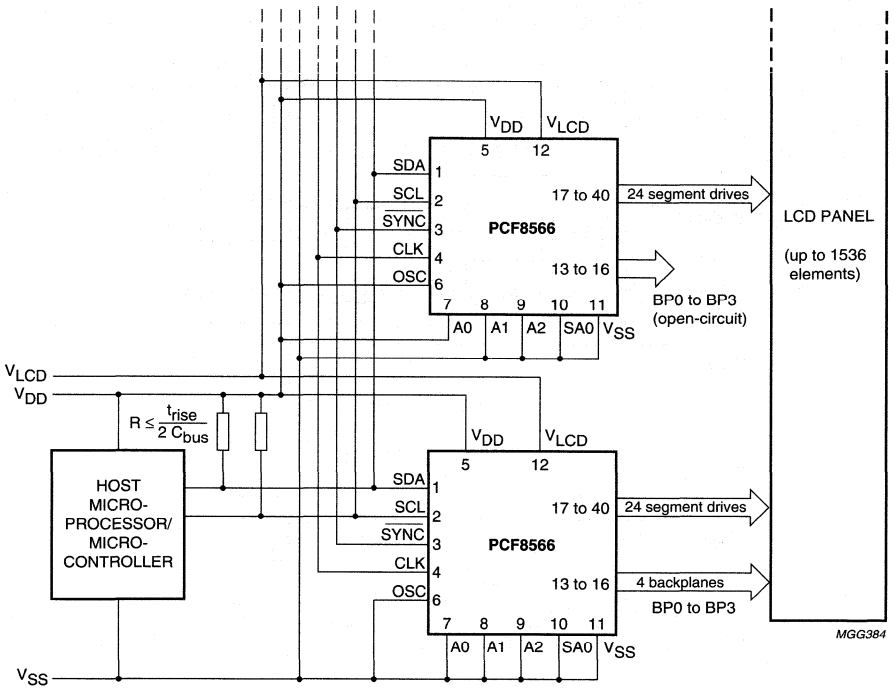


Fig.17 Cascaded PCF8566 configuration.

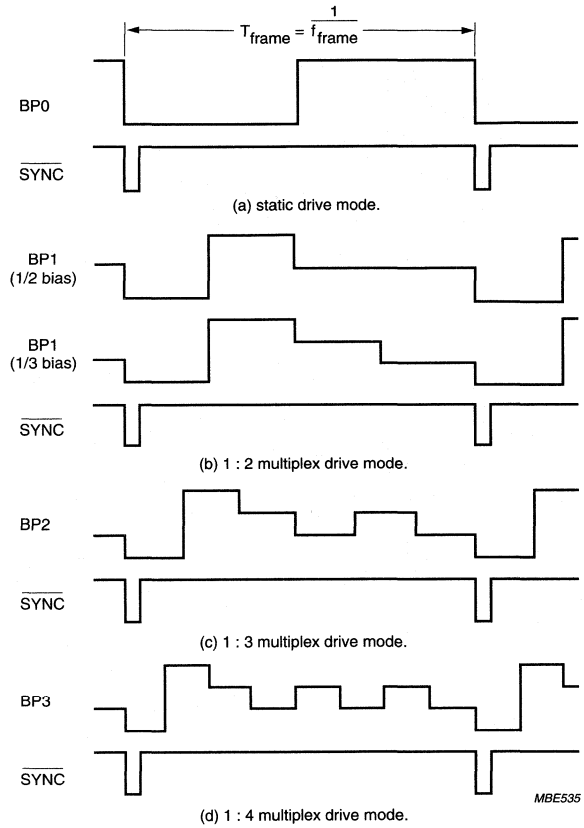


Fig.18 Synchronization of the cascade for the various PCF8566 drive modes.

For single plane wiring of PCF8566s, see Chapter “Application information”.

8 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.5	+7	V
V_{LCD}	LCD supply voltage	V_{DD} − 7	V_{DD}	V
V_I	input voltage (SCL, SDA, A0 to A2, OSC, CLK, $\overline{SYNC}$ and SA0)	V_{SS} − 0.5	V_{DD} + 0.5	V
V_O	output voltage (S0 to S23 and BP0 to BP3)	V_{LCD} − 0.5	V_{DD} + 0.5	V
I_I	DC input current	−	±20	mA
I_O	DC output current	−	±25	mA
I_{DD}, I_{SS}, I_{LCD}	V_{DD}, V_{SS} or V_{LCD} current	−	±50	mA
P_{tot}	power dissipation per package	−	400	mW
P_O	power dissipation per output	−	100	mW
T_{stg}	storage temperature	−65	+150	°C

9 HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advised to take handling precautions appropriate to handling MOS devices (see *"Handling MOS devices"*).

10 DC CHARACTERISTICS

V_{SS} = 0 V; V_{DD} = 2.5 to 6 V; V_{LCD} = V_{DD} − 2.5 to V_{DD} − 6 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	operating supply voltage		2.5	–	6	V
V_{LCD}	LCD supply voltage		V_{DD} − 6	–	V_{DD} − 2.5	V
I_{DD}	operating supply current (normal mode)	f_{CLK} = 200 kHz; note 1	–	30	90	µA
I_{LP}	power saving mode supply current	V_{DD} = 3.5 V; V_{LCD} = 0 V; f_{CLK} = 35 kHz; A0, A1 and A2 tied to V_{SS}; note 1	–	15	40	µA
Logic						
V_{IL}	LOW level input voltage		V_{SS}	–	0.3V_{DD}	V
V_{IH}	HIGH level input voltage		0.7V_{DD}	–	V_{DD}	V
V_{OL}	LOW level output voltage	I_O = 0 mA	–	–	0.05	V
V_{OH}	HIGH level output voltage	I_O = 0 mA	V_{DD} − 0.05	–	–	V
I_{OL1}	LOW level output current (CLK and $\overline{SYNC}$)	V_{OL} = 1 V; V_{DD} = 5 V	1	–	–	mA
I_{OH}	HIGH level output current (CLK)	V_{OH} = 4 V; V_{DD} = 5 V	–	–	−1	mA
I_{OL2}	LOW level output current (SDA and SCL)	V_{OL} = 0.4 V; V_{DD} = 5 V	3	–	–	mA
I_{LI}	leakage current (SA0, CLK, OSC, A0, A1, A2, SCL and SDA)	V_I = V_{SS} or V_{DD}	–	–	±1	µA
I_{pd}	pull-down current (A0, A1, A2 and OSC)	V_I = 1 V; V_{DD} = 5 V	15	50	150	µA
R_{puSYNC}	pull-up resistor ($\overline{SYNC}$)		15	25	60	kΩ
V_{ref}	power-on reset level	note 2	–	1.3	2	V
t_{sw}	tolerable spike width on bus		–	–	100	ns
C_i	input capacitance	note 3	–	–	7	pF
LCD outputs						
V_{BP}	DC voltage component (BP0 to BP3)	C_{BP} = 35 nF	–	±20	–	mV
V_S	DC voltage component (S0 to S23)	C_S = 5 nF	–	±20	–	mV
Z_{BP}	output impedance (BP0 to BP3)	V_{LCD} = V_{DD} − 5 V; note 4	–	1	5	kΩ
Z_S	output impedance (S0 to S23)	V_{LCD} = V_{DD} −5 V; note 4	–	3	7	kΩ

Notes

1. Outputs open; inputs at V_{SS} or V_{DD}; external clock with 50% duty factor; I^2C-bus inactive.
2. Resets all logic when V_{DD} < V_{ref}.
3. Periodically sampled, not 100% tested.
4. Outputs measured one at a time.

11 AC CHARACTERISTICS

V_{SS} = 0 V; V_{DD} = 2.5 to 6 V; V_{LCD} = V_{DD} − 2.5 to V_{DD} − 6 V; T_{amb} = −40 to +85 °C; unless otherwise specified; note 1.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{CLK}	oscillator frequency (normal mode)	V_{DD} = 5 V; note 2	125	200	315	kHz
f_{CLKLP}	oscillator frequency (power saving mode)	V_{DD} = 3.5 V	21	31	48	kHz
t_{CLKH}	CLK HIGH time		1	–	–	µs
t_{CLKL}	CLK LOW time		1	–	–	µs
t_{PSYNC}	$\overline{SYNC}$ propagation delay		–	–	400	ns
t_{SYNCL}	$\overline{SYNC}$ LOW time		1	–	–	µs
t_{PLCD}	driver delays with test loads	V_{LCD} = V_{DD} − 5 V	–	–	30	µs
I²C-bus						
t_{BUF}	bus free time		4.7	–	–	µs
$t_{HD;\,STA}$	START condition hold time		4	–	–	µs
t_{LOW}	SCL LOW time		4.7	–	–	µs
t_{HIGH}	SCL HIGH time		4	–	–	µs
$t_{SU;\,STA}$	START condition set-up time (repeated start code only)		4.7	–	–	µs
$t_{HD;\,DAT}$	data hold time		0	–	–	µs
$t_{SU;\,DAT}$	data set-up time		250	–	–	ns
t_r	rise time		–	–	1	µs
t_f	fall time		–	–	300	ns
$t_{SU;\,STO}$	STOP condition set-up time		4.7	–	–	µs

Notes

1. All timing values referred to V_{IH} and V_{IL} levels with an input voltage swing of V_{SS} to V_{DD}.
2. At f_{CLK} < 125 kHz, I²C-bus maximum transmission speed is derated.

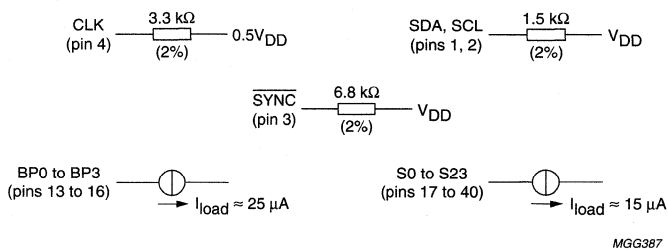


Fig.19 Test loads.

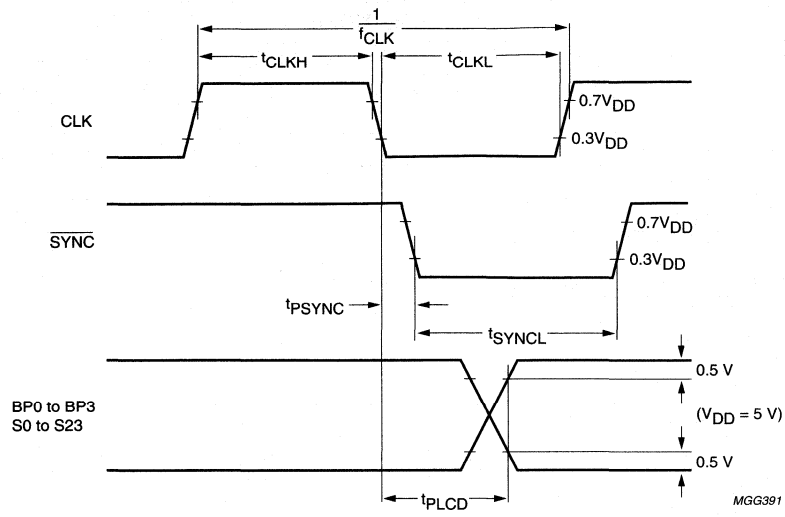


Fig.20 Driver timing waveforms.

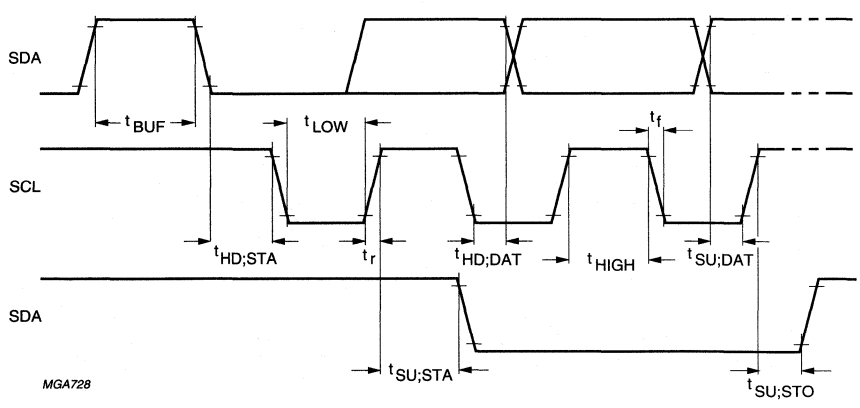
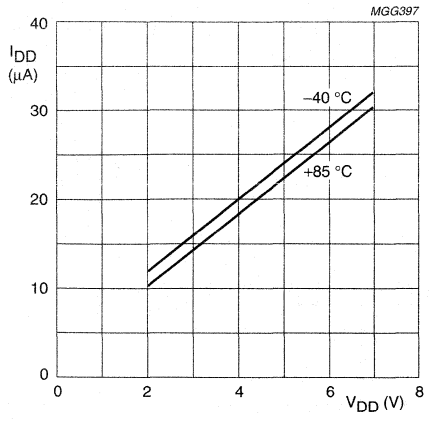
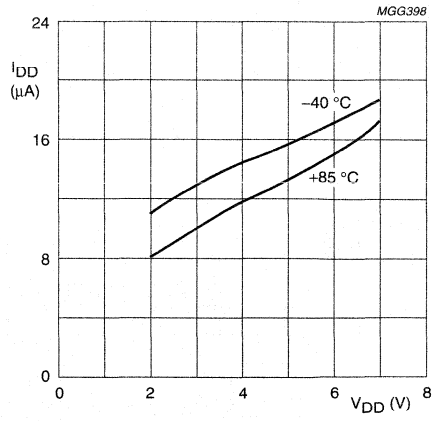


Fig.21 I²C-bus timing waveforms.

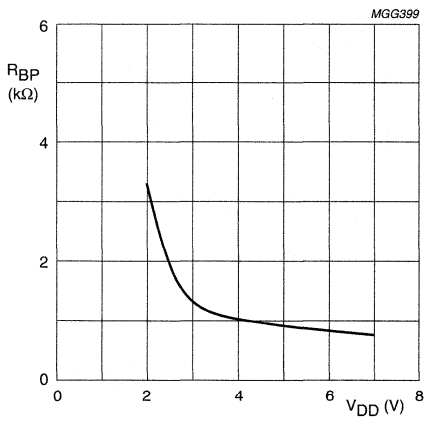


a. Normal mode; V_{LCD} = 0 V; external clock = 200 kHz.

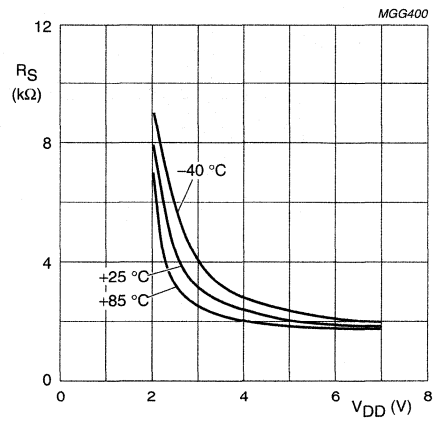


b. Low power mode; V_{LCD} = 0 V; external clock = 35 kHz.

Fig.22 Typical supply current characteristics.



a. Backplane output impedance BP0 to BP3 (R_{BP}); V_{DD} = 5 V; T_{amb} = −40 to +85 °C.



b. Segment output impedance S0 to S23 (R_S); V_{DD} = 5 V.

Fig.23 Typical characteristics of LCD outputs.

12 APPLICATION INFORMATION

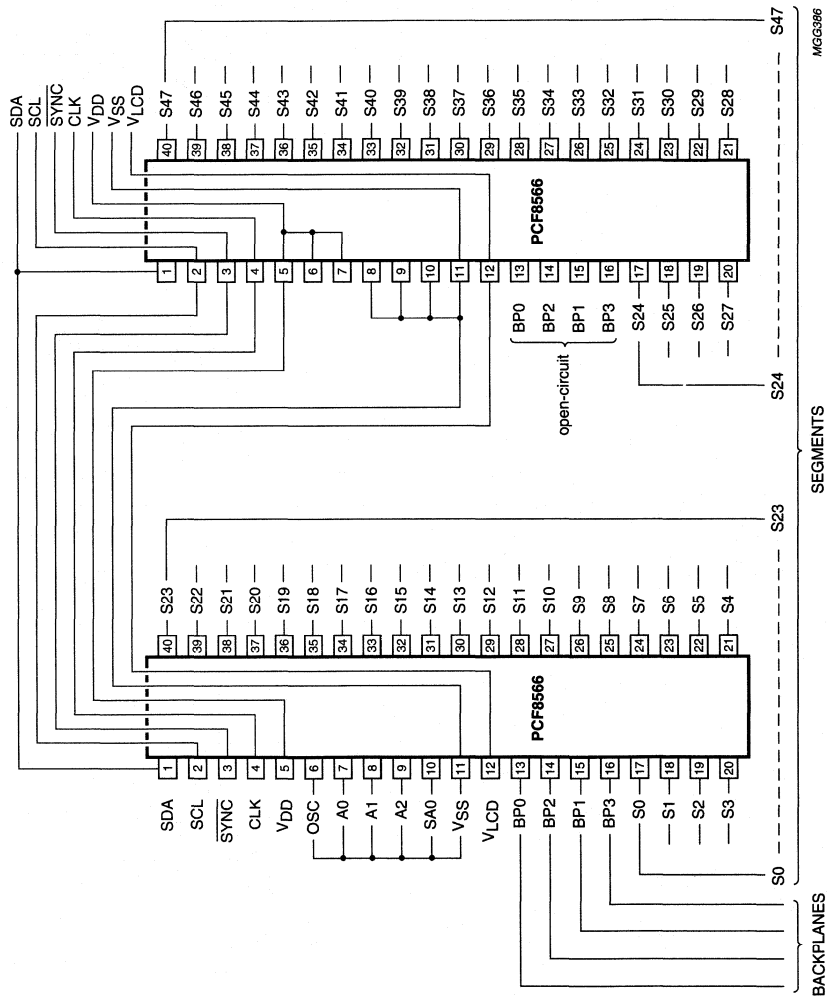
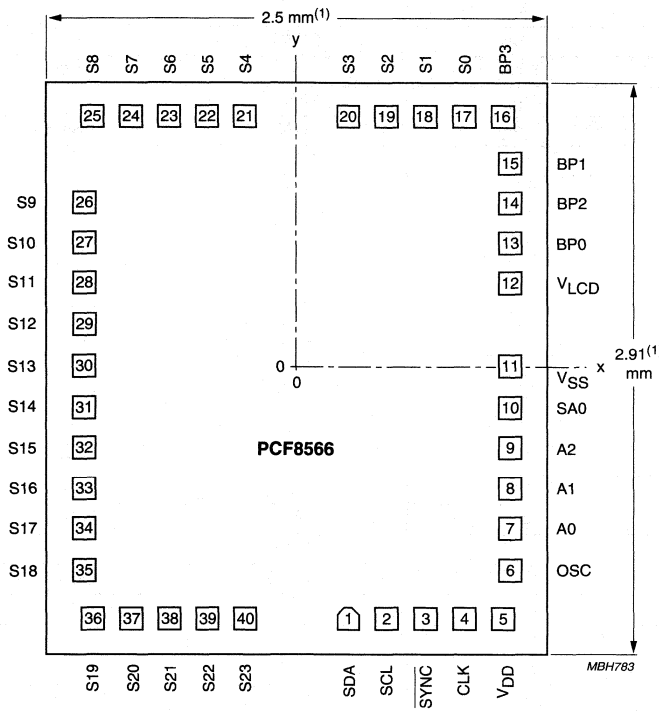


Fig.24 Single plane wiring of package PCF8566s.

13 CHIP DIMENSIONS AND BONDING PAD LOCATIONS



(1) Typical value.
Pad size: 120 × 120 μm
Chip area: 7.27 mm.
The numbers given in the small squares refer to the pad numbers.

Fig.25 Bonding pad locations.

Table 16 Bonding pad locations (dimensions in mm)
All x/y coordinates are referenced to centre of chip, (see Fig.25).

PAD NUMBER	SYMBOL	x	y	PIN
1	SDA	200	−1235	1
2	SCL	400	−1235	2
3	$\overline{SYNC}$	605	−1235	3
4	CLK	856	−1235	4
5	V_{DD}	1062	−1235	5
6	OSC	1080	−1025	6
7	A0	1080	−825	7
8	A1	1080	−625	8
9	A2	1080	−425	9
10	SA0	1080	−225	10
11	V_{SS}	1080	−25	11
12	V_{LCD}	1080	347	12
13	BP0	1080	547	13
14	BP2	1080	747	14
15	BP1	1080	947	15
16	BP3	1074	1235	16
17	S0	874	1235	17
18	S1	674	1235	18
19	S2	474	1235	19
20	S3	274	1235	20
21	S4	−274	1235	21
22	S5	−474	1235	22
23	S6	−674	1235	23
24	S7	−874	1235	24
25	S8	−1074	1235	25
26	S9	−1080	765	26
27	S10	−1080	565	27
28	S11	−1080	365	28
29	S12	−1080	165	29
30	S13	−1080	−35	30
31	S14	−1080	−235	31
32	S15	−1080	−435	32
33	S16	−1080	−635	33
34	S17	−1080	−835	34
35	S18	−1080	−1035	35
36	S19	−1056	−1235	36
37	S20	−830	−1235	37
38	S21	−630	−1235	38
39	S22	−430	−1235	39
40	S23	−230	−1235	40

256 × 8-bit static low-voltage RAM with I²C-bus interface

PCF8570

CONTENTS

256 × 8-bit static low-voltage RAM with I²C-bus interface

PCF8570

1 FEATURES

- Operating supply voltage 2.5 to 6.0 V
- Low data retention voltage; minimum 1.0 V
- Low standby current; maximum 15 µA
- Power-saving mode; typical 50 nA
- Serial input/output bus (I²C-bus)
- Address by 3 hardware address pins
- Automatic word address incrementing
- Available in DIP8 and SO8 packages.

2 APPLICATIONS

- Telephony:
  - RAM expansion for stored numbers in repertory dialling (e.g. PCD33xxA applications)
- General purpose RAM for applications requiring extremely low current and low-voltage RAM retention, such as battery or capacitor-backed.
- Radio, television and video cassette recorder:
  - channel presets
- General purpose:
  - RAM expansion for the microcontroller families PCD33xxA, PCF84CxxxA, P80CLxxx and most other microcontrollers.

3 GENERAL DESCRIPTION

The PCF8570 is a low power static CMOS RAM, organized as 256 words by 8-bits.

Addresses and data are transferred serially via a two-line bidirectional bus (I²C-bus). The built-in word address register is incremented automatically after each written or read data byte. Three address pins, A0, A1 and A2 are used to define the hardware address, allowing the use of up to 8 devices connected to the bus without additional hardware.

4 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		2.5	6.0	
I_{DD}	supply current (standby)	f_{SCL} = 0 Hz	–	15	µA
I_{DDR}	supply current (power-saving mode)	T_{amb} = 25 °C	–	400	nA
T_{amb}	operating ambient temperature		−40	+85	°C
T_{stg}	storage temperature		−65	+150	°C

5 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8570P	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1
PCF8570T	SO8	plastic small outline package; 8 leads; body width 7.5 mm	SOT176-1

6 BLOCK DIAGRAM

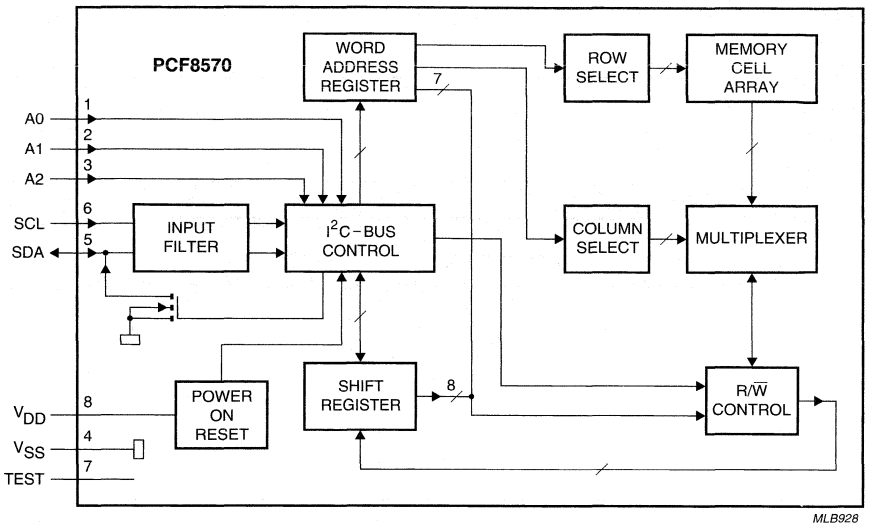


Fig.1 Block diagram.

7 PINNING

SYMBOL	PIN	DESCRIPTION
A0	1	hardware address input 0
A1	2	hardware address input 1
A2	3	hardware address input 2
V_{SS}	4	negative supply
SDA	5	serial data input/output
SCL	6	serial clock input
TEST	7	Input for power-saving mode (see section "Power-saving mode"). Also used as a test output during manufacture. TEST should be tied to V_{SS} during normal operation.
V_{DD}	8	positive supply

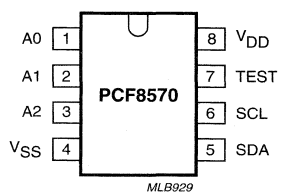


Fig.2 Pin configuration.

8 CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

8.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

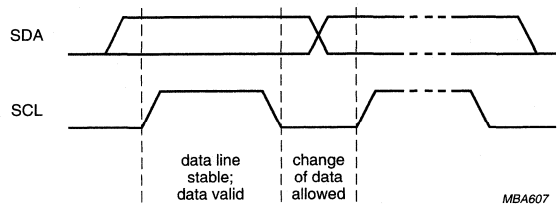


Fig.3 Bit transfer.

8.2 Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

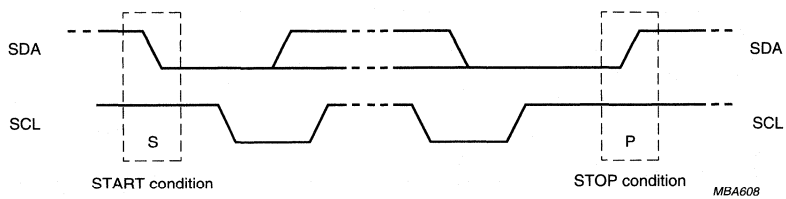


Fig.4 Definition of start and stop conditions.

8.3 System configuration

A device generating a message is a 'transmitter', a device receiving a message is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves'.

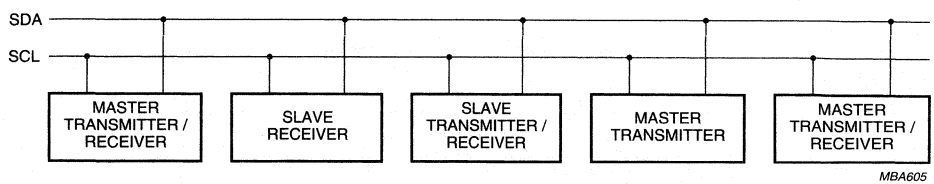


Fig.5 System configuration.

8.4 Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

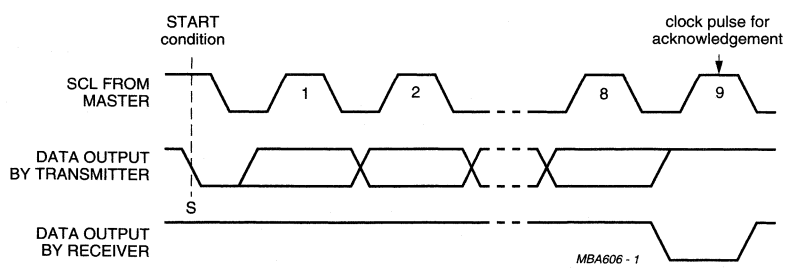


Fig.6 Acknowledgement on the I²C-bus.

8.5 I²C-bus protocol

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always carried out with the first byte transmitted after the start procedure. The I²C-bus configuration for the different PCF8570 WRITE and READ cycles is shown in Figs 7, 8 and 9.

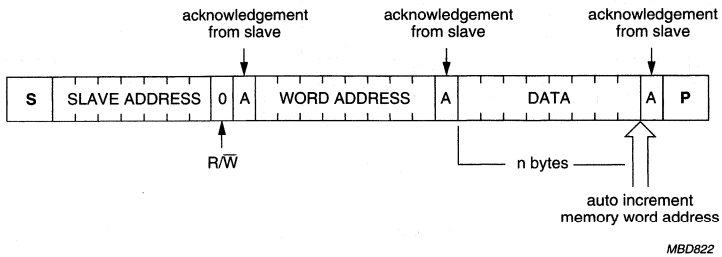


Fig.7 Master transmits to slave receiver (WRITE) mode.

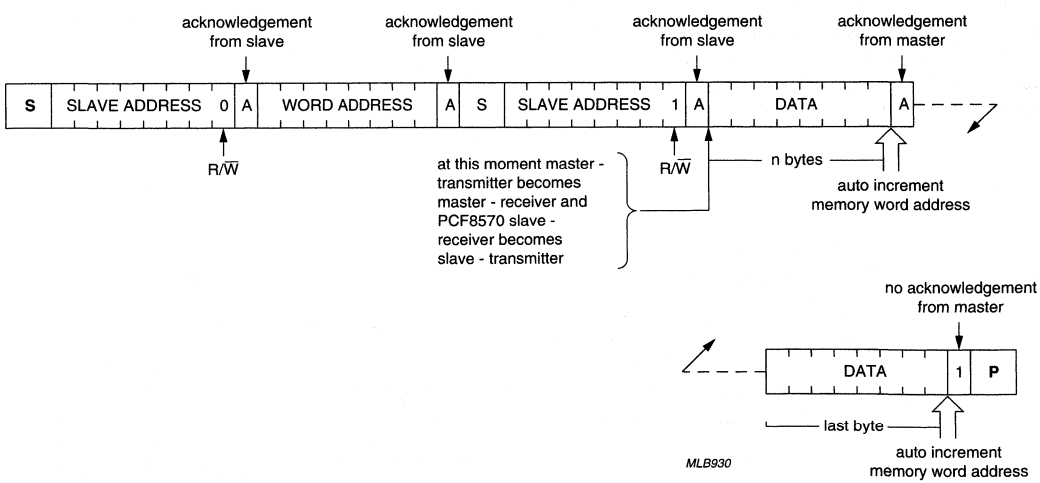


Fig.8 Master reads after setting word address (WRITE word address; READ data).

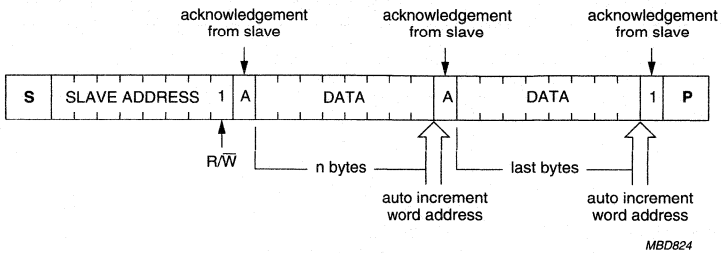


Fig.9 Master reads slave immediately after first byte (READ mode).

9 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage (pin 8)	−0.8	+8.0	V
V_I	input voltage (any input)	−0.8	V_{DD} + 0.8	V
I_I	DC input current	–	±10	mA
I_O	DC output current	–	±10	mA
I_{DD}	positive supply current	–	±50	mA
I_{SS}	negative supply current	–	±50	mA
P_{tot}	total power dissipation per package	–	300	mW
P_O	power dissipation per output	–	50	mW
T_{amb}	operating ambient temperature	−40	+85	°C
T_{stg}	storage temperature	−65	+150	°C

10 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take precautions appropriate to handling MOS devices. Advice can be found in Data Handbook IC12 under *"Handling MOS Devices"*.

11 DC CHARACTERISTICS

V_{DD} = 2.5 to 6.0 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		2.5	–	6.0	V
I_{DD}	supply current					
	standby mode	$V_I = V_{DD}$ or V_{SS}; f_{SCL} = 0 Hz; T_{amb} = −25 to +70 °C	–	–	5	µA
	operating mode	$V_I = V_{DD}$ or V_{SS}; f_{SCL} = 100 Hz	–	–	200	µA
V_{POR}	Power-on reset voltage	note 1	1.5	1.9	2.3	V
Inputs, input/output SDA						
V_{IL}	LOW level input voltage	note 2	−0.8	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage	note 2	$0.7V_{DD}$	–	V_{DD} + 0.8	V
I_{OL}	LOW level output current	V_{OL} = 0.4 V	3	–	–	mA
I_{LI}	input leakage current	$V_I = V_{DD}$ or V_{SS}	−1	–	+1	µA
Inputs A0, A1, A2 and TEST						
I_{LI}	input leakage current	$V_I = V_{DD}$ or V_{SS}	−250	–	+250	nA
Inputs SCL and SDA						
C_i	input capacitance	$V_I = V_{SS}$	–	–	7	pF
Low V_{DD} data retention						
V_{DDR}	supply voltage for data retention		1	–	6	V
I_{DDR}	supply current	V_{DDR} = 1 V	–	–	5	µA
		V_{DDR} = 1 V; T_{amb} = −25 to +70 °C	–	–	2	µA
Power-saving mode (see Figs 13 and 14)						
I_{DDR}	supply current	TEST = V_{DD}; T_{amb} = 25 °C	–	50	400	nA
t_{HD2}	recovery time		–	50	–	µs

Notes

1. The Power-on reset circuit resets the I²C-bus logic when $V_{DD} < V_{POR}$. The status of the device after a Power-on reset condition can be tested by sending the slave address and testing the acknowledge bit.
2. If the input voltages are a diode voltage above or below the supply voltage V_{DD} or V_{SS} an input current will flow; this current must not exceed ±0.5 mA.

12 AC CHARACTERISTICS

All timing values are valid within the operating supply voltage and ambient temperature range and reference to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
I²C-bus timing (see Fig.10; note 1)					
f_{SCL}	SCL clock frequency	–	–	100	kHz
t_{SP}	tolerable spike width on bus	–	–	100	ns
t_{BUF}	bus free time	4.7	–	–	µs
$t_{SU;STA}$	START condition set-up time	4.7	–	–	µs
$t_{HD;STA}$	START condition hold time	4.0	–	–	µs
t_{LOW}	SCL LOW time	4.7	–	–	µs
t_{HIGH}	SCL HIGH time	4.0	–	–	µs
t_r	SCL and SDA rise time	–	–	1.0	µs
t_f	SCL and SDA fall time	–	–	0.3	µs
$t_{SU;DAT}$	data set-up time	250	–	–	ns
$t_{HD;DAT}$	data hold time	0	–	–	ns
$t_{VD;DAT}$	SCL LOW-to-data out valid	–	–	3.4	µs
$t_{SU;STO}$	STOP condition set-up time	4.0	–	–	µs

Note

1. A detailed description of the I²C-bus specification, with applications, is given in brochure *"The I²C-bus and how to use it"*. This brochure may be ordered using the code 9398 393 40011.

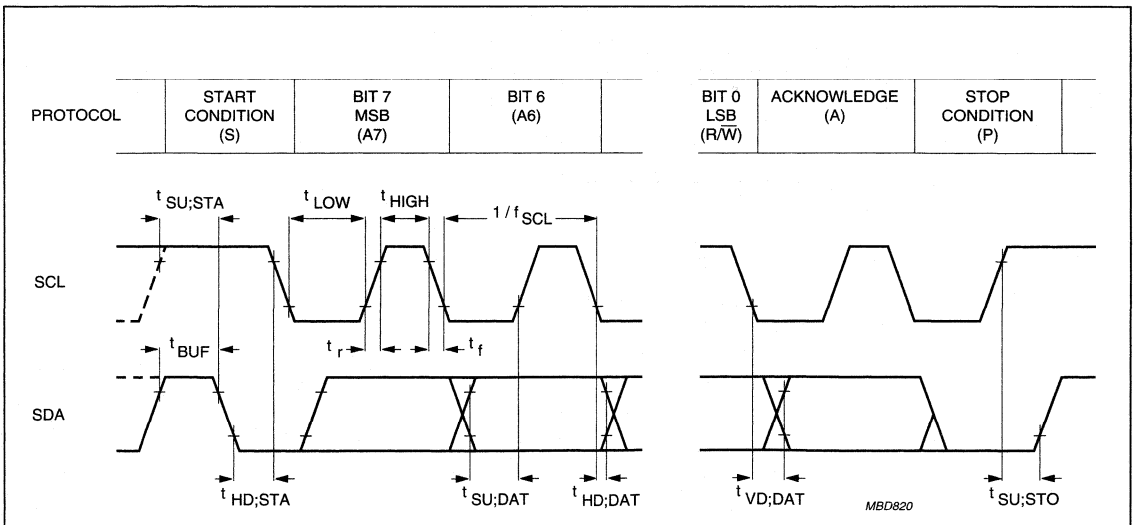
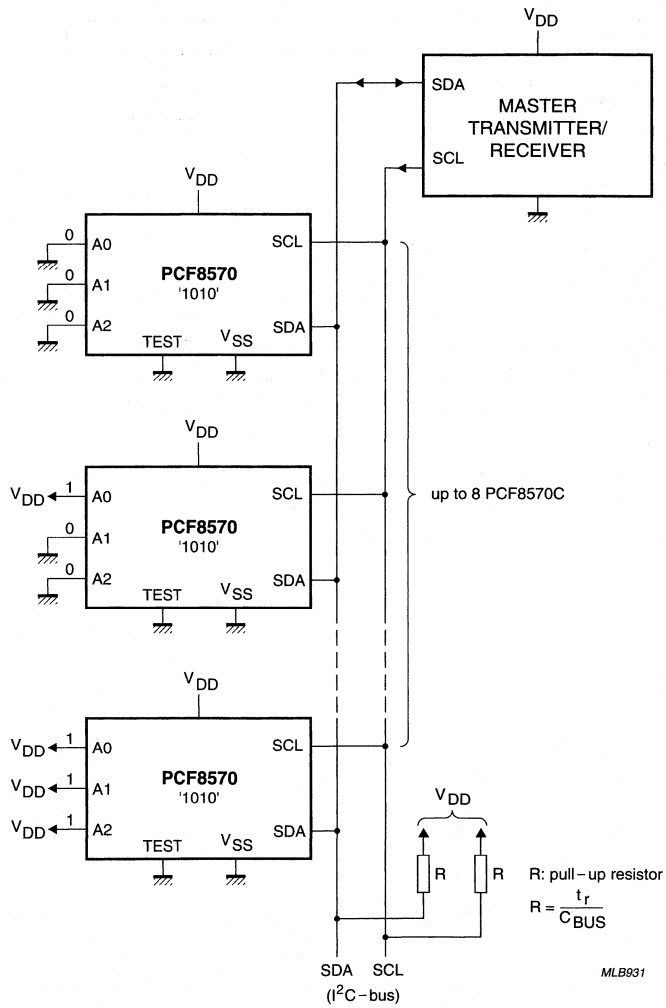


Fig.10 I²C-bus timing diagram; rise and fall times refer to V_{IL} and V_{IH}.

13 APPLICATION INFORMATION

13.1 Application example



It is recommended that a 4.7 μF/10 V solid aluminium capacitor (SAL) be connected between V_{DD} and V_{SS}.

Fig.11 Application diagram.

13.2 Slave address

The PCF8570 has a fixed combination 1 0 1 0 as group 1, while group 2 is fully programmable (see Fig.12).

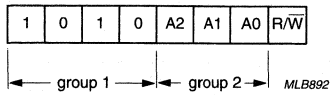
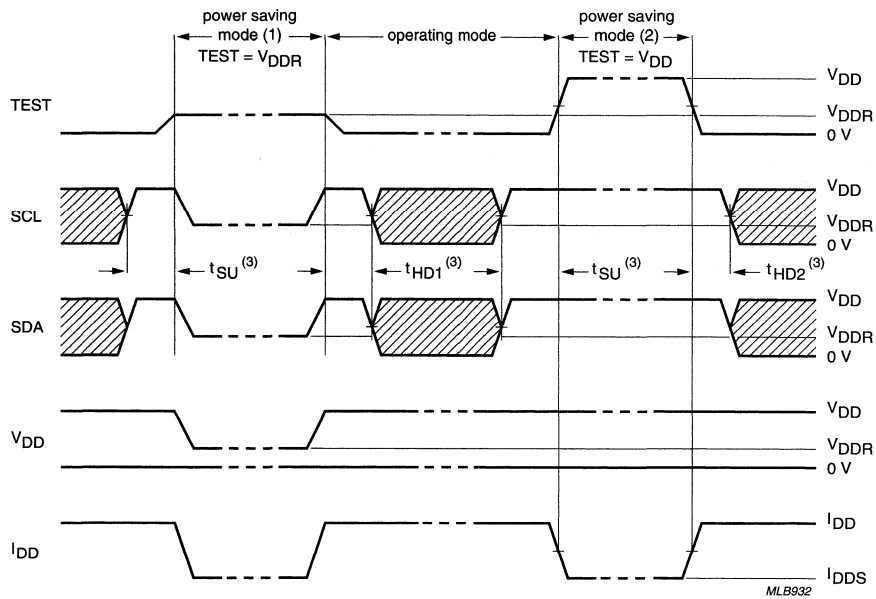


Fig.12 Slave address.

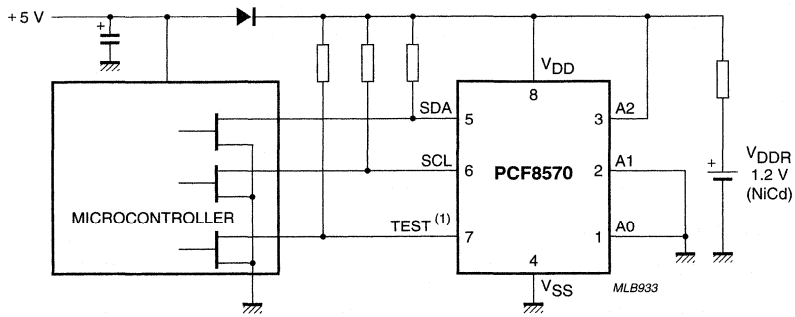
13.3 Power-saving mode

With the condition TEST = V_{DD} or V_{DDR} the PCF8570 goes into the power-saving mode and I²C-bus logic is reset.



(1) Power-saving mode without 5 V supply voltage.
(2) Power-saving mode with 5 V supply voltage.
(3) t_{SU} and $t_{HD1} \geq 4$ µs and $t_{HD2} \geq 50$ µs.

Fig.13 Timing for power-saving mode.



It is recommended that a 4.7 μF/10 V solid aluminium capacitor (SAL) be connected between V_{DD} and V_{SS}.

(1) In the operating mode TEST = 0 V; in the power-saving mode TEST = V_{DDR}.

Fig.14 Application example for power-saving mode.

CONTENTS

Clock/calendar with Power Fail Detector PCF8573

1 FEATURES

- Serial input/output I²C-bus interface for minutes, hours, days and months
- Additional pulse outputs for seconds and minutes
- Alarm register for presetting a time for alarm or remote switching functions
- On-chip power fail detector
- Separate ground pin for the clock allows easy implementation of battery back-up during supply interruption
- Crystal oscillator control (32.768 kHz)
- Low power consumption.

2 GENERAL DESCRIPTION

The PCF8573 is a low threshold, CMOS circuit that functions as a real time clock/calendar. Addresses and data are transferred serially via the two-line bidirectional I²C-bus.

The IC incorporates an addressable time counter and an addressable alarm register for minutes, hours, days and months. Three special control/status flags, COMP, POWF and NODA, are also available. Back-up for the clock during supply interruptions is provided by a 1.2 V nickel cadmium battery. The time base is generated from a 32.768 kHz crystal-controlled oscillator.

3 QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
$V_{DD} - V_{SS1}$	supply voltage, clock (pin 16 to pin 15)	1.1	–	6.0	V
$V_{DD} - V_{SS2}$	supply voltage, I²C-bus (pin 16 to pin 8)	2.5	–	6.0	V
f_{osc}	crystal oscillator frequency	–	32.768	–	kHz

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8573P	DIP16	plastic dual in-line package; 16 leads (300 mil); long body	SOT38-1
PCF8573T	SO16	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1

5 BLOCK DIAGRAM

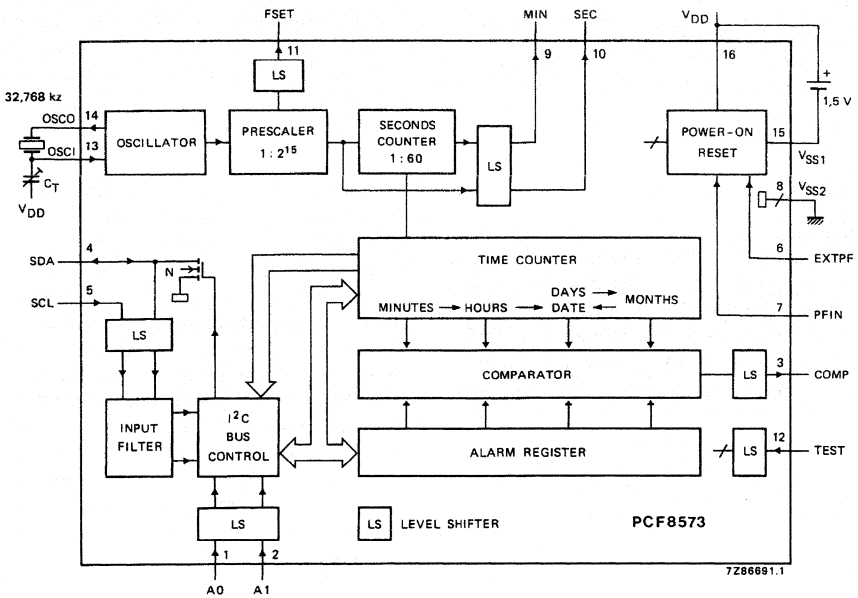


Fig.1 Block diagram.

6 PINNING

SYMBOL	PIN	DESCRIPTION
A0	1	address input
A1	2	address input
COMP	3	comparator output
SDA	4	serial data line; I^2C-bus
SCL	5	serial clock line; I^2C-bus
EXTPF	6	enable power fail flag input
PFIN	7	power fail flag input
V_{SS2}	8	negative supply 2 (I^2C interface)
MIN	9	one pulse per minute output
SEC	10	one pulse per second output
FSET	11	oscillator tuning output
TEST	12	test input; connect to V_{SS2} if not in use
OSCI	13	oscillator input
OSCO	14	oscillator input/output
V_{SS1}	15	negative supply 1 (clock)
V_{DD}	16	common positive supply

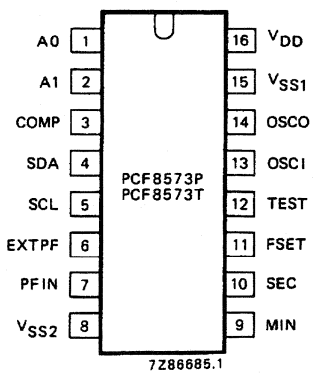


Fig.2 Pinning diagram.

7 FUNCTIONAL DESCRIPTION

7.1 Oscillator

The PCF8573 has an integrated crystal-controlled oscillator which provides the timebase for the prescaler. The frequency is determined by a single 32.76 kHz crystal connected between OSCI and OSCO. A trimmer is connected between OSCI and V_{DD}.

7.2 Prescaler and time counter

The prescaler provides a 128 Hz signal at the FSET output for fine adjustment of the crystal oscillator without loading it. The prescaler also generates a pulse once a second to advance the seconds counter. The carry of the prescaler and the seconds counter are available at the outputs SEC, MIN respectively, and are also readable via the I²C-bus. The mark-to-space ratio of both signals is 1 : 1. The time counter is advanced one count by the falling edge of output signal MIN. A transition from HIGH-to-LOW of output signal SEC triggers MIN to change state. The time counter counts minutes, hours, days and months, and provides a full calendar function which needs to be corrected only once every four years - to allow for leap-year. Cycle lengths are shown in Table 1.

7.3 Alarm register

The alarm register is a 24-bit memory. It stores the time-point for the next setting of the status flag COMP. Details of writing and reading of the alarm register are included in the description of the characteristics of the I²C-bus.

7.4 Comparator

The comparator compares the contents of the alarm register and the time counter, each with a length of 24 bits. When these contents are equal the flag COMP will be set 4 ms after the falling edge of MIN. This set condition occurs once at the beginning of each minute. This information is latched, but can be cleared by an instruction via the I²C-bus. A clear instruction may be transmitted immediately after the flag is set and will be executed. Flag COMP information is also available at the output COMP. The comparison may be based upon hours and minutes only if the internal flag NODA (no date) is set. Flag NODA can be set and cleared by separate instructions via the I²C-bus, but it is undefined until the first set or clear instruction has been received. Both COMP and NODA flags are readable via the I²C-bus.

Table 1 Cycle length of the time counter

UNIT	NUMBER OF BITS	COUNTING CYCLE	CARRY FOR FOLLOWING UNIT	CONTENT OF MONTH COUNTER
minutes	7	00 to 59	59 → 00	
hours	6	00 to 23	23 → 00	
days(1)	6	01 to 28	28 → 01	2 (note 1)
			or 29 → 01	2 (note 1)
		01 to 30	30 → 01	4, 6, 9, 11
		01 to 31	31 → 01	1, 3, 5, 7, 8, 10, 12
months	5	01 to 12	12 → 01	

Note

1. During February of a leap-year the 'Time Counter Days' may be set to 29 by directly writing into it using the 'execute address' function. Leap-years must be tracked by the system software.

7.5 Power on/power fail detection

If the voltage $V_{DD} - V_{SS1}$ falls below a certain value the operation of the clock becomes undefined. Thus a warning signal is required to indicate that faultless operation of the clock is not guaranteed. This information is latched in a flag called POWF (Power Fail) and remains latched after restoration of the correct supply voltage until a write procedure with EXECUTE ADDRESS has been received. The flag POWF can be set by an internally generated power fail level-discriminator signal for application with ($V_{DD} - V_{SS1}$) greater than V_{TH1}, or by an externally generated power fail signal for application with ($V_{DD} - V_{SS1}$) less than V_{TH1}. The external signal must be applied to the input PFIN. The input stage operates with signals of slow rise and fall times. Internally or externally controlled POWF can be selected by input EXTPF as shown in Table 2.

Table 2 Power fail selection

EXTPF(1)	PFIN(1)	FUNCTION
0	0	power fail is sensed internally
0	1	test mode
1	0	power fail is sensed externally
1	1	no power fail sensed

Note

1. 0 = V_{SS1} (LOW); 1 = V_{DD} (HIGH).

The external power fail control operates by absence of the $V_{DD} - V_{SS2}$ supply. Therefore the input levels applied to PFIN and EXTPF must be within the range of V_{DD}–V_{SS1}. A LOW level at PFIN indicates a power fail. POWF is readable via the I^2C-bus. A power-on reset for the I^2C-bus control is generated on-chip when the supply voltage $V_{DD} - V_{SS2}$ is less than V_{TH2}.

7.6 Interface level shifters

The level shifters adjust the 5 V operating voltage ($V_{DD} - V_{SS2}$) of the microcontroller to the internal supply voltage ($V_{DD} - V_{SS1}$) of the clock/calendar. The oscillator and counter are not influenced by the $V_{DD} - V_{SS2}$ supply voltage. If the voltage $V_{DD} - V_{SS2}$ is absent ($V_{DD} = V_{SS2}$) the output signal of the level shifter is HIGH because V_{DD} is the common node of the $V_{DD} - V_{SS2}$ and the $V_{DD} - V_{SS1}$ supplies. Because the level shifters invert the input signals, the internal circuit behaves as if a LOW signal is present on the inputs. FSET, SEC, MIN and COMP are CMOS push-pull output stages. The driving capability of these outputs is lost when the supply voltage $V_{DD} - V_{SS2} = 0$.

8 CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

8.1 Bit transfer (see Fig.3)

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

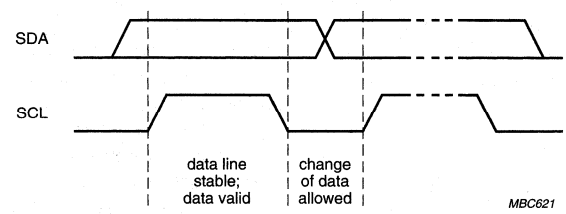


Fig.3 Bit transfer.

8.2 Start and stop conditions (see Fig.4)

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

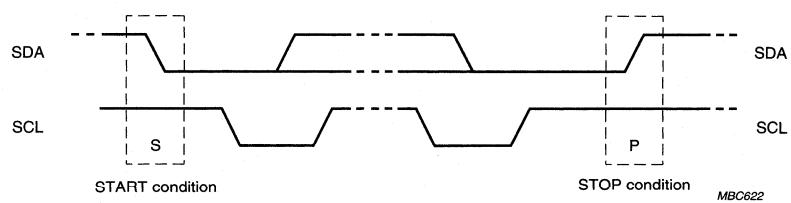


Fig.4 Definition of start and stop conditions.

8.3 System configuration (see Fig.5)

A device generating a message is a 'transmitter', a device receiving a message is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves'.

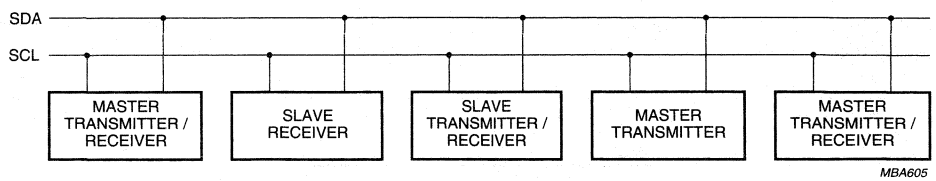


Fig.5 System configuration.

8.4 Acknowledge (see Fig.6)

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by **not** generating an acknowledge on the **last byte** that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition, see Figs. 9 and 10.

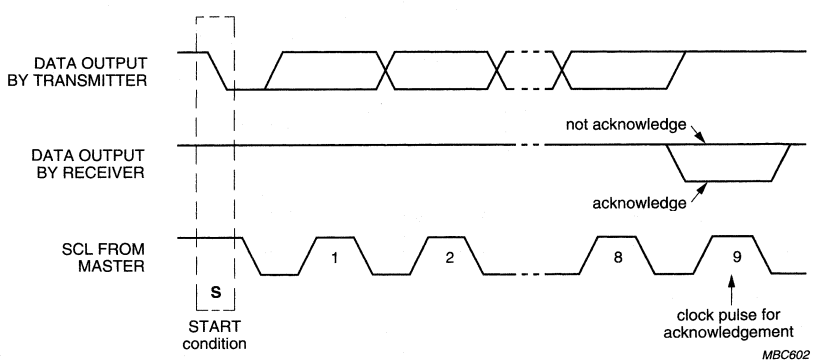


Fig.6 Acknowledgment on the I²C-bus.

9 I²C-BUS PROTOCOL

9.1 Addressing

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure.

The clock/calendar acts as a slave receiver or slave transmitter. Therefore the clock signal SCL is only an input signal, but the data signal SDA is a bidirectional line.

The clock/calendar slave address is shown in Fig.7. Bits A0 and A1 correspond to the two hardware address pins A0 and A1. Connecting these to V_{DD} or V_{SS} allows the device to have 1 of 4 different addresses.

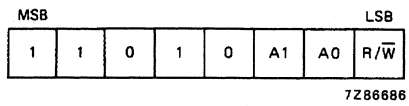


Fig.7 Slave address.

9.2 Clock/calendar READ/WRITE cycles

The I²C-bus configuration for different clock/calendar READ and WRITE cycles is shown in Figs 8, 9 and 10.

The write cycle is used to set the time counter, the alarm register and the flags. The transmission of the clock/calendar address is followed by the MODE-POINTER-word which contains a CONTROL-nibble (Table 3) and an ADDRESS-nibble (Table 4). The ADDRESS-nibble is valid only if the preceding CONTROL-nibble is set to EXECUTE ADDRESS. The third transmitted word contains the data to be written into the time counter or alarm register.

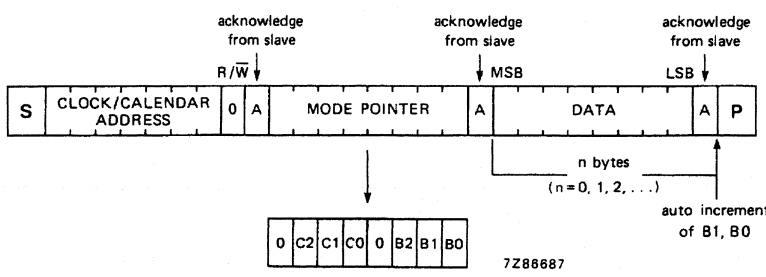
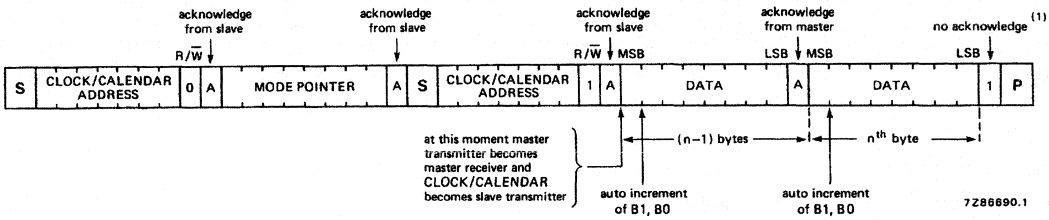
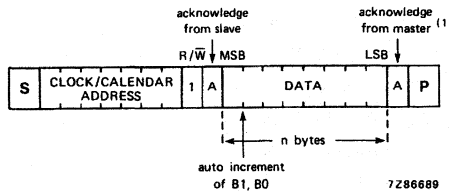


Fig.8 Master transmitter transmits to clock/calendar slave receiver.



(1) The master receiver must signal an end of data to the slave transmitter by **not** generating an acknowledge on the **last byte** that has been clocked out of the slave.

Fig.9 Master transmitter reads clock/calendar after setting mode pointer.



(1) The master receiver must signal an end of data to the slave transmitter by **not** generating an acknowledge on the **last byte** that has been clocked out of the slave.

Fig.10 Master reads clock/calendar immediately after first byte.

Table 3 MODE-POINTER-word, CONTROL-nibble (bits 8, 7, 6 and 5)

BIT 8	C2	C1	C0	FUNCTION
0	0	0	0	execute address
0	0	0	1	read control/status flags
0	0	1	0	reset prescaler, including seconds counter; without carry for minute counter
0	0	1	1	time adjust, with carry for minute counter (note 1)
0	1	0	0	reset NODA flag
0	1	0	1	set NODA flag
0	1	1	0	reset COMP flag

Note

1. If the seconds counter is below 30 there is no carry. This causes a time adjustment of max. −30 s. From the count 30 there is a carry which adjusts the time by max. +30 s.

Table 4 MODE-POINTER-word, ADDRESS-nibble (bits 4, 3, 2 and 1)

BIT 4	B2	B1	B0	ADDRESSED TO:
0	0	0	0	time counter hours
0	0	0	1	time counter minutes
0	0	1	0	time counter days
0	0	1	1	time counter months
0	1	0	0	alarm register hours
0	1	0	1	alarm register minutes
0	1	1	0	alarm register days
0	1	1	1	alarm register months

At the end of each data word the address bits B1, B0 will be incremented automatically provided the preceding CONTROL-nibble is set to EXECUTE ADDRESS. There is no carry to B2.

Table 5 shows the placement of the BCD upper and lower digits in the DATA byte for writing into the addressed part of the time counter and alarm register respectively.

Table 6 shows the acknowledgement response of the clock calendar as a slave receiver.

Table 5 Placement of BCD digits in the DATA byte; note 1

MSB			DATA				LSB	
UPPER DIGIT				LOWER DIGIT				
UD	UC	UB	UA	LD	LC	LB	LA	ADDRESSED TO:
X	X	D	D	D	D	D	D	hours
X	D	D	D	D	D	D	D	minutes
X	X	D	D	D	D	D	D	days
X	X	X	D	D	D	D	D	months

Note

1. 'X' is the don't care bit; 'D' is the data bit.

Acknowledgement response of the PCF8573 as slave-receiver is shown in Table 6. Note that data is only associated with the 'execute address' function where C0, C1, C2 = 0, 0, 0.

Table 6 Slave receiver acknowledgement; note 1

MODE POINTER								ACKNOWLEDGE ON BYTE:		
BIT 8	C2	C1	C0	BIT 4	B2	B1	B0	ADDRESS	MODE POINTER	DATA
0	0	0	0	0	X	X	X	yes	yes	yes
0	0	0	0	1	X	X	X	yes	no	no
0	0	0	1	X	X	X	X	yes	yes	no
0	0	1	0	X	X	X	X	yes	yes	no
0	0	1	1	X	X	X	X	yes	yes	no
0	1	0	0	X	X	X	X	yes	yes	no
0	1	0	1	X	X	X	X	yes	yes	no
0	1	1	0	X	X	X	X	yes	yes	no
0	1	1	1	X	X	X	X	yes	no	no
1	X	X	X	X	X	X	X	yes	no	no

Note

1. 'X' is 'don't care'.

To read the addressed part of the time counter and alarm register, plus information from specified control/status flags, the BCD digits in the DATA byte are organized as shown in Table 7.

The status of the CONTROL-nibble of the MODE-POINTER-WORD (C2, C1, C0) remains unchanged until re-written.

Table 7 Organization of the BCD digits in the DATA byte; note 1

MSB			DATA				LSB	
UPPER DIGIT				LOWER DIGIT				
UD	UC	UB	UA	LD	LC	LB	LA	ADDRESSED TO:
0	0	D	D	D	D	D	D	hours
0	D	D	D	D	D	D	D	minutes
0	0	D	D	D	D	D	D	days
0	0	0	D	D	D	D	D	months
0	0	0	m	s	NODA	COMP	POWF	control/status flags

Note

1. 'D' is the data bit; 'm' = minutes; 's' = seconds.

10 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$V_{DD} - V_{SS1}$	supply voltage (pin 16 to pin 15)	−0.3	+8.0	V
$V_{DD} - V_{SS2}$	supply voltage (pin 16 to pin 8)	−0.3	+8.0	V
V_I	input voltage			
	pins 4 and 5 (with input impedance of minimum 500 Ω)	$V_{SS2} - 0.8$	$V_{DD} + 0.8$	V
	pins 6, 7, 13 and 14	$V_{SS1} - 0.6$	$V_{DD} + 0.6$	V
	any other pin	$V_{SS2} - 0.6$	$V_{DD} + 0.6$	V
I_I	DC input current	–	10	mA
I_O	DC output current	–	10	mA
P_{tot}	total power dissipation per package	–	200	mW
P_O	power dissipation per output	–	100	mW
T_{amb}	operating ambient temperature	−40	+85	°C
T_{stg}	storage temperature	−55	+125	°C

11 HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices. Advice can be found in Data Handbook IC12 under *"Handling MOS Devices"*.

12 DC CHARACTERISTICS

V_{SS2} = 0 V; T_{amb} = −40 to + 85 °C unless otherwise specified. Typical values at T_{amb} = 25 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
$V_{DD} - V_{SS2}$	supply voltage (I^2C interface)		2.5	5.0	6.0	V
$V_{DD} - V_{SS1}$	supply voltage (clock)	$t_{HD;DAT} \geq 300$ ns	1.1	1.5	$V_{DD} - V_{SS2}$	V
I_{SS1}	supply current at V_{SS1} (pin 15)	see Fig.11				
		$V_{DD} - V_{SS1}$ = 1.5 V	–	−3	−10	µA
		$V_{DD} - V_{SS1}$ = 5 V	–	−12	−50	µA
I_{SS2}	supply current at V_{SS2} (pin 8)	$V_{DD} - V_{SS2}$ = 5 V; I_O = 0 all outputs	–	–	−50	µA
Input SCL, input/output SDA						
V_{IL}	LOW level input voltage		–	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	–	V
I_{LI}	input leakage current	$V_I = V_{SS2}$ or V_{DD}	−1	–	+1	µA
C_i	input capacitance		–	–	7	pF
Inputs A0, A1, TEST						
V_{IL}	LOW level input voltage		–	–	$0.2V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	–	V
I_{LI}	input leakage current	$V_I = V_{SS2}$ or V_{DD}	−250	–	+250	nA
Inputs EXTPF, PFIN						
V_{IL}	LOW level input voltage		0	–	$0.2V_{DD} - V_{SS1}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD} - V_{SS1}$	–	–	V
I_{LI}	input leakage current	$V_I = V_{SS1}$ to V_{DD}	−1.0	–	+1.0	µA
		$V_I = V_{SS1}$ to V_{DD}; T_{amb} = 25 °C	−0.1	–	+0.1	µA
Output SDA (n channel open-drain)						
V_{OL}	LOW level output voltage	output ON; I_O = 3 mA; $V_{DD} - V_{SS2}$ = 2.5 to 6 V	–	–	0.4	V
I_{LI}	input leakage current	$V_{DD} - V_{SS2}$ = 6 V; V_O = 6 V	−1.0	–	+1.0	µA
Output SEC, MIN, COMP, FSET (normal buffer outputs)						
V_{OL}	LOW level output voltage	$V_{DD} - V_{SS2}$ = 2.5 V; I_O = 0.3 mA	–	–	0.4	V
		$V_{DD} - V_{SS2}$ = 4 to 6 V; I_O = 1.6 mA	–	–	0.4	V
V_{OH}	HIGH level output voltage	$V_{DD} - V_{SS2}$ = 2.5 V; I_O = −0.1 mA	$V_{DD} - 0.4$	–	–	V
		$V_{DD} - V_{SS2}$ = 4 to 6 V; I_O = −0.5 mA	$V_{DD} - 0.4$	–	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Internal threshold voltages						
V_{TH1}	Power failure detection		1	1.2	1.4	V
V_{TH2}	Power-on reset		1.5	2.0	2.5	V

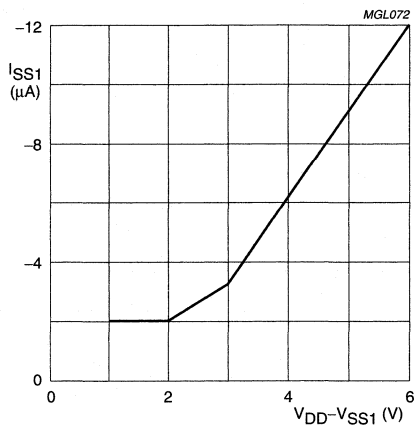


Fig.11 Typical supply current (I_{SS1}) as a function of clock supply voltage ($V_{DD} - V_{SS1}$) at T_{amb} = −40 to +85 °C.

13 AC CHARACTERISTICS

V_{SS2} = 0 V; T_{amb} = −40 to +85 °C unless otherwise specified. Typical values at T_{amb} = +25 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Rise and fall times of input signals						
t_r	rise time	input EXTPF	–	–	1	µs
		input PFIN	–	–	∞	µs
		all other inputs (levels between V_{IL} and V_{IH})	–	–	1	µs
t_f	fall time	input EXTPF	–	–	1	µs
		input PFIN	–	–	∞	µs
		all other inputs (levels between V_{IL} and V_{IH})	–	–	0.3	µs
Oscillator						
C_{osc}	integrated oscillator capacitance		–	40	–	pF
R_f	oscillator feedback resistance		–	3	–	MΩ
Δf_{osc}	oscillator stability	$\Delta(V_{DD} - V_{SS1})$ = 100 mV; T_{amb} = 25 °C; $(V_{DD} - V_{SS1})$ = 1.55 V	–	2×10^{-7}	–	
Quartz crystal parameters (f = 32.768 kHz)						
R_s	series resistance		–	–	40	kΩ
C_L	parallel load capacitance		–	10	–	pF
C_T	trimmer capacitance		5	–	25	pF
I²C-bus timing (see Fig.12; notes 1 and 2)						
f_{SCL}	SCL clock frequency		–	–	100	kHz
t_{SP}	tolerable spike width on bus		–	–	100	ns
t_{BUF}	bus free time		4.7	–	–	µs
$t_{SU;STA}$	START condition set-up time		4.7	–	–	µs
$t_{HD;STA}$	START condition hold time		4.0	–	–	µs
t_{LOW}	SCL LOW time		4.7	–	–	µs
t_{HIGH}	SCL HIGH time		4.0	–	–	µs
t_r	SCL and SDA rise time		–	–	1.0	µs
t_f	SCL and SDA fall time		–	–	0.3	µs
$t_{SU;DAT}$	data set-up time		250	–	–	ns
$t_{HD;DAT}$	data hold time		0	–	–	ns
$t_{VD;DAT}$	SCL LOW to data out valid		–	–	3.4	µs
$t_{SU;STO}$	STOP condition set-up time		4.0	–	–	µs

Notes

1. All timing values are valid within the operating supply voltage and ambient temperature range and reference to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.
2. A detailed description of the I²C-bus specification, with applications, is given in brochure *"The I²C-bus and how to use it"*. This brochure may be ordered using the code 9398 393 40011.

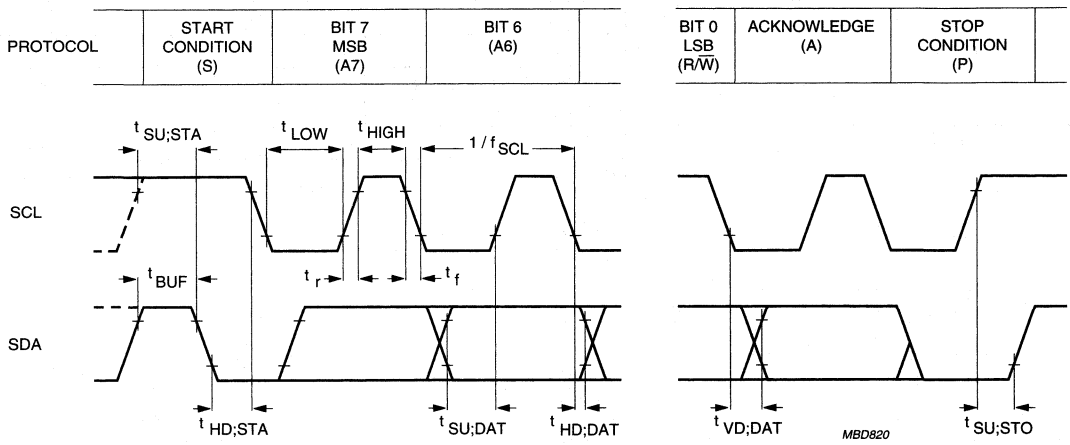


Fig.12 I²C-bus timing diagram; rise and fall times refer to V_{IL} and V_{IH}.

14 APPLICATION INFORMATION

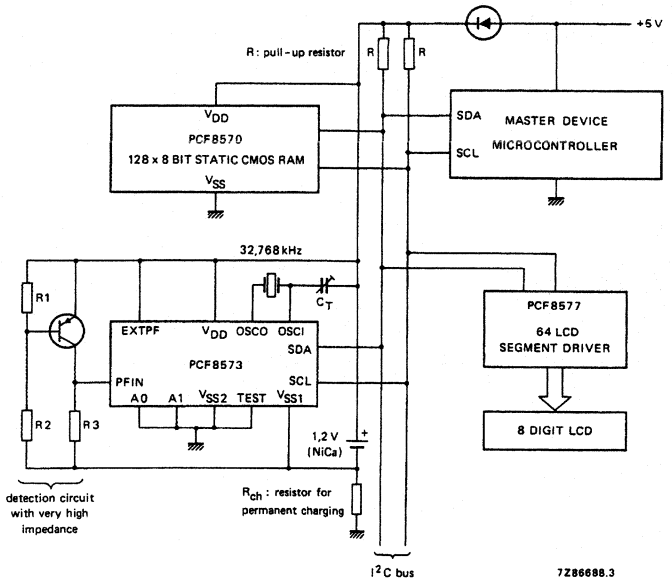


Fig.13 Application example of the PCF8573 clock/calendar with battery backup.

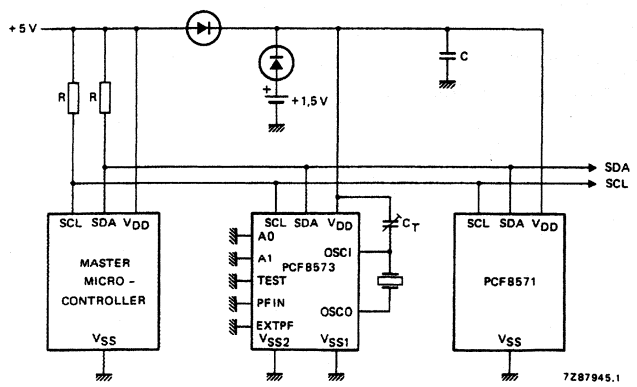


Fig.14 Application example of the PCF8573 with common V_{SS1} and V_{SS2} supply.

Remote 8-bit I/O expander for I²C-bus PCF8574

CONTENTS

Remote 8-bit I/O expander for I²C-bus PCF8574

1 FEATURES

- Operating supply voltage 2.5 to 6 V
- Low standby current consumption of 10 μA maximum
- I²C to parallel port expander
- Open-drain interrupt output
- 8-bit remote I/O port for the I²C-bus
- Compatible with most microcontrollers
- Latched outputs with high current drive capability for directly driving LEDs
- Address by 3 hardware address pins for use of up to 8 devices (up to 16 with PCF8574A)
- DIP16, or space-saving SO16 or SSOP20 packages.

2 GENERAL DESCRIPTION

The PCF8574 is a silicon CMOS circuit. It provides general purpose remote I/O expansion for most microcontroller families via the two-line bidirectional bus (I²C).

The device consists of an 8-bit quasi-bidirectional port and an I²C-bus interface. The PCF8574 has a low current consumption and includes latched outputs with high current drive capability for directly driving LEDs. It also possesses an interrupt line ($\overline{INT}$) which can be connected to the interrupt logic of the microcontroller. By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I²C-bus. This means that the PCF8574 can remain a simple slave device.

The PCF8574 and PCF8574A versions differ only in their slave address as shown in Fig.9.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8574P; PCF8574AP	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-1
PCF8574T; PCF8574AT	SO16	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1
PCF8574TS	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

4 BLOCK DIAGRAM

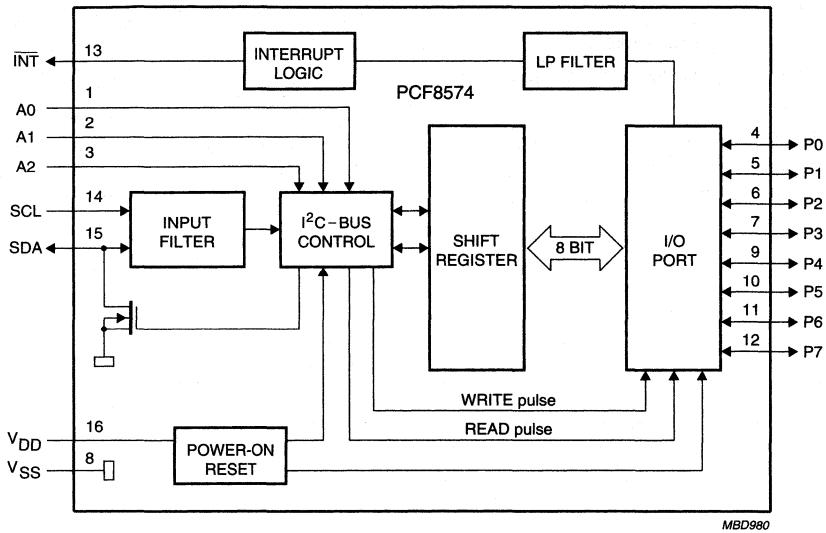


Fig.1 Block diagram (SOT38-1 and SOT162-1).

5 PINNING

SYMBOL	PIN		DESCRIPTION
	DIP16; SO16	SSOP20	
A0	1	6	address input 0
A1	2	7	address input 1
A2	3	9	address input 2
P0	4	10	quasi-bidirectional I/O 0
P1	5	11	quasi-bidirectional I/O 1
P2	6	12	quasi-bidirectional I/O 2
P3	7	14	quasi-bidirectional I/O 3
V_{SS}	8	15	supply ground
P4	9	16	quasi-bidirectional I/O 4
P5	10	17	quasi-bidirectional I/O 5
P6	11	19	quasi-bidirectional I/O 6
P7	12	20	quasi-bidirectional I/O 7
$\overline{INT}$	13	1	interrupt output (active LOW)
SCL	14	2	serial clock line
SDA	15	4	serial data line
V_{DD}	16	5	supply voltage
n.c.	–	3	not connected
n.c.	–	8	not connected
n.c.	–	13	not connected
n.c.	–	18	not connected

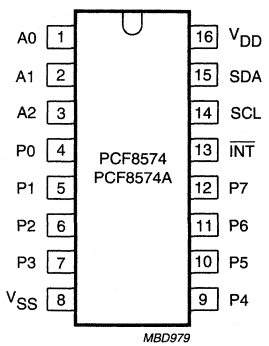


Fig.2 Pin configuration (DIP16; SO16).

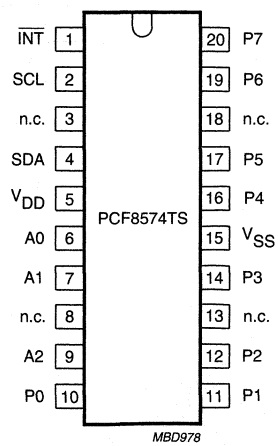


Fig.3 Pin configuration (SSOP20).

6 CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

6.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see Fig.4).

6.2 Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S).
A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P) (see Fig.5).

6.3 System configuration

A device generating a message is a 'transmitter', a device receiving is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves' (see Fig.6).

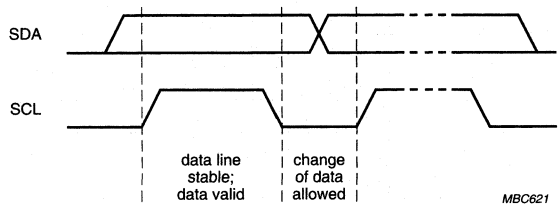


Fig.4 Bit transfer.

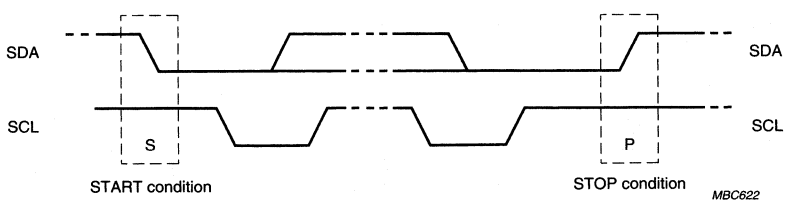


Fig.5 Definition of start and stop conditions.

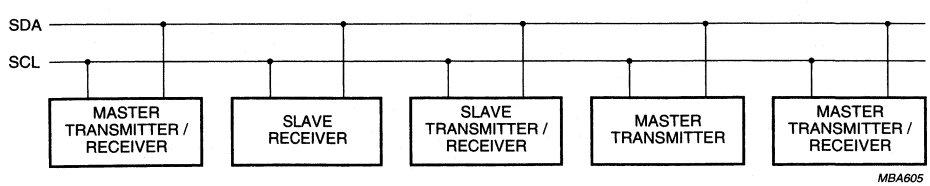


Fig.6 System configuration.

6.4 Acknowledge

The number of data bytes transferred between the start and the stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account.

A master receiver must signal an end of data to the transmitter by **not** generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

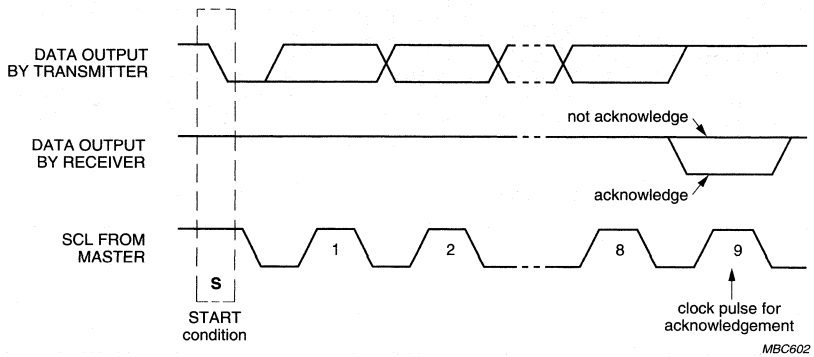


Fig.7 Acknowledgment on the I²C-bus.

7 FUNCTIONAL DESCRIPTION

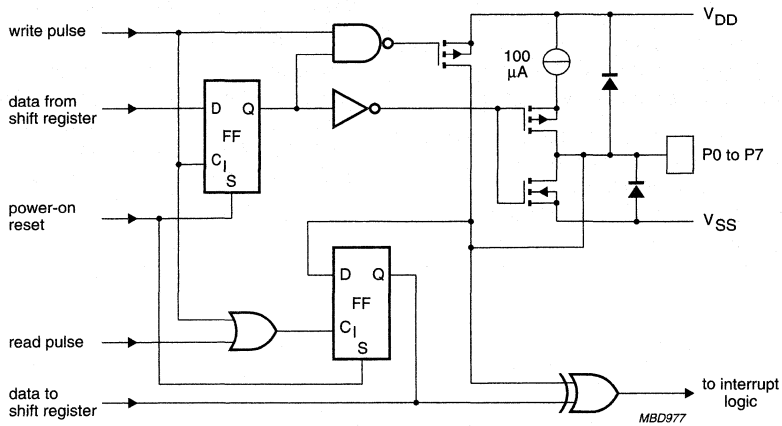
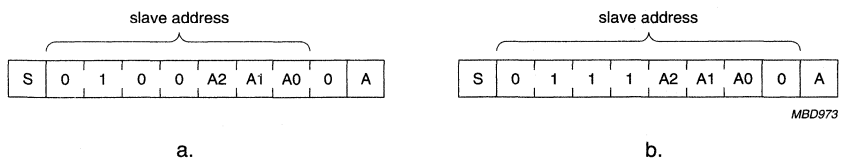


Fig.8 Simplified schematic diagram of each I/O.

7.1 Addressing

For addressing see Figs 9, 10 and 11.



(a) PCF8574.
(b) PCF8574A.

Fig.9 PCF8574 and PCF8574A slave addresses.

Each of the PCF8574's eight I/Os can be independently used as an input or output. Input data is transferred from the port to the microcontroller by the READ mode (see Fig.11). Output data is transmitted to the port by the WRITE mode (see Fig.10).

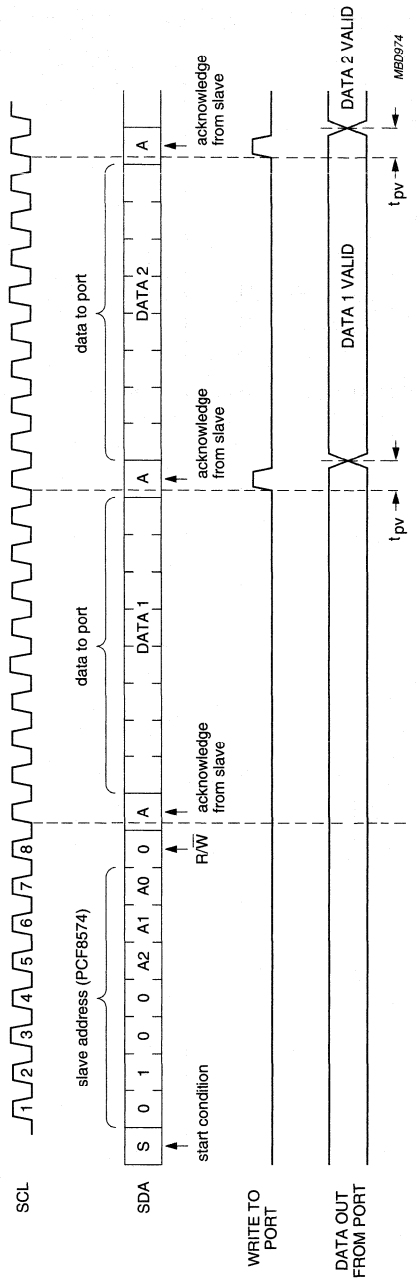
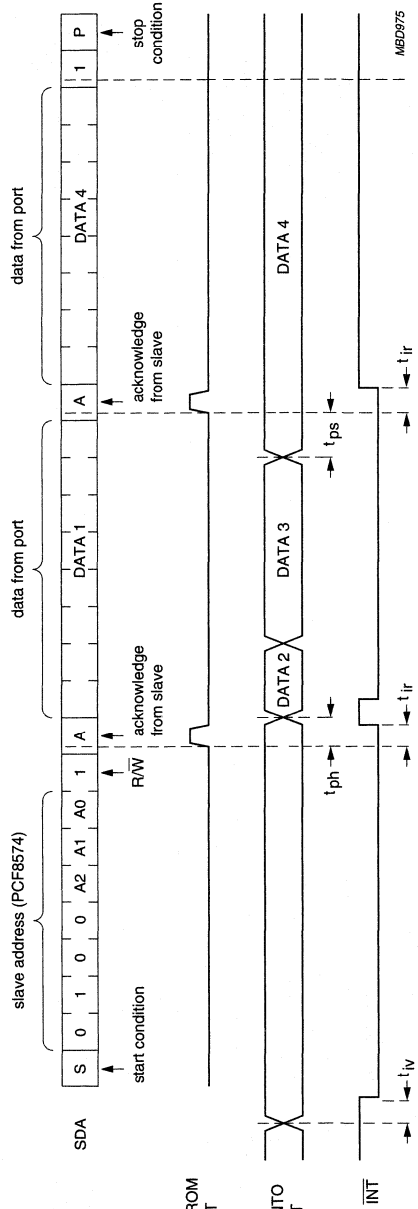


Fig.10 WRITE mode (output).



A LOW-to-HIGH transition of SDA, while SCL is HIGH is defined as the stop condition (P). Transfer of data can be stopped at any moment by a stop condition. When this occurs, data present at the last acknowledge phase is valid (output mode). Input data is lost.

Fig.11 READ mode (input).

7.2 **Interrupt** (see Figs 12 and 13)

The PCF8574 provides an open drain output ($\overline{INT}$) which can be fed to a corresponding input of the microcontroller. This gives these chips a type of master function which can initiate an action elsewhere in the system.

An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time t_{iv} the signal $\overline{INT}$ is valid.

Resetting and reactivating the interrupt circuit is achieved when data on the port is changed to the original setting or data is read from or written to the port which has generated the interrupt.

Resetting occurs as follows:

- In the READ mode at the acknowledge bit after the rising edge of the SCL signal
- In the WRITE mode at the acknowledge bit after the HIGH-to-LOW transition of the SCL signal
- Interrupts which occur during the acknowledge clock pulse may be lost (or very short) due to the resetting of the interrupt during this pulse.

Each change of the I/Os after resetting will be detected and, after the next rising clock edge, will be transmitted as $\overline{INT}$. Reading from or writing to another device does not affect the interrupt circuit.

7.3 **Quasi-bidirectional I/Os** (see Fig.14)

A quasi-bidirectional I/O can be used as an input or output without the use of a control signal for data direction. At power-on the I/Os are HIGH. In this mode only a current source to V_{DD} is active. An additional strong pull-up to V_{DD} allows fast rising edges into heavily loaded outputs. These devices turn on when an output is written HIGH, and are switched off by the negative edge of SCL. The I/Os should be HIGH before being used as inputs.

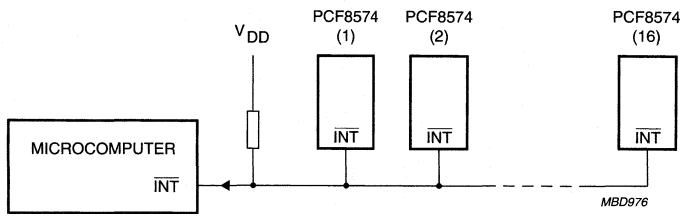


Fig.12 Application of multiple PCF8574s with interrupt.

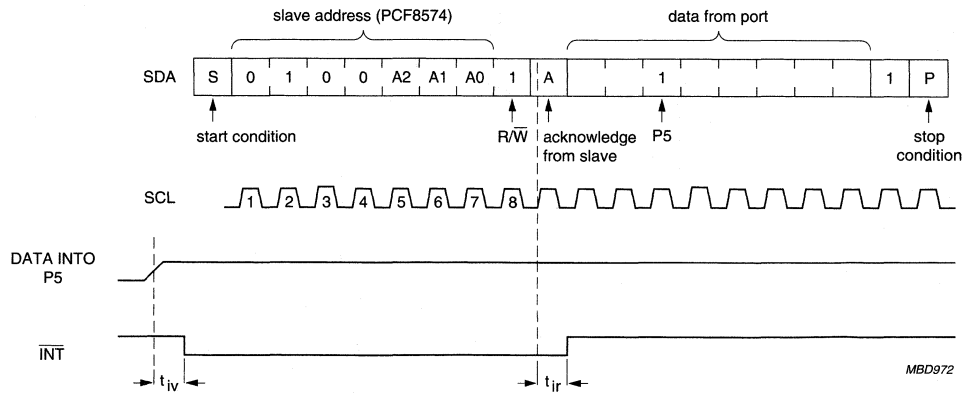


Fig.13 Interrupt generated by a change of input to I/O P5.

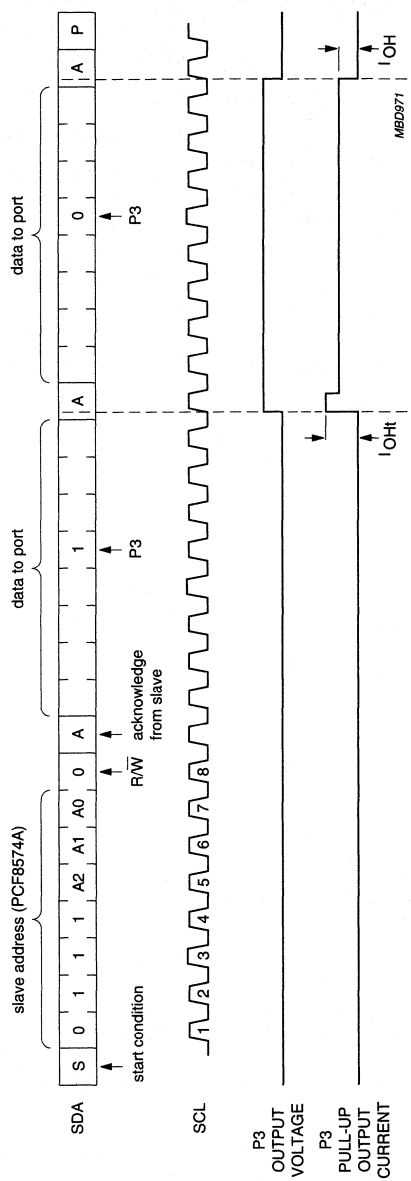


Fig.14 Transient pull-up current I_{OHt} while P3 changes from LOW-to-HIGH and back to LOW.

8 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.5	+7.0	V
V_I	input voltage	V_{SS} − 0.5	V_{DD} + 0.5	V
I_I	DC input current	−	±20	mA
I_O	DC output current	−	±25	mA
I_{DD}	supply current	−	±100	mA
I_{SS}	supply current	−	±100	mA
P_{tot}	total power dissipation	−	400	mW
P_O	power dissipation per output	−	100	mW
T_{stg}	storage temperature	−65	+150	°C
T_{amb}	operating ambient temperature	−40	+85	°C

9 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take precautions appropriate to handling MOS devices. Advice can be found in Data Handbook IC12 under *"Handling MOS Devices"*.

10 DC CHARACTERISTICS

V_{DD} = 2.5 to 6 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		2.5	−	6.0	V
I_{DD}	supply current	operating mode; V_{DD} = 6 V; no load; $V_I = V_{DD}$ or V_{SS}; f_{SCL} = 100 kHz	−	40	100	µA
I_{stb}	standby current	standby mode; V_{DD} = 6 V; no load; $V_I = V_{DD}$ or V_{SS}	−	2.5	10	µA
V_{POR}	Power-on reset voltage	V_{DD} = 6 V; no load; $V_I = V_{DD}$ or V_{SS}; note 1	−	1.3	2.4	V
Input SCL; input/output SDA						
V_{IL}	LOW level input voltage		−0.5	−	$+0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	−	V_{DD} + 0.5	V
I_{OL}	LOW level output current	V_{OL} = 0.4 V	3	−	−	mA
I_L	leakage current	$V_I = V_{DD}$ or V_{SS}	−1	−	+1	µA
C_i	input capacitance	$V_I = V_{SS}$	−	−	7	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I/Os						
V_{IL}	LOW level input voltage		−0.5	−	$+0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	−	$V_{DD} + 0.5$	V
$I_{IHL(max)}$	maximum allowed input current through protection diode	$V_I \geq V_{DD}$ or $V_I \leq V_{SS}$	−	−	±400	μA
I_{OL}	LOW level output current	V_{OL} = 1 V; V_{DD} = 5 V	10	25	−	mA
I_{OH}	HIGH level output current	$V_{OH} = V_{SS}$	30	−	300	μA
I_{OHt}	transient pull-up current	HIGH during acknowledge (see Fig.14); $V_{OH} = V_{SS}$; V_{DD} = 2.5 V	−	−1	−	mA
C_i	input capacitance		−	−	10	pF
C_o	output capacitance		−	−	10	pF
Port timing; $C_L \leq$ 100 pF (see Figs 10 and 11)						
t_{pv}	output data valid		−	−	4	μs
t_{su}	input data set-up time		0	−	−	μs
t_h	input data hold time		4	−	−	μs
Interrupt $\overline{INT}$ (see Fig.13)						
I_{OL}	LOW level output current	V_{OL} = 0.4 V	1.6	−	−	mA
I_L	leakage current	$V_I = V_{DD}$ or V_{SS}	−1	−	+1	μA
TIMING; $C_L \leq$ 100 pF						
t_{iv}	input data valid time		−	−	4	μs
t_{ir}	reset delay time		−	−	4	μs
Select inputs A0 to A2						
V_{IL}	LOW level input voltage		−0.5	−	$+0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	−	$V_{DD} + 0.5$	V
I_{LI}	input leakage current	pin at V_{DD} or V_{SS}	−250	−	+250	nA

Note

1. The Power-on reset circuit resets the I²C-bus logic with $V_{DD} < V_{POR}$ and sets all I/Os to logic 1 (with current source to V_{DD}).

11 I²C-BUS TIMING CHARACTERISTICS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
I²C-BUS TIMING (see Fig.15; note 1)					
f_{SCL}	SCL clock frequency	–	–	100	kHz
t_{SW}	tolerable spike width on bus	–	–	100	ns
t_{BUF}	bus free time	4.7	–	–	µs
$t_{SU;STA}$	START condition set-up time	4.7	–	–	µs
$t_{HD;STA}$	START condition hold time	4.0	–	–	µs
t_{LOW}	SCL LOW time	4.7	–	–	µs
t_{HIGH}	SCL HIGH time	4.0	–	–	µs
t_r	SCL and SDA rise time	–	–	1.0	µs
t_f	SCL and SDA fall time	–	–	0.3	µs
$t_{SU;DAT}$	data set-up time	250	–	–	ns
$t_{HD;DAT}$	data hold time	0	–	–	ns
$t_{VD;DAT}$	SCL LOW to data out valid	–	–	3.4	µs
$t_{SU;STO}$	STOP condition set-up time	4.0	–	–	µs

Note

1. All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

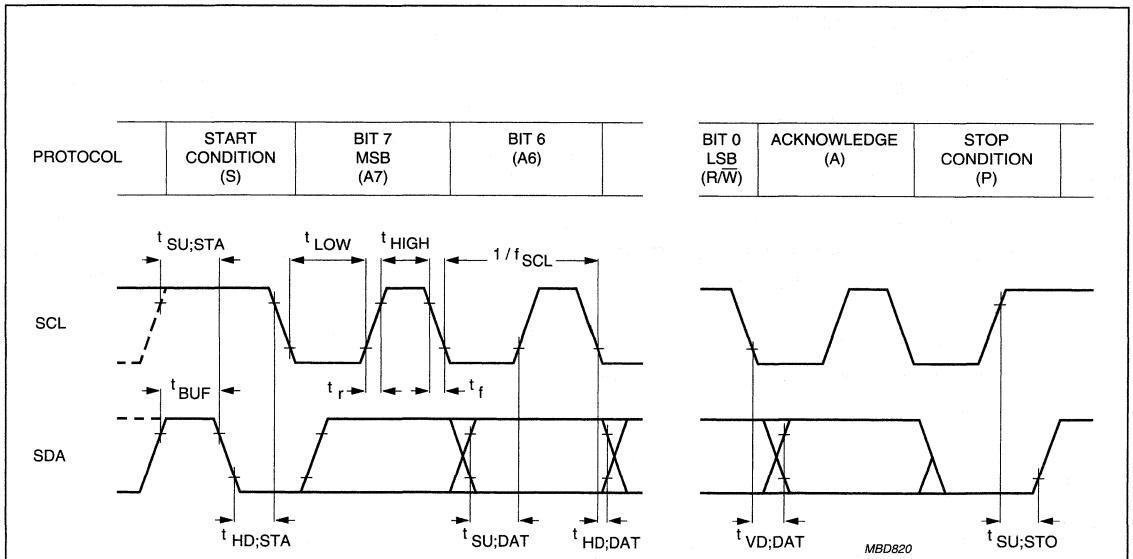


Fig.15 I²C-bus timing diagram.

CONTENTS

Remote 16-bit I/O expander for I²C-bus PCF8575

1 FEATURES

- Operating supply voltage 2.5 to 5.5 V
- Low standby current consumption of 10 μA maximum
- I²C-bus to parallel port expander
- 400 kbits/s FAST I²C-bus
- Open-drain interrupt output
- 16-bit remote I/O port for the I²C-bus
- Compatible with most microcontrollers
- Latched outputs with high current drive capability for directly driving LEDs
- Address by 3 hardware address pins for use of up to 8 devices
- SSOP24 package.

2 GENERAL DESCRIPTION

The PCF8575 is a silicon CMOS circuit. It provides general purpose remote I/O expansion for most microcontroller families via the two-line bidirectional bus (I²C-bus).

The device consists of a 16-bit quasi-bidirectional port and an I²C-bus interface. The PCF8575 has a low current consumption and includes latched outputs with high current drive capability for directly driving LEDs. It also possesses an interrupt line ($\overline{INT}$) which can be connected to the interrupt logic of the microcontroller. By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I²C-bus. This means that the PCF8575 is an I²C-bus slave transmitter/receiver.

Every data transmission from the PCF8575 must consist of an even number of bytes, the first byte will be referred to as P07 to P00 and the second byte as P17 to P10. The third will be referred to as P07 to P00 and so on.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8575TS	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1

4 BLOCK DIAGRAM

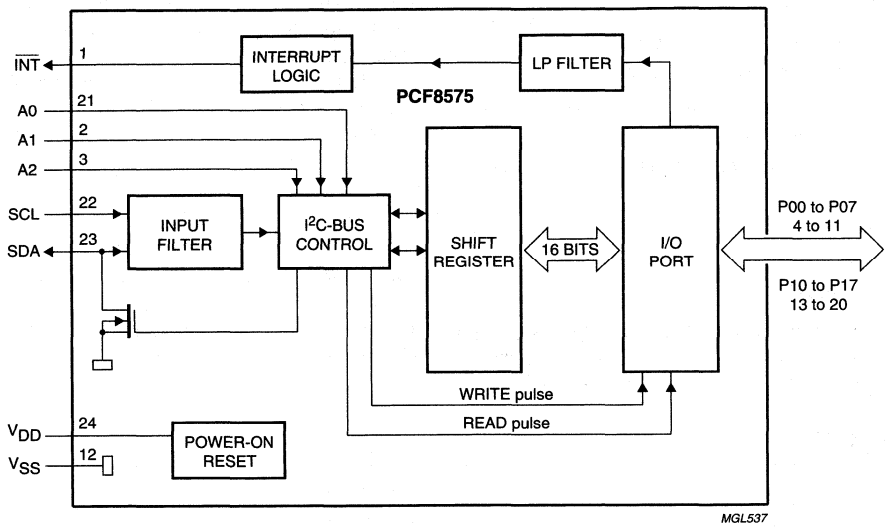


Fig.1 Block diagram.

5 PINNING

SYMBOL	PIN	DESCRIPTION
$\overline{INT}$	1	interrupt output (active LOW)
A1	2	address input 1
A2	3	address input 2
P00	4	quasi-bidirectional I/O 00
P01	5	quasi-bidirectional I/O 01
P02	6	quasi-bidirectional I/O 02
P03	7	quasi-bidirectional I/O 03
P04	8	quasi-bidirectional I/O 04
P05	9	quasi-bidirectional I/O 05
P06	10	quasi-bidirectional I/O 06
P07	11	quasi-bidirectional I/O 07
V_{SS}	12	supply ground
P10	13	quasi-bidirectional I/O 10
P11	14	quasi-bidirectional I/O 11
P12	15	quasi-bidirectional I/O 12
P13	16	quasi-bidirectional I/O 13
P14	17	quasi-bidirectional I/O 14
P15	18	quasi-bidirectional I/O 15
P16	19	quasi-bidirectional I/O 16
P17	20	quasi-bidirectional I/O 17
A0	21	address input 0
SCL	22	serial clock line input
SDA	23	serial data line input/output
V_{DD}	24	supply voltage

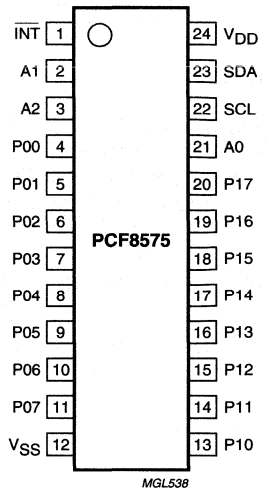


Fig.2 Pin configuration.

6 CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for bidirectional, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

6.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see Fig.3).

6.2 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S).

A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition P (see Fig.4).

6.3 System configuration

A device generating a message is a 'transmitter', a device receiving the message is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves' (see Fig.5).

6.4 Acknowledge

The number of data bytes transferred between the START and the STOP conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The transmitter must release the SDA line before the receiver can send an acknowledge bit.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account.

A master receiver must signal an end of data to the transmitter by **not** generating an acknowledge after the last byte that has been clocked out of the slave. This is done by the master receiver by holding the SDA line HIGH. In this event the transmitter must release the data line to enable the master to generate a STOP condition.

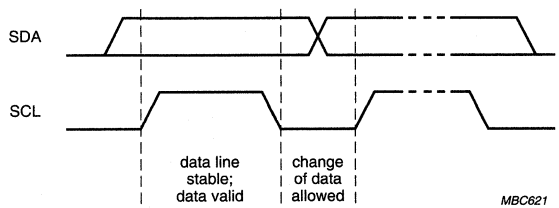


Fig.3 Bit transfer.

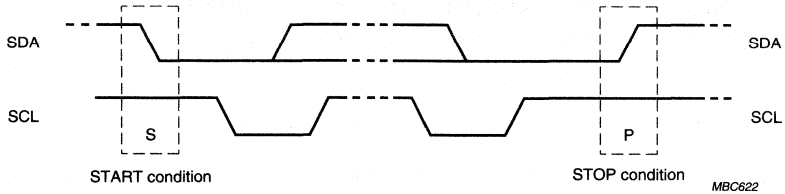


Fig.4 Definition of START and STOP conditions.

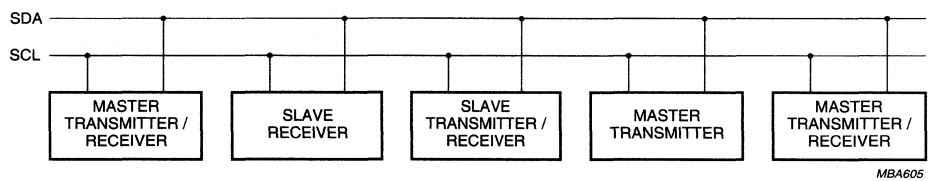


Fig.5 System configuration.

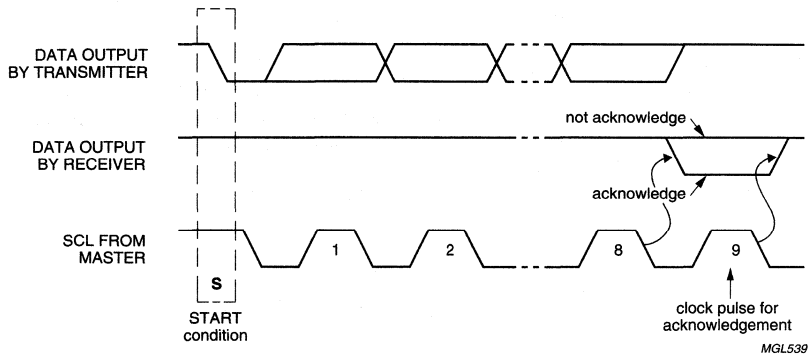


Fig.6 Acknowledgment on the I²C-bus.

7 FUNCTIONAL DESCRIPTION

7.1 Quasi-bidirectional I/Os

The PCF8575's 16 ports (see Fig.7) are entirely independent and can be used either as input or output ports. Input data is transferred from the ports to the microcontroller in the READ mode (see Fig.10). Output data is transmitted to the ports in the WRITE mode (see Fig.9).

This quasi-bidirectional I/O can be used as an input or output without the use of a control signal for data direction. At power-on the I/Os are HIGH. In this mode only a current source (I_{OH}) to V_{DD} is active. An additional strong pull-up to V_{DD} (I_{OHt}) allows fast rising edges into heavily loaded outputs. These devices turn on when an output is written HIGH, and are switched off by the negative edge of SCL. The I/Os should be HIGH before being used as inputs. After power-on as all the I/Os are set HIGH all of them can be used as input. Any change in setting of the I/Os as either inputs or outputs can be done with the write mode. Warning: If a HIGH is applied to an I/O which has been written earlier to LOW, a large current (I_{OL}) will flow to V_{SS}. (see Characteristics note 3).

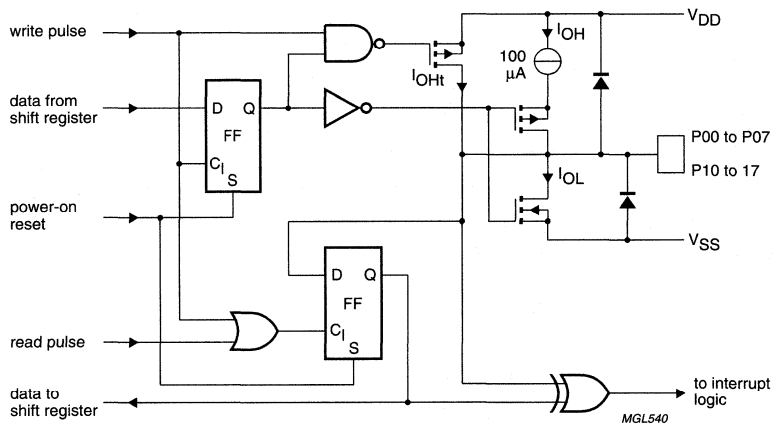


Fig.7 Simplified schematic diagram of each I/O.

7.2 Addressing

Figures 8, 9 and 10 show the address and timing diagrams. Before any data is transmitted or received the master must send the address of the receiver via the SDA line. The first byte transmitted after the START condition carries the address of the slave device and the read/write bit. The address of the slave device must not be changed between the START and the STOP conditions. The PCF8575 acts as a slave receiver or a slave transmitter.

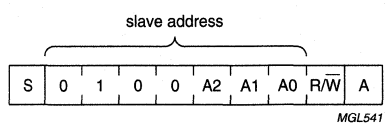


Fig.8 Byte containing the slave address and the R/$\overline{W}$ bits.

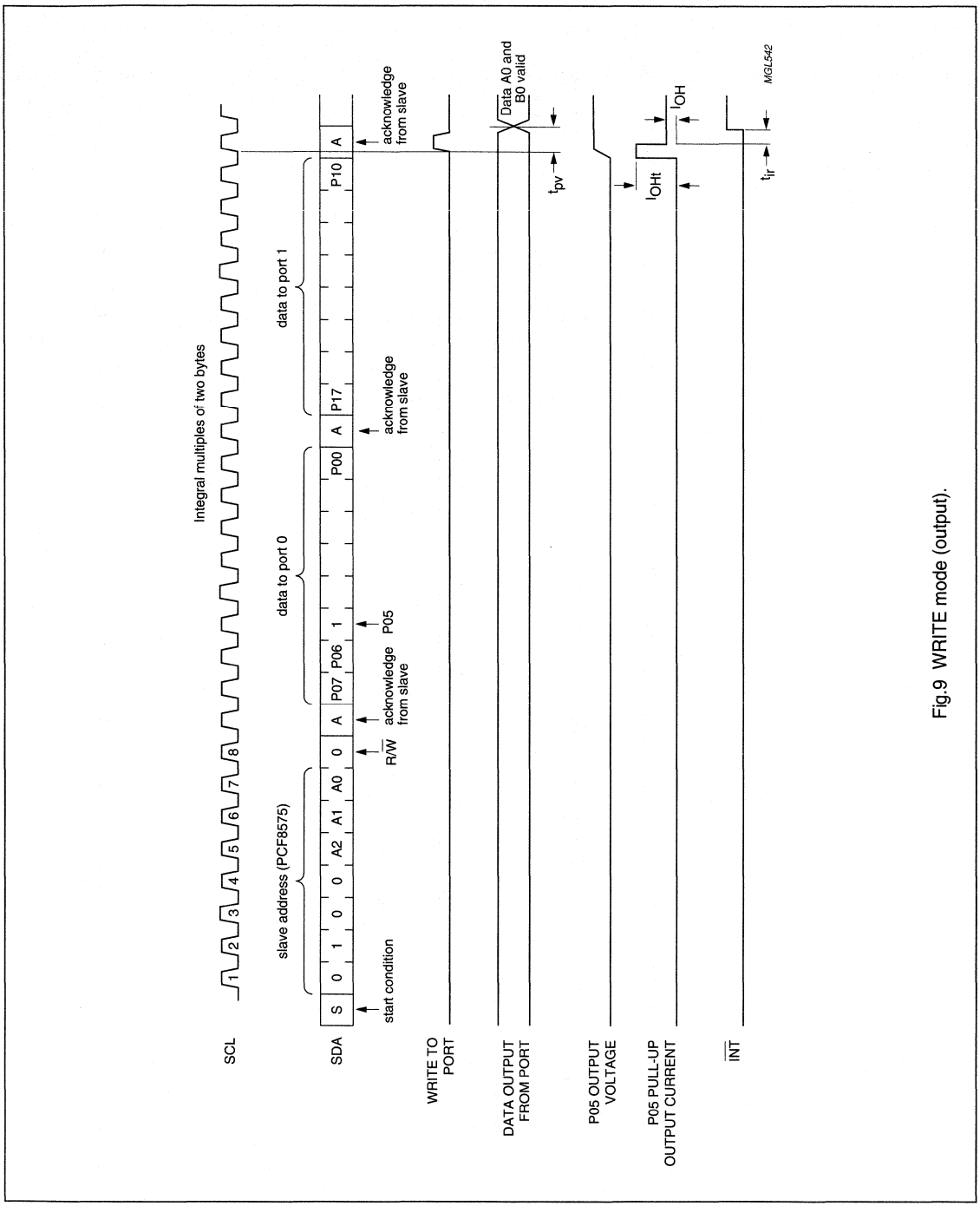
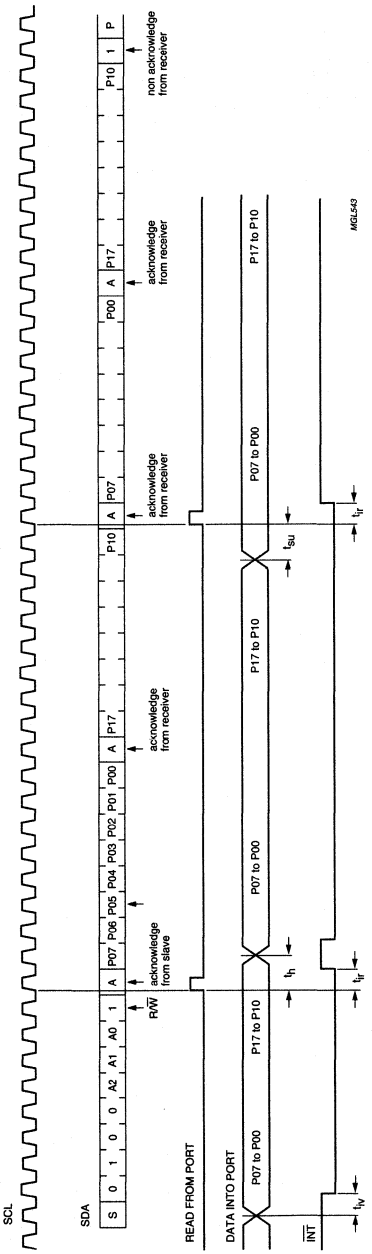


Fig.9 WRITE mode (output).



A LOW-to-HIGH transition of SDA, while SCL is HIGH is defined as the STOP condition (P). Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). Input data is lost.

Fig.10 READ mode (input).

7.3 Reading from a port (input mode)

All ports programmed as input should be set to logic 1. To read, the master (microcontroller) first addresses the slave device after it receives the interrupt. By setting the last bit of the byte containing the slave address to logic 1 the read mode is entered. The data bytes that follow on the SDA are the values on the ports.

If the data on the input port changes faster than the master can read, this data may be lost.

7.4 Writing to the port (output mode)

To write, the master (microcontroller) first addresses the slave device. By setting the last bit of the byte containing the slave address to logic 0 the write mode is entered. The PCF8575 acknowledges and the master sends the first data byte for P07 to P00. After the first data byte is acknowledged by the PCF8575, the second data byte P17 to P10 is sent by the master. Once again the PCF8575 acknowledges the receipt of the data after which this 16-bit data is presented on the port lines.

The number of data bytes that can be sent successively is not limited. After every two bytes the previous data is overwritten.

The first data byte in every pair refers to Port 0 (P07 to P00), whereas the second data byte in every pair refers to Port 1 (P17 to P10), see Fig.11.

7.5 Interrupt

The PCF8575 provides an open-drain interrupt ($\overline{INT}$) which can be fed to a corresponding input of the microcontroller (see Figs 9, 10 and 12). This gives these chips a kind of a master function which can initiate an action elsewhere in the system.

An interrupt is generated by any rising or falling edge of the port inputs. After time t_{iv} the signal $\overline{INT}$ is valid.

The interrupt disappears when data on the port is changed to the original setting or data is read from or written to the device which has generated the interrupt.

In the write mode the interrupt may become deactivated (HIGH) on the rising edge of the write to port pulse. On the falling edge of the write to port pulse the interrupt is definitely deactivated (HIGH).

The interrupt is reset in the read mode on the rising edge of the read from port pulse.

During the resetting of the interrupt itself any changes on the I/Os may not generate an interrupt. After the interrupt is reset any change in I/Os will be detected and transmitted as an $\overline{INT}$.

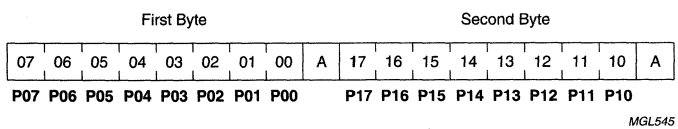


Fig.11 Correlation between bits and ports.

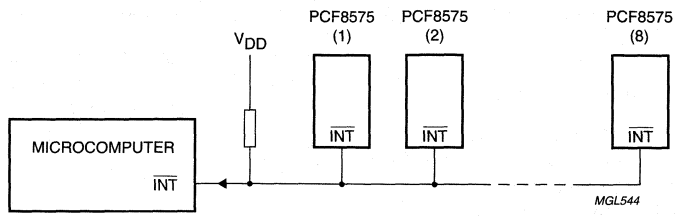


Fig.12 Application of multiple PCF8575s with interrupt.

8 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); note 1.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.5	+6.5	V
I_{DD}	supply current	−	±100	mA
I_{SS}	supply current	−	±100	mA
V_I	input voltage	V_{SS} − 0.5	V_{DD} + 0.5	V
I_I	DC input current	−	±20	mA
I_O	DC output current	−	±25	mA
P_{tot}	total power dissipation	−	400	mW
P_O	power dissipation per output	−	100	mW
T_{stg}	storage temperature	−65	+150	°C
T_{amb}	operating ambient temperature	−40	+85	°C

Note

1. Stress above those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

9 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take precautions appropriate to handling MOS devices. Advice can be found in Data Handbook IC12 under *"Handling MOS Devices"*.

10 CHARACTERISTICS

V_{DD} = 2.5 to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage		2.5	−	5.5	V
I_{DD}	supply current	operating mode; no load; $V_I = V_{DD}$ or V_{SS}; f_{SCL} = 400 kHz	−	100	200	μA
$I_{DD(stb)}$	standby current	standby mode; no load; $V_I = V_{DD}$ or V_{SS}	−	2.5	10	μA
V_{POR}	power-on reset voltage	note 1	−	1.2	1.8	V
V_{IL1}	LOW-level input voltage pins A0, A1 and A2		0.0	−	$0.2V_{DD}$	V
V_{IL2}	LOW-level input voltage on all other signal pins		0.0	−	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	−	V_{DD}	V
I_{L1}	leakage current at pins A0, A1 and A2	$V_I = V_{DD}$ or V_{SS}	−1	−	+1	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{L2}	leakage current on all other signal pins	$V_I = V_{DD}$ or V_{SS}	−10	–	+10	μA
Input SCL; input/output SDA						
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; note 3	3	–	–	mA
C_I	input capacitance	$V_I = V_{SS}$; note 2	–	–	7	pF
I/Os; P00 to P07 and P10 to P17						
I_{OL}	LOW-level output current	V_{OL} = 1 V; note 3	10	25	–	mA
I_{OH}	HIGH-level output current	$V_{OH} = V_{SS}$	−30	–	−300	μA
I_{OHt}	transient pull-up current	$V_{OH} = V_{SS}$; see Fig.9	−0.5	−1.0	–	mA
C_I	input capacitance	note 2	–	–	10	pF
C_O	output capacitance	note 2	–	–	10	pF
Port timing; $C_L \leq$ 100 pF (see Figs 9 and 10)						
t_{pv}	output data valid		–	–	4	μs
t_{su}	input data set-up time		0	–	–	μs
t_h	input data hold time		4	–	–	μs
Interrupt $\overline{INT}$ (see Fig.13)						
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	1.6	–	–	mA
TIMING; $C_L \leq$ 100 pF (see Figs 9 and 10)						
t_{iv}	input data valid time		–	–	4	μs
t_{ir}	reset delay time		–	–	4	μs

Notes

1. The power-on reset circuit resets the I²C-bus logic with $V_{DD} < V_{POR}$ and sets all I/Os to logic 1 (with current source to V_{DD}).
2. The value is not tested, but verified on sampling basis.
3. A single LOW-level output current (I_{OL}) must not exceed 20 mA for an extended time. The sum of all I_{OLs} at any point in time must not exceed 100 mA.

11 I²C-BUS TIMING CHARACTERISTICS

See Fig.13 and note 1.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
f_{SCL}	SCL clock frequency		–	400	kHz
t_{SW}	tolerable spike width on bus	note 2	–	50	ns
t_{BUF}	BUS free time between a STOP and START condition		1.3	–	µs
$t_{SU;STA}$	START condition set-up time		0.6	–	µs
$t_{HD;STA}$	START condition hold time		0.6	–	µs
t_{LOW}	SCL LOW time		1.3	–	µs
t_{HIGH}	SCL HIGH time		0.6	–	µs
t_r	SCL and SDA rise time	note 3	$20 + 0.1C_b$	300	ns
t_f	SCL and SDA fall time	note 3	$20 + 0.1C_b$	300	ns
$t_{SU;DAT}$	data set-up time		100	–	ns
$t_{HD;DAT}$	data hold time		0	–	ns
$t_{SU;STO}$	STOP condition set-up time		0.6	–	µs
C_b	capacitive load represented by each bus line		–	400	pF

Notes

1. All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.
2. The device inputs SDA and SCL are filtered and will reject spikes on the bus lines of widths less than $t_{SW(max)}$.
3. The rise and fall times specified here refer to the driver device (PCF8575) and are part of the general fast I²C-bus specification when PCF8575 asserts an acknowledge on SDA, the minimum fall time is 20 ns + $0.1C_b$.

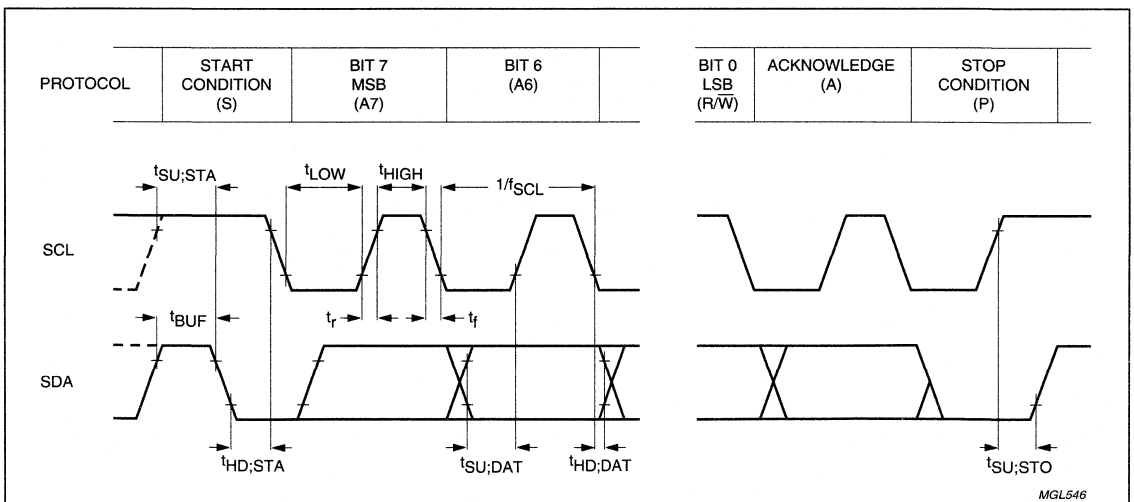


Fig.13 I²C-bus timing diagram.

12 DEVICE PROTECTION

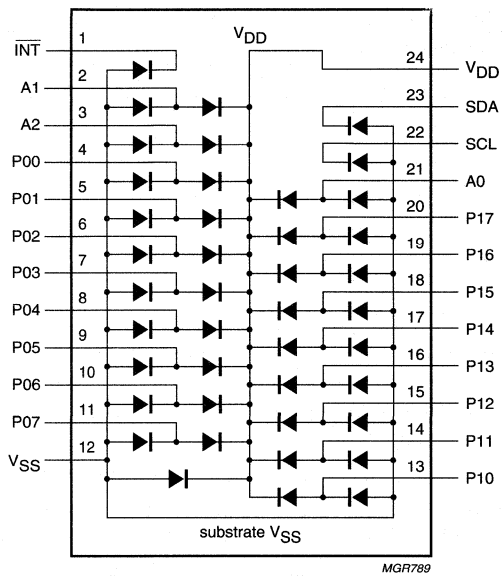


Fig.14 Device protection diagram.

CONTENTS

Remote 16-bit I/O expander for I²C-bus PCF8575C

1 FEATURES

- Operating supply voltage from 4.5 to 5.5 V
- Low standby current consumption of 10 μA maximum
- I²C-bus to parallel port expander
- 400 kbits/s FAST I²C-bus
- Open-drain interrupt output
- 16-bit remote I/O port for the I²C-bus
- Compatible with most microcontrollers
- Latched outputs with high current drive capability for directly driving LEDs
- Address by 3 hardware address pins for use of up to 8 devices
- SSOP24 package.

2 GENERAL DESCRIPTION

The device is a silicon CMOS circuit. It provides general purpose remote I/O expansion for most microcontroller families via the two-line bidirectional bus (I²C-bus).

The device consists of a 16-bit quasi-bidirectional port and an I²C-bus interface. The PCF8575C has a low current consumption and includes latched outputs with high current drive capability for directly driving LEDs. It also possesses an interrupt line ($\overline{INT}$) which can be connected to the interrupt logic of the microcontroller. By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I²C-bus. This means that the device is an I²C-bus slave transmitter/receiver.

Every data transmission from the PCF8575C must consist of an even number of bytes, the first byte will be referred to as P07 to P00 and the second byte as P17 to P10. The third will be referred to as P07 to P00 and so on.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8575CTS	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1

4 BLOCK DIAGRAM

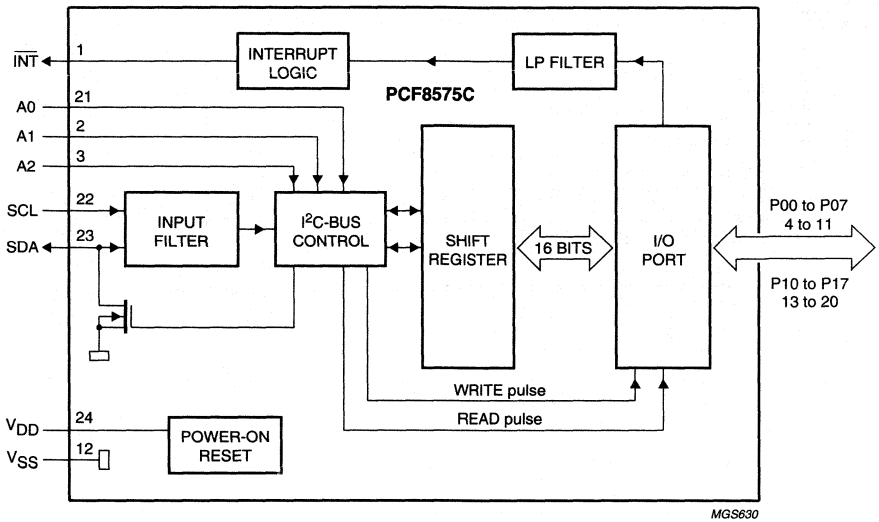


Fig.1 Block diagram.

5 PINNING

SYMBOL	PIN	DESCRIPTION
$\overline{INT}$	1	interrupt output (active LOW)
A1	2	address input 1
A2	3	address input 2
P00	4	quasi-bidirectional I/O 00
P01	5	quasi-bidirectional I/O 01
P02	6	quasi-bidirectional I/O 02
P03	7	quasi-bidirectional I/O 03
P04	8	quasi-bidirectional I/O 04
P05	9	quasi-bidirectional I/O 05
P06	10	quasi-bidirectional I/O 06
P07	11	quasi-bidirectional I/O 07
V_{SS}	12	supply ground
P10	13	quasi-bidirectional I/O 10
P11	14	quasi-bidirectional I/O 11
P12	15	quasi-bidirectional I/O 12
P13	16	quasi-bidirectional I/O 13
P14	17	quasi-bidirectional I/O 14
P15	18	quasi-bidirectional I/O 15
P16	19	quasi-bidirectional I/O 16
P17	20	quasi-bidirectional I/O 17
A0	21	address input 0
SCL	22	serial clock line input
SDA	23	serial data line input/output
V_{DD}	24	supply voltage

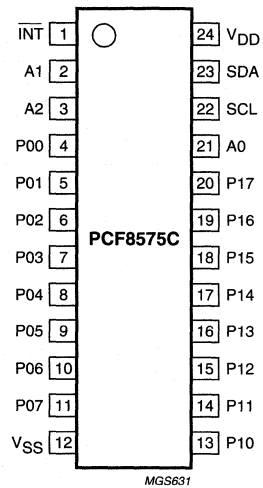


Fig.2 Pin configuration.

6 FUNCTIONAL DESCRIPTION

6.1 Quasi-bidirectional I/Os

The 16 ports (see Fig.3) are entirely independent and can be used either as input or output ports. Input data is transferred from the ports to the microcontroller in the READ mode (see Fig.6). Output data is transmitted to the ports in the WRITE mode (see Fig.5).

This quasi-bidirectional I/O can be used as an input or output without the use of a control signal for data direction. At power-on all the I/Os are in 3-state mode. The strong pull-up to V_{DD} (I_{OHt}) allows a fast rising edge into a heavily loaded output. This strong pull-up turns on when the output is written HIGH, and is switched off by the negative edge of SCL. After this short period the output is in 3-state mode. The I/O should be written HIGH before being used as an input. After power-on as all the I/Os are set to 3-state all of them can be used as inputs. Any change in setting of the I/Os as either inputs or outputs can be done with the write mode. Warning: If a HIGH is applied to an I/O which has been written earlier to LOW, a large current (I_{OL}) will flow to V_{SS} (see Chapter 10; note 3).

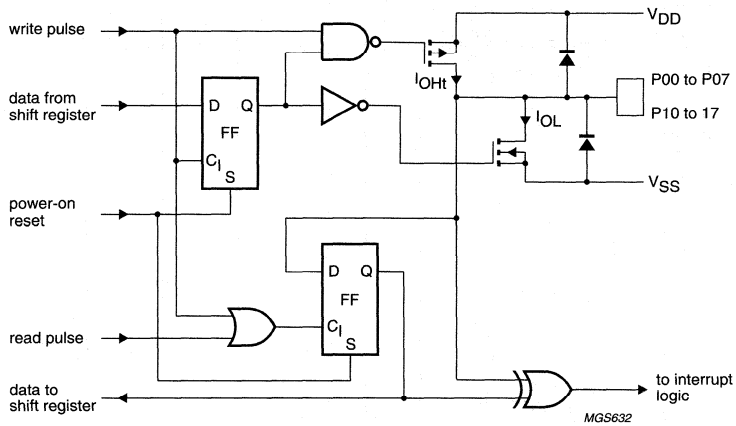


Fig.3 Simplified schematic diagram of each I/O.

6.2 Addressing

Figures 4, 5 and 6 show the address and timing diagrams. Before any data is transmitted or received the master must send the address of the receiver via the SDA line. The first byte transmitted after the START condition carries the address of the slave device and the read/write bit. The address of the slave device must not be changed between the START and the STOP conditions. The PCF8575C acts as a slave receiver or a slave transmitter.

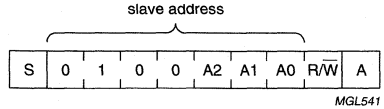


Fig.4 Byte containing the slave address and the R/$\overline{W}$ bits.

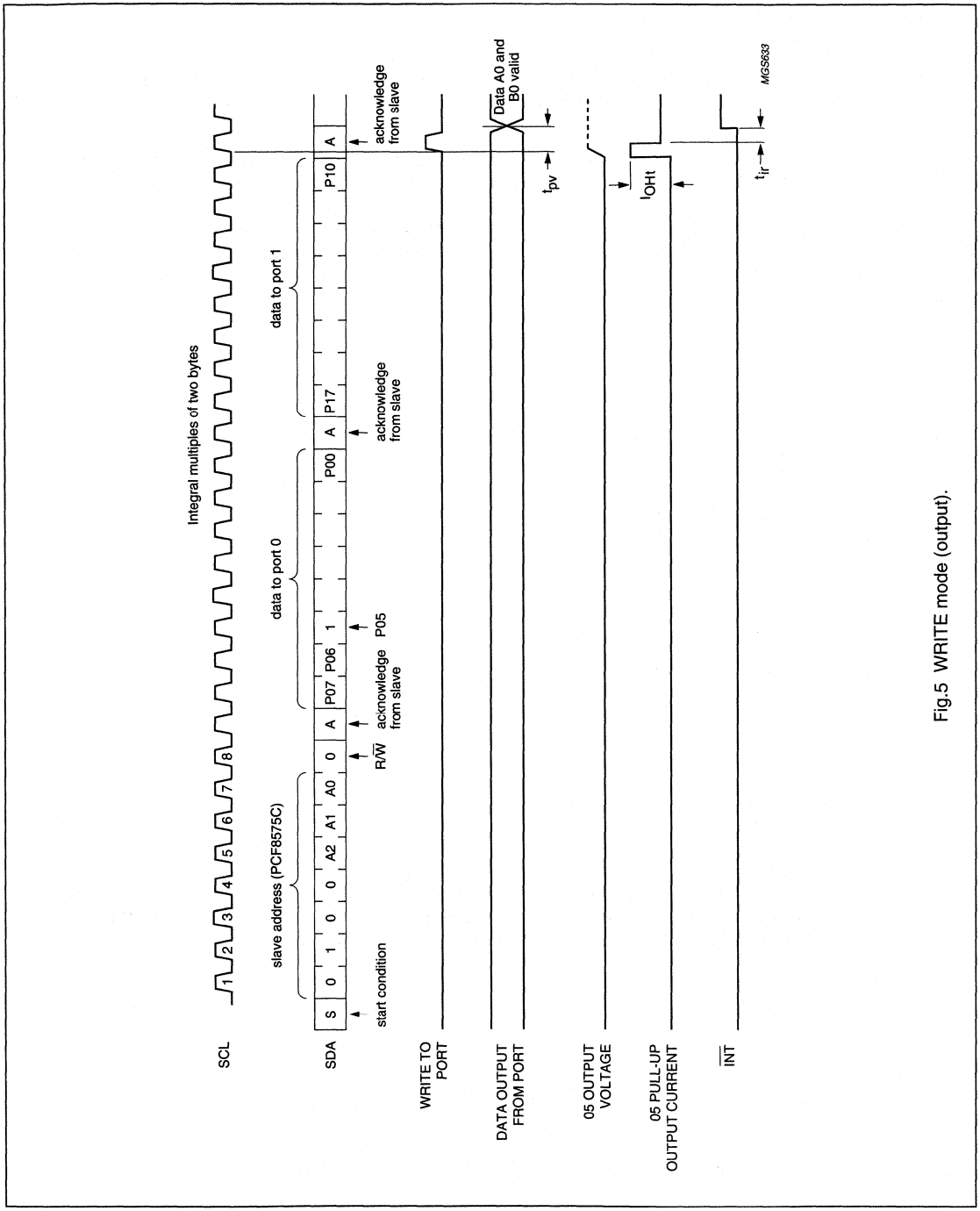
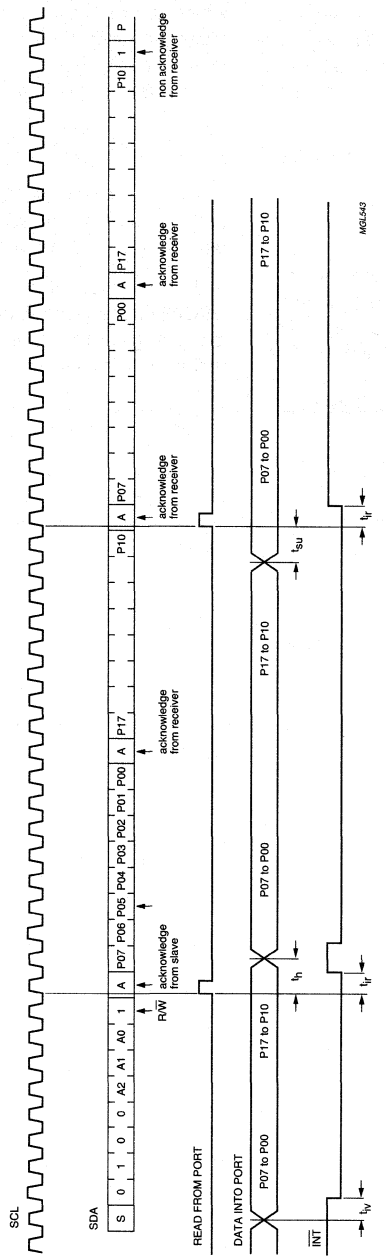


Fig.5 WRITE mode (output).



A LOW-to-HIGH transition of SDA, while SCL is HIGH is defined as the STOP condition (P). Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). Input data is lost.

Fig.6 READ mode (input).

6.3 Reading from a port (input mode)

All ports programmed as input should be set to logic 1. To read, the master (microcontroller) first addresses the slave device after it receives the interrupt. By setting the last bit of the byte containing the slave address to logic 1 the read mode is entered. The data bytes that follow on the SDA are the values on the ports.

If the data on the input port changes faster than the master can read, this data may be lost.

6.4 Writing to the port (output mode)

To write, the master (microcontroller) first addresses the slave device. By setting the last bit of the byte containing the slave address to logic 0 the write mode is entered. The PCF8575C acknowledges and the master sends the first data byte for P07 to P00. After the first data byte is acknowledged by the PCF8575C, the second data byte P17 to P10 is sent by the master. Once again the PCF8575C acknowledges the receipt of the data after which this 16-bit data is presented on the port lines.

The number of data bytes that can be sent successively is not limited. After every two bytes the previous data is overwritten.

The first data byte in every pair refers to Port 0 (P07 to P00), whereas the second data byte in every pair refers to Port 1 (P17 to P10), see Fig.7.

6.5 Interrupt

The PCF8575C provides an open-drain interrupt ($\overline{INT}$) which can be fed to a corresponding input of the microcontroller (see Figs 5, 6 and 8). This gives these chips a kind of a master function which can initiate an action elsewhere in the system.

An interrupt is generated by any rising or falling edge of the port inputs. After time t_{iv} the signal $\overline{INT}$ is valid.

The interrupt disappears when data on the port is changed to the original setting or data is read from or written to the device which has generated the interrupt.

In the write mode the interrupt may become deactivated (HIGH) on the rising edge of the write to port pulse. On the falling edge of the write to port pulse the interrupt is definitely deactivated (HIGH).

The interrupt is reset in the read mode on the rising edge of the read from port pulse.

During the resetting of the interrupt itself any changes on the I/Os may not generate an interrupt. After the interrupt is reset any change in I/Os will be detected and transmitted as an $\overline{INT}$.

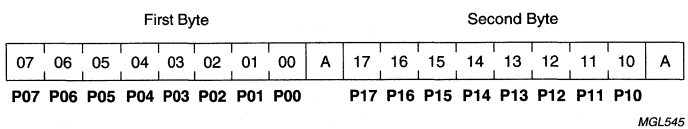


Fig.7 Correlation between bits and ports.

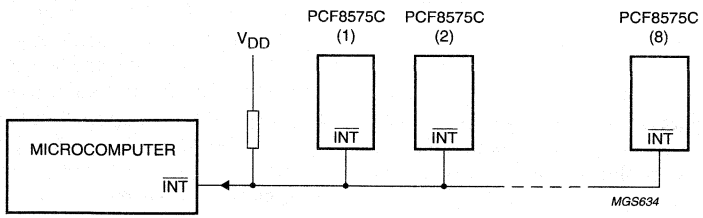


Fig.8 Application of multiple PCF8575Cs with interrupt.

7 CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for bidirectional, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

7.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see Fig.9).

7.2 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S).

A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition P (see Fig.10).

7.3 System configuration

A device generating a message is a 'transmitter', a device receiving the message is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves' (see Fig.11).

7.4 Acknowledge

The number of data bytes transferred between the START and the STOP conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The transmitter must release the SDA line before the receiver can send an acknowledge bit.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account.

A master receiver must signal an end of data to the transmitter by **not** generating an acknowledge after the last byte that has been clocked out of the slave. This is done by the master receiver by holding the SDA line HIGH. In this event the transmitter must release the data line to enable the master to generate a STOP condition.

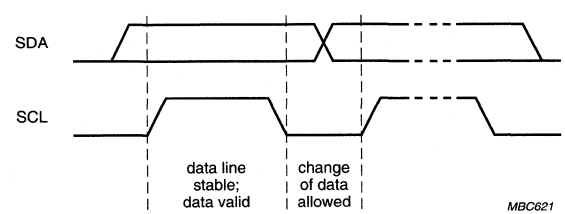


Fig.9 Bit transfer.

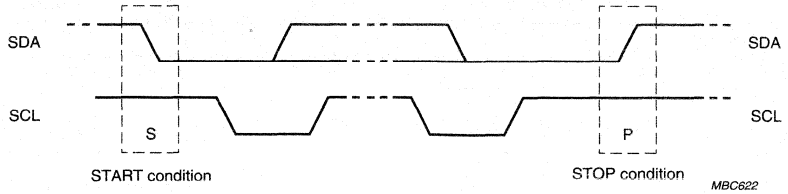


Fig.10 Definition of START and STOP conditions.

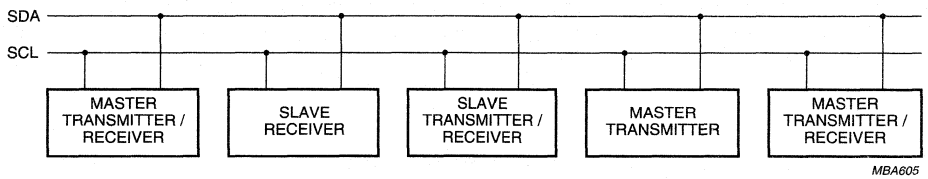


Fig.11 System configuration.

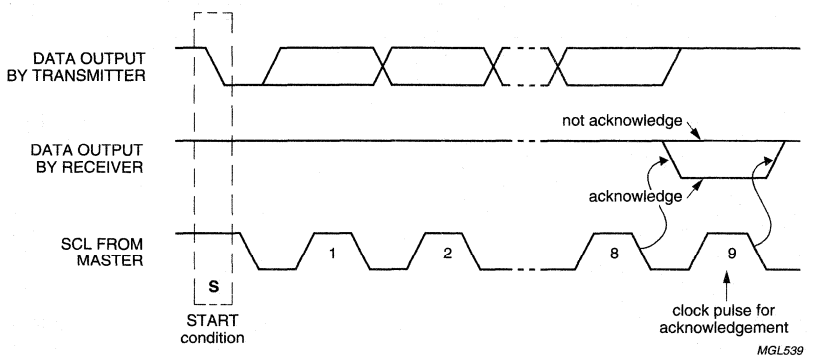


Fig.12 Acknowledgment on the I²C-bus.

8 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); note 1.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.5	+6.5	V
I_{DD}	supply current	−	±100	mA
I_{SS}	supply current	−	±100	mA
V_I	input voltage	V_{SS} − 0.5	V_{DD} + 0.5	V
I_I	DC input current	−	±20	mA
I_O	DC output current	−	±25	mA
P_{tot}	total power dissipation	−	400	mW
P_O	power dissipation per output	−	100	mW
T_{stg}	storage temperature	−65	+150	°C
T_{amb}	ambient temperature	−40	+85	°C

Note

1. Stress above those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

9 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take precautions appropriate to handling MOS devices. Advice can be found in Data Handbook IC12 under *"Handling MOS Devices"*.

10 CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage		4.5	−	5.5	V
I_{DD}	supply current	operating mode; no load; $V_I = V_{DD}$ or V_{SS}; f_{SCL} = 400 kHz	−	100	200	μA
$I_{DD(stb)}$	standby current	standby mode; no load; $V_I = V_{DD}$ or V_{SS}	−	2.5	10	μA
V_{POR}	Power-on reset voltage	note 1	−	1.2	1.8	V
V_{IL1}	LOW-level input voltage pins A0, A1, A2, SDA and SCL		−0.8	−	$0.3V_{DD}$	V
V_{IL2}	LOW-level input voltage pins P00 to P17		−0.8	−	$0.6V_{DD}$	V
V_{IH1}	HIGH-level input voltage pins A0, A1, A2, SDA and SCL		$0.7V_{DD}$	−	V_{DD} + 0.8	V
V_{IH2}	HIGH-level input voltage pins P00 to P17		$0.8V_{DD}$	−	V_{DD} + 0.8	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_L	leakage current at all pins	$V_I = V_{DD}$ or V_{SS}	−2	–	+2	μA
I_{IHL}	current through protection diode	$V_I > V_{DD}$ or $V_I < V_{SS}$; note 2	–	–	±2	mA
Input SCL; input/output SDA						
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; note 3	3	–	–	mA
C_I	input capacitance	$V_I = V_{SS}$; note 2	–	–	7	pF
I/Os; P00 to P07 and P10 to P17						
I_{OL}	LOW-level output current	V_{OL} = 1 V; note 3	10	25	–	mA
I_{OHt}	transient pull-up current	$V_{OH} = V_{SS}$; see Fig.5	−0.5	−1.0	–	mA
C_I	input capacitance	note 2	–	–	10	pF
C_O	output capacitance	note 2	–	–	10	pF
Port timing; $C_L \leq$ 100 pF (see Figs 5 and 6)						
t_{pv}	output data valid		–	–	4	μs
t_{su}	input data set-up time		0	–	–	μs
t_h	input data hold time		4	–	–	μs
Interrupt $\overline{INT}$ (see Fig.13)						
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	1.6	–	–	mA
TIMING; $C_L \leq$ 100 pF (see Figs 5 and 6)						
t_{iv}	input data valid time		–	–	4	μs
t_{ir}	reset delay time		–	–	4	μs

Notes

1. The Power-on reset circuit resets the I²C-bus logic with $V_{DD} < V_{POR}$ and sets all I/Os to logic 1 (with current source to V_{DD}).
2. The value is not tested, but verified on sampling basis.
3. A single LOW-level output current (I_{OL}) must not exceed 20 mA for an extended time. The sum of all I_{OLs} at any point in time must not exceed 100 mA.

11 I²C-BUS TIMING CHARACTERISTICS

See Fig.13 and note 1.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
f_{SCL}	SCL clock frequency		–	400	kHz
t_{SW}	tolerable spike width on bus	note 2	–	50	ns
t_{BUF}	BUS free time between a STOP and START condition		1.3	–	µs
$t_{SU;STA}$	START condition set-up time		0.6	–	µs
$t_{HD;STA}$	START condition hold time		0.6	–	µs
t_{LOW}	SCL LOW time		1.3	–	µs
t_{HIGH}	SCL HIGH time		0.6	–	µs
t_r	SCL and SDA rise time	note 3	$20 + 0.1C_b$	300	ns
t_f	SCL and SDA fall time	note 3	$20 + 0.1C_b$	300	ns
$t_{SU;DAT}$	data set-up time		100	–	ns
$t_{HD;DAT}$	data hold time		0	–	ns
$t_{SU;STO}$	STOP condition set-up time		0.6	–	µs
C_b	capacitive load represented by each bus line		–	400	pF

Notes

1. All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.
2. The device inputs SDA and SCL are filtered and will reject spikes on the bus lines of widths less than $t_{SW(max)}$.
3. The rise and fall times specified here refer to the driver device (PCF8575C) and are part of the general fast I²C-bus specification when PCF8575C asserts an acknowledge on SDA, the minimum fall time is 20 ns + $0.1C_b$.

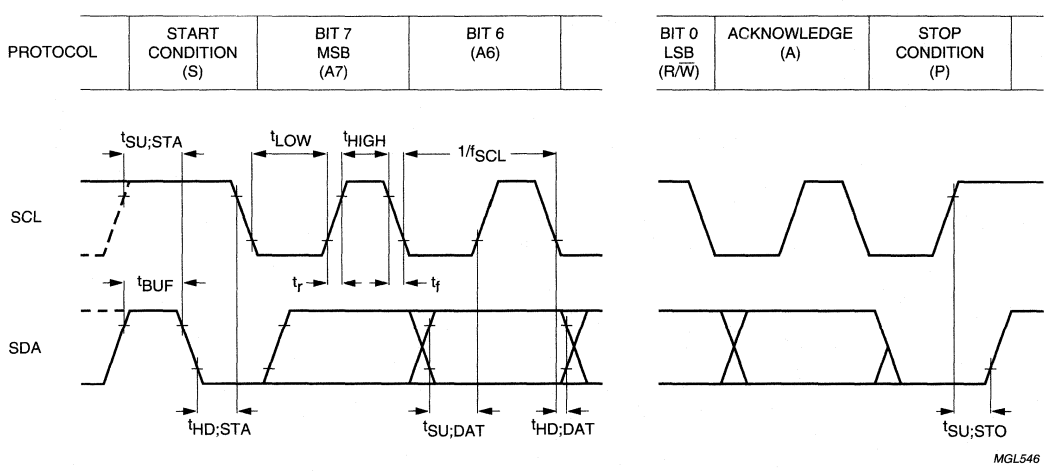


Fig.13 I²C-bus timing diagram.

12 DEVICE PROTECTION

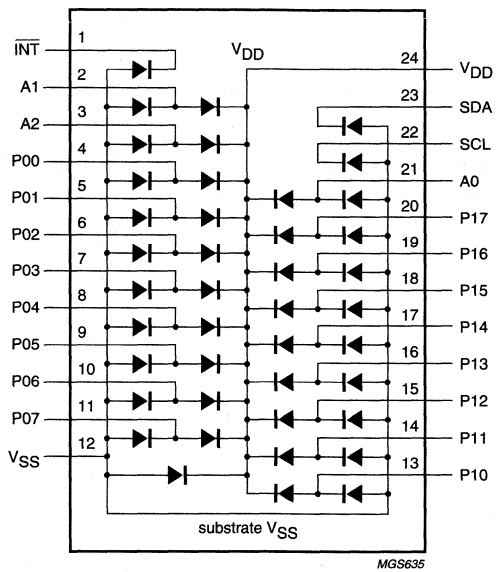


Fig.14 Device protection diagram.

Universal LCD driver for low multiplex rates

PCF8576

CONTENTS

Universal LCD driver for low multiplex rates PCF8576

1 FEATURES

- Single-chip LCD controller/driver
- Selectable backplane drive configuration: static or 2/3/4 backplane multiplexing
- Selectable display bias configuration: static, $\frac{1}{2}$ or $\frac{1}{3}$
- Internal LCD bias generation with voltage-follower buffers
- 40 segment drives: up to twenty 8-segment numeric characters; up to ten 15-segment alphanumeric characters; or any graphics of up to 160 elements
- 40 × 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- LCD and logic supplies may be separated
- Wide power supply range: from 2 V for low-threshold LCDs and up to 9 V for guest-host LCDs and high-threshold (automobile) twisted nematic LCDs
- Low power consumption
- Power-saving mode for extremely low power consumption in battery-operated and telephone applications
- I^2C-bus interface
- TTL/CMOS compatible
- Compatible with any 4-bit, 8-bit or 16-bit microprocessors/microcontrollers
- May be cascaded for large LCD applications (up to 2560 segments possible)
- Cascadable with 24-segment LCD driver PCF8566
- Optimized pinning for plane wiring in both single and multiple PCF8576 applications
- Space-saving 56-lead plastic very small outline package (VSO56)
- Very low external component count (at most one resistor, even in multiple device applications)
- Compatible with chip-on-glass technology
- Manufactured in silicon gate CMOS process.

2 GENERAL DESCRIPTION

The PCF8576 is a peripheral device which interfaces to almost any Liquid Crystal Display (LCD) with low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 40 segments and can easily be cascaded for larger LCD applications. The PCF8576 is compatible with most microprocessors/microcontrollers and communicates via a two-line bidirectional I^2C-bus. Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8576T	VSO56	plastic very small outline package; 56 leads	SOT190-1
PCF8576U	–	chip in tray	–
PCF8576U/2	–	chip with bumps in tray	–
PCF8576U/5	–	unsawn wafer	–
PCF8576U/7	–	chip with bumps on tape	–
PCF8576U/10	FFC	chip on film frame carrier (FFC)	–
PCF8576U/12	FFC	chip with bumps on film frame carrier (FFC)	–

4 BLOCK DIAGRAM

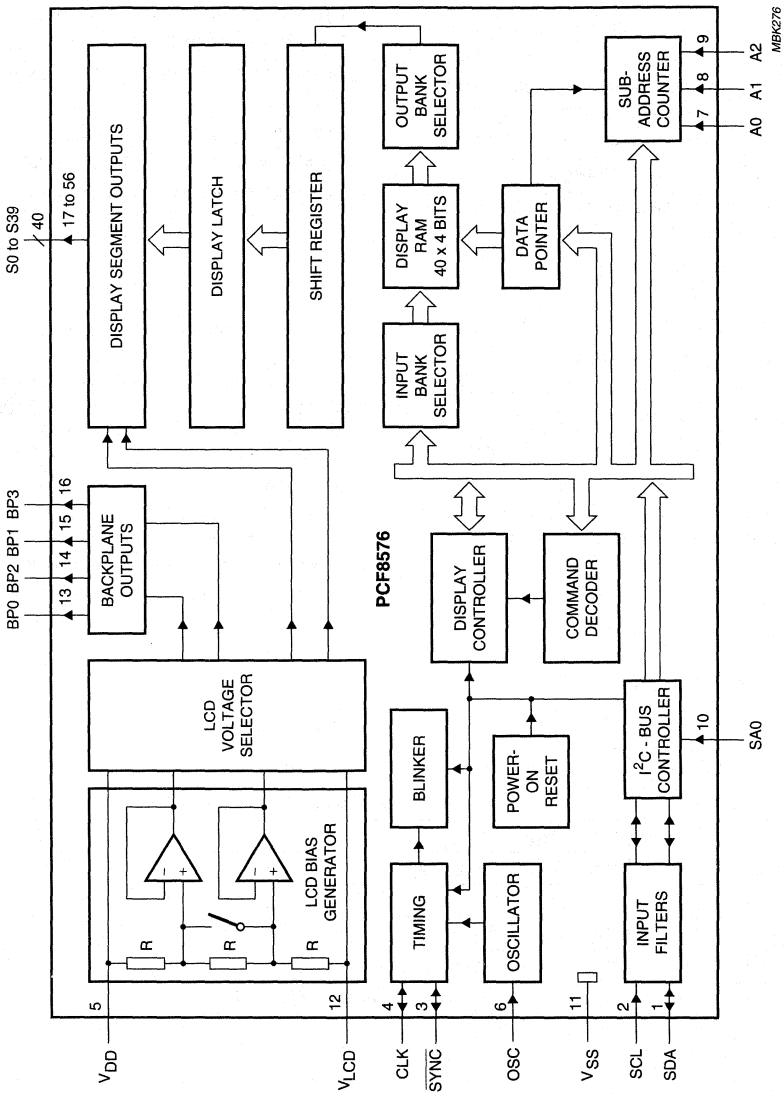


Fig.1 Block diagram (for VSO56 package; SOT190-1).

5 PINNING

SYMBOL	PIN	DESCRIPTION
SDA	1	I^2C-bus serial data input/output
SCL	2	I^2C-bus serial clock input
$\overline{SYNC}$	3	cascade synchronization input/output
CLK	4	external clock input/output
V_{DD}	5	supply voltage
OSC	6	oscillator input
A0 to A2	7 to 9	I^2C-bus subaddress inputs
SA0	10	I^2C-bus slave address input; bit 0
V_{SS}	11	logic ground
V_{LCD}	12	LCD supply voltage
BP0, BP2, BP1 and BP3	13 to 16	LCD backplane outputs
S0 to S39	17 to 56	LCD segment outputs

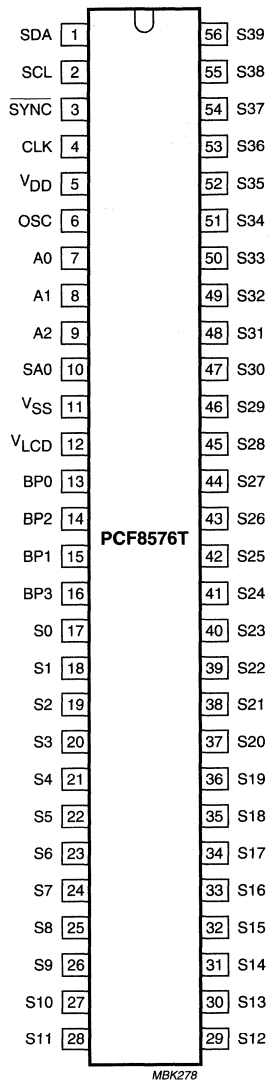


Fig.2 Pin configuration; SOT190-1.

6 FUNCTIONAL DESCRIPTION

The PCF8576 is a versatile peripheral device designed to interface to any microprocessor/microcontroller to a wide variety of LCDs. It can directly drive any static or multiplexed LCD containing up to four backplanes and up to 40 segments. The display configurations possible with the PCF8576 depend on the number of active backplane outputs required; a selection of display configurations is given in Table 1.

All of the display configurations given in Table 1 can be implemented in the typical system shown in Fig.3.

The host microprocessor/microcontroller maintains the 2-line I^2C-bus communication channel with the PCF8576. The internal oscillator is selected by connecting pin OSC to pin V_{SS}. The appropriate biasing voltages for the multiplexed LCD waveforms are generated internally. The only other connections required to complete the system are to the power supplies (V_{DD}, V_{SS} and V_{LCD}) and the LCD panel chosen for the application.

Table 1 Selection of display configurations

NUMBER OF		7-SEGMENTS NUMERIC		14-SEGMENTS ALPHANUMERIC		DOT MATRIX
BACKPLANES	SEGMENTS	DIGITS	INDICATOR SYMBOLS	CHARACTERS	INDICATOR SYMBOLS	
4	160	20	20	10	20	160 dots (4 × 40)
3	120	15	15	8	8	120 dots (3 × 40)
2	80	10	10	5	10	80 dots (2 × 40)
1	40	5	5	2	12	40 dots (1 × 40)

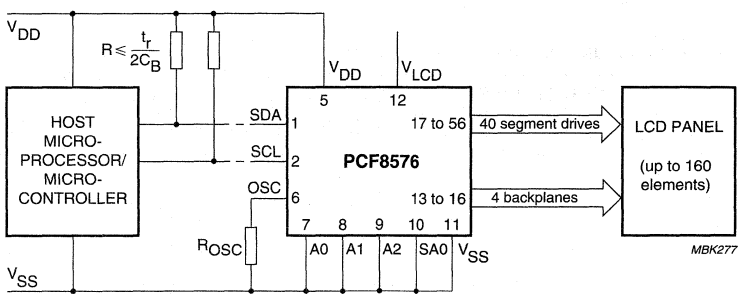


Fig.3 Typical system configuration.

6.1 Power-on reset

At power-on the PCF8576 resets to a starting condition as follows:

1. All backplane outputs are set to V_{DD}.
2. All segment outputs are set to V_{DD}.
3. The drive mode '1 : 4 multiplex with ⅓bias' is selected.
4. Blinking is switched off.
5. Input and output bank selectors are reset (as defined in Table 5).
6. The I²C-bus interface is initialized.
7. The data pointer and the subaddress counter are cleared.

Data transfers on the I²C-bus should be avoided for 1 ms following power-on to allow completion of the reset action.

6.2 LCD bias generator

The full-scale LCD voltage (V_{op}) is obtained from $V_{DD} - V_{LCD}$. The LCD voltage may be temperature compensated externally through the V_{LCD} supply to pin 12. Fractional LCD biasing voltages are obtained from an internal voltage divider of the three series resistors connected between V_{DD} and V_{LCD}. The centre resistor can be switched out of the circuit to provide a ½bias voltage level for the 1 : 2 multiplex configuration.

6.3 LCD voltage selector

The LCD voltage selector co-ordinates the multiplexing of the LCD in accordance with the selected LCD drive configuration. The operation of the voltage selector is controlled by MODE SET commands from the command decoder. The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of $V_{op} = V_{DD} - V_{LCD}$ and the resulting discrimination ratios (D), are given in Table 2.

A practical value for V_{op} is determined by equating $V_{off(rms)}$ with a defined LCD threshold voltage (V_{th}), typically when the LCD exhibits approximately 10% contrast. In the static drive mode a suitable choice is $V_{op} > 3V_{th}$ approximately.

Multiplex drive ratios of 1 : 3 and 1 : 4 with ½bias are possible but the discrimination and hence the contrast ratios are smaller ($\sqrt{3} = 1.732$ for 1 : 3 multiplex or $\frac{\sqrt{21}}{3} = 1.528$ for 1 : 4 multiplex).

The advantage of these modes is a reduction of the LCD full-scale voltage V_{op} as follows:

- 1 : 3 multiplex (½bias):

  $V_{op} = \sqrt{6} \times V_{off\langle rms\rangle} = 2.449\ V_{off(rms)}$

- 1 : 4 multiplex (½bias):

  $V_{op} = \left[\frac{(4 \times \sqrt{3})}{3}\right] = 2.309\ V_{off(rms)}$

These compare with $V_{op} = 3\ V_{off(rms)}$ when ⅓bias is used.

Table 2 Preferred LCD drive modes: summary of characteristics

LCD DRIVE MODE	NUMBER OF		LCD BIAS CONFIGURATION	$\frac{V_{off(rms)}}{V_{op}}$	$\frac{V_{on(rms)}}{V_{op}}$	$D = \frac{V_{on(rms)}}{V_{off(rms)}}$
	BACKPLANES	LEVELS				
static	1	2	static	0	1	∞
1 : 2	2	3	½	0.354	0.791	2.236
1 : 2	2	4	⅓	0.333	0.745	2.236
1 : 3	3	4	⅓	0.333	0.638	1.915
1 : 4	4	4	⅓	0.333	0.577	1.732

6.4 LCD drive mode waveforms

6.4.1 STATIC DRIVE MODE

The static LCD drive mode is used when a single backplane is provided in the LCD. Backplane and segment drive waveforms for this mode are shown in Fig.4.

6.4.2 1 : 2 MULTIPLEX DRIVE MODE

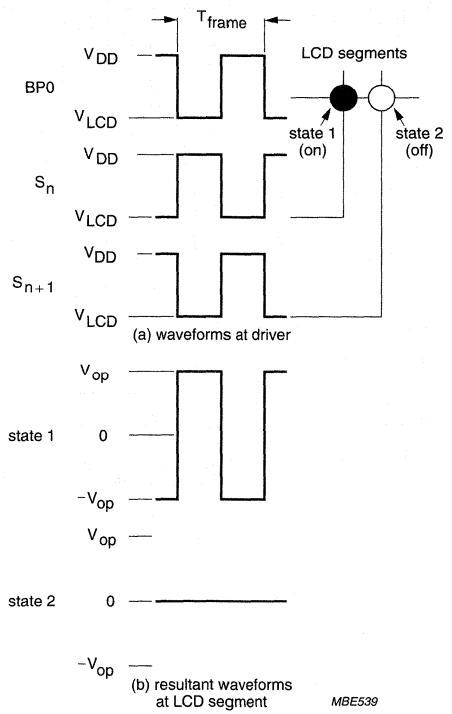
When two backplanes are provided in the LCD, the 1 : 2 multiplex mode applies. The PCF8576 allows use of ½bias or ⅓bias in this mode as shown in Figs 5 and 6.

6.4.3 1 : 3 MULTIPLEX DRIVE MODE

When three backplanes are provided in the LCD, the 1 : 3 multiplex drive mode applies, as shown in Fig.7.

6.4.4 1 : 4 MULTIPLEX DRIVE MODE

When four backplanes are provided in the LCD, the 1 : 4 multiplex drive mode applies, as shown in Fig.8.



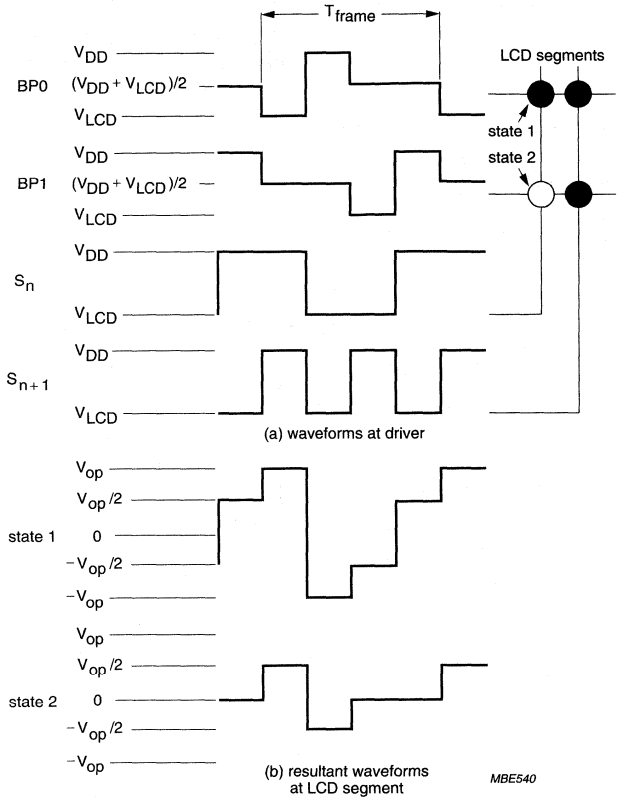
$V_{state1}(t) = V_{S_n}(t) - V_{BP0}(t)$

$V_{on(rms)} = V_{op}$

$V_{state2}(t) = V_{S_{n+1}}(t) - V_{BP0}(t)$

$V_{off(rms)} = 0\ V$

Fig.4 Static drive mode waveforms ($V_{op} = V_{DD} - V_{LCD}$).



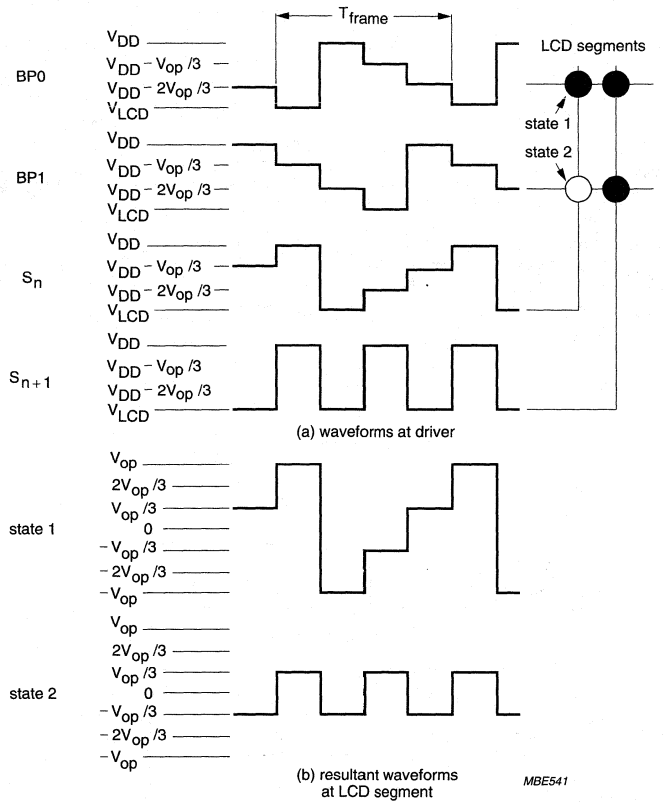
$V_{state1}(t) = V_{S_n}(t) - V_{BP0}(t)$

$V_{on(rms)} = 0.791 V_{op}$

$V_{state2}(t) = V_{S_n}(t) - V_{BP1}(t)$

$V_{off(rms)} = 0.354 V_{op}$

Fig.5 Waveforms for the 1 : 2 multiplex drive mode with ½bias ($V_{op} = V_{DD} - V_{LCD}$).



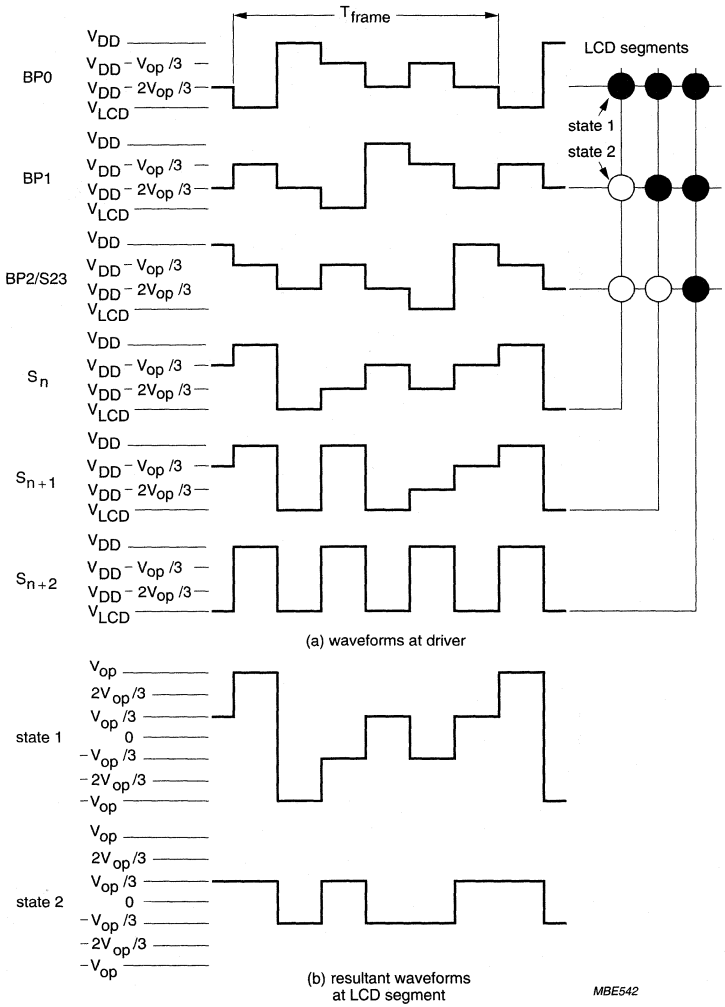
$V_{state1}(t) = V_{S_n}(t) - V_{BP0}(t)$

$V_{on(rms)} = 0.745V_{op}$

$V_{state2}(t) = V_{S_n}(t) - V_{BP1}(t)$

$V_{off(rms)} = 0.333V_{op}$

Fig.6 Waveforms for the 1 : 2 multiplex drive mode with ⅓bias ($V_{op} = V_{DD} - V_{LCD}$).



$V_{state1}(t) = V_{S_n}(t) - V_{BP0}(t)$

$V_{on(rms)} = 0.638V_{op}$

$V_{state2}(t) = V_{S_n}(t) - V_{BP1}(t)$

$V_{off(rms)} = 0.333V_{op}$

Fig.7 Waveforms for the 1 : 3 multiplex drive mode ($V_{op} = V_{DD} - V_{LCD}$).

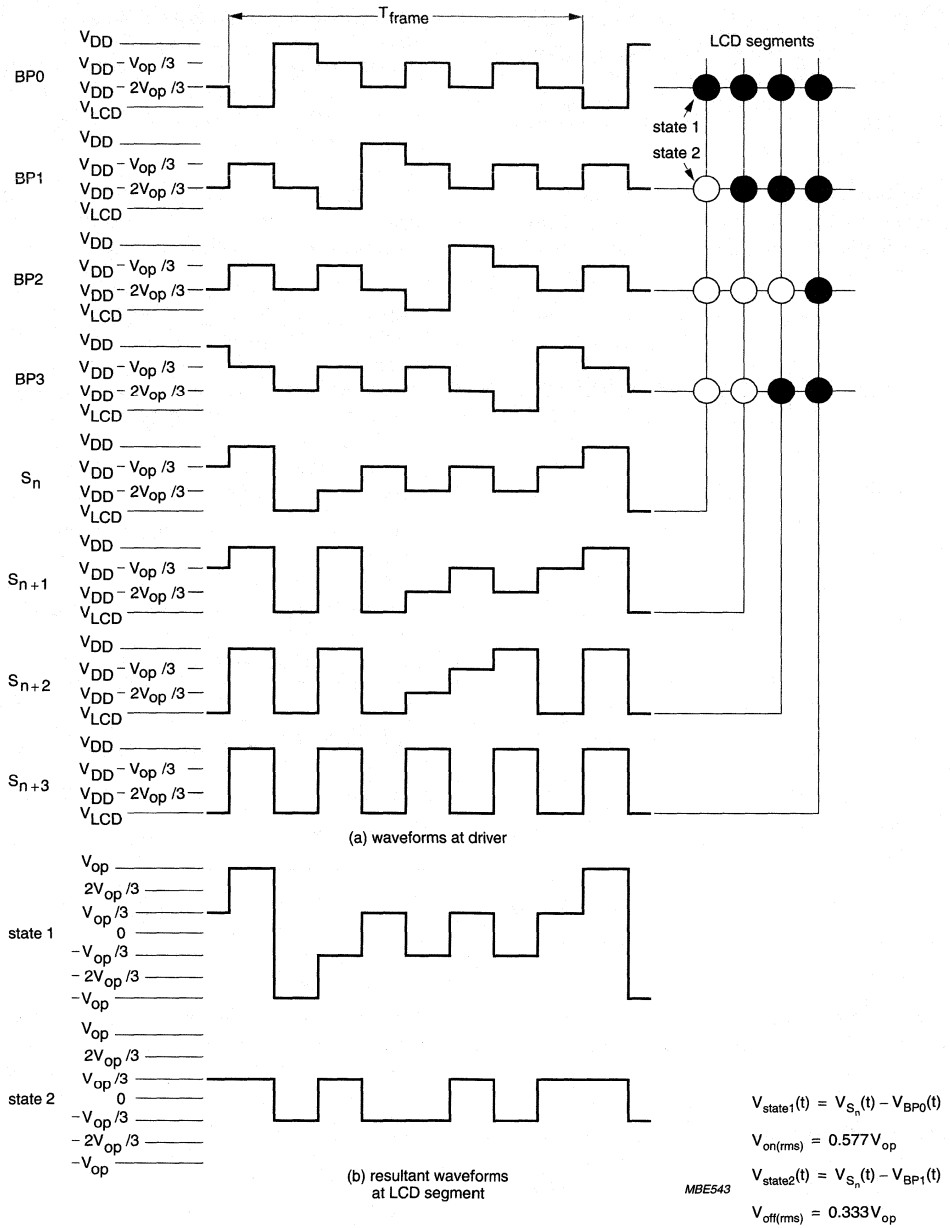


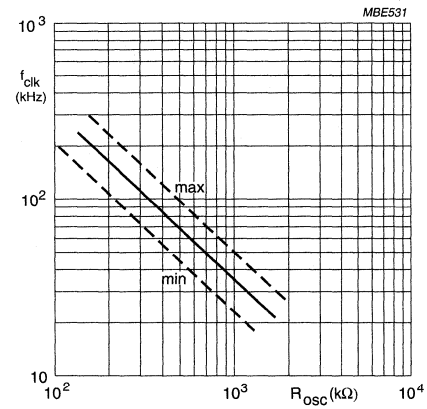
Fig.8 Waveforms for the 1 : 4 multiplex drive mode ($V_{op} = V_{DD} - V_{LCD}$).

6.5 Oscillator

6.5.1 INTERNAL CLOCK

The internal logic and the LCD drive signals of the PCF8576 are timed either by the internal oscillator or from an external clock. When the internal oscillator is used, pin OSC should be connected to pin V_{SS}. In this event, the output from pin CLK provides the clock signal for cascaded PCF8566s in the system.

Where resistor R_{osc} to V_{SS} is present, the internal oscillator is selected. The relationship between the oscillator frequency on pin CLK (f_{clk}) and R_{osc} is shown in Fig.9.



$$f_{clk} \approx \left(\frac{3.4 \times 10^7}{R_{osc}}\right)(kHz)$$

Fig.9 Oscillator frequency as a function of R_{osc}.

6.5.2 EXTERNAL CLOCK

The condition for external clock is made by connecting pin OSC to pin V_{DD}; pin CLK then becomes the external clock input.

The clock frequency (f_{clk}) determines the LCD frame frequency and the maximum rate for data reception from the I²C-bus. To allow I²C-bus transmissions at their maximum data rate of 100 kHz, f_{clk} should be chosen to be above 125 kHz.

A clock signal must always be supplied to the device; removing the clock may freeze the LCD in a DC state.

6.6 Timing

The timing of the PCF8576 organizes the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. In cascaded applications, the synchronization signal $\overline{SYNC}$ maintains the correct timing relationship between the PCF8576s in the system. The timing also generates the LCD frame frequency which it derives as an integer multiple of the clock frequency (see Table 3). The frame frequency is set by the MODE SET commands when internal clock is used, or by the frequency applied to pin CLK when external clock is used.

The ratio between the clock frequency and the LCD frame frequency depends on the mode in which the device is operating. In the power-saving mode the reduction ratio is six times smaller; this allows the clock frequency to be reduced by a factor of six. The reduced clock frequency results in a significant reduction in power dissipation. The lower clock frequency has the disadvantage of increasing the response time when large amounts of display data are transmitted on the I²C-bus.

When a device is unable to digest a display data byte before the next one arrives, it holds the SCL line LOW until the first display data byte is stored. This slows down the transmission rate of the I²C-bus but no data loss occurs.

Table 3 LCD frame frequencies

PCF8576 MODE	FRAME FREQUENCY	NOMINAL FRAME FREQUENCY (Hz)
Normal mode	$\frac{f_{clk}}{2880}$	64
Power-saving mode	$\frac{f_{clk}}{480}$	64

6.7 Display latch

The display latch holds the display data while the corresponding multiplex signals are generated. There is a one-to-one relationship between the data in the display latch, the LCD segment outputs and one column of the display RAM.

6.8 Shift register

The shift register serves to transfer display information from the display RAM to the display latch while previous data is displayed.

6.9 Segment outputs

The LCD drive section includes 40 segment outputs pins S0 to S39 which should be connected directly to the LCD. The segment output signals are generated in accordance with the multiplexed backplane signals and with data resident in the display latch. When less than 40 segment outputs are required the unused segment outputs should be left open-circuit.

6.10 Backplane outputs

The LCD drive section includes four backplane outputs BP0 to BP3 which should be connected directly to the LCD. The backplane output signals are generated in accordance with the selected LCD drive mode. If less than four backplane outputs are required the unused outputs can be left open-circuit. In the 1 : 3 multiplex drive mode BP3 carries the same signal as BP1, therefore these two adjacent outputs can be connected together to give enhanced drive capabilities. In the 1 : 2 multiplex drive mode BP0 and BP2, BP1 and BP3 respectively carry the same signals and may also be paired to increase the drive capabilities. In the static drive mode the same signal is carried by all four backplane outputs and they can be connected in parallel for very high drive requirements.

6.11 Display RAM

The display RAM is a static 40 × 4-bit RAM which stores LCD data. A logic 1 in the RAM bit-map indicates the on state of the corresponding LCD segment; similarly, a logic 0 indicates the off state. There is a one-to-one correspondence between the RAM addresses and the segment outputs, and between the individual bits of a RAM word and the backplane outputs. The first RAM column corresponds to the 40 segments operated with respect to backplane BP0 (see Fig.10). In multiplexed LCD applications the segment data of the second, third and fourth column of the display RAM are time-multiplexed with BP1, BP2 and BP3 respectively.

When display data is transmitted to the PCF8576 the display bytes received are stored in the display RAM in accordance with the selected LCD drive mode.
To illustrate the filling order, an example of a 7-segment numeric display showing all drive modes is given in Fig.11; the RAM filling organization depicted applies equally to other LCD types.

With reference to Fig.11, in the static drive mode the eight transmitted data bits are placed in bit 0 of eight successive display RAM addresses. In the 1 : 2 multiplex drive mode the eight transmitted data bits are placed in bits 0 and 1 of four successive display RAM addresses. In the 1 : 3 multiplex drive mode these bits are placed in bits 0, 1 and 2 of three successive addresses, with bit 2 of the third address left unchanged. This last bit may, if necessary, be controlled by an additional transfer to this address but care should be taken to avoid overriding adjacent data because full bytes are always transmitted. In the 1 : 4 multiplex drive mode the eight transmitted data bits are placed in bits 0, 1, 2 and 3 of two successive display RAM addresses.

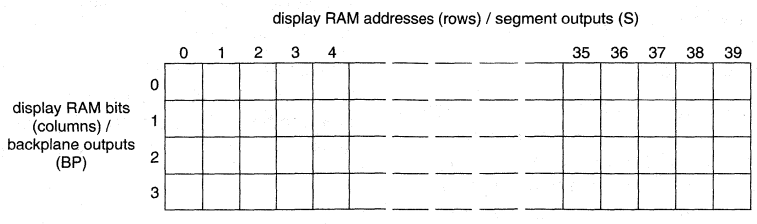


Fig.10 Display RAM bit-map showing direct relationship between display RAM addresses and segment outputs, and between bits in a RAM word and backplane outputs.

6.12 Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the data pointer by the LOAD DATA POINTER command. Following this, an arriving data byte is stored starting at the display RAM address indicated by the data pointer thereby observing the filling order shown in Fig.11. The data pointer is automatically incremented in accordance with the chosen LCD configuration. That is, after each byte is stored, the contents of the data pointer are incremented by eight (static drive mode), by four (1 : 2 multiplex drive mode) or by two (1 : 4 multiplex drive mode).

6.13 Subaddress counter

The storage of display data is conditioned by the contents of the subaddress counter. Storage is allowed to take place only when the contents of the subaddress counter agree with the hardware subaddress applied to A0, A1 and A2. The subaddress counter value is defined by the DEVICE SELECT command. If the contents of the subaddress counter and the hardware subaddress do not agree then data storage is inhibited but the data pointer is incremented as if data storage had taken place.
The subaddress counter is also incremented when the data pointer overflows.

The storage arrangements described lead to extremely efficient data loading in cascaded applications. When a series of display bytes are sent to the display RAM, automatic wrap-over to the next PCF8576 occurs when the last RAM address is exceeded. Subaddressing across device boundaries is successful even if the change to the next device in the cascade occurs within a transmitted character (such as during the 14th display data byte transmitted in 1 : 3 multiplex mode).

6.14 Output bank selector

This selects one of the four bits per display RAM address for transfer to the display latch. The actual bit chosen depends on the particular LCD drive mode in operation and on the instant in the multiplex sequence. In 1 : 4 multiplex, all RAM addresses of bit 0 are the first to be selected, these are followed by the contents of bit 1, bit 2 and then bit 3. Similarly in 1 : 3 multiplex, bits 0, 1 and 2 are selected sequentially. In 1 : 2 multiplex, bits 0 and 1 are selected and, in the static mode, bit 0 is selected.

The PCF8576 includes a RAM bank switching feature in the static and 1 : 2 multiplex drive modes. In the static drive mode, the BANK SELECT command may request the contents of bit 2 to be selected for display instead of bit 0 contents. In the 1 : 2 drive mode, the contents of bits 2 and 3 may be selected instead of bits 0 and 1. This gives the provision for preparing display information in an alternative bank and to be able to switch to it once it is assembled.

6.15 Input bank selector

The input bank selector loads display data into the display RAM in accordance with the selected LCD drive configuration. Display data can be loaded in bit 2 in static drive mode or in bits 2 and 3 in 1 : 2 drive mode by using the BANK SELECT command. The input bank selector functions independent of the output bank selector.

6.16 Blinker

The display blinking capabilities of the PCF8576 are very versatile. The whole display can be blinked at frequencies selected by the BLINK command. The blinking frequencies are integer multiples of the clock frequency; the ratios between the clock and blinking frequencies depend on the mode in which the device is operating, as shown in Table 4.

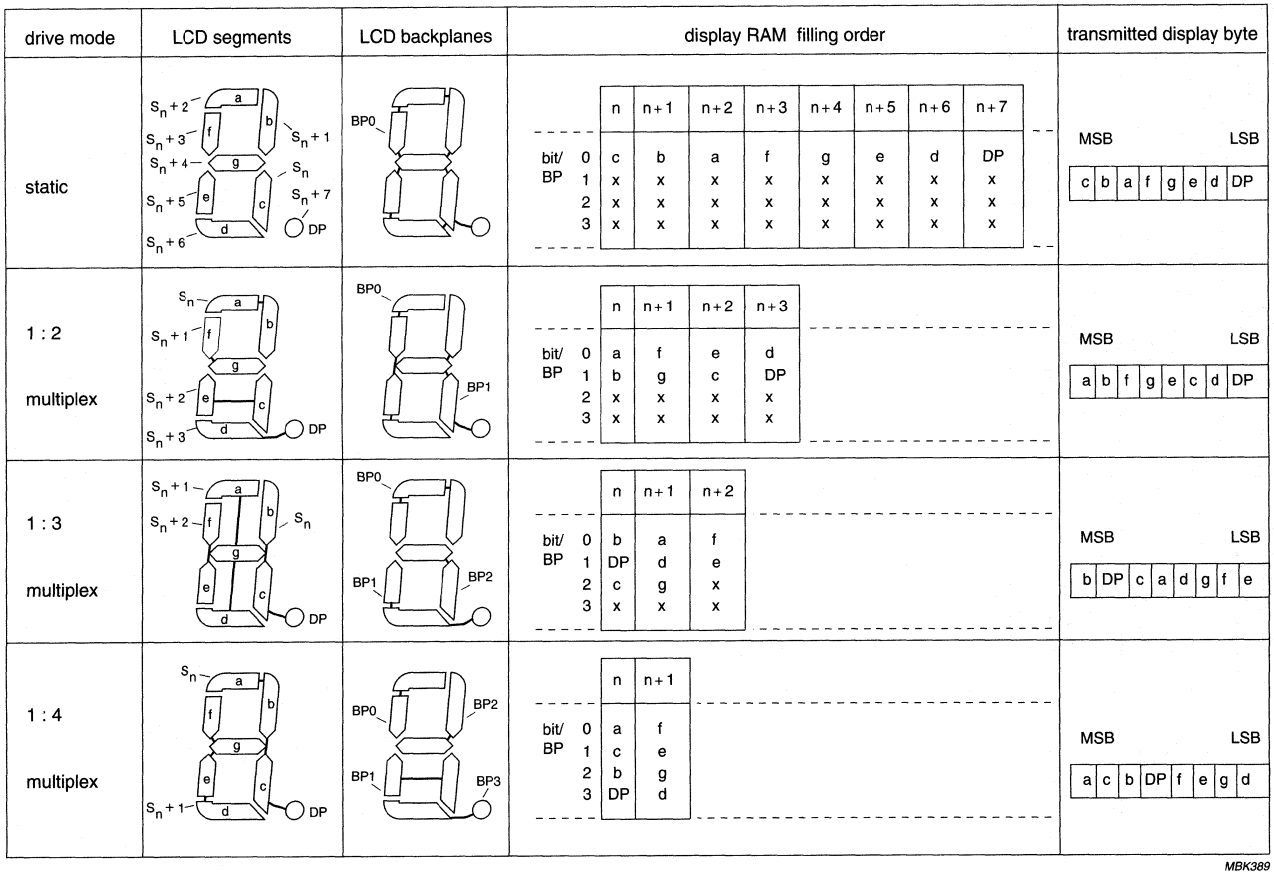
An additional feature is for an arbitrary selection of LCD segments to be blinked. This applies to the static and 1 : 2 LCD drive modes and can be implemented without any communication overheads. By means of the output bank selector, the displayed RAM banks are exchanged with alternate RAM banks at the blinking frequency. This mode can also be specified by the BLINK command.

In the 1 : 3 and 1 : 4 multiplex modes, where no alternate RAM bank is available, groups of LCD segments can be blinked by selectively changing the display RAM data at fixed time intervals.

If the entire display is to be blinked at a frequency other than the nominal blinking frequency, this can be effectively performed by resetting and setting the display enable bit E at the required rate using the MODE SET command.

Table 4 Blinking frequencies

BLINKING MODE	NORMAL OPERATING MODE RATIO	POWER-SAVING MODE RATIO	NOMINAL BLINKING FREQUENCY
Off	–	–	blinking off
2 Hz	$\frac{f_{clk}}{92160}$	$\frac{f_{clk}}{15360}$	2 Hz
1 Hz	$\frac{f_{clk}}{184320}$	$\frac{f_{clk}}{30720}$	1 Hz
0.5 Hz	$\frac{f_{clk}}{368640}$	$\frac{f_{clk}}{61440}$	0.5 Hz



x = data bit unchanged.

Fig.11 Relationships between LCD layout, drive mode, display RAM filling order and display data transmitted over the I²C-bus.

7 CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

7.1 Bit transfer (see Fig.12)

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

7.2 START and STOP conditions (see Fig.13)

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P).

7.3 System configuration (see Fig.14)

A device generating a message is a 'transmitter', a device receiving a message is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves'.

7.4 Acknowledge (see Fig.15)

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

7.5 PCF8576 I²C-bus controller

The PCF8576 acts as an I²C-bus slave receiver. It does not initiate I²C-bus transfers or transmit data to an I²C-bus master receiver. The only data output from the PCF8576 are the acknowledge signals of the selected devices. Device selection depends on the I²C-bus slave address, on the transferred command data and on the hardware subaddress.

In single device application, the hardware subaddress inputs A0, A1 and A2 are normally connected to V_{SS} which defines the hardware subaddress 0. In multiple device applications A0, A1 and A2 are connected to V_{SS} or V_{DD} in accordance with a binary coding scheme such that no two devices with a common I²C-bus slave address have the same hardware subaddress.

In the power-saving mode it is possible that the PCF8576 is not able to keep up with the highest transmission rates when large amounts of display data are transmitted. If this situation occurs, the PCF8576 forces the SCL line to LOW until its internal operations are completed. This is known as the 'clock synchronization feature' of the I²C-bus and serves to slow down fast transmitters. Data loss does not occur.

7.6 Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

7.7 I²C-bus protocol

Two I²C-bus slave addresses (0111000 and 0111001) are reserved for the PCF8576. The least significant bit of the slave address that a PCF8576 will respond to is defined by the level connected at its input pin SA0. Therefore, two types of PCF8576 can be distinguished on the same I²C-bus which allows:

- Up to 16 PCF8576s on the same I²C-bus for very large LCD applications
- The use of two types of LCD multiplex on the same I²C-bus.

The I²C-bus protocol is shown in Fig.16. The sequence is initiated with a START condition (S) from the I²C-bus master which is followed by one of the two PCF8576 slave addresses available. All PCF8576s with the corresponding SA0 level acknowledge in parallel with the slave address but all PCF8576s with the alternative SA0 level ignore the whole I²C-bus transfer.

After acknowledgement, one or more command bytes (m) follow which define the status of the addressed PCF8576s.

The last command byte is tagged with a cleared most significant bit, the continuation bit C. The command bytes are also acknowledged by all addressed PCF8576s on the bus.

After the last command byte, a series of display data bytes (n) may follow. These display bytes are stored in the display RAM at the address specified by the data pointer and the subaddress counter. Both data pointer and subaddress counter are automatically updated and the data is directed to the intended PCF8576 device. The acknowledgement after each byte is made only by the (A0, A1 and A2) addressed PCF8576. After the last display byte, the I²C-bus master issues a STOP condition (P).

7.8 Command decoder

The command decoder identifies command bytes that arrive on the I²C-bus. All available commands carry a continuation bit C in their most significant bit position (Fig.17). When this bit is set, it indicates that the next byte of the transfer to arrive will also represent a command. If this bit is reset, it indicates the last command byte of the transfer. Further bytes will be regarded as display data.

The five commands available to the PCF8576 are defined in Table 5.

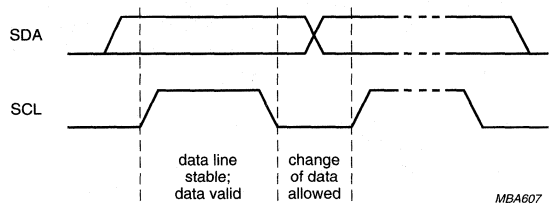


Fig.12 Bit transfer.

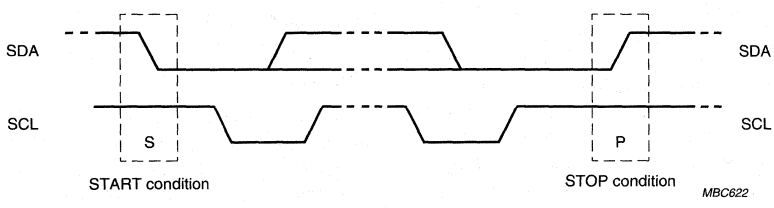


Fig.13 Definition of START and STOP conditions.

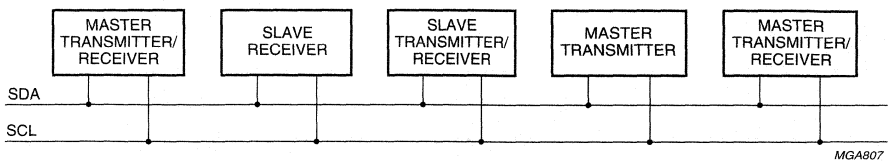


Fig.14 System configuration.

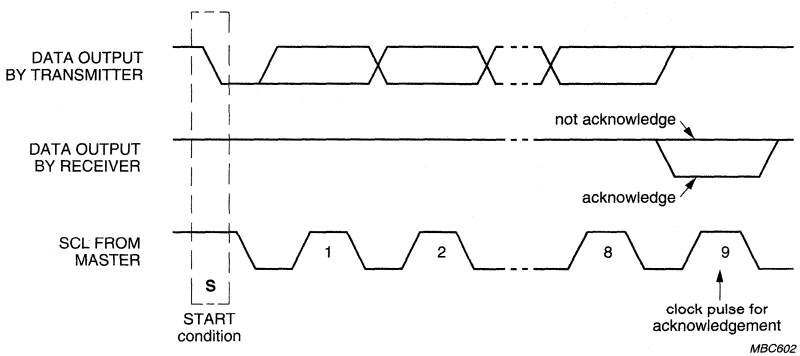


Fig.15 Acknowledgement on the I^2C-bus.

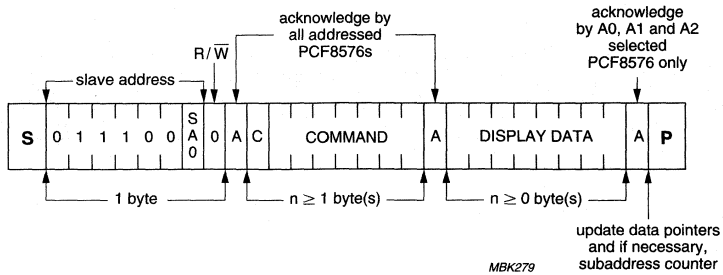
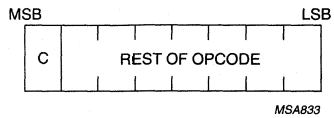


Fig.16 I²C-bus protocol.



C = 0; last command.
C = 1; commands continue.

Fig.17 General format of command byte.

Table 5 Definition of PCF8576 commands

COMMAND	OPCODE	OPTIONS	DESCRIPTION
MODE SET	C 1 0 LP E B M1 M0	Table 6	Defines LCD drive mode.
		Table 7	Defines LCD bias configuration.
		Table 8	Defines display status. The possibility to disable the display allows implementation of blinking under external control.
		Table 9	Defines power dissipation mode.
LOAD DATA POINTER	C 0 P5 P4 P3 P2 P1 P0	Table 10	Six bits of immediate data, bits P5 to P0, are transferred to the data pointer to define one of forty display RAM addresses.
DEVICE SELECT	C 1 1 0 0 A2 A1 A0	Table 11	Three bits of immediate data, bits A2 to A0, are transferred to the subaddress counter to define one of eight hardware subaddresses.
BANK SELECT	C 1 1 1 1 0 I O	Table 12	Defines input bank selection (storage of arriving display data).
		Table 13	Defines output bank selection (retrieval of LCD display data). The BANK SELECT command has no effect in 1 : 3 and 1 : 4 multiplex drive modes.
BLINK	C 1 1 1 0 A BF1 BF0	Table 14	Defines the blinking frequency.
		Table 15	Selects the blinking mode; normal operation with frequency set by BF1, BF0 or blinking by alternation of display RAM banks. Alternation blinking does not apply in 1 : 3 and 1 : 4 multiplex drive modes.

Table 6 MODE SET option 1

LCD DRIVE MODE		BITS	
DRIVE MODE	BACKPLANE	M1	M0
Static	1 BP	0	1
1 : 2	MUX (2 BP)	1	0
1 : 3	MUX (3 BP)	1	1
1 : 4	MUX (4 BP)	0	0

Table 7 MODE SET option 2

LCD BIAS	BIT B
$\frac{1}{3}$bias	0
$\frac{1}{2}$bias	1

Table 8 MODE SET option 3

DISPLAY STATUS	BIT E
Disabled (blank)	0
Enabled	1

Table 9 MODE SET option 4

MODE	BIT LP
Normal mode	0
Power-saving mode	1

Table 10 LOAD DATA POINTER option 1

DESCRIPTION	BITS					
6-bit binary value of 0 to 39	P5	P4	P3	P2	P1	P0

Table 11 DEVICE SELECT option 1

DESCRIPTION	BITS		
3-bit binary value of 0 to 7	A2	A1	A0

Table 12 BANK SELECT option 1

STATIC	1 : 2 MUX	BIT I
RAM bit 0	RAM bits 0 and 1	0
RAM bit 2	RAM bits 2 and 3	1

Table 13 BANK SELECT option 2

STATIC	1 : 2 MUX	BIT O
RAM bit 0	RAM bits 0 and 1	0
RAM bit 2	RAM bits 2 and 3	1

Table 14 BLINK option 1

BLINK FREQUENCY	BITS	
	BF1	BF0
Off	0	0
2 Hz	0	1
1 Hz	1	0
0.5 Hz	1	1

Table 15 BLINK option 2

BLINK MODE	BIT A
Normal blinking	0
Alternation blinking	1

7.9 Display controller

The display controller executes the commands identified by the command decoder. It contains the status registers of the PCF8576 and co-ordinates their effects.
The controller is also responsible for loading display data into the display RAM as required by the filling order.

7.10 Cascaded operation

In large display configurations, up to 16 PCF8576s can be distinguished on the same I²C-bus by using the 3-bit hardware subaddress (A0, A1 and A2) and the programmable I²C-bus slave address (SA0). When cascaded PCF8576s are synchronized so that they can share the backplane signals from one of the devices in the cascade. Such an arrangement is cost-effective in large LCD applications since the backplane outputs of only one device need to be through-plated to the backplane electrodes of the display. The other PCF8576s of the cascade contribute additional segment outputs but their backplane outputs are left open-circuit (see Fig.18).

The $\overline{\text{SYNC}}$ line is provided to maintain the correct synchronization between all cascaded PCF8576s. This synchronization is guaranteed after the Power-on reset. The only time that $\overline{\text{SYNC}}$ is likely to be needed is if synchronization is accidentally lost (e.g. by noise in adverse electrical environments; or by the definition of a multiplex mode when PCF8576s with differing SA0 levels are cascaded). $\overline{\text{SYNC}}$ is organized as an input/output pin; the output selection being realized as an open-drain driver with an internal pull-up resistor. A PCF8576 asserts the $\overline{\text{SYNC}}$ line at the onset of its last active backplane signal and monitors the $\overline{\text{SYNC}}$ line at all other times. Should synchronization in the cascade be lost, it will be restored by the first PCF8576 to assert $\overline{\text{SYNC}}$. The timing relationship between the backplane waveforms and the $\overline{\text{SYNC}}$ signal for the various drive modes of the PCF8576 are shown in Fig.19.

For single plane wiring of packaged PCF8576s and chip-on-glass cascading, see Chapter 12.

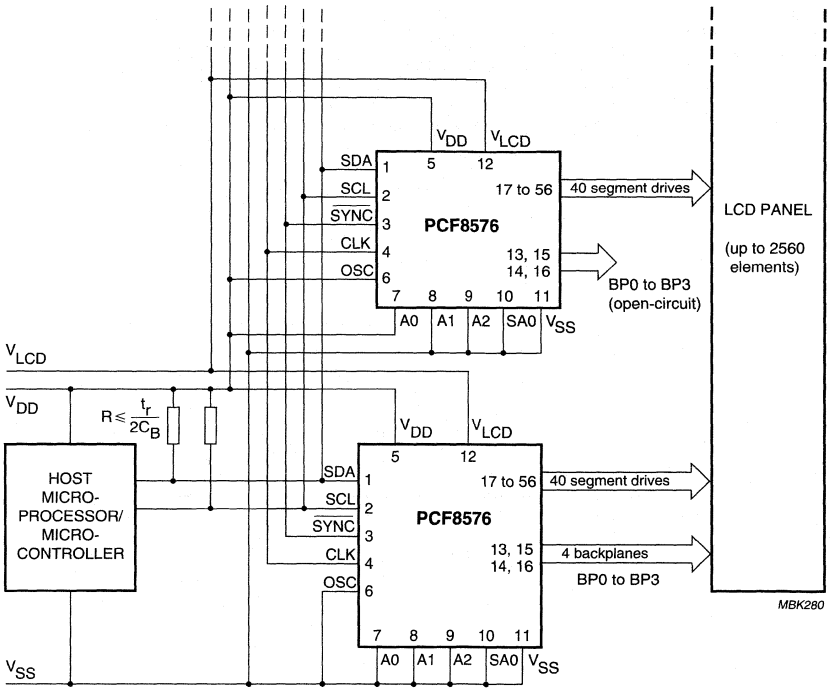
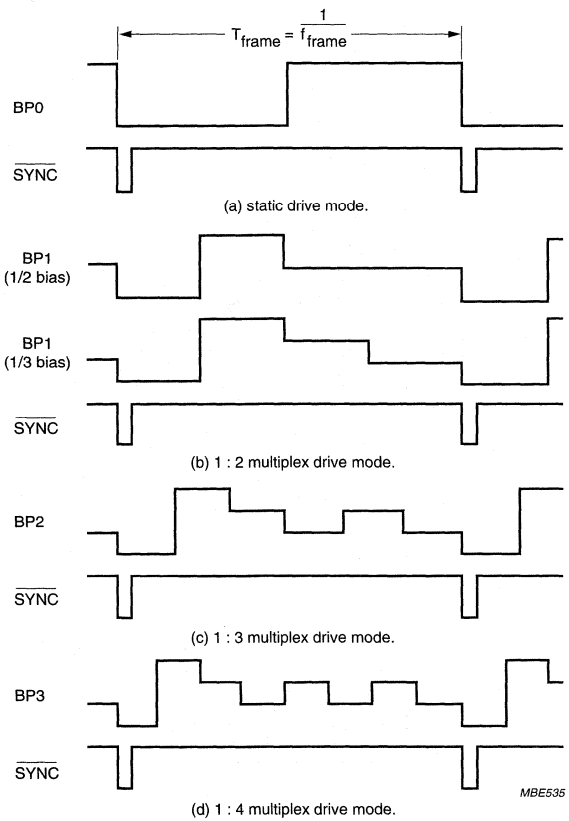


Fig.18 Cascaded PCF8576 configuration.



Excessive capacitive coupling between SCL or CLK and $\overline{SYNC}$ may cause erroneous synchronization. If this proves to be a problem, the capacitance of the $\overline{SYNC}$ line should be increased (e.g. by an external capacitor between $\overline{SYNC}$ and V_{DD}). Degradation of the positive edge of the $\overline{SYNC}$ pulse may be countered by an external pull-up resistor.

Fig.19 Synchronization of the cascade for the various PCF8576 drive modes.

8 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.5	+11.0	V
V_{LCD}	LCD supply voltage	V_{DD} − 11.0	V_{DD}	V
V_I	input voltage SDA, SCL, CLK, $\overline{SYNC}$, SA0, OSC, A0 to A2	V_{SS} − 0.5	V_{DD} + 0.5	V
V_O	output voltage S0 to S39, BP0 to BP3	V_{LCD} − 0.5	V_{DD} + 0.5	V
I_I	DC input current	−	20	mA
I_O	DC output current	−	25	mA
I_{DD}, I_{SS}, I_{LCD}	V_{DD}, V_{SS} or V_{LCD} current	−	50	mA
P_{tot}	total power dissipation	−	400	mW
P_O	power dissipation per output	−	100	mW
T_{stg}	storage temperature	−65	+150	°C

9 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see *"Handling MOS Devices"*).

10 DC CHARACTERISTICS

V_{DD} = 2 to 9 V; V_{SS} = 0 V; V_{LCD} = V_{DD} − 2 V to V_{DD} − 9 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage		2	–	9	V
V_{LCD}	LCD supply voltage	note 1	V_{DD} − 9	–	V_{DD} − 2	V
I_{DD}	supply current	note 2				
	normal mode	f_{clk} = 200 kHz	–	–	180	μA
	power-saving mode	f_{clk} = 35 kHz; V_{DD} = 3.5 V; V_{LCD} = 0 V; A0, A1 and A2 connected to V_{SS}	–	–	60	μA
Logic						
V_{IL}	LOW-level input voltage		V_{SS}	–	0.3V_{DD}	V
V_{IH}	HIGH-level input voltage		0.7V_{DD}	–	V_{DD}	V
V_{OL}	LOW-level output voltage	I_{OL} = 0 mA	–	–	0.05	V
V_{OH}	HIGH-level output voltage	I_{OH} = 0 mA	V_{DD} − 0.05	–	–	V
I_{OL1}	LOW-level output current CLK, $\overline{SYNC}$	V_{OL} = 1 V; V_{DD} = 5 V	1	–	–	mA
I_{OH1}	HIGH-level output current CLK	V_{OH} = 4 V; V_{DD} = 5 V	1	–	–	mA
I_{OL2}	LOW-level output current SDA and SCL	V_{OL} = 0.4 V; V_{DD} = 5 V	3	–	–	mA
I_{L1}	leakage current SA0, A0 to A2, CLK, SDA and SCL	V_I = V_{DD} or V_{SS}	–	–	1	μA
I_{L2}	leakage current OSC	V_I = V_{DD}	–	–	1	μA
I_{pd}	A0, A1, A2 and OSC pull-down current	V_I = 1 V; V_{DD} = 5 V	20	50	150	μA
R_{SYNC}	pull-up resistor ($\overline{SYNC}$)		20	50	150	kΩ
V_{POR}	Power-on reset voltage level	note 3	–	1.0	1.6	V
C_I	input capacitance	note 4	–	–	7	pF
LCD outputs						
V_{BP}	DC voltage component BP0 to BP3	C_{BP} = 35 nF	–	20	–	mV
V_S	DC voltage component S0 to S39	C_S = 5 nF	–	20	–	mV
R_{BP}	output resistance BP0 to BP3	note 5; V_{LCD} = V_{DD} − 5 V	–	–	5	kΩ
R_S	output resistance S0 to S39	note 5; V_{LCD} = V_{DD} − 5 V	–	–	7.5	kΩ

Notes

1. $V_{LCD} \leq V_{DD} - 3$ V for ⅓bias.
2. LCD outputs are open-circuit; inputs at V_{SS} or V_{DD}; external clock with 50% duty factor; I²C-bus inactive.
3. Resets all logic when $V_{DD} < V_{POR}$.
4. Periodically sampled, not 100% tested.
5. Outputs measured one at a time.

11 AC CHARACTERISTICS

V_{DD} = 2 to 9 V; V_{SS} = 0 V; V_{LCD} = V_{DD} − 2 V to V_{DD} − 9 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{clk}	oscillator frequency on pin CLK					
	normal mode	V_{DD} = 5 V; note 1	125	200	288	kHz
	power-saving mode	V_{DD} = 3.5 V	21	31	48	kHz
t_{clkH}	CLK HIGH time	see Fig.21	1	–	–	µs
t_{clkL}	CLK LOW time		1	–	–	µs
t_{PSYNC}	$\overline{SYNC}$ propagation delay time		–	–	400	ns
t_{SYNCL}	$\overline{SYNC}$ LOW time		1	–	–	µs
t_{PLCD}	driver delays with test loads	V_{LCD} = V_{DD} − 5 V; see Fig.20	–	–	30	µs
Timing characteristics: I²C-bus; note 2; see Fig.22						
t_{SW}	tolerable spike width on bus		–	–	100	ns
t_{BUF}	bus free time		4.7	–	–	µs
$t_{HD;STA}$	START condition hold time		4.0	–	–	µs
$t_{SU;STA}$	set-up time for a repeated START condition		4.7	–	–	µs
t_{LOW}	SCL LOW time		4.7	–	–	µs
t_{HIGH}	SCL HIGH time		4.0	–	–	µs
t_r	SCL and SDA rise time		–	–	1	µs
t_f	SCL and SDA fall time		–	–	0.3	µs
C_B	capacitive bus line load		–	–	400	pF
$t_{SU;DAT}$	data set-up time		250	–	–	ns
$t_{HD;DAT}$	data hold time		0	–	–	ns
$t_{SU;STO}$	set-up time for STOP condition		4.0	–	–	µs

Notes

1. At f_{clk} < 125 kHz, I²C-bus maximum transmission speed is derated.
2. All timing values are valid within the operating supply voltage and ambient temperature range and are referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

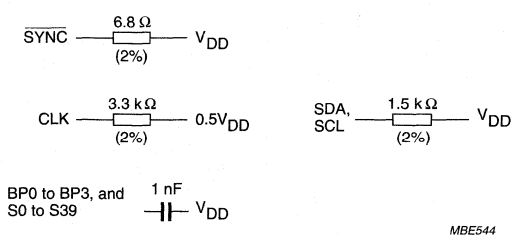


Fig.20 Test loads.

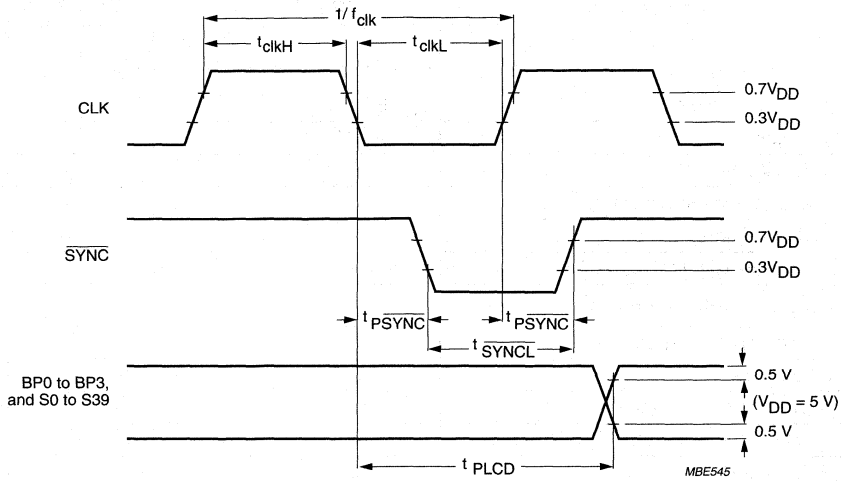


Fig.21 Driver timing waveforms.

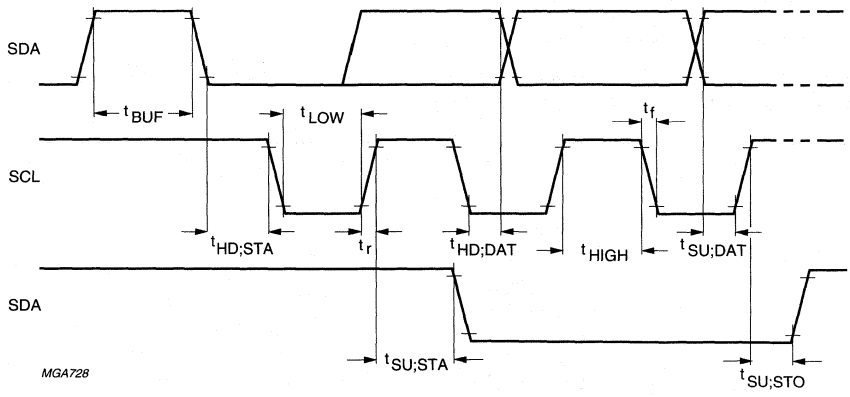
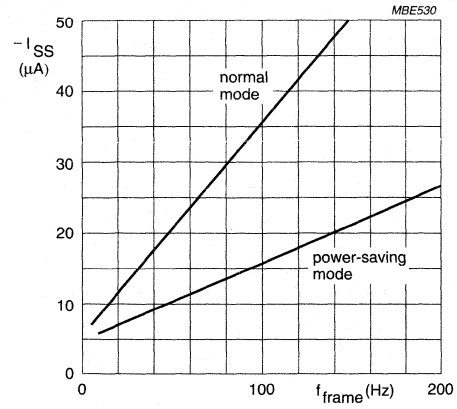


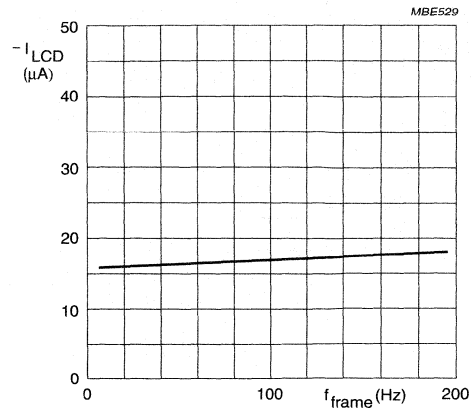
Fig.22 I²C-bus timing waveforms.

11.1 Typical supply current characteristics



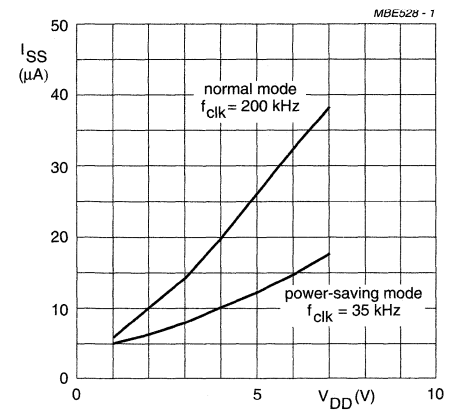
V_{DD} = 5 V; V_{LCD} = 0 V; T_{amb} = 25 °C.

Fig.23 $-I_{SS}$ as a function of f_{frame}.



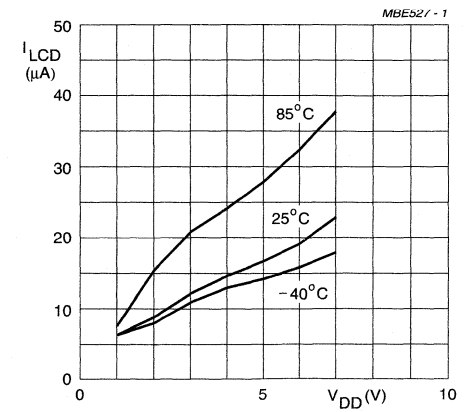
V_{DD} = 5 V; V_{LCD} = 0 V; T_{amb} = 25 °C.

Fig.24 $-I_{LCD}$ as a function of f_{frame}.



V_{LCD} = 0 V; external clock; T_{amb} = 25 °C.

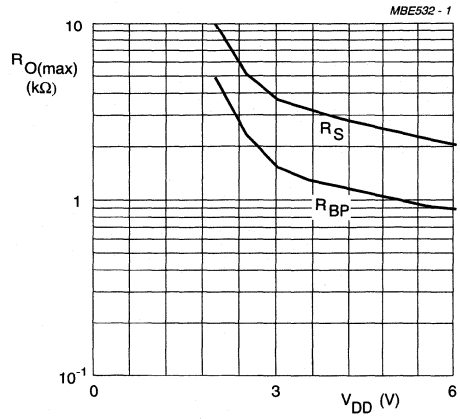
Fig.25 I_{SS} as a function of V_{DD}.



V_{LCD} = 0 V; external clock; f_{clk} = nominal frequency.

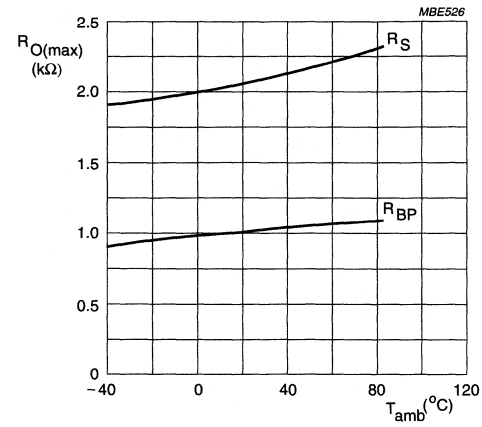
Fig.26 I_{LCD} as a function of V_{DD}.

11.2 Typical characteristics of LCD outputs



V_{LCD} = 0 V; T_{amb} = 25 °C.

Fig.27 $R_{O(max)}$ as a function of V_{DD}.



V_{DD} = 5 V; V_{LCD} = 0 V.

Fig.28 $R_{O(max)}$ as a function of T_{amb}.

12 APPLICATION INFORMATION

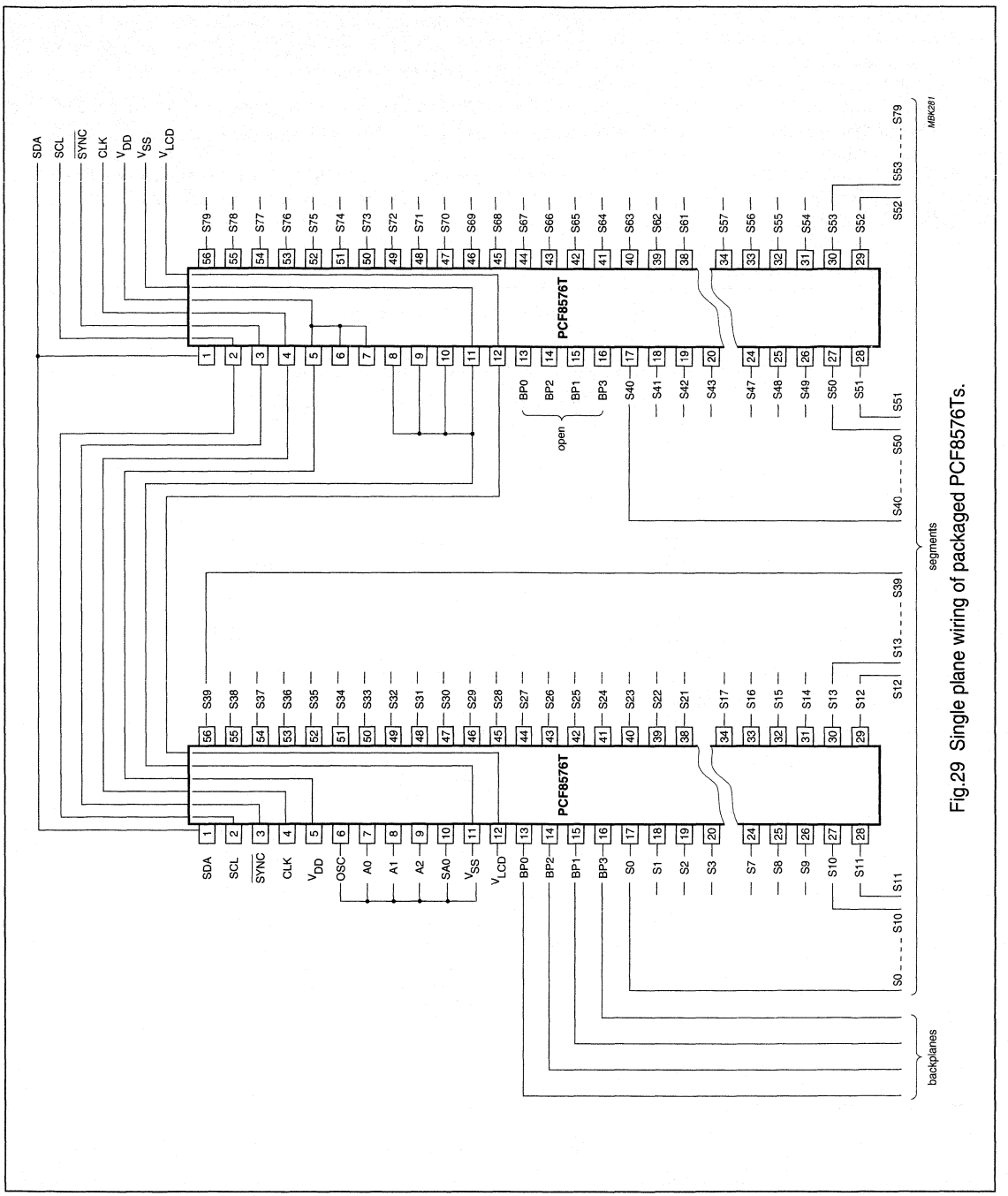


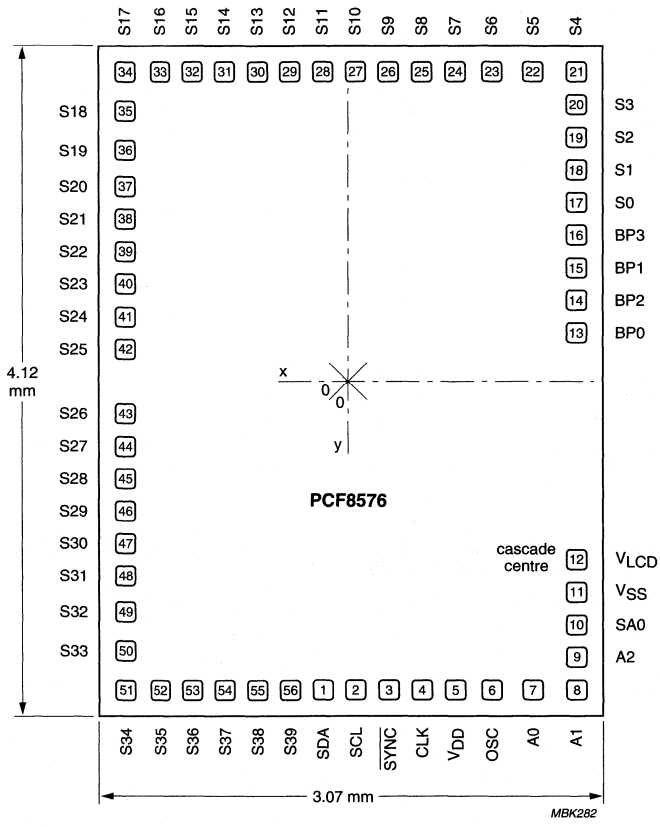
Fig.29 Single plane wiring of packaged PCF8576Ts.

12.1 Chip-on-glass cascadability in single plane

In chip-on-glass technology, where driver devices are bonded directly onto glass of the LCD, it is important that the devices may be cascaded without the crossing of conductors, but the paths of conductors can be continued on the glass under the chip. All of this is facilitated by the PCF8576 bonding pad layout (see Fig.30). Pads needing bus interconnection between all PCF8576s of the cascade are V_{DD}, V_{SS}, V_{LCD}, CLK, SCL, SDA and $\overline{SYNC}$. These lines may be led to the corresponding pads of the next PCF8576 through the wide opening between V_{LCD} pad and the backplane output pads. The only bus line that does not require a second opening to lead through to the next PCF8576 is V_{LCD}, being the cascade centre. The placing of V_{LCD} adjacent to V_{SS} allows the two supplies to be connected together.

When an external clocking source is to be used, OSC of all devices should be connected to V_{DD}.
The pads OSC, A0, A1, A2 and SA0 have been placed between V_{SS} and V_{DD} to facilitate wiring of oscillator, hardware subaddress and slave address.

13 BONDING PAD LOCATIONS



Bonding pad dimensions: 120 × 120 μm.

Fig.30 Bonding pad locations.

Table 16 Bonding pad locations (dimensions in μm)
All x/y coordinates are referenced to centre of chip (see Fig.30).

SYMBOL	PAD	x	y
SDA	1	−155	−1900
SCL	2	45	−1900
$\overline{SYNC}$	3	245	−1900
CLK	4	445	−1900
V_{DD}	5	645	−1900
OSC	6	865	−1900
A0	7	1105	−1900
A1	8	1375	−1900
A2	9	1375	−1700
SA0	10	1375	−1500
V_{SS}	11	1375	−1300
V_{LCD}	12	1375	−1100
BP0	13	1375	300
BP2	14	1375	500
BP1	15	1375	700
BP3	16	1375	900
S0	17	1375	1100
S1	18	1375	1300
S2	19	1375	1500
S3	20	1375	1700
S4	21	1375	1900
S5	22	1105	1900
S6	23	865	1900
S7	24	645	1900
S8	25	445	1900
S9	26	245	1900
S10	27	45	1900
S11	28	−155	1900

SYMBOL	PAD	x	y
S12	29	−355	1900
S13	30	−555	1900
S14	31	−755	1900
S15	32	−955	1900
S16	33	−1155	1900
S17	34	−1375	1900
S18	35	−1375	1660
S19	36	−1375	1420
S20	37	−1375	1200
S21	38	−1375	1000
S22	39	−1375	800
S23	40	−1375	600
S24	41	−1375	400
S25	42	−1375	200
S26	43	−1375	−200
S27	44	−1375	−400
S28	45	−1375	−600
S29	46	−1375	−800
S30	47	−1375	−1000
S31	48	−1375	−1200
S32	49	−1375	−1420
S33	50	−1375	−1660
S34	51	−1375	−1900
S35	52	−1155	−1900
S36	53	−955	−1900
S37	54	−755	−1900
S38	55	−555	−1900
S39	56	−355	−900

Universal LCD driver for low multiplex rates

PCF8576C

CONTENTS

Universal LCD driver for low multiplex rates PCF8576C

1 FEATURES

- Single-chip LCD controller/driver
- Selectable backplane drive configuration: static or 2/3/4 backplane multiplexing
- Selectable display bias configuration: static, 1/2 or 1/3
- Internal LCD bias generation with voltage-follower buffers
- 40 segment drives: up to twenty 8-segment numeric characters; up to ten 15-segment alphanumeric characters; or any graphics of up to 160 elements
- 40 × 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- LCD and logic supplies may be separated
- Wide power supply range: from 2 V for low-threshold LCDs and up to 6 V for guest-host LCDs and high-threshold (automobile) twisted nematic LCDs.

  A 9 V version is also available on request.
- Low power consumption
- Power-saving mode for extremely low power consumption in battery-operated and telephone applications
- I²C-bus interface
- TTL/CMOS compatible
- Compatible with any 4-bit, 8-bit or 16-bit microprocessors/microcontrollers
- May be cascaded for large LCD applications (up to 2560 segments possible)
- Cascadable with 24-segment LCD driver PCF8566
- Optimized pinning for plane wiring in both and multiple PCF8576C applications
- Space-saving 56-lead plastic very small outline package (VSO56) or 64-lead low profile quad flat package (LQFP64)
- No external components
- Compatible with chip-on-glass technology
- Manufactured in silicon gate CMOS process.

2 GENERAL DESCRIPTION

The PCF8576C is a peripheral device which interfaces to almost any Liquid Crystal Display (LCD) with low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 40 segments and can easily be cascaded for larger LCD applications. The PCF8576C is compatible with most microprocessors/microcontrollers and communicates via a two-line bidirectional I²C-bus. Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8576CT	VSO56	plastic very small outline package; 56 leads	SOT190-1
PCF8576CU	–	chip in tray	–
PCF8576CU/2	–	chip with bumps in tray	–
PCF8576CU/5	–	unsawn wafer	–
PCF8576CU/7	–	chip with bumps on tape	–
PCF8576CU/10	FFC	chip-on-film frame carrier	–
PCF8576CU/12	FFC	chip with bumps on film frame carrier	–
PCF8576CH	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2

4 BLOCK DIAGRAM

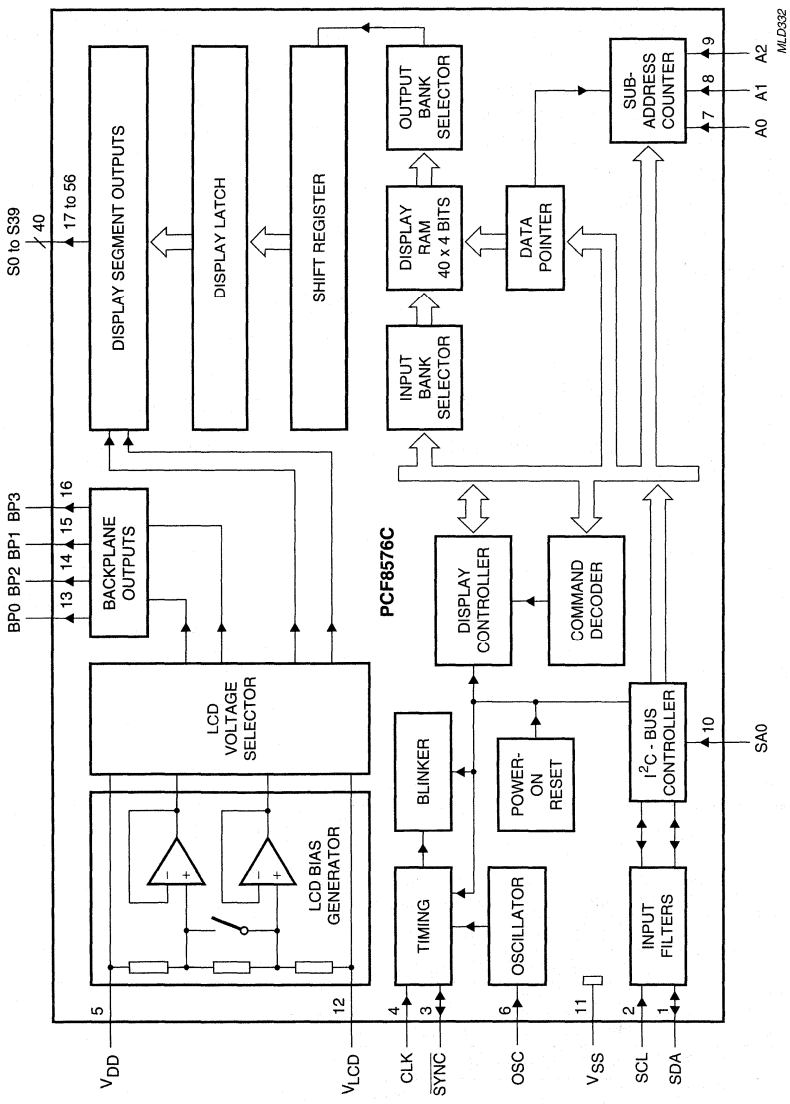


Fig.1 Block diagram; VSO56.

5 PINNING

SYMBOL	PIN		DESCRIPTION
	SOT190	SOT314	
SDA	1	10	I²C-bus serial data input/output
SCL	2	11	I²C-bus serial clock input
$\overline{SYNC}$	3	12	cascade synchronization input/output
CLK	4	13	external clock input
V_{DD}	5	14	supply voltage
OSC	6	15	oscillator input
A0 to A2	7 to 9	16 to 18	I²C-bus subaddress inputs
SA0	10	19	I²C-bus slave address input; bit 0
V_{SS}	11	20	logic ground
V_{LCD}	12	21	LCD supply voltage
BP0, BP2, BP1, BP3	13 to 16	25 to 28	LCD backplane outputs
S0 to S39	17 to 56	29 to 32, 34 to 47, 49 to 64, 2 to 7	LCD segment outputs
n.c.	–	1, 8, 9, 22 to 24, 33 and 48	not connected

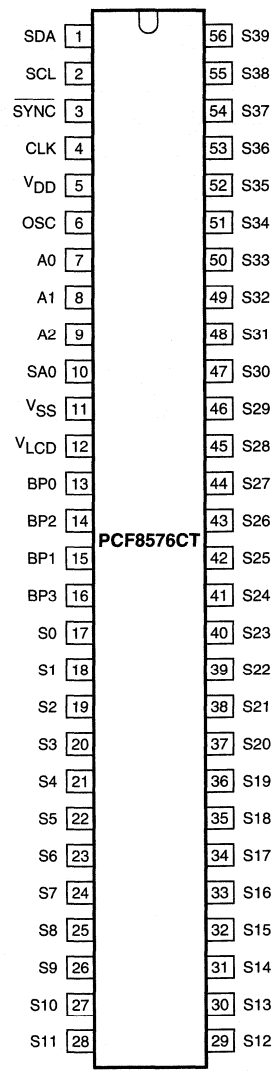


Fig.2 Pin configuration; VSO56.

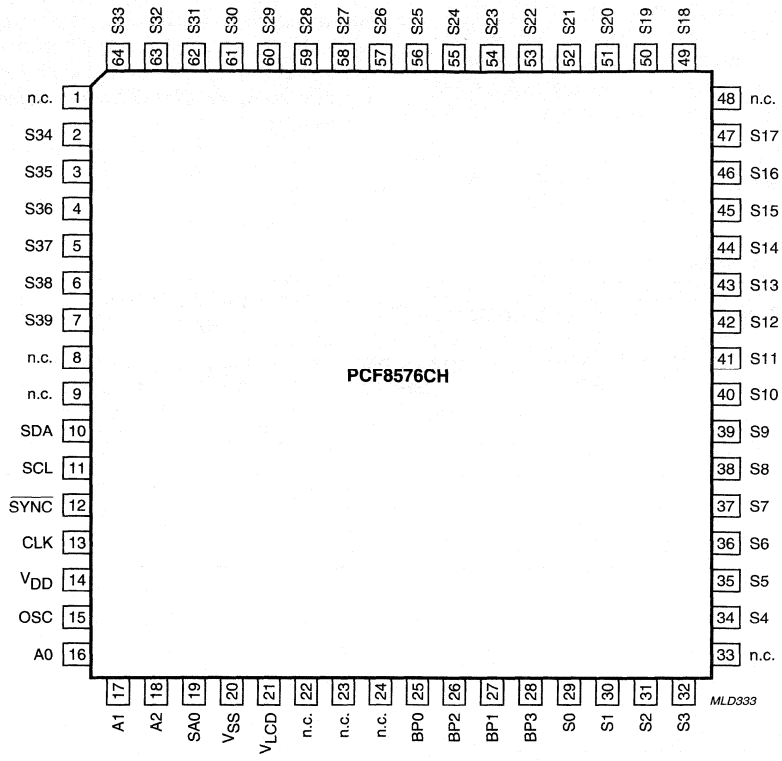


Fig.3 Pin configuration; LQFP64.

6 FUNCTIONAL DESCRIPTION

The PCF8576C is a versatile peripheral device designed to interface to any microprocessor/microcontroller to a wide variety of LCDs. It can directly drive any static or multiplexed LCD containing up to four backplanes and up to 40 segments. The display configurations possible with the PCF8576C depend on the number of active backplane outputs required; a selection of display configurations is given in Table 1.

All of the display configurations given in Table 1 can be implemented in the typical system shown in Fig.4.

The host microprocessor/microcontroller maintains the 2-line I^2C-bus communication channel with the PCF8576C. The internal oscillator is selected by tying OSC (pin 6) to V_{SS} (pin 11). The appropriate biasing voltages for the multiplexed LCD waveforms are generated internally. The only other connections required to complete the system are to the power supplies (V_{DD}, V_{SS} and V_{LCD}) and the LCD panel chosen for the application.

Table 1 Selection of display configurations

NUMBER OF		7-SEGMENTS NUMERIC		14-SEGMENTS ALPHANUMERIC		DOT MATRIX
BACKPLANES	SEGMENTS	DIGITS	INDICATOR SYMBOLS	CHARACTERS	INDICATOR SYMBOLS	
4	160	20	20	10	20	160 dots (4 × 40)
3	120	15	15	8	8	120 dots (3 × 40)
2	80	10	10	5	10	80 dots (2 × 40)
1	40	5	5	2	12	40 dots (1 × 40)

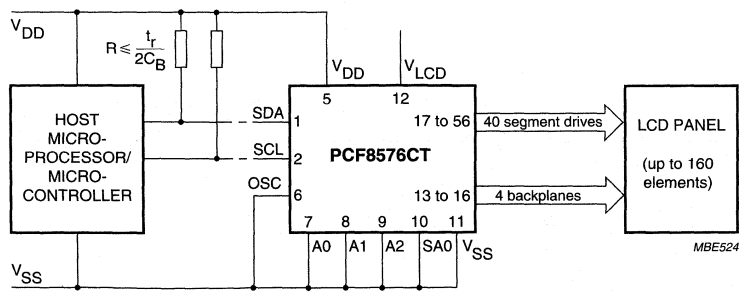


Fig.4 Typical system configuration.

6.1 Power-on reset

At power-on the PCF8576C resets to a starting condition as follows:

1. All backplane outputs are set to V_{DD}.
2. All segment outputs are set to V_{DD}.
3. The drive mode '1 : 4 multiplex with $\frac{1}{3}$bias' is selected.
4. Blinking is switched off.
5. Input and output bank selectors are reset (as defined in Table 5).
6. The I²C-bus interface is initialized.
7. The data pointer and the subaddress counter are cleared.

Data transfers on the I²C-bus should be avoided for 1 ms following power-on to allow completion of the reset action.

6.2 LCD bias generator

The full-scale LCD voltage (V_{op}) is obtained from $V_{DD} - V_{LCD}$. The LCD voltage may be temperature compensated externally through the V_{LCD} supply to pin 12. Fractional LCD biasing voltages are obtained from an internal voltage divider of the three series resistors connected between V_{DD} and V_{LCD}. The centre resistor can be switched out of the circuit to provide a $\frac{1}{2}$bias voltage level for the 1 : 2 multiplex configuration.

6.3 LCD voltage selector

The LCD voltage selector co-ordinates the multiplexing of the LCD in accordance with the selected LCD drive configuration. The operation of the voltage selector is controlled by MODE SET commands from the command decoder. The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of $V_{op} = V_{DD} - V_{LCD}$ and the resulting discrimination ratios (D), are given in Table 2.

A practical value for V_{op} is determined by equating $V_{off(rms)}$ with a defined LCD threshold voltage (V_{th}), typically when the LCD exhibits approximately 10% contrast. In the static drive mode a suitable choice is $V_{op} > 3V_{th}$ approximately.

Multiplex drive ratios of 1 : 3 and 1 : 4 with $\frac{1}{2}$bias are possible but the discrimination and hence the contrast ratios are smaller ($\sqrt{3} = 1.732$ for 1 : 3 multiplex or $\frac{\sqrt{21}}{3} = 1.528$ for 1 : 4 multiplex).

The advantage of these modes is a reduction of the LCD full-scale voltage V_{op} as follows:

- 1 : 3 multiplex ($\frac{1}{2}$bias):

  $V_{op} = \sqrt{6} \times V_{off(rms)} = 2.449\ V_{off(rms)}$

- 1 : 4 multiplex ($\frac{1}{2}$bias):

  $V_{op} = \left[\frac{(4 \times \sqrt{3})}{3}\right] = 2.309\ V_{off(rms)}$

These compare with $V_{op} = 3\ V_{off(rms)}$ when $\frac{1}{3}$bias is used.

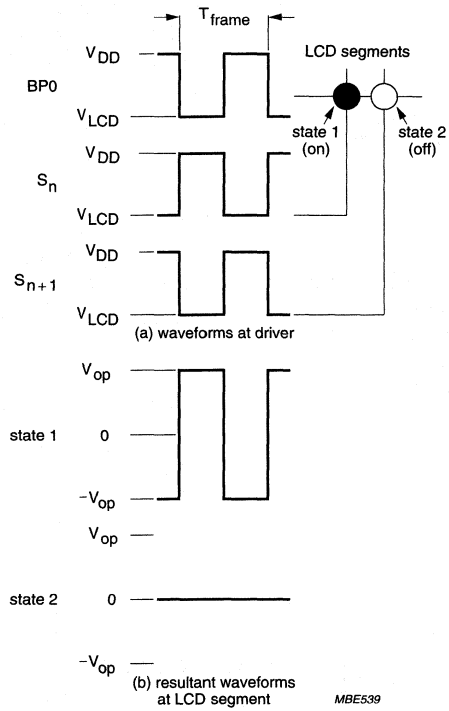
Table 2 Preferred LCD drive modes: summary of characteristics

LCD DRIVE MODE	NUMBER OF		LCD BIAS CONFIGURATION	$\frac{V_{off(rms)}}{V_{op}}$	$\frac{V_{on(rms)}}{V_{op}}$	$D = \frac{V_{on(rms)}}{V_{off(rms)}}$
	BACKPLANES	LEVELS				
static	1	2	static	0	1	∞
1 : 2	2	3	$\frac{1}{2}$	0.354	0.791	2.236
1 : 2	2	4	$\frac{1}{3}$	0.333	0.745	2.236
1 : 3	3	4	$\frac{1}{3}$	0.333	0.638	1.915
1 : 4	4	4	$\frac{1}{3}$	0.333	0.577	1.732

6.4 LCD drive mode waveforms

6.4.1 STATIC DRIVE MODE

The static LCD drive mode is used when a single backplane is provided in the LCD. Backplane and segment drive waveforms for this mode are shown in Fig.5.



$V_{state1}(t) = V_{S_n}(t) - V_{BP0}(t)$

$V_{on(rms)} = V_{op}$

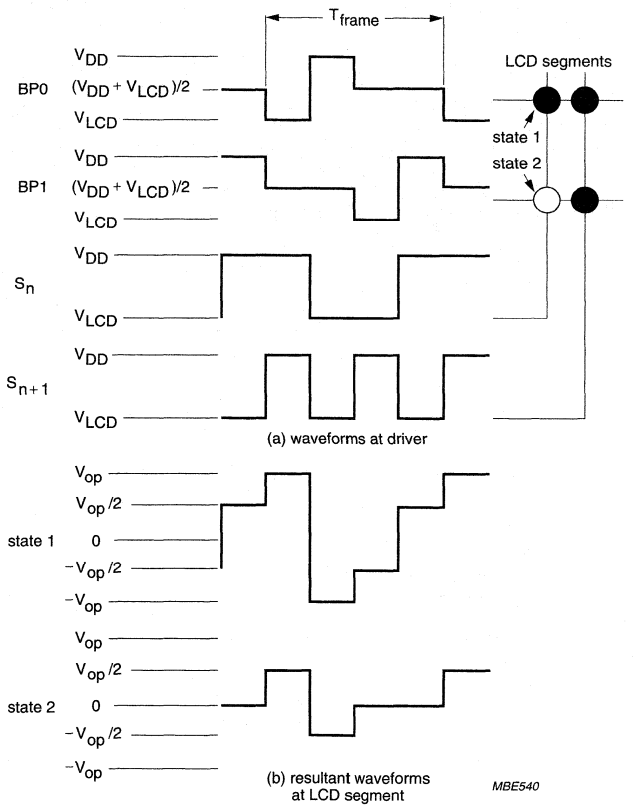
$V_{state2}(t) = V_{S_{n+1}}(t) - V_{BP0}(t)$

$V_{off(rms)} = 0\ V$

Fig.5 Static drive mode waveforms ($V_{op} = V_{DD} - V_{LCD}$).

6.4.2 1 : 2 MULTIPLEX DRIVE MODE

When two backplanes are provided in the LCD, the 1 : 2 multiplex mode applies. The PCF8576C allows use of ½bias or ⅓bias in this mode as shown in Figs 6 and 7.



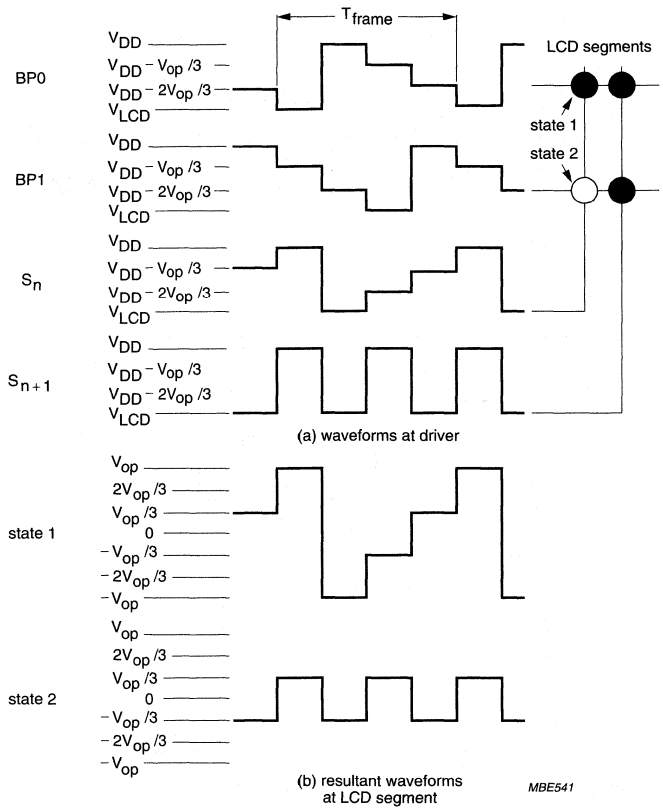
$V_{state1}(t) = V_{S_n}(t) - V_{BP0}(t)$

$V_{on(rms)} = 0.791 V_{op}$

$V_{state2}(t) = V_{S_n}(t) - V_{BP1}(t)$

$V_{off(rms)} = 0.354 V_{op}$

Fig.6 Waveforms for the 1 : 2 multiplex drive mode with ½bias ($V_{op} = V_{DD} - V_{LCD}$).



$V_{state1}(t) = V_{S_n}(t) - V_{BP0}(t)$

$V_{on(rms)} = 0.745V_{op}$

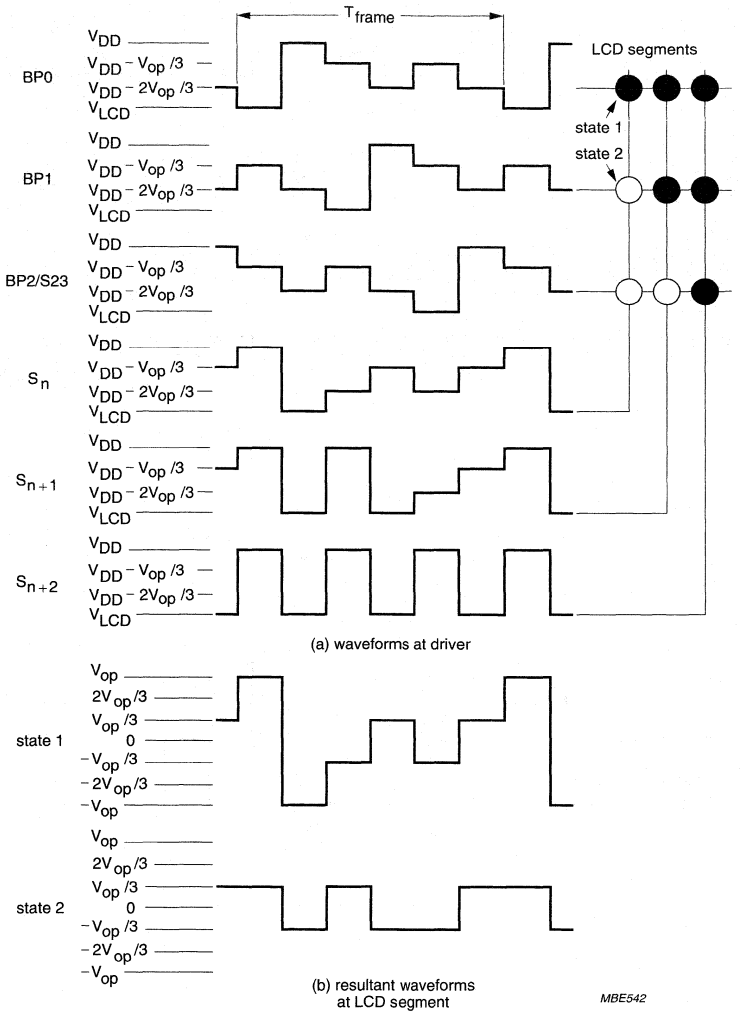
$V_{state2}(t) = V_{S_n}(t) - V_{BP1}(t)$

$V_{off(rms)} = 0.333V_{op}$

Fig.7 Waveforms for the 1 : 2 multiplex drive mode with ⅓bias ($V_{op} = V_{DD} - V_{LCD}$).

6.4.3 1 : 3 MULTIPLEX DRIVE MODE

When three backplanes are provided in the LCD, the 1 : 3 multiplex drive mode applies, as shown in Fig.8.



$V_{state1}(t) = V_{S_n}(t) - V_{BP0}(t)$

$V_{on(rms)} = 0.638V_{op}$

$V_{state2}(t) = V_{S_n}(t) - V_{BP1}(t)$

$V_{off(rms)} = 0.333V_{op}$

Fig.8 Waveforms for the 1 : 3 multiplex drive mode ($V_{op} = V_{DD} - V_{LCD}$).

6.4.4 1 : 4 MULTIPLEX DRIVE MODE

When four backplanes are provided in the LCD, the 1 : 4 multiplex drive mode applies, as shown in Fig.9.

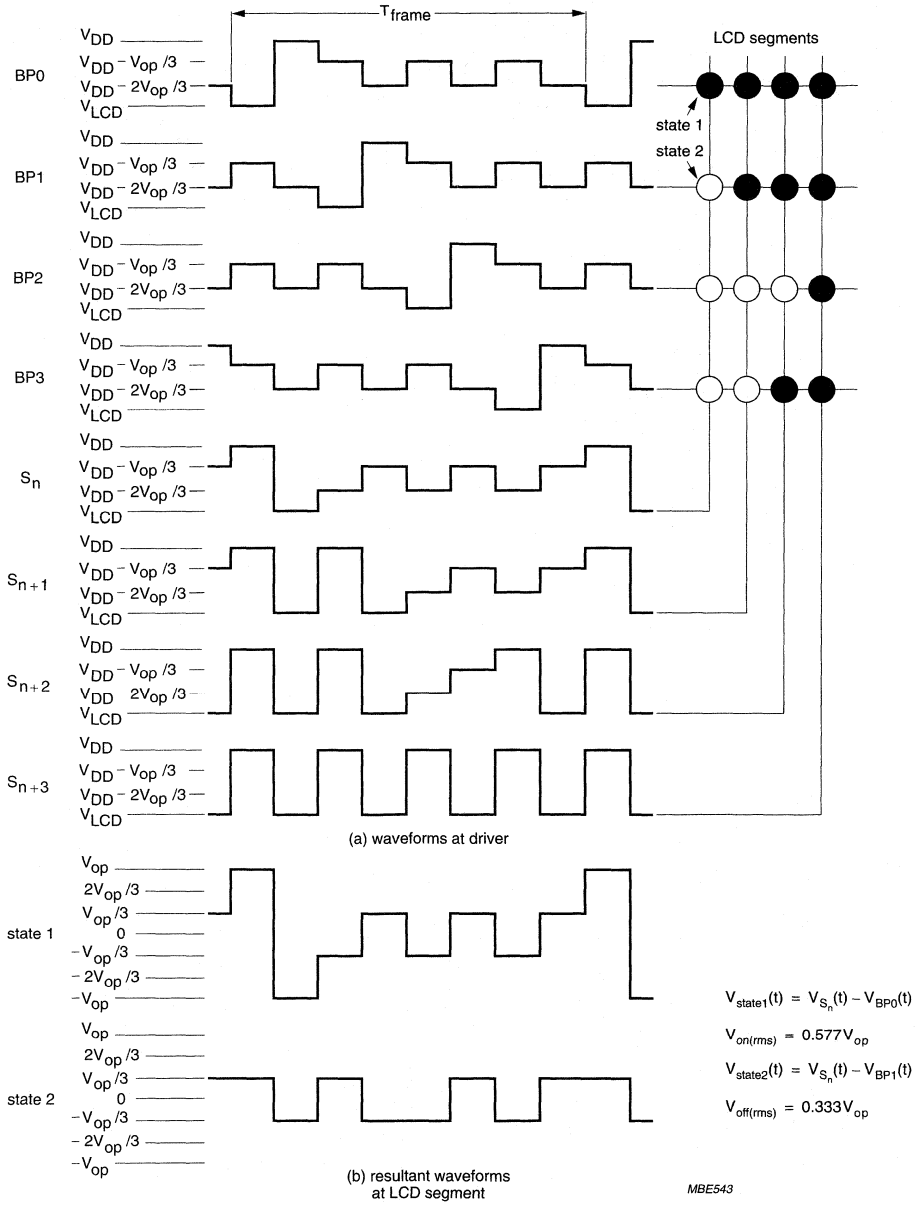


Fig.9 Waveforms for the 1 : 4 multiplex drive mode ($V_{op} = V_{DD} - V_{LCD}$).

6.5 Oscillator

6.5.1 INTERNAL CLOCK

The internal logic and the LCD drive signals of the PCF8576C are timed either by the built-in oscillator or from an external clock. When the internal oscillator is used, OSC (pin 6) should be connected to V_{SS} (pin 11). In this event, the output from CLK (pin 4) provides the clock signal for cascaded PCF8566s or PCF8576Cs in the system.

Note that the PCF8576C is backwards compatible with the PCF8576. Where resistor R_{osc} to V_{SS} is present, the internal oscillator is selected.

6.5.2 EXTERNAL CLOCK

The condition for external clock is made by tying OSC (pin 6) to V_{DD}; CLK (pin 4) then becomes the external clock input.

The clock frequency (f_{clk}) determines the LCD frame frequency and the maximum rate for data reception from the I^2C-bus. To allow I^2C-bus transmissions at their maximum data rate of 100 kHz, f_{clk} should be chosen to be above 125 kHz.

A clock signal must always be supplied to the device; removing the clock may freeze the LCD in a DC state.

6.6 Timing

The timing of the PCF8576C organizes the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. In cascaded applications, the synchronization signal $\overline{SYNC}$ maintains the correct timing relationship between the PCF8576Cs in the system. The timing also generates the LCD frame frequency which it derives as an integer multiple of the clock frequency (see Table 3). The frame frequency is set by the MODE SET commands when internal clock is used, or by the frequency applied to pin 4 when external clock is used.

The ratio between the clock frequency and the LCD frame frequency depends on the mode in which the device is operating. In the power-saving mode the reduction ratio is six times smaller; this allows the clock frequency to be reduced by a factor of six. The reduced clock frequency results in a significant reduction in power dissipation. The lower clock frequency has the disadvantage of increasing the response time when large amounts of display data are transmitted on the I^2C-bus.

When a device is unable to digest a display data byte before the next one arrives, it holds the SCL line LOW until the first display data byte is stored. This slows down the transmission rate of the I^2C-bus but no data loss occurs.

6.7 Display latch

The display latch holds the display data while the corresponding multiplex signals are generated. There is a one-to-one relationship between the data in the display latch, the LCD segment outputs and one column of the display RAM.

6.8 Shift register

The shift register serves to transfer display information from the display RAM to the display latch while previous data is displayed.

6.9 Segment outputs

The LCD drive section includes 40 segment outputs S0 to S39 (pins 17 to 56) which should be connected directly to the LCD. The segment output signals are generated in accordance with the multiplexed backplane signals and with data resident in the display latch. When less than 40 segment outputs are required the unused segment outputs should be left open-circuit.

6.10 Backplane outputs

The LCD drive section includes four backplane outputs BP0 to BP3 which should be connected directly to the LCD. The backplane output signals are generated in accordance with the selected LCD drive mode. If less than four backplane outputs are required the unused outputs can be left open-circuit. In the 1 : 3 multiplex drive mode BP3 carries the same signal as BP1, therefore these two adjacent outputs can be tied together to give enhanced drive capabilities. In the 1 : 2 multiplex drive mode BP0 and BP2, BP1 and BP3 respectively carry the same signals and may also be paired to increase the drive capabilities. In the static drive mode the same signal is carried by all four backplane outputs and they can be connected in parallel for very high drive requirements.

6.11 Display RAM

The display RAM is a static 40 × 4-bit RAM which stores LCD data. A logic 1 in the RAM bit-map indicates the on state of the corresponding LCD segment; similarly, a logic 0 indicates the off state. There is a one-to-one correspondence between the RAM addresses and the segment outputs, and between the individual bits of a RAM word and the backplane outputs. The first RAM column corresponds to the 40 segments operated with respect to backplane BP0 (see Fig.10). In multiplexed LCD applications the segment data of the second, third and fourth column of the display RAM are time-multiplexed with BP1, BP2 and BP3 respectively.

When display data is transmitted to the PCF8576C the display bytes received are stored in the display RAM in accordance with the selected LCD drive mode.
To illustrate the filling order, an example of a 7-segment numeric display showing all drive modes is given in Fig.11; the RAM filling organization depicted applies equally to other LCD types.

With reference to Fig.11, in the static drive mode the eight transmitted data bits are placed in bit 0 of eight successive display RAM addresses.

In the 1 : 2 multiplex drive mode the eight transmitted data bits are placed in bits 0 and 1 of four successive display RAM addresses. In the 1 : 3 multiplex drive mode these bits are placed in bits 0, 1 and 2 of three successive addresses, with bit 2 of the third address left unchanged. This last bit may, if necessary, be controlled by an additional transfer to this address but care should be taken to avoid overriding adjacent data because full bytes are always transmitted. In the 1 : 4 multiplex drive mode the eight transmitted data bits are placed in bits 0, 1, 2 and 3 of two successive display RAM addresses.

Table 3 LCD frame frequencies

PCF8576C MODE	FRAME FREQUENCY	NOMINAL FRAME FREQUENCY (Hz)
Normal mode	$\frac{f_{clk}}{2880}$	64
Power-saving mode	$\frac{f_{clk}}{480}$	64

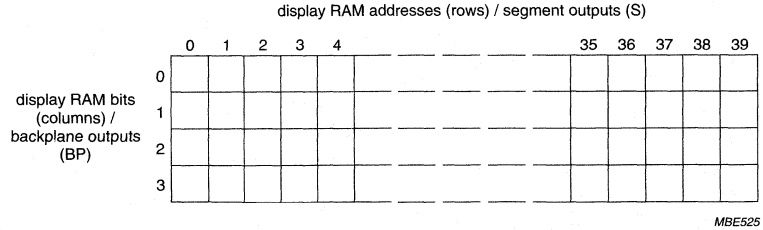


Fig.10 Display RAM bit-map showing direct relationship between display RAM addresses and segment outputs, and between bits in a RAM word and backplane outputs.

6.12 Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the data pointer by the LOAD DATA POINTER command. Following this, an arriving data byte is stored starting at the display RAM address indicated by the data pointer thereby observing the filling order shown in Fig.11. The data pointer is automatically incremented in accordance with the chosen LCD configuration. That is, after each byte is stored, the contents of the data pointer are incremented by eight (static drive mode), by four (1 : 2 multiplex drive mode) or by two (1 : 4 multiplex drive mode).

6.13 Subaddress counter

The storage of display data is conditioned by the contents of the subaddress counter. Storage is allowed to take place only when the contents of the subaddress counter agree with the hardware subaddress applied to A0, A1 and A2. The subaddress counter value is defined by the DEVICE SELECT command. If the contents of the subaddress counter and the hardware subaddress do not agree then data storage is inhibited but the data pointer is incremented as if data storage had taken place. The subaddress counter is also incremented when the data pointer overflows.

The storage arrangements described lead to extremely efficient data loading in cascaded applications. When a series of display bytes are sent to the display RAM, automatic wrap-over to the next PCF8576C occurs when the last RAM address is exceeded. Subaddressing across device boundaries is successful even if the change to the next device in the cascade occurs within a transmitted character (such as during the 14th display data byte transmitted in 1 : 3 multiplex mode).

6.14 Output bank selector

This selects one of the four bits per display RAM address for transfer to the display latch. The actual bit chosen depends on the particular LCD drive mode in operation and on the instant in the multiplex sequence. In 1 : 4 multiplex, all RAM addresses of bit 0 are the first to be selected, these are followed by the contents of bit 1, bit 2 and then bit 3. Similarly in 1 : 3 multiplex, bits 0, 1 and 2 are selected sequentially. In 1 : 2 multiplex, bits 0 and 1 are selected and, in the static mode, bit 0 is selected.

The PCF8576C includes a RAM bank switching feature in the static and 1 : 2 multiplex drive modes. In the static drive mode, the BANK SELECT command may request the contents of bit 2 to be selected for display instead of bit 0 contents. In the 1 : 2 drive mode, the contents of bits 2 and 3 may be selected instead of bits 0 and 1. This gives the provision for preparing display information in an alternative bank and to be able to switch to it once it is assembled.

6.15 Input bank selector

The input bank selector loads display data into the display RAM in accordance with the selected LCD drive configuration. Display data can be loaded in bit 2 in static drive mode or in bits 2 and 3 in 1 : 2 drive mode by using the BANK SELECT command. The input bank selector functions independent of the output bank selector.

6.16 Blinker

The display blinking capabilities of the PCF8576C are very versatile. The whole display can be blinked at frequencies selected by the BLINK command. The blinking frequencies are integer multiples of the clock frequency; the ratios between the clock and blinking frequencies depend on the mode in which the device is operating, as shown in Table 4.

An additional feature is for an arbitrary selection of LCD segments to be blinked. This applies to the static and 1 : 2 LCD drive modes and can be implemented without any communication overheads.

By means of the output bank selector, the displayed RAM banks are exchanged with alternate RAM banks at the blinking frequency. This mode can also be specified by the BLINK command.

In the 1 : 3 and 1 : 4 multiplex modes, where no alternate RAM bank is available, groups of LCD segments can be blinked by selectively changing the display RAM data at fixed time intervals.

If the entire display is to be blinked at a frequency other than the nominal blinking frequency, this can be effectively performed by resetting and setting the display enable bit E at the required rate using the MODE SET command.

Table 4 Blinking frequencies

BLINKING MODE	NORMAL OPERATING MODE RATIO	POWER-SAVING MODE RATIO	NOMINAL BLINKING FREQUENCY
Off	–	–	blinking off
2 Hz	$\frac{f_{clk}}{92160}$	$\frac{f_{clk}}{15360}$	2 Hz
1 Hz	$\frac{f_{clk}}{184320}$	$\frac{f_{clk}}{30720}$	1 Hz
0.5 Hz	$\frac{f_{clk}}{368640}$	$\frac{f_{clk}}{61440}$	0.5 Hz

x = data bit unchanged.

Fig.11 Relationships between LCD layout, drive mode, display RAM filling order and display data transmitted over the I²C-bus.

7 CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

7.1 Bit transfer (see Fig.12)

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

7.2 Start and stop conditions (see Fig.13)

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P).

7.3 System configuration (see Fig.14)

A device generating a message is a 'transmitter', a device receiving a message is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves'.

7.4 Acknowledge (see Fig.15)

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

7.5 PCF8576C I²C-bus controller

The PCF8576C acts as an I²C-bus slave receiver. It does not initiate I²C-bus transfers or transmit data to an I²C-bus master receiver. The only data output from the PCF8576C are the acknowledge signals of the selected devices. Device selection depends on the I²C-bus slave address, on the transferred command data and on the hardware subaddress.

In single device application, the hardware subaddress inputs A0, A1 and A2 are normally tied to V_{SS} which defines the hardware subaddress 0. In multiple device applications A0, A1 and A2 are tied to V_{SS} or V_{DD} in accordance with a binary coding scheme such that no two devices with a common I²C-bus slave address have the same hardware subaddress.

In the power-saving mode it is possible that the PCF8576C is not able to keep up with the highest transmission rates when large amounts of display data are transmitted. If this situation occurs, the PCF8576C forces the SCL line LOW until its internal operations are completed. This is known as the 'clock synchronization feature' of the I²C-bus and serves to slow down fast transmitters. Data loss does not occur.

7.6 Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

7.7 I²C-bus protocol

Two I²C-bus slave addresses (0111000 and 0111001) are reserved for the PCF8576C. The least significant bit of the slave address that a PCF8576C will respond to is defined by the level tied at its input SA0 (pin 10). Therefore, two types of PCF8576C can be distinguished on the same I²C-bus which allows:

1. Up to 16 PCF8576Cs on the same I²C-bus for very large LCD applications.
2. The use of two types of LCD multiplex on the same I²C-bus.

The I²C-bus protocol is shown in Fig.16. The sequence is initiated with a START condition (S) from the I²C-bus master which is followed by one of the two PCF8675C slave addresses available. All PCF8576Cs with the corresponding SA0 level acknowledge in parallel with the slave address but all PCF8576Cs with the alternative SA0 level ignore the whole I²C-bus transfer.

After acknowledgement, one or more command bytes (m) follow which define the status of the addressed PCF8576Cs.

The last command byte is tagged with a cleared most significant bit, the continuation bit C. The command bytes are also acknowledged by all addressed PCF8576Cs on the bus.

After the last command byte, a series of display data bytes (n) may follow. These display bytes are stored in the display RAM at the address specified by the data pointer and the subaddress counter. Both data pointer and subaddress counter are automatically updated and the data is directed to the intended PCF8576C device. The acknowledgement after each byte is made only by the (A0, A1 and A2) addressed PCF8576C. After the last display byte, the I²C-bus master issues a STOP condition (P).

7.8 Command decoder

The command decoder identifies command bytes that arrive on the I²C-bus. All available commands carry a continuation bit C in their most significant bit position (Fig.17). When this bit is set, it indicates that the next byte of the transfer to arrive will also represent a command. If this bit is reset, it indicates the last command byte of the transfer. Further bytes will be regarded as display data.

The five commands available to the PCF8576C are defined in Table 5.

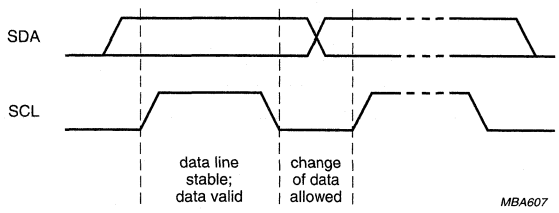


Fig.12 Bit transfer.

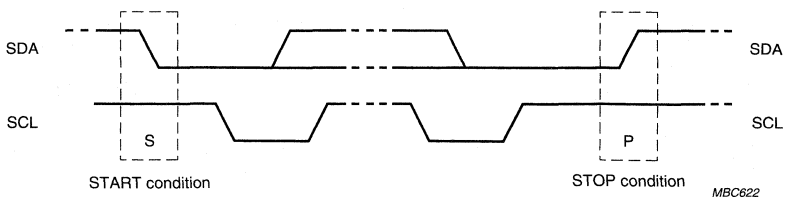


Fig.13 Definition of START and STOP conditions.

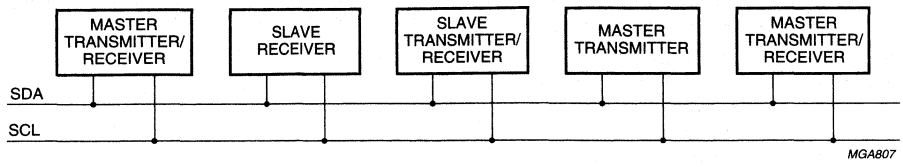


Fig.14 System configuration.

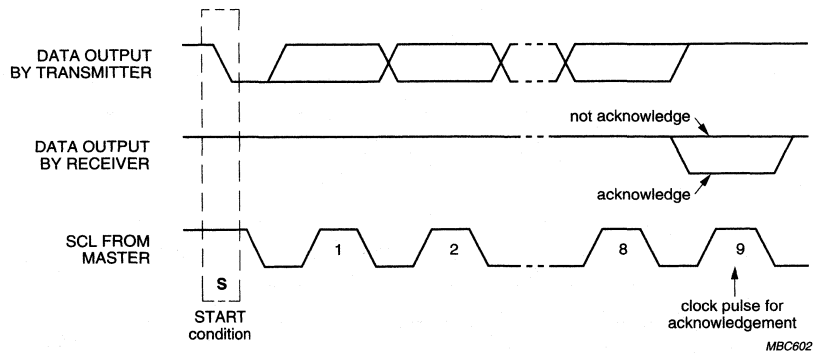


Fig.15 Acknowledgement on the I²C-bus.

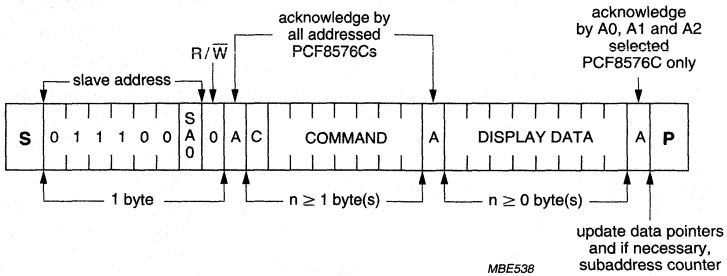
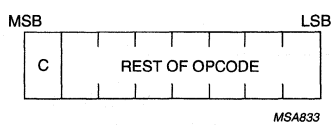


Fig.16 I²C-bus protocol.



C = 0; last command.
C = 1; commands continue.

Fig.17 General format of command byte.

Table 5 Definition of PCF8576C commands

COMMAND	OPCODE								OPTIONS	DESCRIPTION
MODE SET	C	1	0	LP	E	B	M1	M0	Table 6	Defines LCD drive mode.
									Table 7	Defines LCD bias configuration.
									Table 8	Defines display status. The possibility to disable the display allows implementation of blinking under external control.
									Table 9	Defines power dissipation mode.
LOAD DATA POINTER	C	0	P5	P4	P3	P2	P1	P0	Table 10	Six bits of immediate data, bits P5 to P0, are transferred to the data pointer to define one of forty display RAM addresses.
DEVICE SELECT	C	1	1	0	0	A2	A1	A0	Table 11	Three bits of immediate data, bits A0 to A3, are transferred to the subaddress counter to define one of eight hardware subaddresses.
BANK SELECT	C	1	1	1	1	0	I	O	Table 12	Defines input bank selection (storage of arriving display data).
									Table 13	Defines output bank selection (retrieval of LCD display data). The BANK SELECT command has no effect in 1 : 3 and 1 : 4 multiplex drive modes.
BLINK	C	1	1	1	0	A	BF1	BF0	Table 14	Defines the blinking frequency.
									Table 15	Selects the blinking mode; normal operation with frequency set by BF1, BF0 or blinking by alternation of display RAM banks. Alternation blinking does not apply in 1 : 3 and 1 : 4 multiplex drive modes.

Table 6 Mode set option 1

LCD DRIVE MODE		BITS	
DRIVE MODE	BACKPLANE	M1	M0
Static	1 BP	0	1
1 : 2	MUX (2 BP)	1	0
1 : 3	MUX (3 BP)	1	1
1 : 4	MUX (4 BP)	0	0

Table 7 Mode set option 2

LCD BIAS	BIT B
1/3 bias	0
1/2 bias	1

Table 8 Mode set option 3

DISPLAY STATUS	BIT E
Disabled (blank)	0
Enabled	1

Table 9 Mode set option 4

MODE	BIT LP
Normal mode	0
Power-saving mode	1

Table 10 Load data pointer option 1

DESCRIPTION	BITS					
6 bit binary value of 0 to 39	P5	P4	P3	P2	P1	P0

Table 11 Device select option 1

DESCRIPTION	BITS		
3 bit binary value of 0 to 7	A0	A1	A2

Table 12 Bank select option 1

STATIC	1 : 2 MUX	BIT I
RAM bit 0	RAM bits 0 and 1	0
RAM bit 2	RAM bits 2 and 3	1

Table 13 Bank select option 2

STATIC	1 : 2 MUX	BIT O
RAM bit 0	RAM bits 0 and 1	0
RAM bit 2	RAM bits 2 and 3	1

Table 14 Blink option 1

BLINK FREQUENCY	BITS	
	BF1	BF0
Off	0	0
2 Hz	0	1
1 Hz	1	0
0.5 Hz	1	1

Table 15 Blink option 2

BLINK MODE	BIT A
Normal blinking	0
Alternation blinking	1

7.9 Display controller

The display controller executes the commands identified by the command decoder. It contains the status registers of the PCF8576C and co-ordinates their effects.
The controller is also responsible for loading display data into the display RAM as required by the filling order.

7.10 Cascaded operation

In large display configurations, up to 16 PCF8576Cs can be distinguished on the same I^2C-bus by using the 3-bit hardware subaddress (A0, A1 and A2) and the programmable I^2C-bus slave address (SA0). When cascaded PCF8576Cs are synchronized so that they can share the backplane signals from one of the devices in the cascade. Such an arrangement is cost-effective in large LCD applications since the backplane outputs of only one device need to be through-plated to the backplane electrodes of the display. The other PCF8576Cs of the cascade contribute additional segment outputs but their backplane outputs are left open-circuit (Fig.18).

The $\overline{SYNC}$ line is provided to maintain the correct synchronization between all cascaded PCF8576Cs. This synchronization is guaranteed after the power-on reset. The only time that $\overline{SYNC}$ is likely to be needed is if synchronization is accidentally lost (e.g. by noise in adverse electrical environments; or by the definition of a multiplex mode when PCF8576Cs with differing SA0 levels are cascaded). $\overline{SYNC}$ is organized as an input/output pin; the output selection being realized as an open-drain driver with an internal pull-up resistor.
A PCF8576C asserts the $\overline{SYNC}$ line at the onset of its last active backplane signal and monitors the $\overline{SYNC}$ line at all other times. Should synchronization in the cascade be lost, it will be restored by the first PCF8675C to assert $\overline{SYNC}$. The timing relationship between the backplane waveforms and the $\overline{SYNC}$ signal for the various drive modes of the PCF8576C are shown in Fig.19.

For single plane wiring of packaged PCF8576Cs and chip-on-glass cascading, see Chapter "Application information".

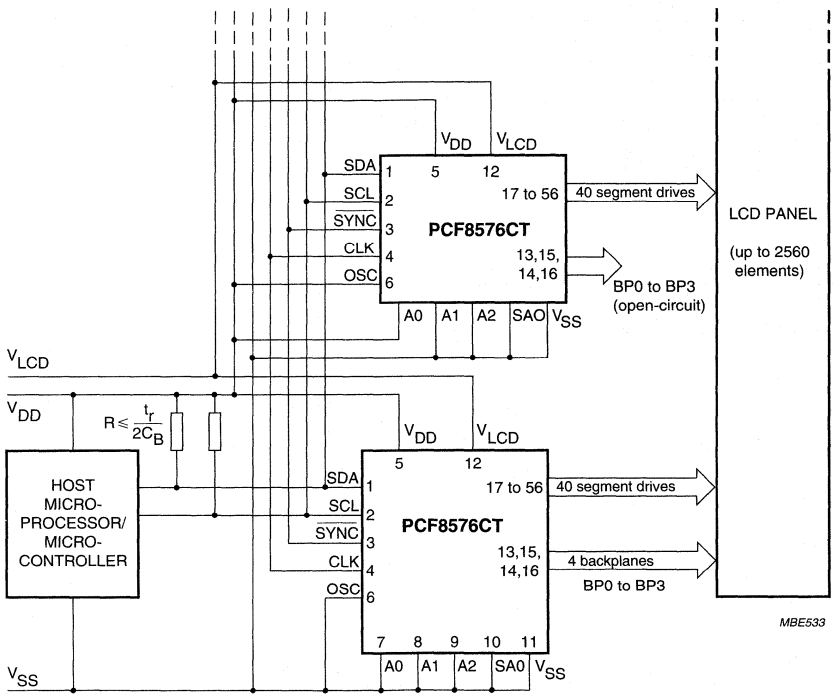
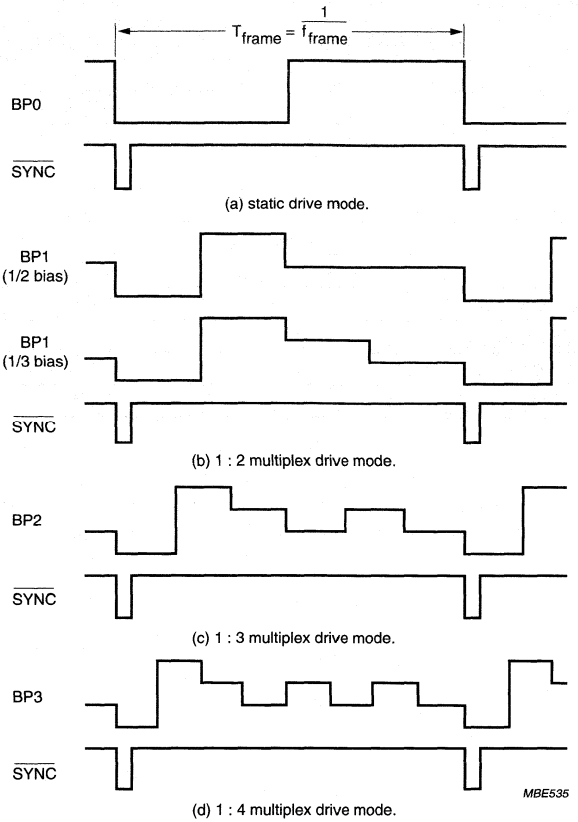


Fig.18 Cascaded PCF8576C configuration.



Excessive capacitive coupling between SCL or CLK and $\overline{SYNC}$ may cause erroneous synchronization. If this proves to be a problem, the capacitance of the $\overline{SYNC}$ line should be increased (e.g. by an external capacitor between $\overline{SYNC}$ and V_{DD}). Degradation of the positive edge of the $\overline{SYNC}$ pulse may be countered by an external pull-up resistor.

(a) static drive mode.

(b) 1 : 2 multiplex drive mode.

(c) 1 : 3 multiplex drive mode.

(d) 1 : 4 multiplex drive mode.

Fig.19 Synchronization of the cascade for the various PCF8576C drive modes.

8 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.5	+8.0	V
V_{LCD}	LCD supply voltage	V_{DD} − 8.0	V_{DD}	V
V_{I1}	input voltage CLK, $\overline{SYNC}$, SA0, OSC, A0 to A2	V_{SS} − 0.5	V_{DD} + 0.5	V
V_{I2}	input voltage SDA, SCL	V_{SS} − 0.5	+8.0	V
V_O	output voltage S0 to S39, BP0 to BP3	V_{LCD} − 0.5	V_{DD} + 0.5	V
I_I	DC input current	−20	+20	mA
I_O	DC output current	−25	+25	mA
I_{DD}, I_{SS}, I_{LCD}	V_{DD}, V_{SS} or V_{LCD} current	−50	+50	mA
P_{tot}	total power dissipation	−	400	mW
P_O	power dissipation per output	−	100	mW
T_{stg}	storage temperature	−65	+150	°C

9 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see *"Handling MOS Devices"*).

10 DC CHARACTERISTICS

V_{DD} = 2 to 6 V; V_{SS} = 0 V; V_{LCD} = V_{DD} − 2 V to V_{DD} − 6 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage		2	–	6	V
V_{LCD}	LCD supply voltage	note 1	V_{DD} − 6	–	V_{DD} − 2	V
I_{DD}	supply current	note 2				
	normal mode	f_{clk} = 200 kHz	–	–	120	μA
	power-saving mode	f_{clk} = 35 kHz; V_{DD} = 3.5 V; V_{LCD} = 0 V; A0, A1 and A2 tied to V_{SS}	–	–	60	μA
Logic						
V_{IL}	LOW-level input voltage SDA, SCL, CLK, $\overline{SYNC}$, SA0, OSC, A0 to A2		V_{SS}	–	0.3V_{DD}	V
V_{IH1}	HIGH-level input voltage CLK, $\overline{SYNC}$, SA0, OSC, A0 to A2		0.7V_{DD}	–	V_{DD}	V
V_{IH2}	HIGH-level input voltage SDA, SCL		0.7V_{DD}	–	6.0	V
V_{OL}	LOW-level output voltage	I_{OL} = 0 mA	–	–	0.05	V
V_{OH}	HIGH-level output voltage	I_{OH} = 0 mA	V_{DD} − 0.05	–	–	V
I_{OL1}	LOW-level output current CLK, $\overline{SYNC}$	V_{OL} = 1 V; V_{DD} = 5 V	1	–	–	mA
I_{OH1}	HIGH-level output current CLK	V_{OH} = 4 V; V_{DD} = 5 V	−1	–	–	mA
I_{OL2}	LOW-level output current SDA, SCL	V_{OL} = 0.4 V; V_{DD} = 5 V	3	–	–	mA
I_{L1}	leakage current SA0, A0 to A2, CLK, SDA and SCL	V_I = V_{DD} or V_{SS}	−1	–	+1	μA
I_{L2}	leakage current OSC	V_I = V_{DD}	−1	–	+1	μA
I_{pd}	A0, A1, A2 and OSC pull-down current	V_I = 1 V; V_{DD} = 5 V	15	50	150	μA
$R_{\overline{SYNC}}$	pull-up resistor ($\overline{SYNC}$)		20	50	150	kΩ
V_{POR}	power-on reset voltage level	note 3	–	1.0	1.6	V
t_{SW}	tolerable spike width on bus		–	–	100	ns
C_I	input capacitance	note 4	–	–	7	pF
LCD outputs						
V_{BP}	DC voltage component BP0 to BP3	C_{BP} = 35 nF	−20	–	+20	mV
V_S	DC voltage component S0 to S39	C_S = 5 nF	−20	–	+20	mV
R_{BP}	output resistance BP0 to BP3	note 5; V_{LCD} = V_{DD} − 5 V	–	–	5	kΩ
R_S	output resistance S0 to S39	note 5; V_{LCD} = V_{DD} − 5 V	–	–	7.5	kΩ

Notes

1. $V_{LCD} \leq V_{DD} - 3$ V for ⅓bias.
2. LCD outputs are open-circuit; inputs at V_{SS} or V_{DD}; external clock with 50% duty factor; I^2C-bus inactive.
3. Resets all logic when $V_{DD} < V_{POR}$.
4. Periodically sampled, not 100% tested.
5. Outputs measured one at a time.

11 AC CHARACTERISTICS

V_{DD} = 2 to 6 V; V_{SS} = 0 V; V_{LCD} = V_{DD} − 2 V to V_{DD} − 6 V; T_{amb} = −40 to + 85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{clk}	oscillator frequency					
	normal mode	V_{DD} = 5 V; note 1	125	200	315	kHz
	power-saving mode	V_{DD} = 3.5 V	21	31	48	kHz
t_{clkH}	CLK HIGH time		1	–	–	µs
t_{clkL}	CLK LOW time		1	–	–	µs
t_{PSYNC}	$\overline{SYNC}$ propagation delay time		–	–	400	ns
$t_{\overline{SYNC}L}$	$\overline{SYNC}$ LOW time		1	–	–	µs
t_{PLCD}	driver delays with test loads	V_{LCD} = V_{DD} − 5 V	–	–	30	µs
Timing characteristics: I²C-bus; note 2						
t_{BUF}	bus free time		4.7	–	–	µs
$t_{HD;STA}$	START condition hold time		4.0	–	–	µs
$t_{SU;STA}$	set-up time for a repeated START condition		4.7	–	–	µs
t_{LOW}	SCL LOW time		4.7	–	–	µs
t_{HIGH}	SCL HIGH time		4.0	–	–	µs
t_r	SCL and SDA rise time		–	–	1	µs
t_f	SCL and SDA fall time		–	–	0.3	µs
C_B	capacitive bus line load		–	–	400	pF
$t_{SU;DAT}$	data set-up time		250	–	–	ns
$t_{HD;DAT}$	data hold time		0	–	–	ns
$t_{SU;STO}$	set-up time for STOP condition		4.0	–	–	µs

Notes

1. At f_{clk} < 125 kHz, I²C-bus maximum transmission speed is derated.
2. All timing values are valid within the operating supply voltage and ambient temperature range and are referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

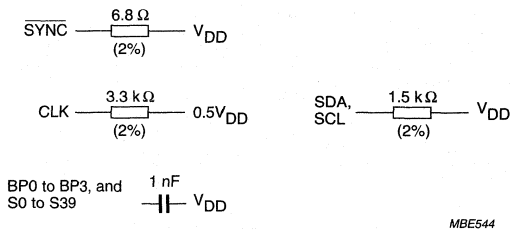


Fig.20 Test loads.

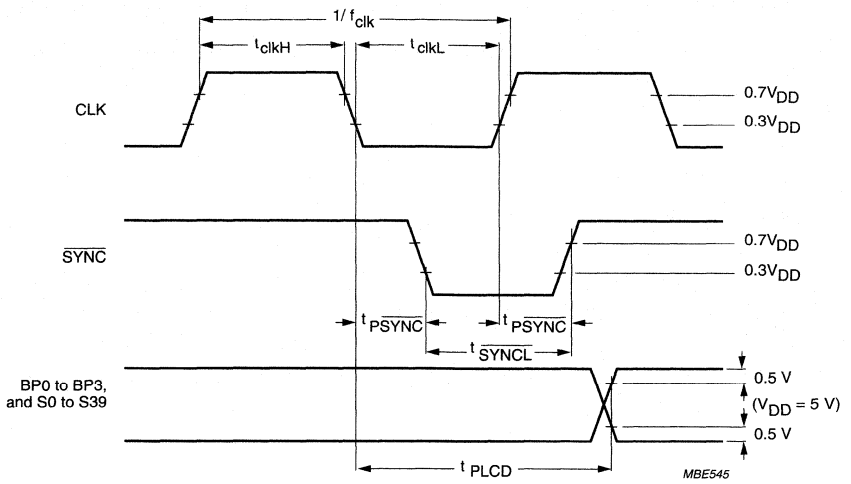


Fig.21 Driver timing waveforms.

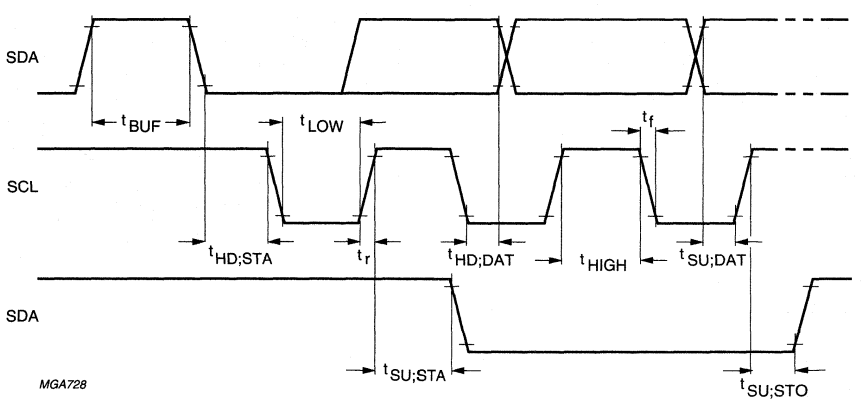
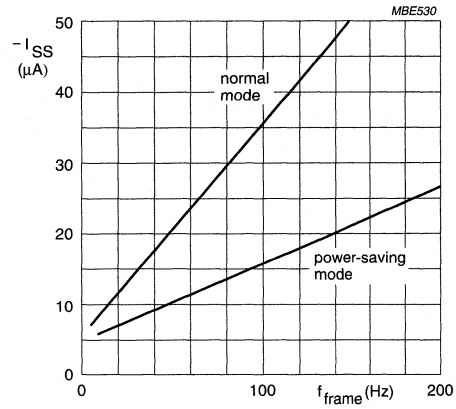


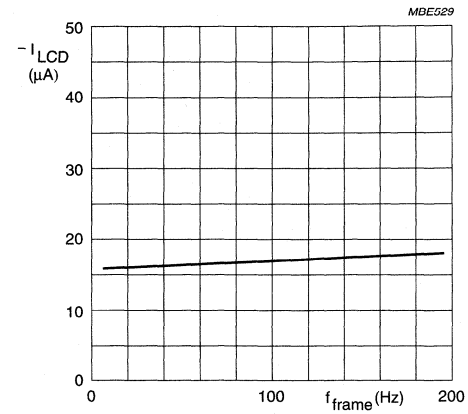
Fig.22 I²C-bus timing waveforms.

11.1 Typical supply current characteristics



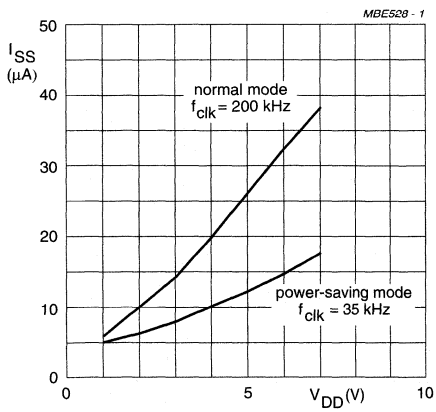
V_{DD} = 5 V; V_{LCD} = 0 V; T_{amb} = 25 °C.

Fig.23 $-I_{SS}$ as a function of f_{frame}.



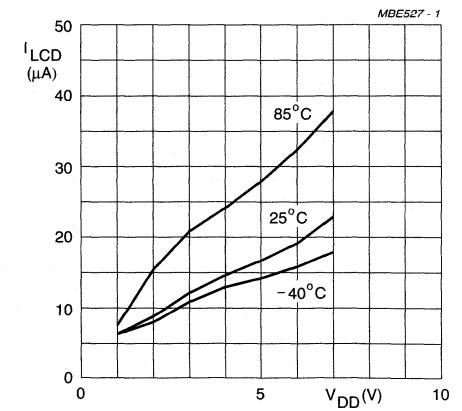
V_{DD} = 5 V; V_{LCD} = 0 V; T_{amb} = 25 °C.

Fig.24 $-I_{LCD}$ as a function of f_{frame}.



V_{LCD} = 0 V; external clock; T_{amb} = 25 °C.

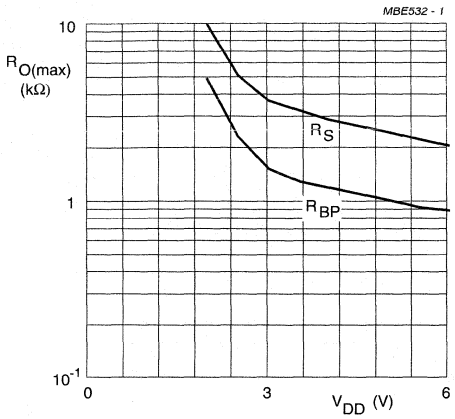
Fig.25 I_{SS} as a function of V_{DD}.



V_{LCD} = 0 V; external clock; f_{clk} = nominal frequency.

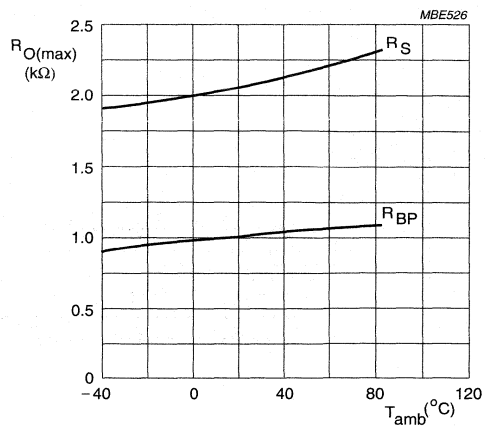
Fig.26 I_{LCD} as a function of V_{DD}.

11.2 Typical characteristics of LC D outputs



V_{LCD} = 0 V; T_{amb} = 25 °C.

Fig.27 $R_{O(max)}$ as a function of V_{DD}.



V_{DD} = 5 V; V_{LCD} = 0 V.

Fig.28 $R_{O(max)}$ as a function of T_{amb}.

12 APPLICATION INFORMATION

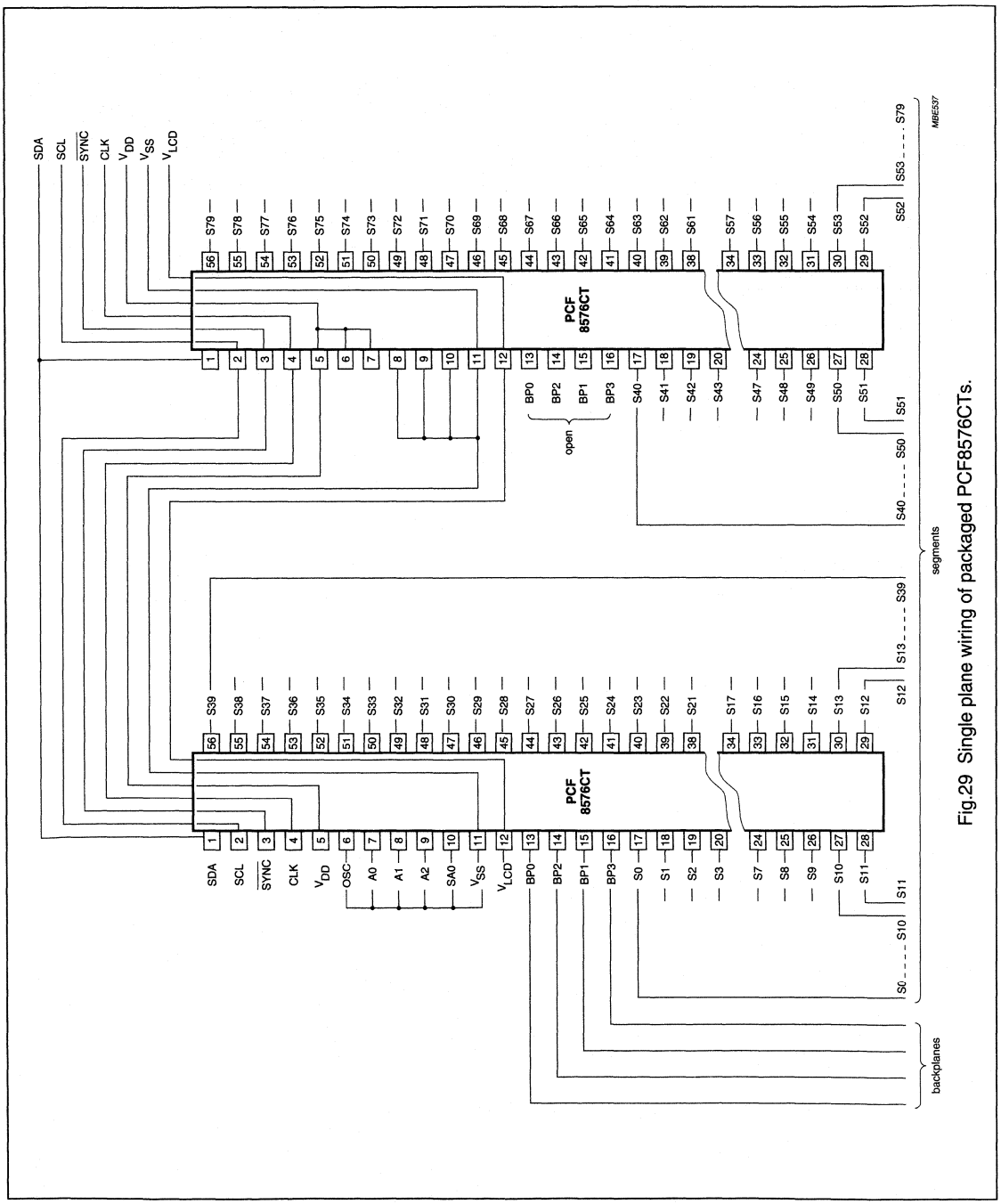


Fig.29 Single plane wiring of packaged PCF8576CTs.

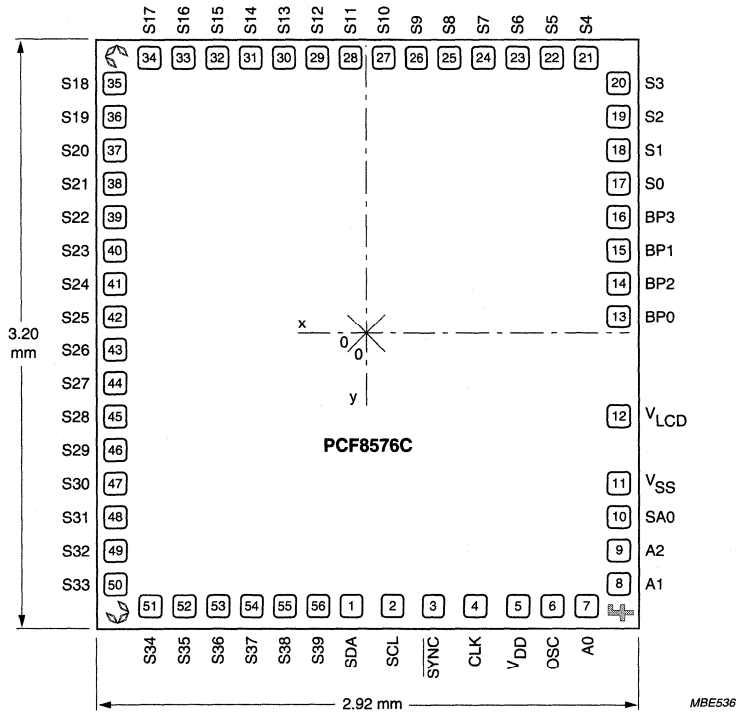
12.1 Chip-on-glass cascadability in single plane

In chip-on-glass technology, where driver devices are bonded directly onto glass of the LCD, it is important that the devices may be cascaded without the crossing of conductors, but the paths of conductors can be continued on the glass under the chip. All of this is facilitated by the PCF8576C bonding pad layout (Fig.30). Pads needing bus interconnection between all PCF8576Cs of the cascade are V_{DD}, V_{SS}, V_{LCD}, CLK, SCL, SDA and $\overline{SYNC}$. These lines may be led to the corresponding pads of the next PCF8576C through the wide opening between V_{LCD} pad and the backplane output pads.

The only bus line that does not require a second opening to lead through to the next PCF8576C is V_{LCD}, being the cascade centre. The placing of V_{LCD} adjacent to V_{SS} allows the two supplies to be tied together.

When an external clocking source is to be used, OSC of all devices should be tied to V_{DD}. The pads OSC, A0, A1, A2 and SA0 have been placed between V_{SS} and V_{DD} to facilitate wiring of oscillator, hardware subaddress and slave address.

13 BONDING PAD LOCATIONS



Chip dimensions: approximately 2.92 × 3.20 mm.
Pad area: 0.0121 mm².
Bonding pad dimensions: 110 × 110 µm.

Fig.30 Bonding pad locations.

Table 16 Bonding pad locations (dimensions in μm)
All x/y coordinates are referenced to the centre of the chip (see Fig.30).

SYMBOL	PAD	x	y
SDA	1	−74	−1380
SCL	2	148	−1380
$\overline{SYNC}$	3	355	−1380
CLK	4	534	−1380
V_{DD}	5	742	−1380
OSC	6	913	−1380
A0	7	1087	−1380
A1	8	1290	−1284
A2	9	1290	−1116
SA0	10	1290	−945
V_{SS}	11	1290	−751
V_{LCD}	12	1290	−485
BP0	13	1290	125
BP2	14	1290	285
BP1	15	1290	458
BP3	16	1290	618
S0	17	1290	791
S1	18	1290	951
S2	19	1290	1124
S3	20	1290	1284
S4	21	1074	1380
S5	22	914	1380
S6	23	741	1380
S7	24	581	1380
S8	25	408	1380
S9	26	248	1380
S10	27	75	1380
S11	28	−85	1380
S12	29	−258	1380
S13	30	−418	1380
S14	31	−591	1380
S15	32	−751	1380
S16	33	−924	1380
S17	34	−1084	1380
S18	35	−1290	1243
S19	36	−1290	1083
S20	37	−1290	910
S21	38	−1290	750
S22	39	−1290	577
S23	40	−1290	417
S24	41	−1290	244
S25	42	−1290	84
S26	43	−1290	−89
S27	44	−1290	−249
S28	45	−1290	−422
S29	46	−1290	−582
S30	47	−1290	−755
S31	48	−1290	−915
S32	49	−1290	−1088
S33	50	−1290	−1248
S34	51	−1083	−1380
S35	52	−923	−1380
S36	53	−750	−1380
S37	54	−590	−1380
S38	55	−417	−1380
S39	56	−257	−1380
Alignment marks			
C1	−	−1290	1385
C2	−	−1295	−1385
F	−	1305	−1405

LCD direct/duplex driver with I²C-bus interface

PCF8577C

CONTENTS

LCD direct/duplex driver with I²C-bus interface

PCF8577C

1 FEATURES

- Direct/duplex drive modes with up to 32/64 LCD-segment drive capability per device
- Operating supply voltage: 2.5 to 6 V
- Low power consumption
- I²C-bus interface
- Optimized pinning for single plane wiring
- Single-pin built-in oscillator
- Auto-incremented loading across device subaddress boundaries
- Display memory switching in direct drive mode
- May be used as I²C-bus output expander
- System expansion up to 256 segments
- Power-on reset blanks display
- I²C-bus address: 0111 0100.

2 GENERAL DESCRIPTION

The PCF8577C is a single chip, silicon gate CMOS circuit. It is designed to drive liquid crystal displays with up to 32 segments directly, or 64 segments in a duplex configuration.

The two-line I²C-bus interface substantially reduces wiring overheads in remote display applications. I²C-bus traffic is minimized in multiple IC applications by automatic address incrementing, hardware subaddressing and display memory switching (direct drive mode). To allow partial V_{DD} shutdown the ESD protection system of the SCL and SDA pins does not use a diode connected to V_{DD}.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8577CP	DIP40	plastic dual in-line package; 40 leads (600 mil)	SOT129-1
PCF8577CT	VSO40	plastic very small outline package; 40 leads	SOT158A
PCF8577CT	–	VS040 in blister tape	–
PCF8577CU/10	–	chip on film-frame-carrier (FFC)	–

4 BLOCK DIAGRAM

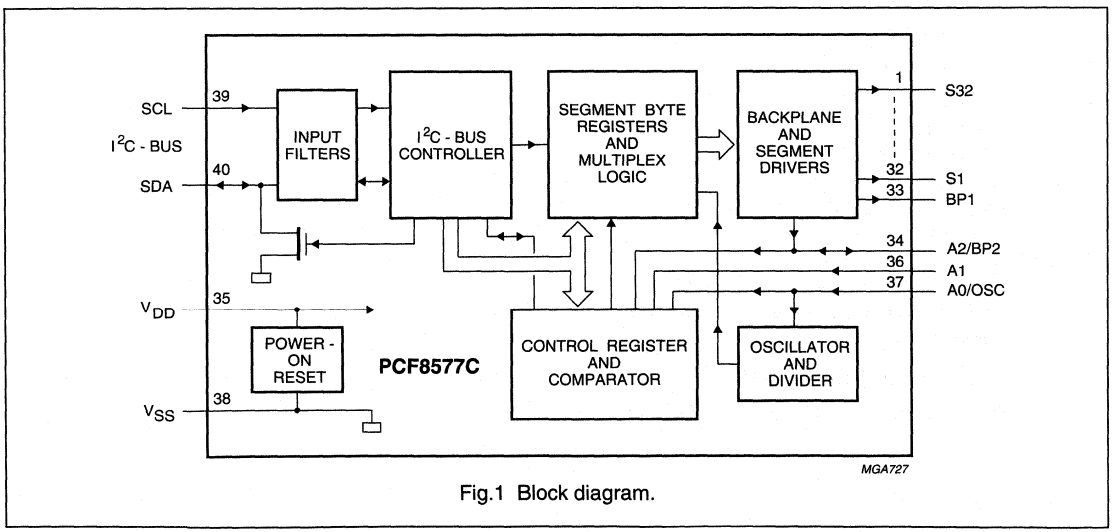


Fig.1 Block diagram.

5 PINNING

SYMBOL	PIN	DESCRIPTION
S32 to S1	1 to 32	segments outputs
BP1	33	cascade sync input/backplane output
A2/BP2	34	hardware address line and cascade sync input/backplane output
V_{DD}	35	positive supply voltage
A1	36	hardware address line input
A0/OSC	37	hardware address line and oscillator pin input
V_{SS}	38	negative supply voltage
SCL	39	I²C-bus clock line input
SDA	40	I²C-bus data line input/output

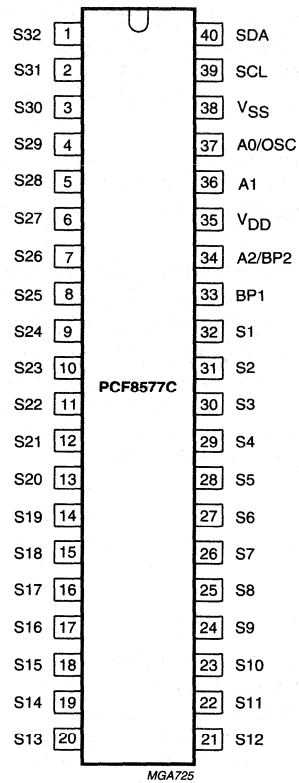


Fig.2 Pin configuration.

6 FUNCTIONAL DESCRIPTION

6.1 Hardware subaddress A0, A1, A2

The hardware subaddress lines A0, A1 and A2 are used to program the device subaddress for each PCF8577C connected to the I²C-bus. Lines A0 and A2 are shared with OSC and BP2 respectively to reduce pin-out requirements.

1. Line A0 is defined as LOW (logic 0) when this pin is used for the local oscillator or when connected to V_{SS}. Line A0 is defined as HIGH (logic 1) when connected to V_{DD}.
2. Line A1 must be defined as LOW (logic 0) or as HIGH (logic 1) by connection to V_{SS} or V_{DD} respectively.
3. In the direct drive mode the second backplane signal BP2 is not used and the A2/BP2 pin is exclusively the A2 input. Line A2 is defined as LOW (logic 0) when connected to V_{SS} or, if this is not possible, by leaving it unconnected (internal pull-down). Line A2 is defined as HIGH (logic 1) when connected to V_{DD}.
4. In the duplex drive mode the second backplane signal BP2 is required and the A2 signal is undefined. In this mode device selection is made exclusively from lines A0 and A1.

6.2 Oscillator A0/OSC

The PCF8577C has a single-pin built-in oscillator which provides the modulation for the LCD segment driver outputs. One external resistor and one external capacitor are connected to the A0/OSC pin to form the oscillator (see Figs 15 and 16). For correct start-up of the oscillator after power on, the resistor and capacitor must be connected to the same V_{SS}/V_{DD} as the chip. In an expanded system containing more than one PCF8577C the backplane signals are usually common to all devices and only one oscillator is required. The devices which are not used for the oscillator are put into the cascade mode by connecting the A0/OSC pin to either V_{DD} or V_{SS} depending on the required state for A0. In the cascade mode each PCF8577C is synchronized from the backplane signal(s).

6.3 User-accessible registers

There are nine user-accessible 1-byte registers. The first is a control register which is used to control the loading of data into the segment byte registers and to select display options. The other eight are segment byte registers, split into two banks of storage, which store the segment data. The set of even numbered segment byte registers is called BANK A. Odd numbered segment byte registers are called BANK B.

There is one slave address for the PCF8577C (see Fig.6). All addressed devices load the second byte into the control register and each device maintains an identical copy of the control byte in the control register at all times (see I²C-bus protocol, Fig.7), i.e. all addressed devices respond to control commands sent on the I²C-bus.

The control register is shown in more detail in Fig.3. The least-significant bits select which device and which segment byte register is loaded next. This part of the register is therefore called the Segment Byte Vector (SBV).

The upper three bits of the SBV (V5 to V3) are compared with the hardware subaddress input signals A2, A1 and A0. If they are the same then the device is enabled for loading, if not the device ignores incoming data but remains active.

The three least-significant bits of the SBV (V2 to V0) address one of the segment byte registers within the enabled chip for loading segment data.

The control register also has two display control bits. These bits are named MODE and BANK. The MODE bit selects whether the display outputs are configured for direct or duplex drive displays. The BANK bit allows the user to display BANK A or BANK B.

6.4 Auto-incremented loading

After each segment byte is loaded the SBV is incremented automatically. Thus auto-incremented loading occurs if more than one segment byte is received in a data transfer.

Since the SBV addresses both device and segment registers in all addressed chips, auto-incremented loading may proceed across device boundaries provided that the hardware subaddresses are arranged contiguously.

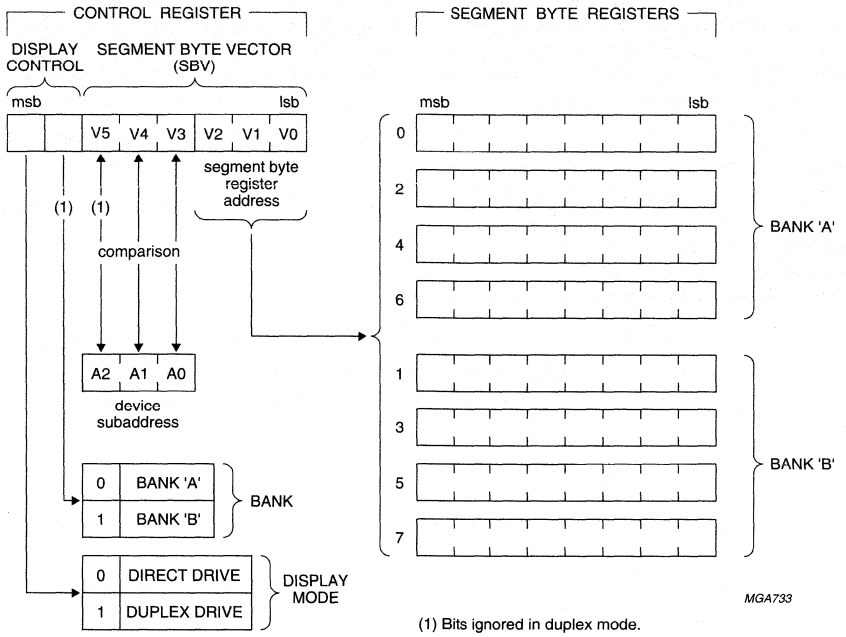
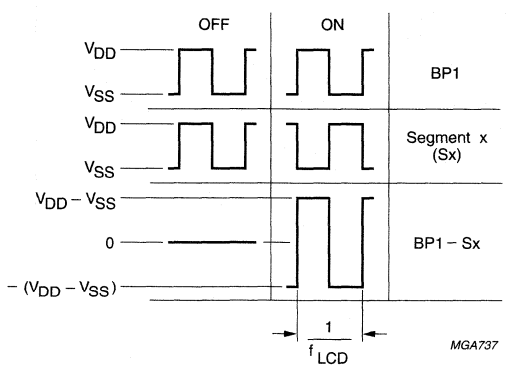


Fig.3 PCF8577C register organization.



$V_{on(rms)} = V_{DD} - V_{SS}$; $V_{off(rms)} = 0$.

Fig.4 Direct drive mode display output waveforms.

6.5 Direct drive mode

The PCF8577C is set to the direct drive mode by loading the MODE control bit with logic 0. In this mode only four bytes are required to store the data for the 32 segment drivers. Setting the BANK bit to logic 0 selects even bytes (BANK A), setting the BANK bit to logic 1 selects odd bytes (BANK B).

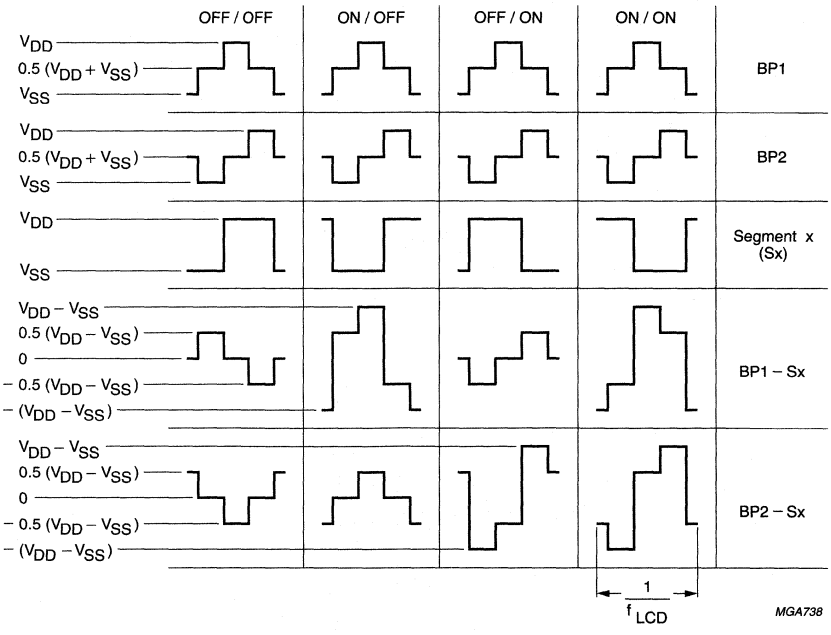
In the direct drive mode the SBV is auto-incremented by two after the loading of each segment byte register. This means that auto-incremented loading of BANK A or BANK B is possible. Either bank may be completely or partially loaded irrespective of which bank is being displayed. Direct drive output waveforms are shown in Fig.4.

6.6 Duplex mode

The PCF8577C is set to the duplex mode by loading the MODE bit with logic 1. In this mode a second backplane signal (BP2) is needed and pin A2/BP2 is used for this; therefore A2 and its equivalent SBV bit V5 are undefined. The SBV auto-increments by one between loaded bytes.

All of the segment bytes are required to store data for the 32 segment drivers and the BANK bit is ignored.

Duplex mode output waveforms are shown in Fig.5.



$V_{on(rms)} = 0.791\ (V_{DD} - V_{SS})$; $V_{off(rms)} = 0.354\ (V_{DD} - V_{SS})$.

$\frac{V_{on(rms)}}{V_{off(rms)}} = 2.236$

Fig.5 Duplex mode display output waveforms.

6.7 Power-on reset

At power-on reset the PCF8577C resets to a defined starting condition as follows:

1. Both backplane outputs are set to V_{SS} in master mode; to 3-state in cascade mode
2. All segment outputs are set to V_{SS}
3. The segment byte registers and control register are cleared
4. The I²C-bus interface is initialized.

6.8 Slave address

The PCF8577C slave address is shown in Fig.6.

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure.

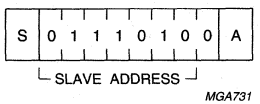


Fig.6 PCF8577C slave address.

6.9 I²C-bus protocol

The PCF8577C I²C-bus protocol is shown in Fig.7.

The PCF8577C is a slave receiver and has a fixed slave address (see Fig.6). All PCF8577Cs with the same slave address acknowledge the slave address in parallel. The second byte is always the control byte and is loaded into the control register of each PCF8577C connected to the I²C-bus. All addressed devices acknowledge the control byte. Subsequent data bytes are loaded into the segment registers of the selected device. Any number of data bytes may be loaded in one transfer and in an expanded system rollover of the SBV from 111 111 to 000 000 is allowed. If a stop (P) condition is given after the control byte acknowledge the segment data will remain unchanged. This allows the BANK bit to be toggled without changing the segment register contents. During loading of segment data only the selected PCF8577C gives an acknowledge. Loading is terminated by generating a stop (P) condition.

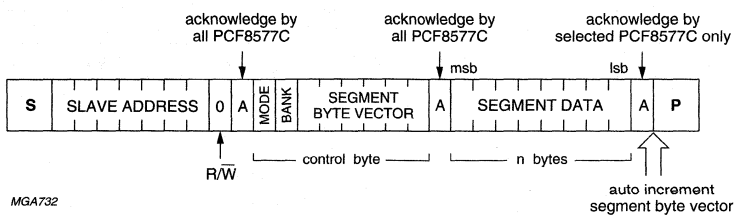


Fig.7 I²C-bus protocol.

6.10 Display memory mapping

The mapping between the eight segment registers and the segment outputs S1 to S32 is given in Tables 1 and 2.

Since only one register bit per segment is needed in the direct drive mode, the BANK bit allows swapping of display information. If BANK is set to logic 0 even bytes (BANK A) are displayed; if BANK is set to logic 1 odd bytes (BANK B) are displayed. BP1 is always used for the backplane output in the direct drive mode. In duplex mode even bytes (BANK A) correspond to backplane 1 (BP1) and odd bytes (BANK B) correspond to backplane 2 (BP2).

Table 1 Segment byte-segment driver mapping in direct drive mode

MODE	BANK	V 2	V 1	V 0	SEGMENT/ BIT/ REGISTER	MSB 7	6	5	4	3	2	1	LSB 0	BACK-PLANE
0	0	0	0	0	0	S8	S7	S6	S5	S4	S3	S2	S1	BP1
0	1	0	0	1	1	S8	S7	S6	S5	S4	S3	S2	S1	BP1
0	0	0	1	0	2	S16	S15	S14	S13	S12	S11	S10	S9	BP1
0	1	0	1	1	3	S16	S15	S14	S13	S12	S11	S10	S9	BP1
0	0	1	0	0	4	S24	S23	S22	S21	S20	S19	S18	S17	BP1
0	1	1	0	1	5	S24	S23	S22	S21	S20	S19	S18	S17	BP1
0	0	1	1	0	6	S32	S31	S30	S29	S28	S27	S26	S25	BP1
0	1	1	1	1	7	S32	S31	S30	S29	S28	S27	S26	S25	BP1

Mapping example: bit 0 of register 7 controls the LCD segment S25 if BANK bit is a logic 1.

Table 2 Segment byte-segment driver mapping in duplex mode

MODE	BANK[1]	V 2	V 1	V 0	SEGMENT/ BIT/ REGISTER	MSB 7	6	5	4	3	2	1	LSB 0	BACK-PLANE
1	X	0	0	0	0	S8	S7	S6	S5	S4	S3	S2	S1	BP1
1	X	0	0	1	1	S8	S7	S6	S5	S4	S3	S2	S1	BP2
1	X	0	1	0	2	S16	S15	S14	S13	S12	S11	S10	S9	BP1
1	X	0	1	1	3	S16	S15	S14	S13	S12	S11	S10	S9	BP2
1	X	1	0	0	4	S24	S23	S22	S21	S20	S19	S18	S17	BP1
1	X	1	0	1	5	S24	S23	S22	S21	S20	S19	S18	S17	BP2
1	X	1	1	0	6	S32	S31	S30	S29	S28	S27	S26	S25	BP1
1	X	1	1	1	7	S32	S31	S30	S29	S28	S27	S26	S25	BP2

Note

1. Where X = don't care.

Mapping example: bit 7 of register 5 controls the LCD segment S24/BP2.

7 CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the I²C-bus is not busy.

7.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

7.2 Start and stop conditions

Both data and clock lines remain HIGH when the I²C-bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

7.3 System configuration

A device generating a message is a 'transmitter', a device receiving a message is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves'.

7.4 Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the I²C-bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, set-up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

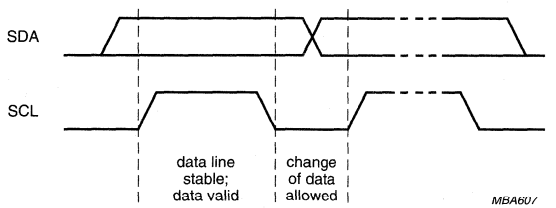


Fig.8 Bit transfer.

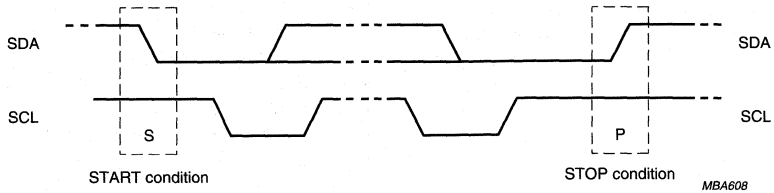


Fig.9 Definition of the start and stop conditions.

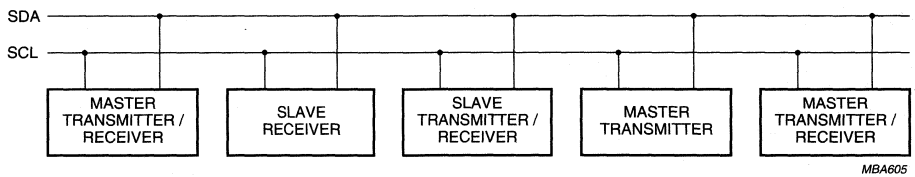


Fig.10 System configuration.

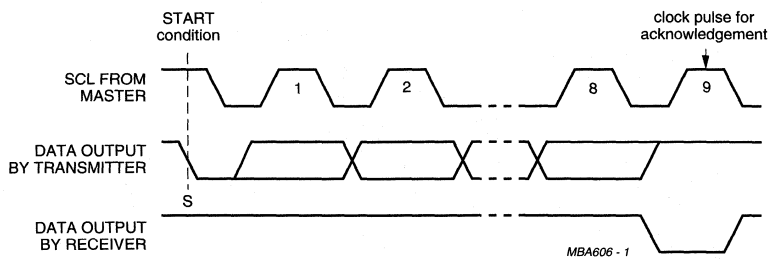


Fig.11 Acknowledgement on the I²C-bus.

8 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		−0.5	+8.0	V
V_I	input voltage on pin		−0.5	V_{DD} + 0.5	V
I_{DD}; I_{SS}	V_{DD} or V_{SS} current		−50	+50	mA
I_I	DC input current		−20	+20	mA
I_O	DC output current		−25	+25	mA
P_{tot}	power dissipation per package	note 1	−	500	mW
P_O	power dissipation per output		−	100	mW
T_{stg}	storage temperature		−65	+150	°C

Note

1. Reduce by 7.7 mW/K when T_{amb} > 60 °C.

9 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe it is desirable to take normal precautions appropriate to handling MOS devices. Advice can be found in Data Handbook IC12 under *"Handling MOS Devices"*.

10 DC CHARACTERISTICS

V_{DD} = 2.5 to 6 V; V_{SS} = 0 V; T_{amb} = −40 to 85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.(1)	MAX.	UNIT
Supply						
V_{DD}	supply voltage		2.5	−	6	V
I_{DD}	supply current for non-specified inputs at V_{DD} or V_{SS}	no load; f_{SCL} = 100 kHz; R_{osc} = 1 MΩ; C_{osc} = 680 pF		50	125	μA
		no load; f_{SCL} = 0; R_{osc} = 1 MΩ; C_{osc} = 680 pF	−	25	75	μA
		no load; f_{SCL} = 0; R_{osc} = 1 MΩ; C_{osc} = 680 pF; V_{DD} = 5 V; T_{amb} = 25 °C	−	25	40	μA
		no load; f_{SCL} = 0; direct mode; A0/OSC = V_{DD}; V_{DD} = 5 V; T_{amb} = 25 °C	−	10	20	μA
V_{POR}	power-on reset level	note 2	−	1.1	2.0	V
Input A0						
$V_{IL(A0)}$	LOW-level input voltage		0	−	0.05	V
$V_{IH(A0)}$	HIGH-level input voltage		V_{DD} − 0.05	−	V_{DD}	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.(1)	MAX.	UNIT
Input A1						
$V_{IL(A1)}$	LOW-level input voltage		0	–	$0.3V_{DD}$	V
$V_{IH(A1)}$	HIGH-level input voltage		$0.7V_{DD}$	–	V_{DD}	V
Input A2						
$V_{IL(A2)}$	LOW-level input voltage		0	–	0.10	V
$V_{IH(A2)}$	HIGH-level input voltage		$V_{DD} - 0.10$	–	V_{DD}	V
Input SCL; SDA						
$V_{IL(SCL; SDA)}$	LOW-level input voltage		0	–	$0.3V_{DD}$	V
$V_{IH(SCL; SDA)}$	HIGH-level input voltage		$0.7V_{DD}$	–	6	V
C_i	input capacitance	note 3	–	–	7	pF
Output SDA						
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; V_{DD} = 5 V	3	–	–	mA
A1; SCL; SDA						
I_{L1}	leakage current	$V_I = V_{DD}$ or V_{SS}	–1	–	+1	µA
A2/BP2; BP1						
I_{L2}	leakage current	$V_I = V_{DD}$ or V_{SS}	–5	–	+5	µA
A2/BP2						
I_{pd}	pull-down current	$V_I = V_{DD}$	–5	–1.5	–	µA
A0/OSC						
I_{L3}	leakage current	$V_I = V_{DD}$	–1	–	–	µA
Oscillator						
I_{OSC}	start-up current	$V_I = V_{SS}$	–	1.2	5	µA
LCD outputs						
V_{DC}	DC component of LCD driver		–	±20	–	mV
I_{OL1}	LOW-level segment output current	V_{DD} = 5 V; V_{OL} = 0.8 V; note 4	0.3	–	–	mA
I_{OH1}	HIGH-level segment output current	V_{DD} = 5 V; $V_{OH} = V_{DD} - 0.8$ V; note 4	–	–	–0.3	mA
R_{BP}	backplane output resistance (BP1; BP2)	$V_O = V_{SS}$ or V_{DD} or $\frac{1}{2}(V_{SS} + V_{DD})$; note 5	–	0.4	5	kΩ

Notes

1. Typical conditions: V_{DD} = 5 V; T_{amb} = 25 °C.
2. Resets all logic when $V_{DD} < V_{POR}$.
3. Periodically sampled, not 100% tested.
4. Outputs measured one at a time.
5. Outputs measured one at a time; V_{DD} = 5 V; I_{load} = 100 µA.

11 AC CHARACTERISTICS

V_{DD} = 2.5 to 6 V; T_{amb} = −40 to 85 °C; unless otherwise specified. All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.(1)	MAX.	UNIT
f_{LCD}	display frequency	C_{osc} = 680 pF; R_{osc} = 1 MΩ	65	90	120	Hz
t_{BS}	driver delays with test loads	V_{DD} = 5 V	–	20	100	µs
I²C-bus						
f_{SCL}	SCL clock frequency		–	–	100	kHz
t_{SW}	tolerable spike width on I²C-bus	T_{amb} = 25 °C	–	–	100	ns
t_{BUF}	I²C-bus free time		4.7	–	–	µs
$t_{SU;STA}$	START condition set-up time		4.0	–	–	µs
$t_{HD;STA}$	START condition hold time		4.0	–	–	µs
t_{LOW}	SCL LOW time		4.7	–	–	µs
t_{HIGH}	SCL HIGH time		4.0	–	–	µs
t_r	SCL and SDA rise time		–	–	1.0	µs
t_f	SCL and SDA fall time		–	–	0.3	µs
$t_{SU;DAT}$	data set-up time		250	–	–	ns
$t_{HD;DAT}$	data hold time		0	–	–	ns
$t_{SU;STO}$	STOP condition set-up time		4.0	–	–	µs

Note

1. Typical conditions: V_{DD} = 5 V; T_{amb} = 25 °C.

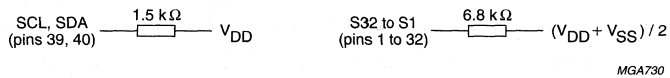


Fig.12 Test loads.

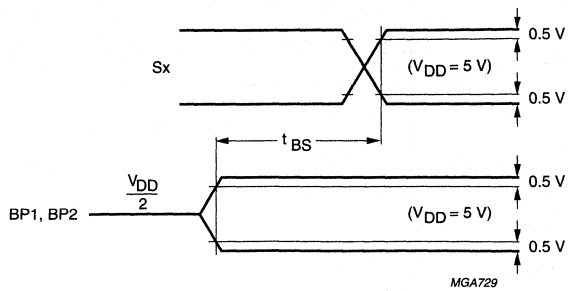


Fig.13 Driver timing waveforms.

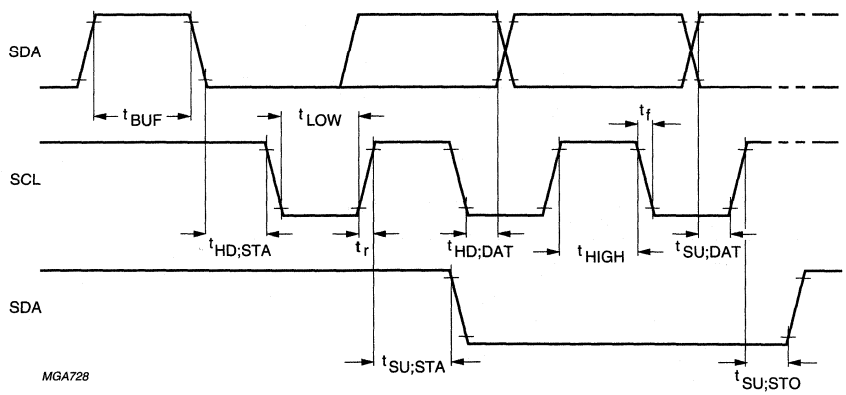


Fig.14 I²C-bus timing diagram; rise and fall times refer to V_{IL} and V_{IH}.

12 APPLICATION INFORMATION

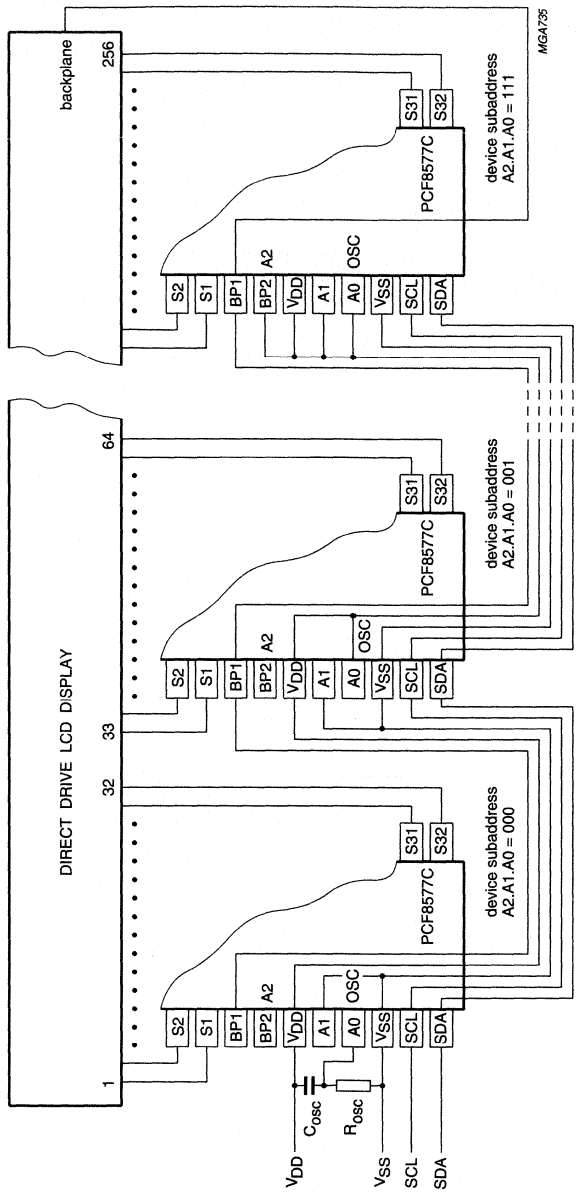


Fig.15 Direct display driver; expansion to 256 segments using eight PCF8577Cs.

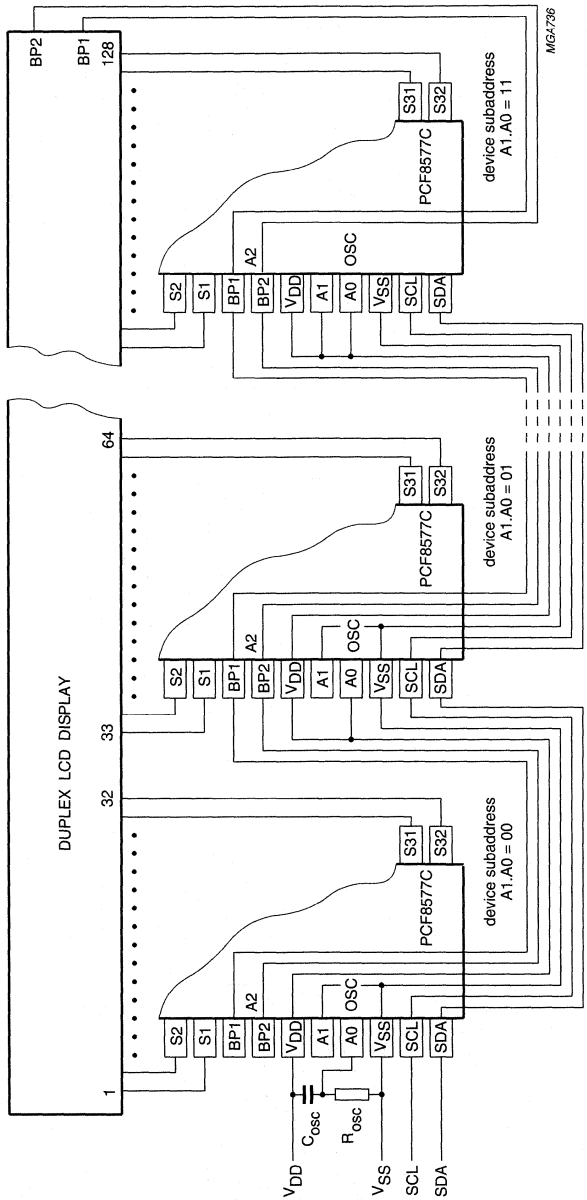
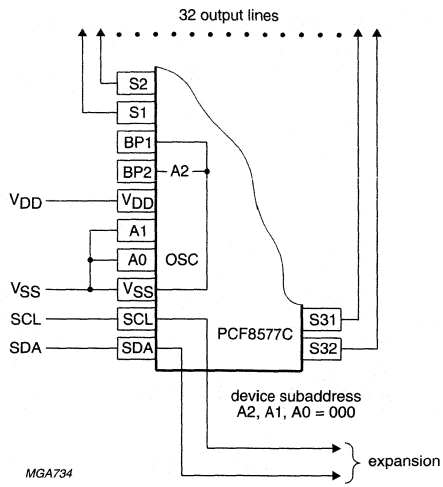


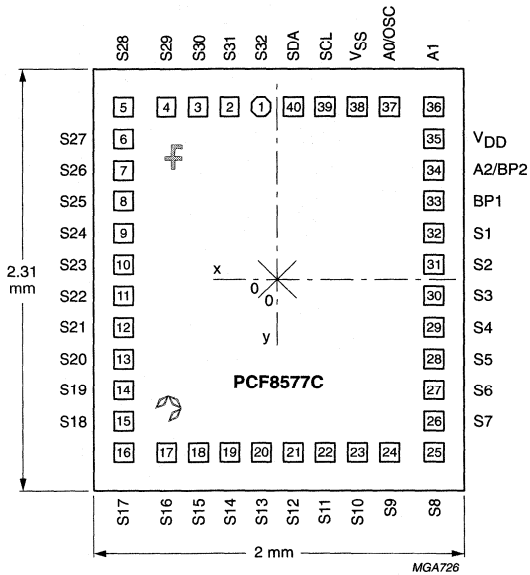
Fig.16 Duplex display; expansion to 2 × 128 segments using four PCF8577Cs.



MODE bit must always be set to logic 0 (direct drive).
BANK switching is permitted.
BP1 must always be connected to V_{SS} and A0/OSC must be connected to either V_{DD} or V_{SS} (no LCD modulation).

Fig.17 Use of PCF8577C as a 32-bit output expander in I²C-bus application.

13 CHIP DIMENSIONS AND BONDING PAD LOCATIONS



Chip area = 4.62 mm².
Thickness = 381 ±25 µm.
n-substrate (back) connected to V_{DD}.
Bonding pad dimensions = 110 µm × 110 µm.

Fig.18 Bonding pad locations.

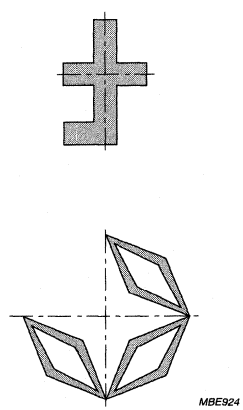


Fig.19 Reference marks.

Table 3 Bonding pad locations (dimensions in μm)
All x and y co-ordinates are referenced to the centre of the chip, see Fig.18.

SIGNAL	PAD POSITION CENTRED	
	x	y
S32	−86	941
S31	−257	941
S30	−428	941
S29	−599	941
S28	−836	941
S27	−836	769
S26	−836	598
S25	−836	427
S24	−836	256
S23	−836	85
S22	−836	−86
S21	−836	−257
S20	−836	−428
S19	−836	−599
S18	−836	−770
S17	−836	−941
S16	−599	−941
S15	−428	−941
S14	−257	−941
S13	−86	−941
S12	85	−941
S11	256	−941

SIGNAL	PAD POSITION CENTRED	
	x	y
S10	427	−941
S9	598	−941
S8	836	−941
S7	836	−770
S6	836	−599
S5	836	−428
S4	836	−257
S3	836	−86
S2	836	85
S1	836	256
BP1	836	427
A2/BP2	836	598
V_{DD}	836	769
A1	836	941
A0/OSC	598	941
V_{SS}	427	941
SCL	256	941
SDA	85	941
Recpats		
C	−586	−699
F	−580	663

LCD row/column driver for dot matrix graphic displays

PCF8578

CONTENTS

LCD row/column driver for dot matrix graphic displays

PCF8578

1 FEATURES

- Single chip LCD controller/driver
- Stand-alone or may be used with up to 32 PCF8579s (40960 dots possible)
- 40 driver outputs, configurable as $^{32}/_{8}$, $^{24}/_{16}$, $^{16}/_{24}$ or $^{8}/_{32}$ rows/columns
- Selectable multiplex rates; 1 : 8, 1 : 16, 1 : 24 or 1 : 32
- Externally selectable bias configuration, 5 or 6 levels
- 1280-bit RAM for display data storage and scratch pad
- Display memory bank switching
- Auto-incremented data loading across hardware subaddress boundaries (with PCF8579)
- Provides display synchronization for PCF8579
- On-chip oscillator, requires only 1 external resistor
- Power-on reset blanks display
- Logic voltage supply range 2.5 to 6 V
- Maximum LCD supply voltage 9 V
- Low power consumption
- I²C-bus interface
- TTL/CMOS compatible
- Compatible with most microcontrollers
- Optimized pinning for single plane wiring in multiple device applications (with PCF8579)
- Space saving 56-lead plastic mini-pack and 64 pin quad flat pack
- Compatible with chip-on-glass technology.

2 APPLICATIONS

- Automotive information systems
- Telecommunication systems
- Point-of-sale terminals
- Computer terminals
- Instrumentation.

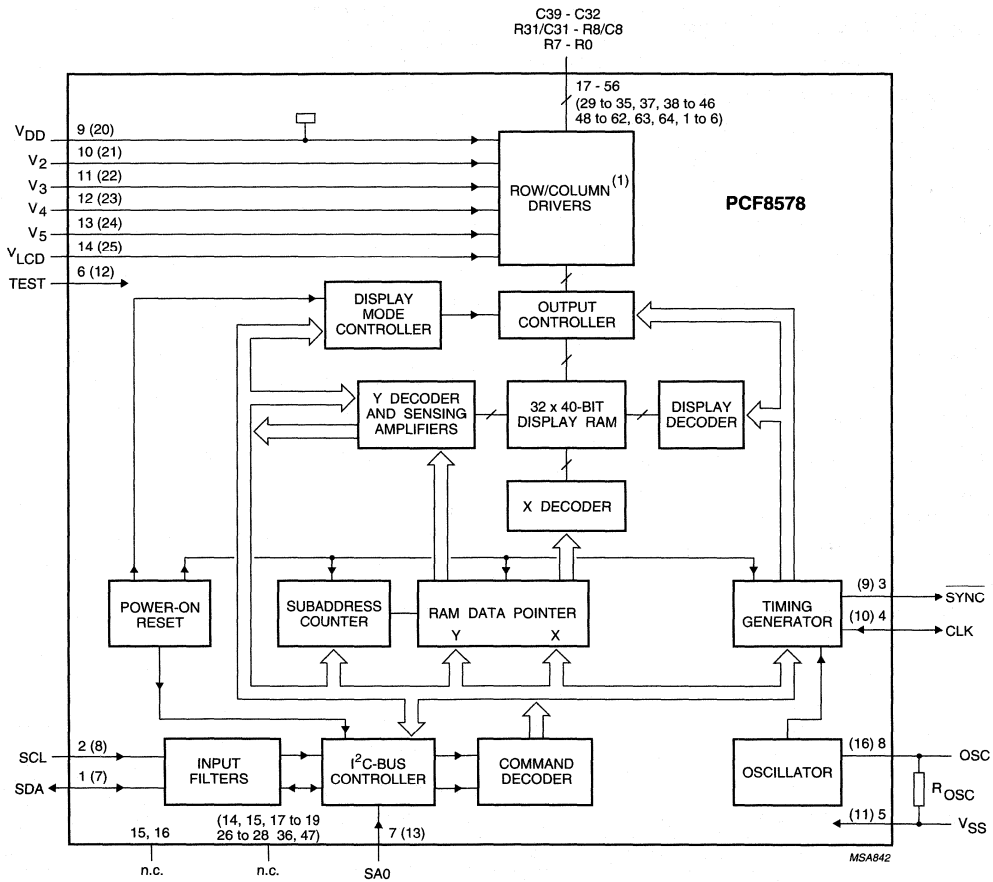
3 GENERAL DESCRIPTION

The PCF8578 is a low power CMOS LCD row/column driver, designed to drive dot matrix graphic displays at multiplex rates of 1 : 8, 1 : 16, 1 : 24 or 1 : 32. The device has 40 outputs, of which 24 are programmable, configurable as $^{32}/_{8}$, $^{24}/_{16}$, $^{16}/_{24}$ or $^{8}/_{32}$ rows/columns. The PCF8578 can function as a stand-alone LCD controller/driver for use in small systems, or for larger systems can be used in conjunction with up to 32 PCF8579s for which it has been optimized. Together these two devices form a general purpose LCD dot matrix driver chip set, capable of driving displays of up to 40960 dots. The PCF8578 is compatible with most microcontrollers and communicates via a two-line bidirectional bus (I²C-bus). Communication overheads are minimized by a display RAM with auto-incremented addressing and display bank switching.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8578T	VSO56	plastic very small outline package; 56 leads	SOT190-1
PCF8578U/2	–	chip with bumps in tray	–
PCF8578H	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2

5 BLOCK DIAGRAM



(1) Operates at LCD voltage levels, all other blocks operate at logic levels.
The pin numbers given in parenthesis refer to the LQFP64 package.

Fig.1 Block diagram.

6 PINNING

SYMBOL	PIN		DESCRIPTION
	VSO56	LQFP64	
SDA	1	7	I^2C-bus serial data input/output
SCL	2	8	I^2C-bus serial clock input
$\overline{SYNC}$	3	9	cascade synchronization output
CLK	4	10	external clock input/output
V_{SS}	5	11	ground (logic)
TEST	6	12	test pin (connect to V_{SS})
SA0	7	13	I^2C-bus slave address input (bit 0)
OSC	8	16	oscillator input
V_{DD}	9	20	positive supply voltage
V_2 to V_5	10 to 13	21 to 24	LCD bias voltage inputs
V_{LCD}	14	25	LCD supply voltage
n.c.	15, 16	14, 15, 17 to 19, 26 to 28, 36, 47	not connected
C39 to C32	17 to 24	29 to 35, 37	LCD column driver outputs
R31/C31 to R8/C8	25 to 48	38 to 46, 48 to 62	LCD row/column driver outputs
R7 to R0	49 to 56	63, 64, 1 to 6	LCD row driver outputs

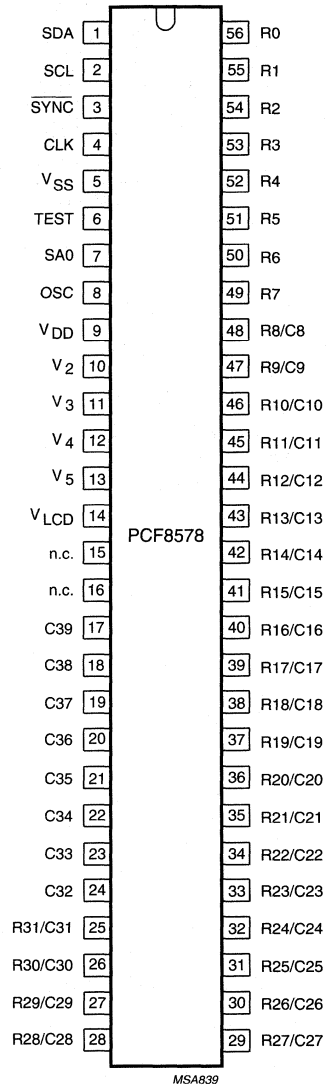


Fig.2 Pin configuration (VSO56).

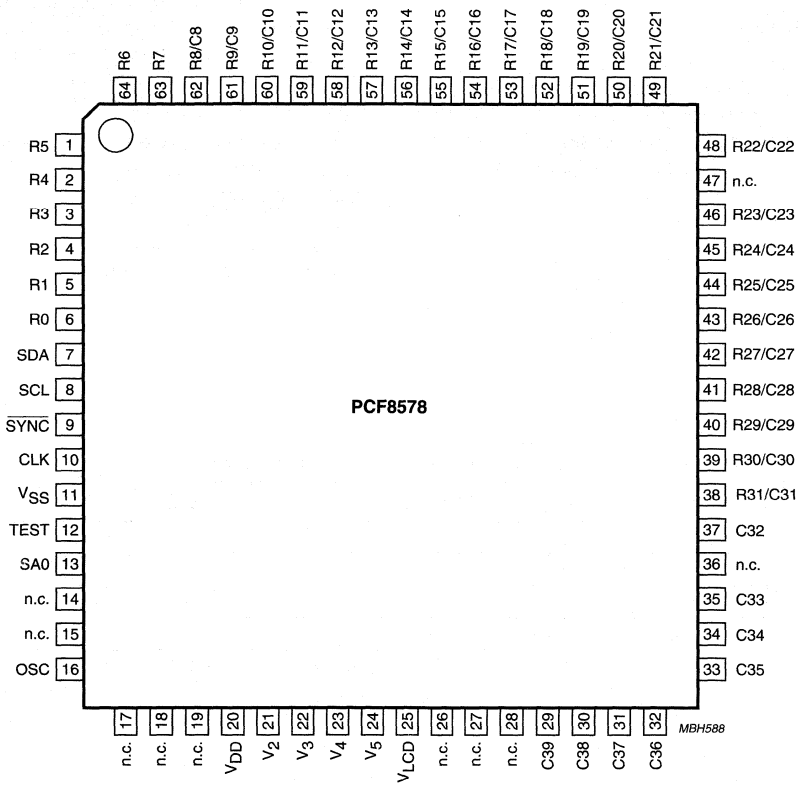


Fig.3 Pin configuration (LQFP64).

7 FUNCTIONAL DESCRIPTION

The PCF8578 row/column driver is designed for use in one of three ways:

- Stand-alone row/column driver for small displays (mixed mode)
- Row/column driver with cascaded PCF8579s (mixed mode)
- Row driver with cascaded PCF8579s (mixed mode).

7.1 Mixed mode

In mixed mode, the device functions as both a row and column driver. It can be used in small stand-alone applications, or for larger displays with up to 15 PCF8579s (31 PCF8579s when two slave addresses are used). See Table 1 for common display configurations.

7.2 Row mode

In row mode, the device functions as a row driver with up to 32 row outputs and provides the clock and synchronization signals for the PCF8579. Up to 16 PCF8579s can normally be cascaded (32 when two slave addresses are used).

Timing signals are derived from the on-chip oscillator, whose frequency is determined by the value of the resistor connected between OSC and V_{SS}.

Commands sent on the I^2C-bus from the host microcontroller set the mode (row or mixed), configuration (multiplex rate and number of rows and columns) and control the operation of the device. The device may have one of two slave addresses. The only difference between these slave addresses is the least significant bit, which is set by the logic level applied to SA0. The PCF8578 and PCF8579 also have subaddresses. The subaddress of the PCF8578 is only defined in mixed mode and is fixed at 0. The RAM may only be accessed in mixed mode and data is loaded as described for the PCF8579.

Bias levels may be generated by an external potential divider with appropriate decoupling capacitors. For large displays, bias sources with high drive capability should be used. A typical mixed mode system operating with up to 15 PCF8579s is shown in Fig.5 (a stand-alone system would be identical but without the PCF8579s).

Table 1 Possible displays configurations

APPLICATION	MULTIPLEX RATE	MIXED MODE		ROW MODE		TYPICAL APPLICATIONS
		ROWS	COLUMNS	ROWS	COLUMNS	
Stand alone	1 : 8	8	32	–	–	small digital or alphanumerical displays
	1 : 16	16	24	–	–	
	1 : 24	24	16	–	–	
	1 : 32	32	8	–	–	
With PCF8579	1 : 8	8[1]	632[1]	8 × 4 4[2]	640[2]	alphanumeric displays and dot matrix graphic displays
	1 : 16	16[1]	624[1]	16 × 2[2]	640[2]	
	1 : 24	24[1]	616[1]	24[2]	640[2]	
	1 : 32	32[1]	608[1]	24[2]	640[2]	

Notes

1. Using 15 PCF8579s.
2. Using 16 PCF8579s.

7.3 Multiplexed LCD bias generation

The bias levels required to produce maximum contrast depend on the multiplex rate and the LCD threshold voltage (V_{th}). V_{th} is typically defined as the RMS voltage at which the LCD exhibits 10% contrast. Table 2 shows the optimum voltage bias levels for the PCF8578 as functions of V_{op} ($V_{op} = V_{DD} - V_{LCD}$), together with the discrimination ratios (D) for the different multiplex rates. A practical value for V_{op} is obtained by equating $V_{off(rms)}$ with V_{th}. Figure 4 shows the first 4 rows of Table 2 as graphs. Table 3 shows the relative values of the resistors required in the configuration of Fig.5 to produce the standard multiplex rates.

Table 2 Optimum LCD voltages

PARAMETER	MULTIPLEX RATE			
	1 : 8	1 : 16	1 : 24	1 : 32
$\frac{V_2}{V_{op}}$	0.739	0.800	0.830	0.850
$\frac{V_3}{V_{op}}$	0.522	0.600	0.661	0.700
$\frac{V_4}{V_{op}}$	0.478	0.400	0.339	0.300
$\frac{V_5}{V_{op}}$	0.261	0.200	0.170	0.150
$\frac{V_{off(rms)}}{V_{op}}$	0.297	0.245	0.214	0.193
$\frac{V_{on(rms)}}{V_{op}}$	0.430	0.316	0.263	0.230
$D = \frac{V_{on(rms)}}{V_{off(rms)}}$	1.447	1.291	1.230	1.196
$\frac{V_{op}}{V_{th}}$	3.370	4.080	4.680	5.190

Table 3 Multiplex rates and resistor values for Fig.5

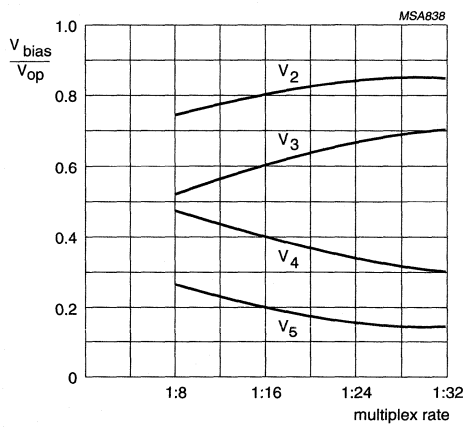
RESISTORS	MULTIPLEX RATE (n)	
	n = 8	n = 16, 24, 32
R1	R	R
R2	$(\sqrt{n-2})R$	R
R3	$(3-\sqrt{n})R$	$(\sqrt{n-3})R$

7.4 Power-on reset

At power-on the PCF8578 resets to a defined starting condition as follows:

1. Display blank
2. 1 : 32 multiplex rate, row mode
3. Start bank, 0 selected
4. Data pointer is set to X, Y address 0, 0
5. Character mode
6. Subaddress counter is set to 0
7. I^2C-bus interface is initialized.

Data transfers on the I^2C-bus should be avoided for 1 ms following power-on, to allow completion of the reset action.



$V_{bias} = V_2, V_3, V_4, V_5$. See Table 2.

Fig.4 V_{bias}/V_{op} as a function of the multiplex rate.

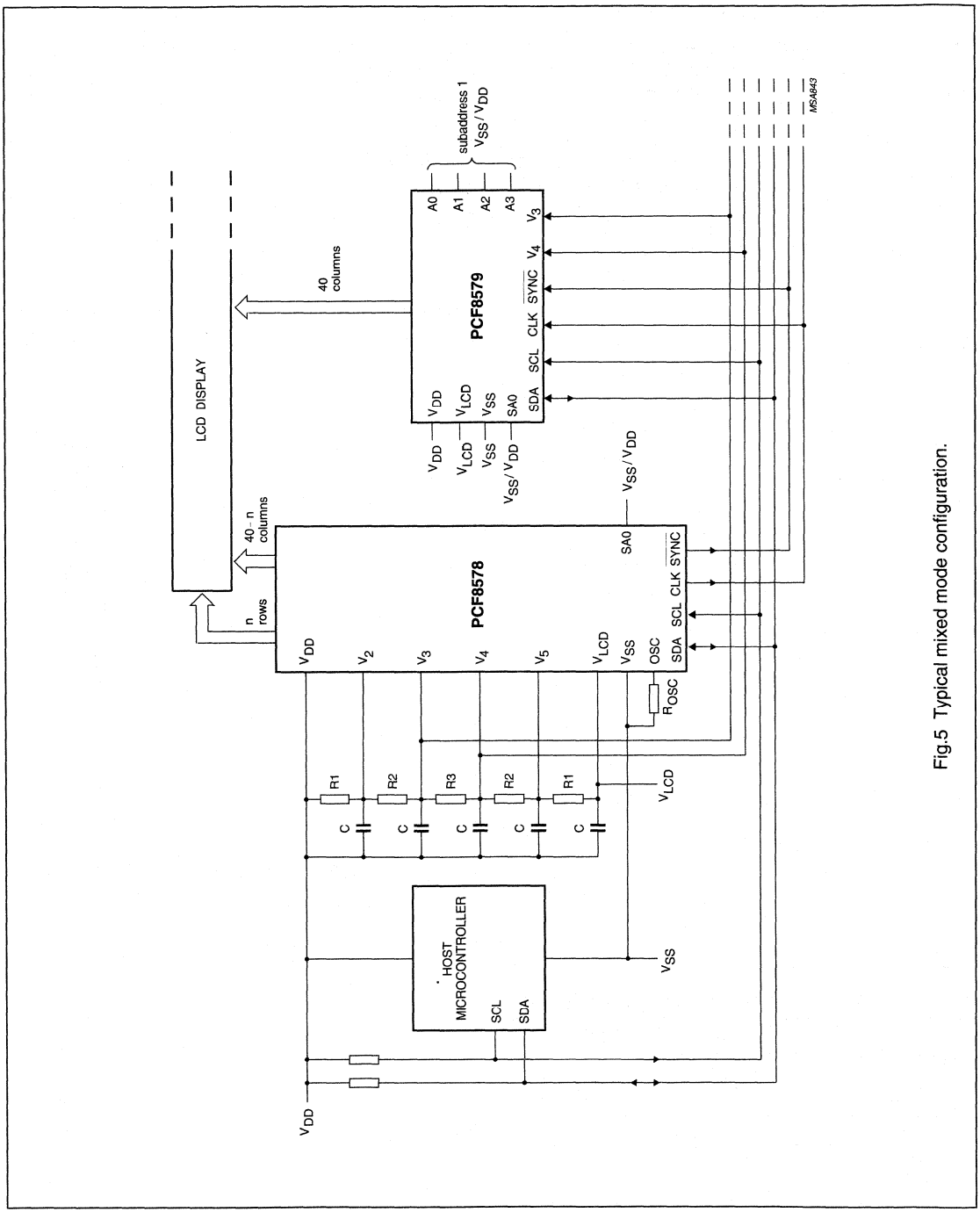


Fig.5 Typical mixed mode configuration.

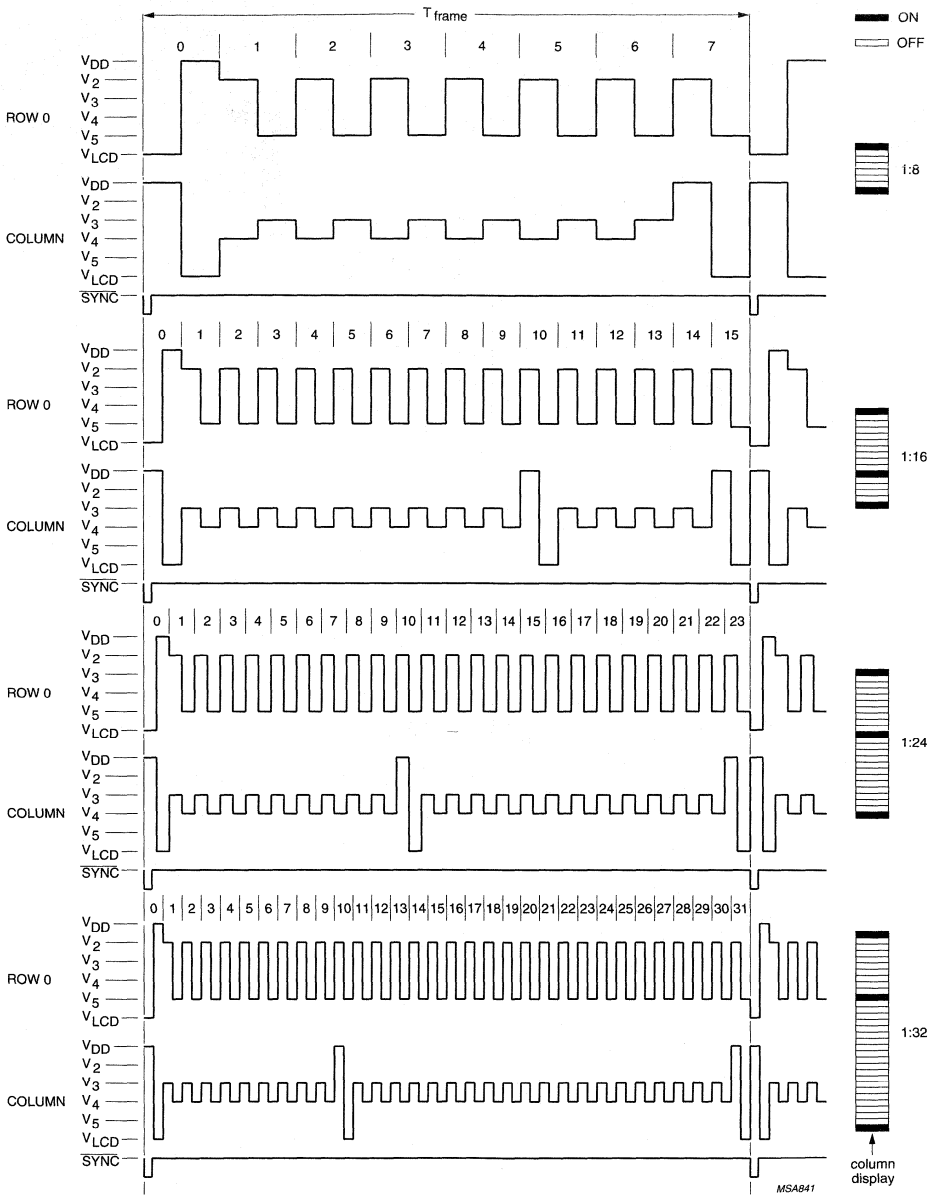
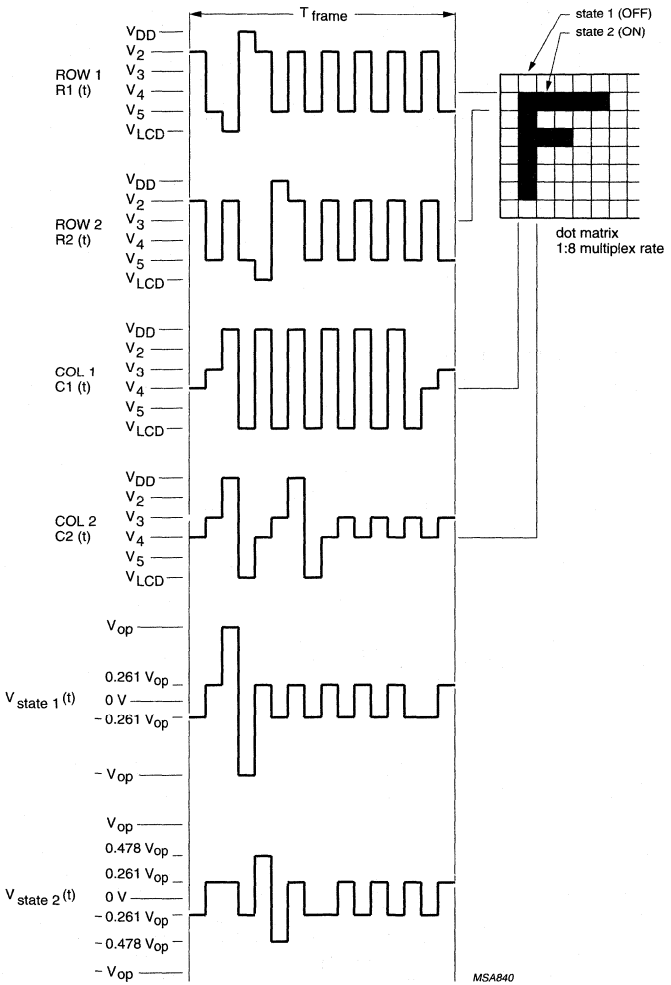


Fig.6 LCD row/column waveforms.



$V_{state\ 1}(t) = C1(t) - R1(t)$:

$$\frac{V_{on(rms)}}{V_{op}} = \sqrt{\frac{1}{8} + \frac{\sqrt{8}-1}{8(\sqrt{8}+1)}} = 0.430$$

$V_{state\ 2}(t) = C2(t) - R2(t)$:

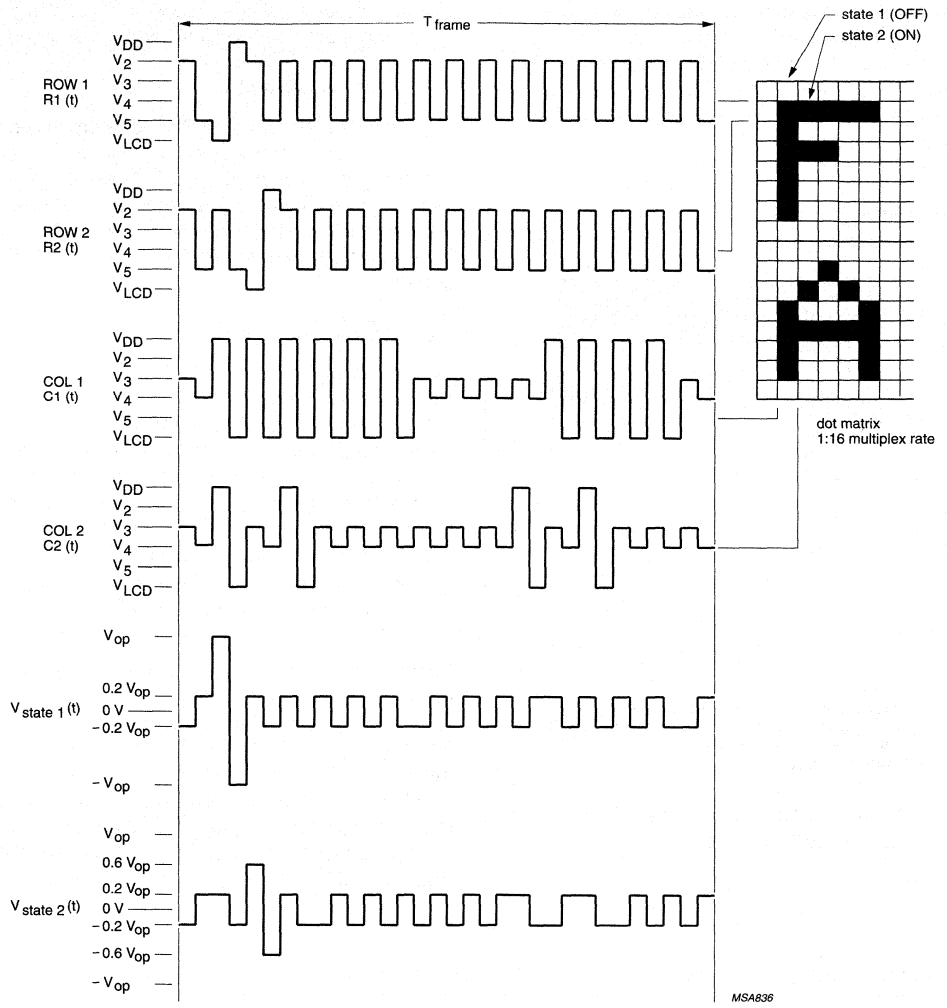
$$\frac{V_{off(rms)}}{V_{op}} = \sqrt{\frac{2(\sqrt{8}-1)}{\sqrt{8}(\sqrt{8}+1)^2}} = 0.297$$

general relationship (n = multiplex rate)

$$\frac{V_{on(rms)}}{V_{op}} = \sqrt{\frac{1}{n} + \frac{\sqrt{n}-1}{n(\sqrt{n}+1)}}$$

$$\frac{V_{off(rms)}}{V_{op}} = \sqrt{\frac{2(\sqrt{n}-1)}{\sqrt{n}(\sqrt{n}+1)^2}}$$

Fig.7 LCD drive mode waveforms for 1 : 8 multiplex rate.



$V_{state\ 1}(t) = C1(t) - R1(t)$:

$$\frac{V_{on(rms)}}{V_{op}} = \sqrt{\frac{1}{16} + \frac{\sqrt{16}-1}{16(\sqrt{16}+1)}} = 0.316$$

$V_{state\ 2}(t) = C2(t) - R2(t)$:

$$\frac{V_{off(rms)}}{V_{op}} = \sqrt{\frac{2(\sqrt{16}-1)}{\sqrt{16}(\sqrt{16}+1)^2}} = 0.254$$

general relationship (n = multiplex rate)

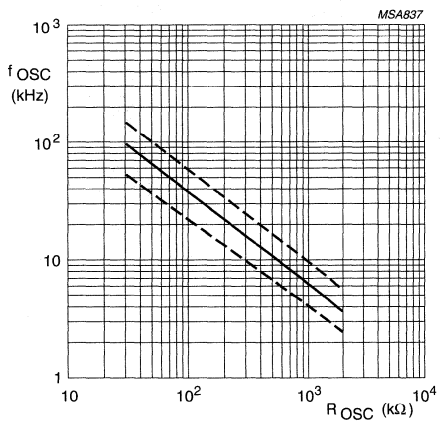
$$\frac{V_{on(rms)}}{V_{op}} = \sqrt{\frac{1}{n} + \frac{\sqrt{n}-1}{n(\sqrt{n}+1)}}$$

$$\frac{V_{off(rms)}}{V_{op}} = \sqrt{\frac{2(\sqrt{n}-1)}{\sqrt{n}(\sqrt{n}+1)^2}}$$

Fig.8 LCD drive mode waveforms for 1 : 16 multiplex rate.

7.5 Internal clock

The clock signal for the system may be generated by the internal oscillator and prescaler. The frequency is determined by the value of the resistor R_{OSC}, see Fig.9. For normal use a value of 330 kΩ is recommended. The clock signal, for cascaded PCF8579s, is output at CLK and has a frequency $\frac{1}{6}$ (multiplex rate 1 : 8, 1 : 16 and 1 : 32) or $\frac{1}{8}$ (multiplex rate 1 : 24) of the oscillator frequency.



To avoid capacitive coupling, which could adversely affect oscillator stability, R_{OSC} should be placed as closely as possible to the OSC pin. If this proves to be a problem, a filtering capacitor may be connected in parallel to R_{OSC}.

Fig.9 Oscillator frequency as a function of external oscillator resistor, R_{OSC}.

7.6 External clock

If an external clock is used, OSC must be connected to V_{DD} and the external clock signal to CLK. Table 4 summarizes the nominal CLK and $\overline{SYNC}$ frequencies.

7.7 Timing generator

The timing generator of the PCF8578 organizes the internal data flow of the device and generates the LCD frame synchronization pulse $\overline{SYNC}$, whose period is an integer multiple of the clock period. In cascaded applications, this signal maintains the correct timing relationship between the PCF8578 and PCF8579s in the system.

7.8 Row/column drivers

Outputs R0 to R7 and C32 to C39 are fixed as row and column drivers respectively. The remaining 24 outputs R8/C8 to R31/C31 are programmable and may be configured (in blocks of 8) to be either row or column drivers. The row select signal is produced sequentially at each output from R0 up to the number defined by the multiplex rate (see Table 1). In mixed mode the remaining outputs are configured as columns. In row mode all programmable outputs (R8/C8 to R31/C31) are defined as row drivers and the outputs C32 to C39 should be left open-circuit.

Using a 1 : 16 multiplex rate, two sets of row outputs are driven, thus facilitating split-screen configurations, i.e. a row select pulse appears simultaneously at R0 and R16/C16, R1 and R17/C17 etc. Similarly, using a multiplex rate of 1 : 8, four sets of row outputs are driven simultaneously. Driver outputs must be connected directly to the LCD. Unused outputs should be left open-circuit. In 1 : 8 R0 to R7 are rows; in 1 : 16 R0 to R15/C15 are rows; in 1 : 24 R0 to R23/C23 are rows; in 1 : 32 R0 to R31/C31 are rows.

Table 4 Signal frequencies required for nominal 64 Hz frame frequency; note 1.

OSCILLATOR FREQUENCY f_{OSC}(2) (Hz)	FRAME FREQUENCY $f_{\overline{SYNC}}$ (Hz)	MULTIPLEX RATE (n)	DIVISION RATIO	CLOCK FREQUENCY f_{CLK} (Hz)
12288	64	1 : 8, 1 : 16, 1 : 32	6	2048
12288	64	1 : 24	8	1536

Notes

1. A clock signal must always be present, otherwise the LCD may be frozen in a DC state.
2. R_{OSC} = 330 kΩ.

7.9 Display mode controller

The configuration of the outputs (row or column) and the selection of the appropriate driver waveforms are controlled by the display mode controller.

7.10 Display RAM

The PCF8578 contains a 32 x 40-bit static RAM which stores the display data. The RAM is divided into 4 banks of 40 bytes (4 x 8 x 40 bits). During RAM access, data is transferred to/from the RAM via the I^2C-bus. The first eight columns of data (0 to 7) cannot be displayed but are available for general data storage and provide compatibility with the PCF8579. There is a direct correspondence between X-address and column output number.

7.11 Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows an individual data byte or a series of data bytes to be written into, or read from, the display RAM, controlled by commands sent on the I^2C-bus.

7.12 Subaddress counter

The storage and retrieval of display data is dependent on the content of the subaddress counter. Storage takes place only when the contents of the subaddress counter agree with the hardware subaddress. The hardware subaddress of the PCF8578, valid in mixed mode only, is fixed at 0000.

7.13 I^2C-bus controller

The I^2C-bus controller detects the I^2C-bus protocol, slave address, commands and display data bytes. It performs the conversion of the data input (serial-to-parallel) and the data output (parallel-to-serial). The PCF8578 acts as an I^2C-bus slave transmitter/receiver in mixed mode, and as a slave receiver in row mode. A slave device cannot control bus communication.

7.14 Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

7.15 RAM access

RAM operations are only possible when the PCF8578 is in mixed mode.

In this event its hardware subaddress is internally fixed at 0000 and the hardware subaddresses of any PCF8579 used in conjunction with the PCF8578 must start at 0001.

There are three RAM ACCESS modes:

- Character
- Half-graphic
- Full-graphic.

These modes are specified by bits G1 to G0 of the RAM ACCESS command. The RAM ACCESS command controls the order in which data is written to or read from the RAM (see Fig.10).

To store RAM data, the user specifies the location into which the first byte will be loaded (see Fig.11):

- Device subaddress (specified by the DEVICE SELECT command)
- RAM X-address (specified by the LOAD X-ADDRESS command)
- RAM bank (specified by bits Y1 and Y0 of the RAM ACCESS command).

Subsequent data bytes will be written or read according to the chosen RAM ACCESS mode. Device subaddresses are automatically incremented between devices until the last device is reached. If the last device has subaddress 15, further display data transfers will lead to a wrap-around of the subaddress to 0.

7.16 Display control

The display is generated by continuously shifting rows of RAM data to the dot matrix LCD via the column outputs. The number of rows scanned depends on the multiplex rate set by bits M1 and M0 of the SET MODE command.

The display status (all dots on/off and normal/inverse video) is set by bits E1 and E0 of the SET MODE command. For bank switching, the RAM bank corresponding to the top of the display is set by bits B1 and B0 of the SET START BANK command. This is shown in Fig.12. This feature is useful when scrolling in alphanumeric applications.

7.17 TEST pin

The TEST pin must be connected to V_{SS}.

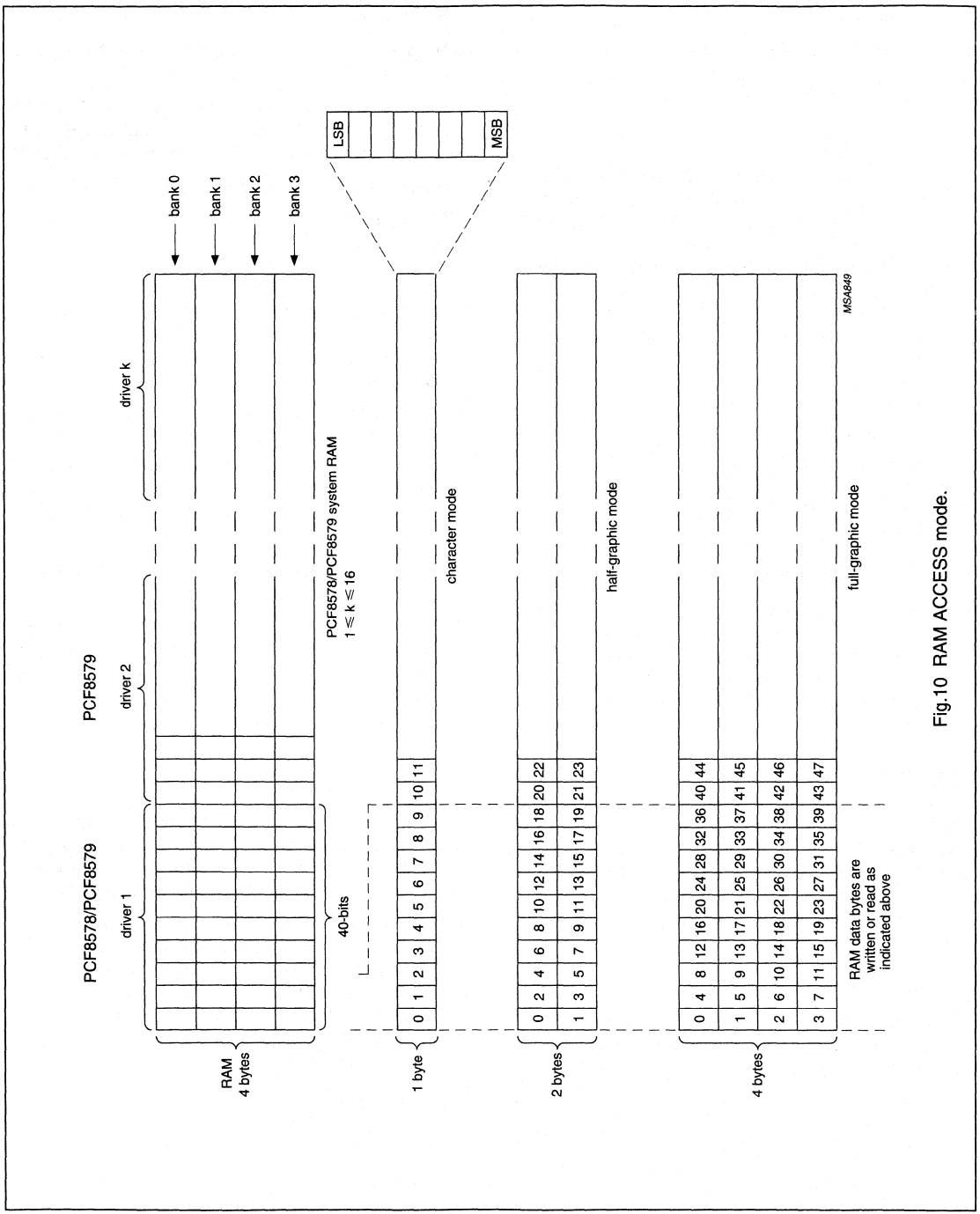


Fig.10 RAM ACCESS mode.

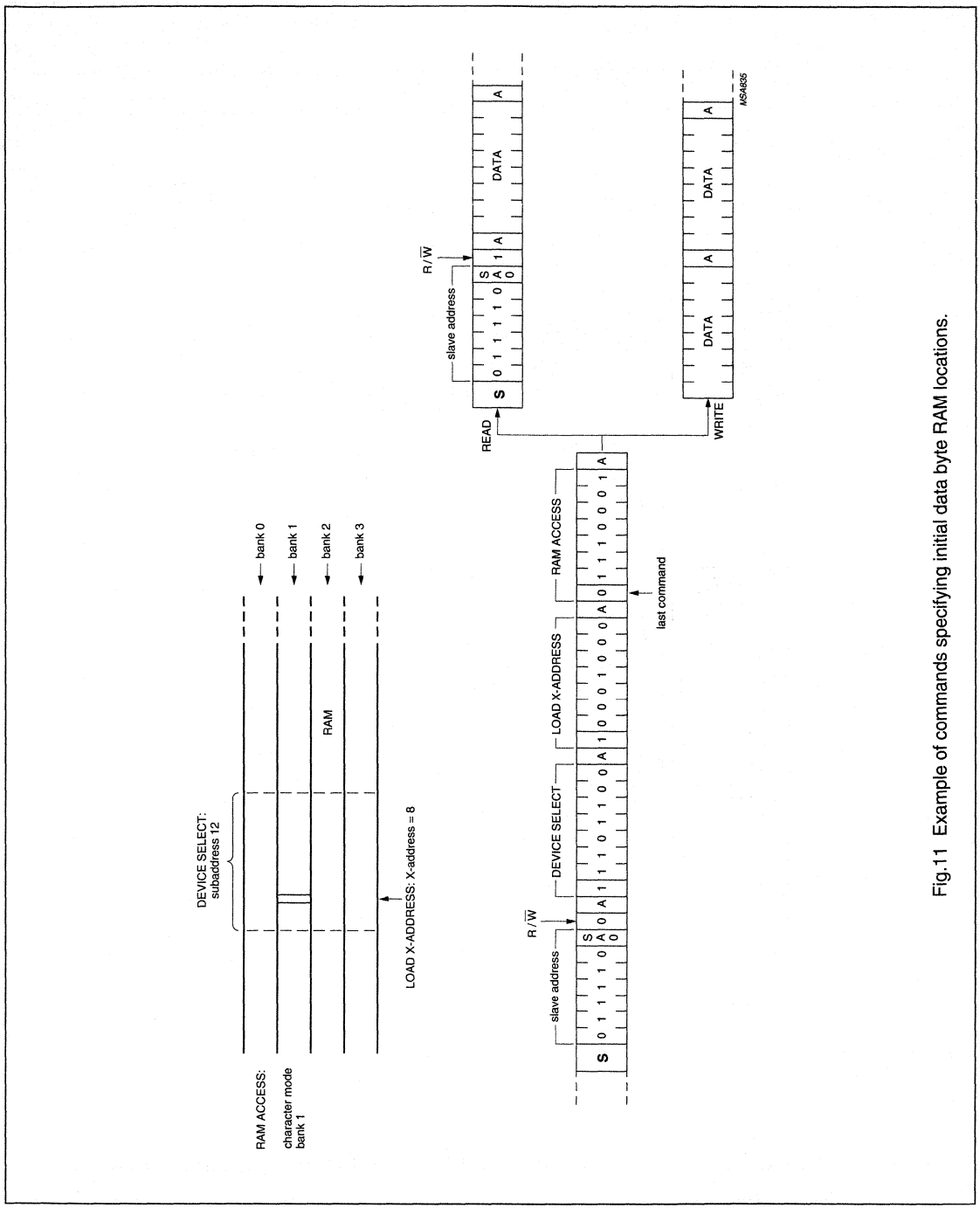


Fig.11 Example of commands specifying initial data byte RAM locations.

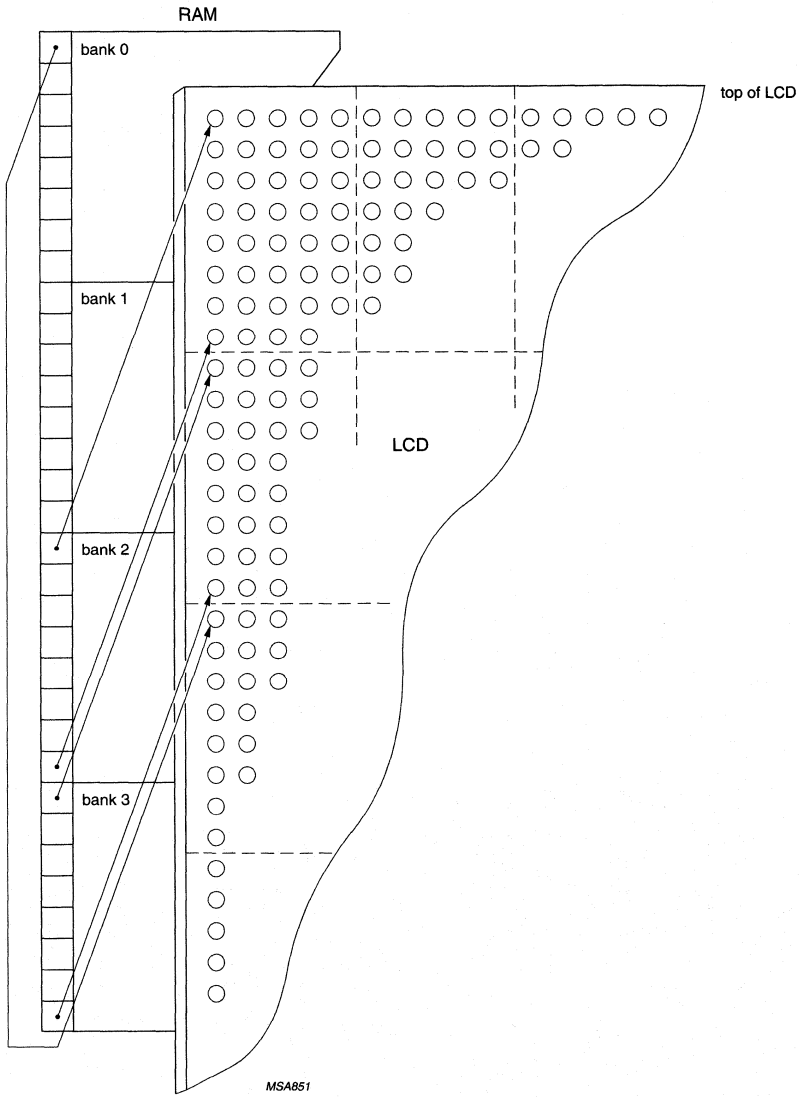


Fig.12 Relationship between display and SET START BANK; 1 : 32 multiplex rate and start bank = 2.

8 I²C-BUS PROTOCOL

Two 7-bit slave addresses (0111100 and 0111101) are reserved for both the PCF8578 and PCF8579. The least significant bit of the slave address is set by connecting input SA0 to either 0 (V_{SS}) or 1 (V_{DD}). Therefore, two types of PCF8578 or PCF8579 can be distinguished on the same I²C-bus which allows:

1. One PCF8578 to operate with up to 32 PCF8579s on the same I²C-bus for very large applications
2. The use of two types of LCD multiplex schemes on the same I²C-bus.

In most applications the PCF8578 will have the same slave address as the PCF8579.

The I²C-bus protocol is shown in Fig.13.
All communications are initiated with a start condition (S) from the I²C-bus master, which is followed by the desired slave address and read/write bit. All devices with this slave address acknowledge in parallel. All other devices ignore the bus transfer.

In WRITE mode (indicated by setting the read/write bit LOW) one or more commands follow the slave address acknowledgement. The commands are also acknowledged by all addressed devices on the bus. The last command must clear the continuation bit C. After the last command a series of data bytes may follow. The acknowledgement after each byte is made only by the (A0, A1, A2 and A3) addressed PCF8579 or PCF8578 with its implicit subaddress 0. After the last data byte has been acknowledged, the I²C-bus master issues a stop condition (P).

In READ mode, indicated by setting the read/write bit HIGH, data bytes may be read from the RAM following the slave address acknowledgement. After this acknowledgement the master transmitter becomes a master receiver and the PCF8578 becomes a slave transmitter. The master receiver must acknowledge the reception of each byte in turn. The master receiver must signal an end of data to the slave transmitter, by not generating an acknowledge on the last byte clocked out of the slave. The slave transmitter then leaves the data line HIGH, enabling the master to generate a stop condition (P).

Display bytes are written into, or read from, the RAM at the address specified by the data pointer and subaddress counter. Both the data pointer and subaddress counter are automatically incremented, enabling a stream of data to be transferred either to, or from, the intended devices.

In multiple device applications, the hardware subaddress pins of the PCF8579s (A0 to A3) are connected to V_{SS} or V_{DD} to represent the desired hardware subaddress code. If two or more devices share the same slave address, then each device **must** be allocated a unique hardware subaddress.

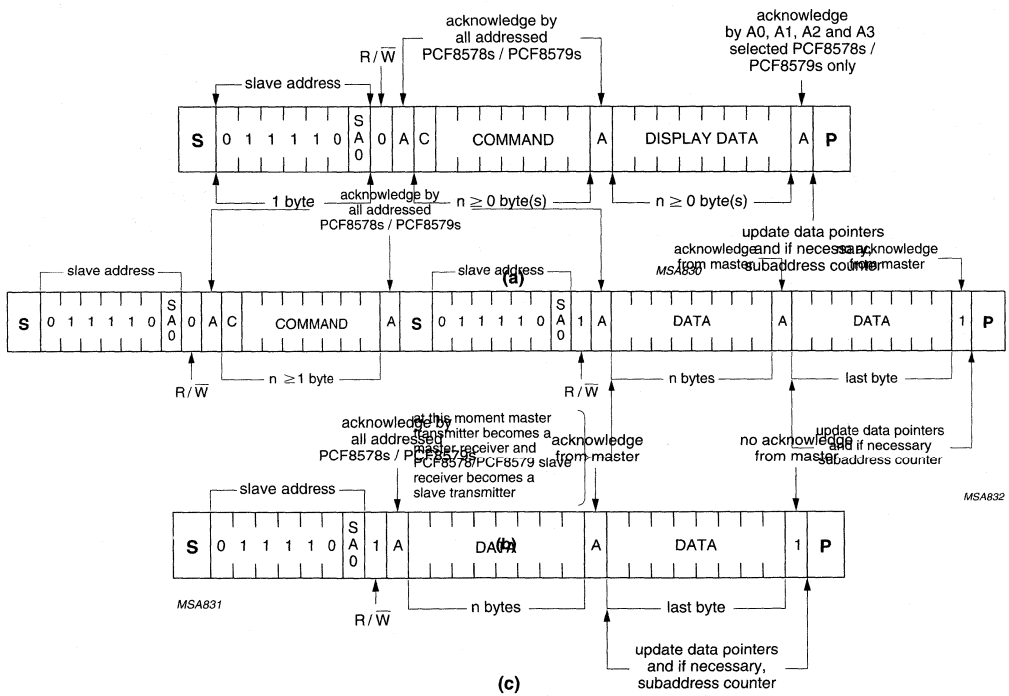
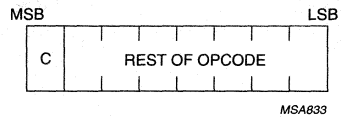


Fig.13 (a) Master transmits to slave receiver (WRITE mode); (b) Master reads after sending command string (WRITE commands; READ data); (c) Master reads slave immediately after sending slave address (READ mode).

8.1 Command decoder

The command decoder identifies command bytes that arrive on the I²C-bus. The most-significant bit of a command is the continuation bit C (see Fig.14). When this bit is set, it indicates that the next byte to be transferred will also be a command. If the bit is reset, it indicates the conclusion of the command transfer. Further bytes will be regarded as display data. Commands are transferred in WRITE mode only.

The five commands available to the PCF8578 are defined in Tables 5 and 6.



C = 0; last command.
C = 1; commands continue.

Fig.14 General information of command byte.

Table 5 Summary of commands

COMMAND	OPCODE(1)								DESCRIPTION
SET MODE	C	1	0	D	D	D	D	D	multiplex rate, display status, system type
SET START BANK	C	1	1	1	1	1	D	D	defines bank at top of LCD
DEVICE SELECT	C	1	1	0	D	D	D	D	defines device subaddress
RAM ACCESS	C	1	1	1	D	D	D	D	graphic mode, bank select (D D D D ≥ 12 is not allowed; see SET START BANK opcode)
LOAD X-ADDRESS	C	0	D	D	D	D	D	D	0 to 39

Note

1. C = command continuation bit. D = may be a logic 1 or 0.

Table 6 Definition of PCF8578/PCF8579 commands

COMMAND	OPCODE								OPTIONS	DESCRIPTION
SET MODE	C	1	0	T	E1	E0	M1	M0	see Table 7	defines LCD drive mode
									see Table 8	defines display status
									see Table 9	defines system type
SET START BANK	C	1	1	1	1	1	B1	B0	see Table 10	defines pointer to RAM bank corresponding to the top of the LCD; useful for scrolling, pseudo-motion and background preparation of new display
DEVICE SELECT	C	1	1	0	A3	A2	A1	A0	see Table 11	four bits of immediate data, bits A0 to A3, are transferred to the subaddress counter to define one of sixteen hardware subaddresses
RAM ACCESS	C	1	1	1	G1	G0	Y1	Y0	see Table 12	defines the auto-increment behaviour of the address for RAM access
									see Table 13	two bits of immediate data, bits Y0 to Y1, are transferred to the X-address pointer to define one of forty display RAM columns
LOAD X-ADDRESS	C	0	X5	X4	X3	X2	X1	X0	see Table 14	six bits of immediate data, bits X0 to X5, are transferred to the X-address pointer to define one of forty display RAM columns

Table 7 Set mode option 1

LCD DRIVE MODE		BITS	
		M1	M0
1 : 8	MUX (8 rows)	0	1
1 : 16	MUX (16 rows)	1	0
1 : 24	MUX (24 rows)	1	1
1 : 32	MUX (32 rows)	0	0

Table 8 Set mode option 2

DISPLAY STATUS	BITS	
	E1	E0
Blank	0	0
Normal	0	1
All segments on	1	0
Inverse video	1	1

Table 9 Set mode option 3

SYSTEM TYPE	BIT T
PCF8578 row only	0
PCF8578 mixed mode	1

Table 10 Set start bank option 1

START BANK POINTER	BITS	
	B1	B0
Bank 0	0	0
Bank 1	0	1
Bank 2	1	0
Bank 3	1	1

Table 11 Device select option 1

DESCRIPTION	BITS			
Decimal value 0 to 15	A3	A2	A1	A0

Table 12 RAM access option 1

RAM ACCESS MODE	BITS	
	G1	G0
Character	0	0
Half-graphic	0	1
Full-graphic	1	0
Not allowed (note 1)	1	1

Note

1. See opcode for SET START BANK in Table 6.

Table 13 Device select option 1

DESCRIPTION	BITS	
Decimal value 0 to 3	Y1	Y0

Table 14 Device select option 1

DESCRIPTION	BITS					
Decimal value 0 to 39	X5	X4	X3	X2	X1	X0

9 CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL) which must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

9.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this moment will be interpreted as control signals.

9.2 Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH, is defined as the STOP condition (P).

9.3 System configuration

A device transmitting a message is a 'transmitter', a device receiving a message is the 'receiver'. The device that controls the message flow is the 'master' and the devices which are controlled by the master are the 'slaves'.

9.4 Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is unlimited. Each data byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal the end of a data transmission to the transmitter by **not** generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

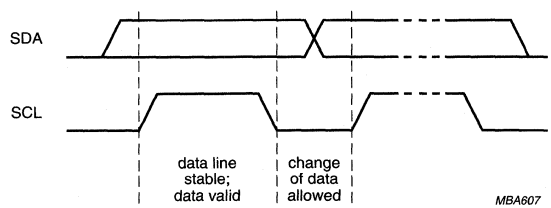


Fig.15 Bit transfer.

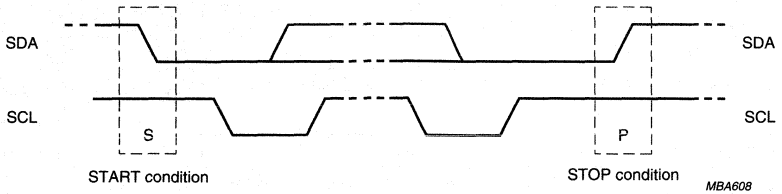


Fig.16 Definition of start and stop condition.

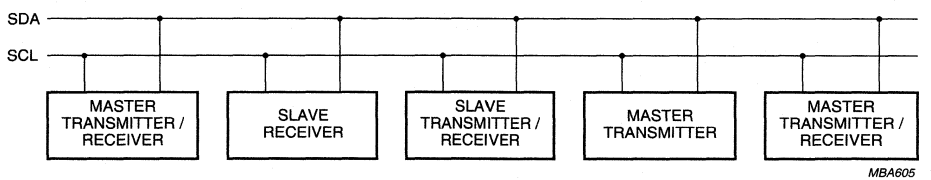
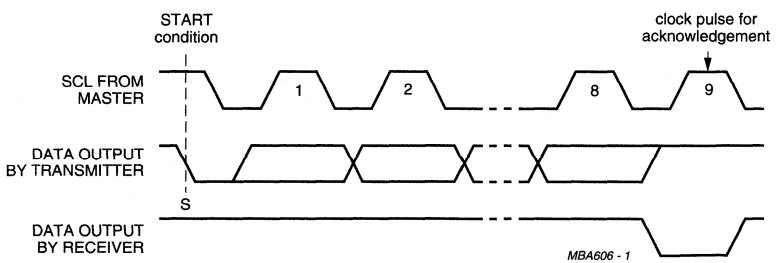


Fig.17 System configuration.



The general characteristics and detailed specification of the I²C-bus are available on request.

Fig.18 Acknowledgement on the I²C-bus.

10 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.5	+8.0	V
V_{LCD}	LCD supply voltage	V_{DD} − 11	V_{DD}	V
V_{I1}	input voltage SDA, SCL, CLK, TEST, SA0 and OSC	V_{SS} − 0.5	V_{DD} + 0.5	V
V_{I2}	input voltage V_2 to V_5	V_{LCD} − 0.5	V_{DD} + 0.5	V
V_{o1}	output voltage $\overline{SYNC}$ and CLK	V_{SS} − 0.5	V_{DD} + 0.5	V
V_{o2}	output voltage R0 to R7, R8/C8 to R31/C31 and C32 to C39	V_{LCD} − 0.5	V_{DD} + 0.5	V
I_I	DC input current	−10	+10	mA
I_O	DC output current	−10	+10	mA
I_{DD}, I_{SS}, I_{LCD}	V_{DD}, V_{SS} or V_{LCD} current	−50	+50	mA
P_{tot}	total power dissipation per package	−	400	mW
P_o	power dissipation per output	−	100	mW
T_{stg}	storage temperature	−65	+150	°C

11 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe it is desirable to take normal precautions appropriate to handling MOS devices. Advice can be found in Data Handbook IC12 under *"Handling MOS Devices"*.

12 DC CHARACTERISTICS

V_{DD} = 2.5 to 6 V; V_{SS} = 0 V; V_{LCD} = V_{DD} − 3.5 V to V_{DD} − 9 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage		2.5	–	6.0	V
V_{LCD}	LCD supply voltage		V_{DD} − 9	–	V_{DD} − 3.5	V
I_{DD1}	supply current external clock	f_{CLK} = 2 kHz; note 1	–	6	15	μA
I_{DD2}	supply current internal clock	R_{OSC} = 330 kΩ	–	20	50	μA
V_{POR}	power-on reset level	note 2	0.8	1.3	1.8	V
Logic						
V_{IL}	LOW level input voltage		V_{SS}	–	0.3V_{DD}	V
V_{IH}	HIGH level input voltage		0.7V_{DD}	–	V_{DD}	V
I_{OL1}	LOW level output current at $\overline{SYNC}$ and CLK	V_{OL} = 1 V; V_{DD} = 5 V	1	–	–	mA
I_{OH1}	HIGH level output current at $\overline{SYNC}$ and CLK	V_{OH} = 4 V; V_{DD} = 5 V	–	–	−1	mA
I_{OL2}	LOW level output current at SDA	V_{OL} = 0.4 V; V_{DD} = 5 V	3	–	–	mA
I_{L1}	leakage current at SDA, SCL, $\overline{SYNC}$, CLK, TEST and SA0	V_i = V_{DD} or V_{SS}	–	–	+1	mA
I_{L2}	leakage current at OSC	V_i = V_{DD}	–	–	+1	μA
C_i	input capacitance at SCL and SDA	note 3	–	–	5	pF
LCD outputs						
I_{L3}	leakage current at V_2 to V_5	V_i = V_{DD} or V_{LCD}	−2	–	+2	μA
V_{DC}	DC component of LCD drivers R0 to R7, R8/C8 to R31/C31 and C32 to C39		–	±20	–	mV
R_{ROW}	output resistance R0 to R7 and R8/C8 to R31/C31	row mode; note 4	–	1.5	3	kΩ
R_{COL}	output resistance R8/C8 to R31/C31 and C32 to C39	column mode; note 4	–	3	6	kΩ

Notes

1. Outputs are open; inputs at V_{DD} or V_{SS}; I^2C-bus inactive; external clock with 50% duty factor.
2. Resets all logic when $V_{DD} < V_{POR}$.
3. Periodically sampled; not 100% tested.
4. Resistance measured between output terminal (R0 to R7, R8/C8 to R31/C31 and C32 to C39) and bias input (V_2 to V_5, V_{DD} and V_{LCD}) when the specified current flows through one output under the following conditions (see Table 2):
   a) $V_{op} = V_{DD} - V_{LCD}$ = 9 V.
   b) Row mode, R0 to R7 and R8/C8 to R31/C31: $V_2 - V_{LCD} \geq 6.65$ V; $V_5 - V_{LCD} \leq 2.35$ V; I_{LOAD} = 150 μA.
   c) Column mode, R8/C8 to R31/C31 and C32 to C39: $V_3 - V_{LCD} \geq 4.70$ V; $V_4 - V_{LCD} \leq 4.30$ V; I_{LOAD} = 100 μA.

13 AC CHARACTERISTICS

All timing values are referenced to V_{IH} and V_{IL} levels with an input voltage swing of V_{SS} to V_{DD}.
V_{DD} = 2.5 to 6 V; V_{SS} = 0 V; V_{LCD} = V_{DD} − 3.5 V to V_{DD} − 9 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{CLK1}	clock frequency at multiplex rates of 1 : 8, 1 : 16 and 1 : 32	R_{OSC} = 330 kΩ; V_{DD} = 6 V	1.2	2.1	3.3	kHz
f_{CLK2}	clock frequency at multiplex rates of 1 : 24	R_{OSC} = 330 kΩ; V_{DD} = 6 V	0.9	1.6	2.5	kHz
t_{PSYNC}	$\overline{SYNC}$ propagation delay		–	–	500	ns
t_{PLCD}	driver delays	V_{DD} − V_{LCD} = 9 V; with test loads	–	–	100	µs
I²C-bus						
f_{SCL}	SCL clock frequency		–	–	100	kHz
t_{SW}	tolerable spike width on bus		–	–	100	ns
t_{BUF}	bus free time		4.7	–	–	µs
$t_{SU;STA}$	start condition set-up time	repeated start codes only	4.7	–	–	µs
$t_{HD;STA}$	start condition hold time		4.0	4.0	–	µs
t_{LOW}	SCL LOW time		4.7	–	–	µs
t_{HIGH}	SCL HIGH time		4.0	–	–	µs
t_r	SCL and SDA rise time		–	–	1	µs
t_f	SCL and SDA fall time		–	–	0.3	µs
$t_{SU;DAT}$	data set-up time		250	–	–	ns
$t_{HD;DAT}$	data hold time		0	–	–	ns
$t_{SU;STO}$	stop condition set-up time		4.0	–	–	µs

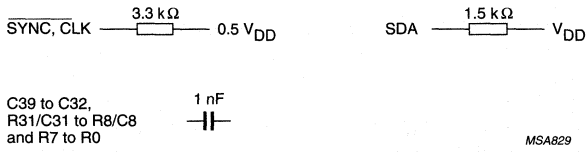


Fig.19 AC test loads.

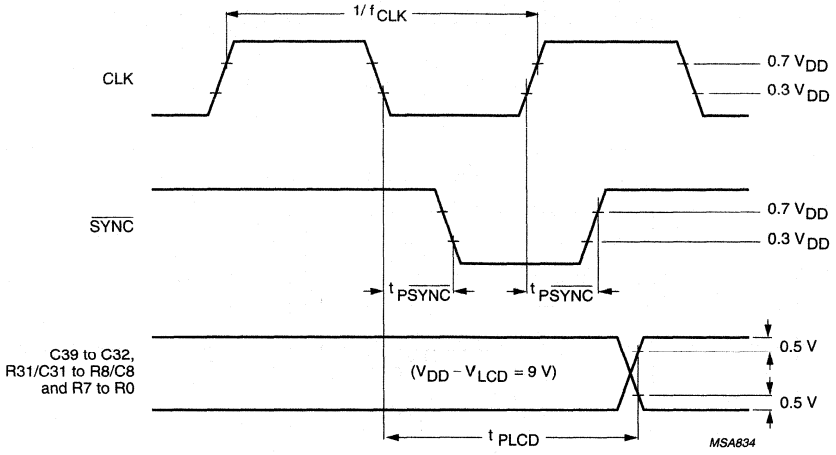


Fig.20 Driver timing waveforms.

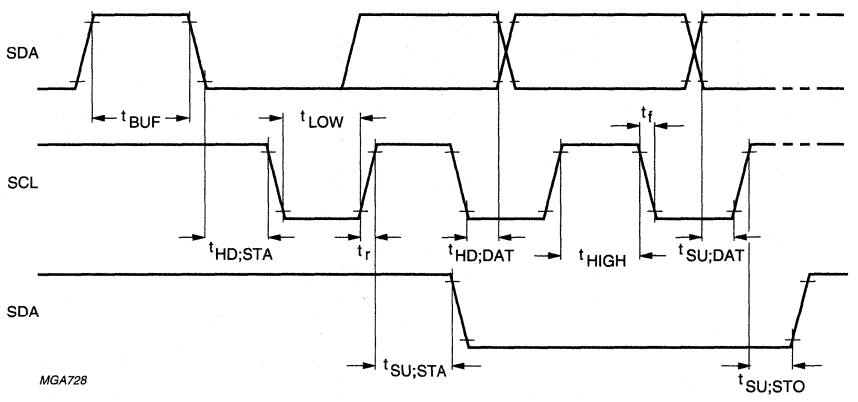


Fig.21 I²C-bus timing waveforms.

14 APPLICATION INFORMATION

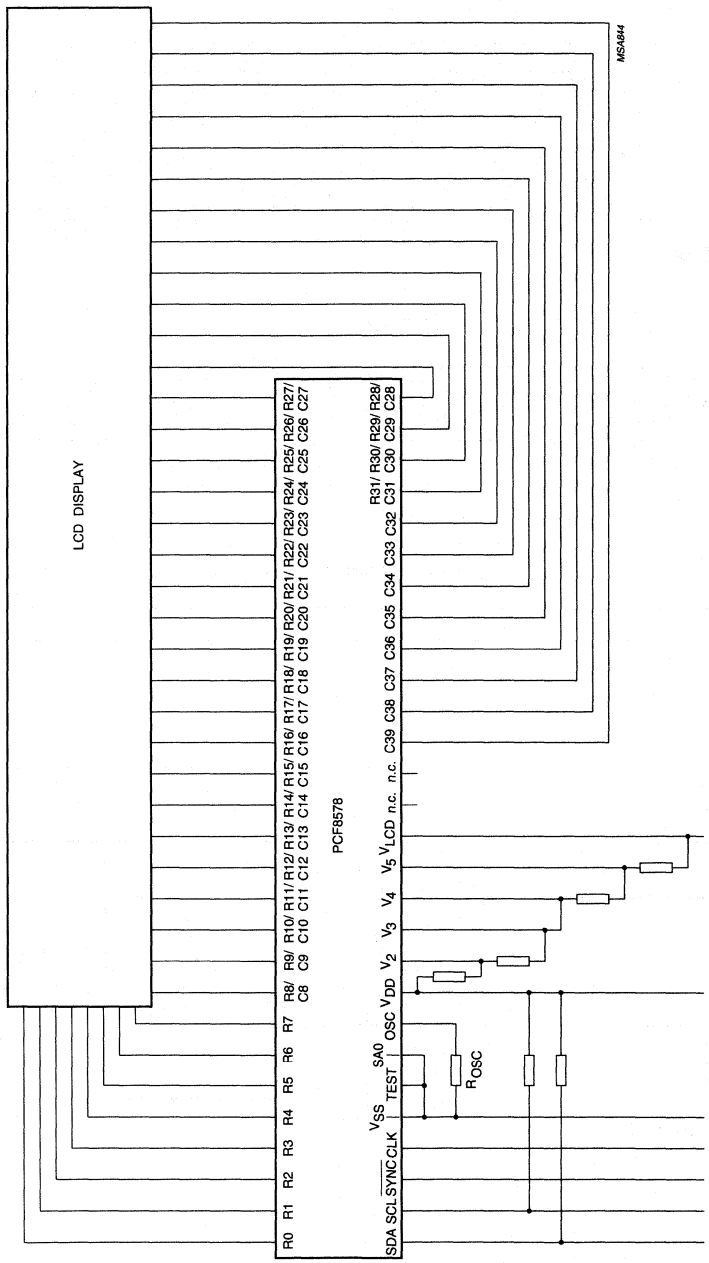


Fig.22 Stand-alone application using 8 rows and 32 columns.

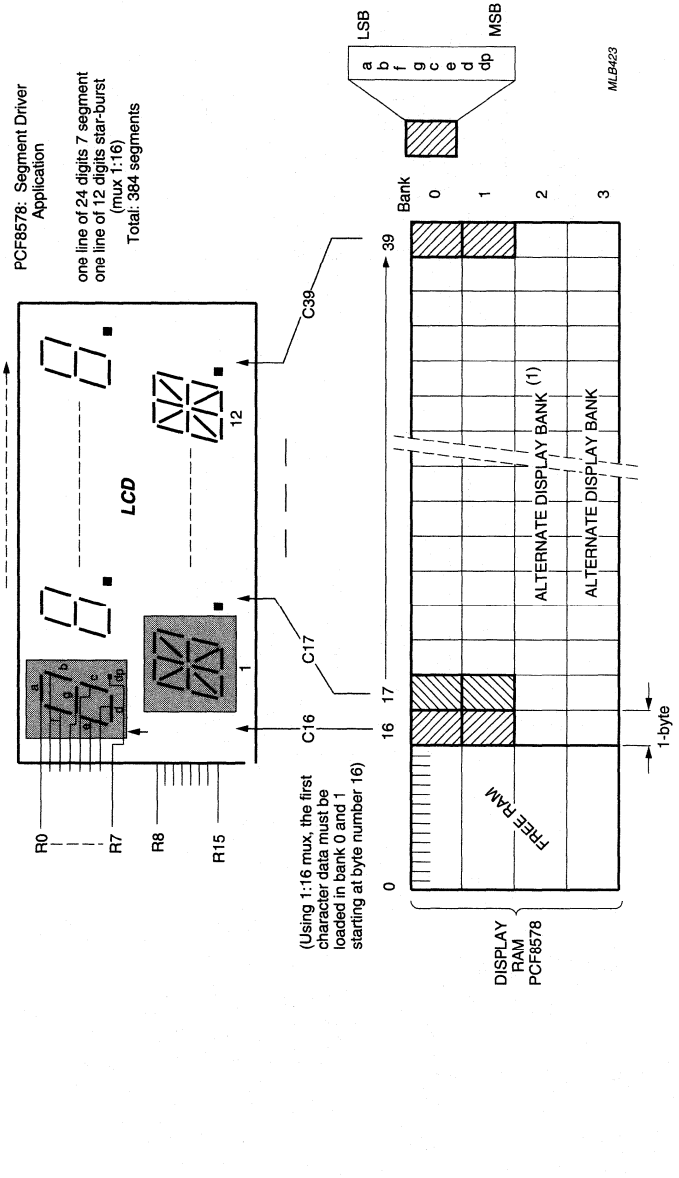


Fig.23 Segment driver application for up to 384 segments.

(1) Can be used for creating blinking characters.

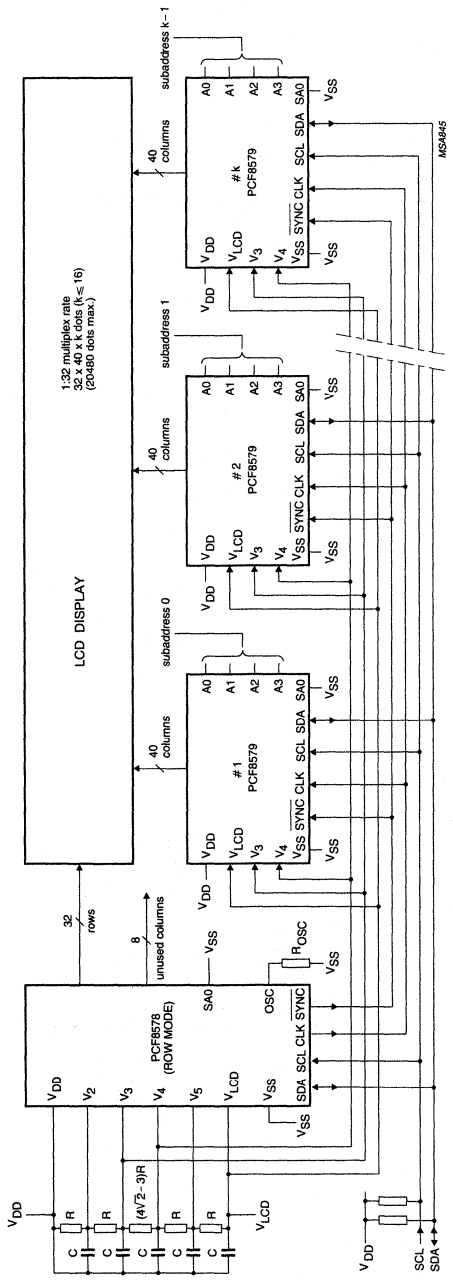


Fig.24 Typical LCD driver system with 1 : 32 multiplex rate.

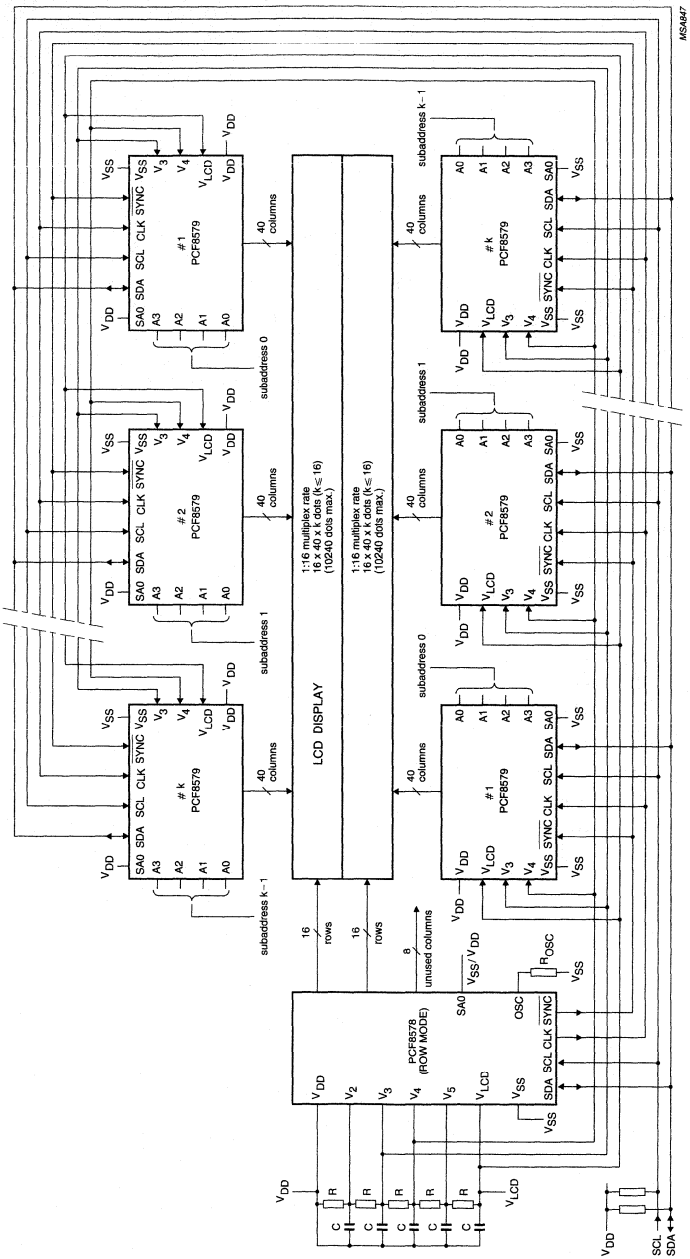


Fig.25 Split screen application with 1 : 16 multiplex rate for improved contrast.

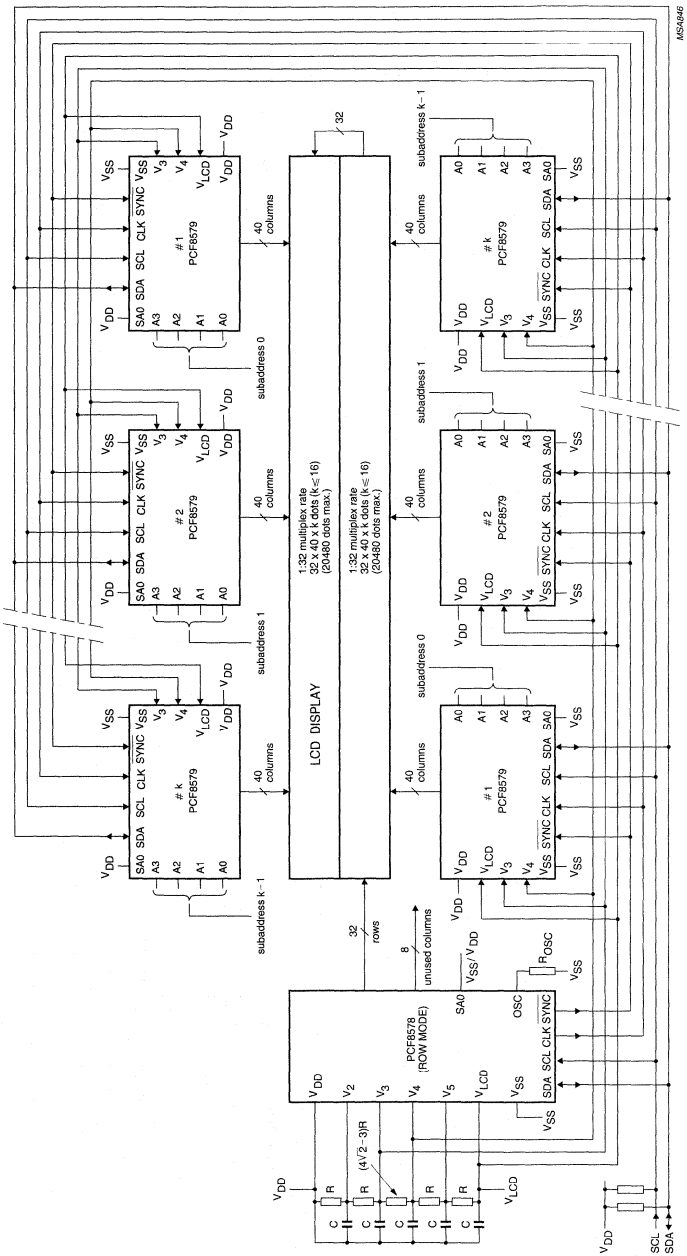


Fig.26 Split screen application with 1 : 32 multiplex rate.

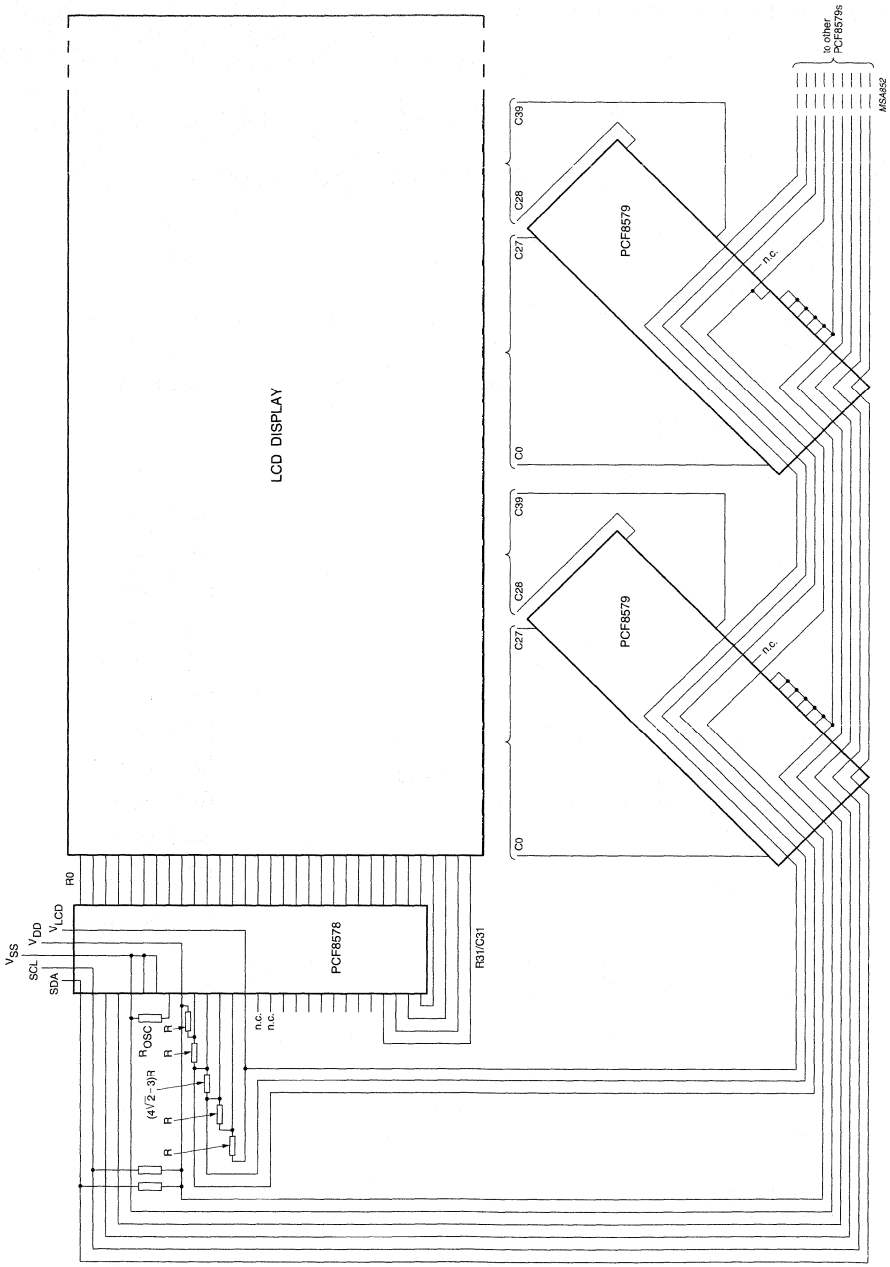
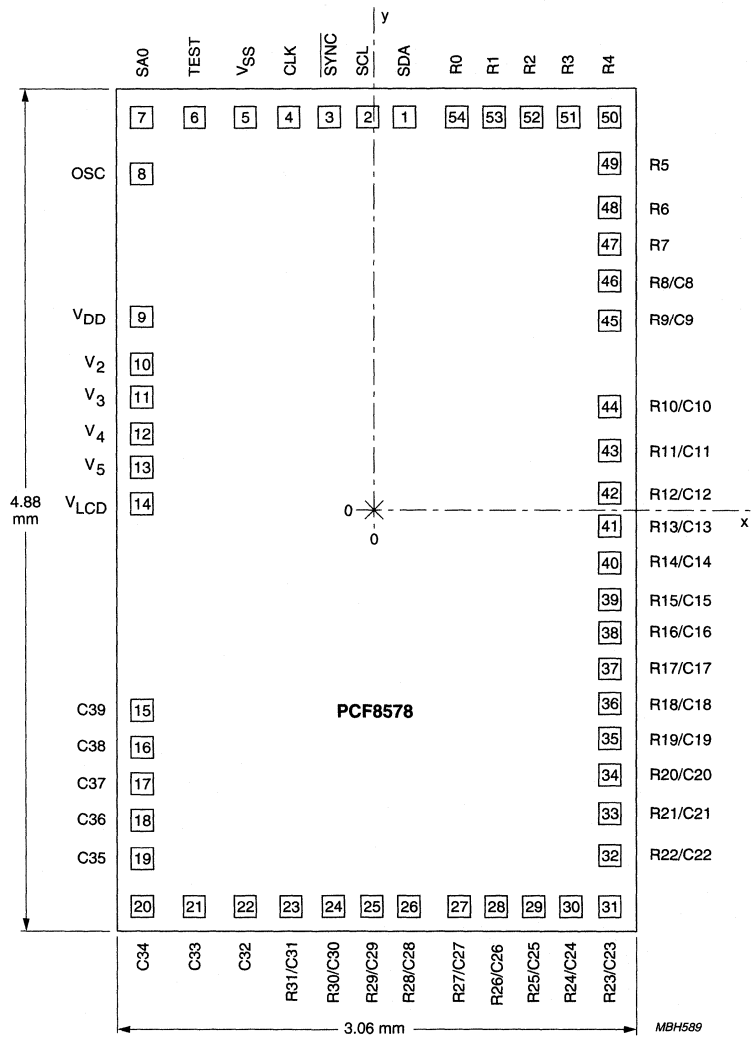


Fig.27 Example of single plane wiring, single screen with 1 : 32 multiplex rate (PCF8578 in row driver mode).

15 CHIP DIMENSIONS AND BONDING PAD LOCATIONS



Chip area: 14.93 mm^2.
Bonding pad dimensions: 120 µm × 120 µm.
The numbers given in the small squares refer to the pad numbers.

Fig.28 Bonding pad locations.

Table 15 Bonding pad locations (dimensions in μm); all x/y coordinates are referenced to centre of chip, see Fig.28

PAD NUMBER	SYMBOL	x	y	PINS	
				VSO56	LQFP64
1	SDA	174	2241	1	7
2	SCL	−30	2241	2	8
3	$\overline{SYNC}$	−234	2241	3	9
4	CLK	−468	2241	4	10
5	V_{SS}	−726	2241	5	11
6	TEST	−1014	2241	6	12
7	SA0	−1308	2241	7	13
8	OSC	−1308	1917	8	16
9	V_{DD}	−1308	1113	9	20
10	V_2	−1308	873	10	21
11	V_3	−1308	663	11	22
12	V_4	−1308	459	12	23
13	V_5	−1308	255	13	24
14	V_{LCD}	−1308	51	14	25
15	C39	−1308	−1149	17	29
16	C38	−1308	−1353	18	30
17	C37	−1308	−1557	19	31
18	C36	−1308	−1773	20	32
19	C35	−1308	−1995	21	33
20	C34	−1308	−2241	22	34
21	C33	−1014	−2241	23	35
22	C32	−726	−2241	24	37
23	R31/C31	−468	−2241	25	38
24	R30/C30	−234	−2241	26	39
25	R29/C29	−30	−2241	27	40
26	R28/C28	174	−2241	28	41
27	R27/C27	468	−2241	29	42
28	R26/C26	672	−2241	30	43
29	R25/C25	876	−2241	31	44
30	R24/C24	1080	−2241	32	45
31	R23/C23	1308	−2241	33	46
32	R22/C22	1308	−1977	34	48
33	R21/C21	1308	−1731	35	49
34	R20/C20	1308	−1515	36	50
35	R19/C19	1308	−1305	37	51
36	R18/C18	1308	−1101	38	52
37	R17/C17	1308	−897	39	53
38	R16/C16	1308	−693	40	54

PAD NUMBER	SYMBOL	x	y	PINS	
				VSO56	LQFP64
39	R15/C15	1308	−489	41	55
40	R14/C14	1308	−285	42	56
41	R13/C13	1308	−81	43	57
42	R12/C12	1308	123	44	58
43	R11/C11	1308	351	45	59
44	R10/C10	1308	603	46	60
45	R9/C9	1308	1101	47	61
46	R8/C8	1308	1305	48	62
47	R7	1308	1515	49	63
48	R6	1308	1731	50	64
49	R5	1308	1977	51	1
50	R4	1308	2241	52	2
51	R3	1080	2241	53	3
52	R2	876	2241	54	4
53	R1	672	2241	55	5
54	R0	468	2241	56	6
–	n.c.	–	–	15, 16	14, 15, 17 to 19, 26 to 28, 36, 47

16 CHIP-ON GLASS INFORMATION

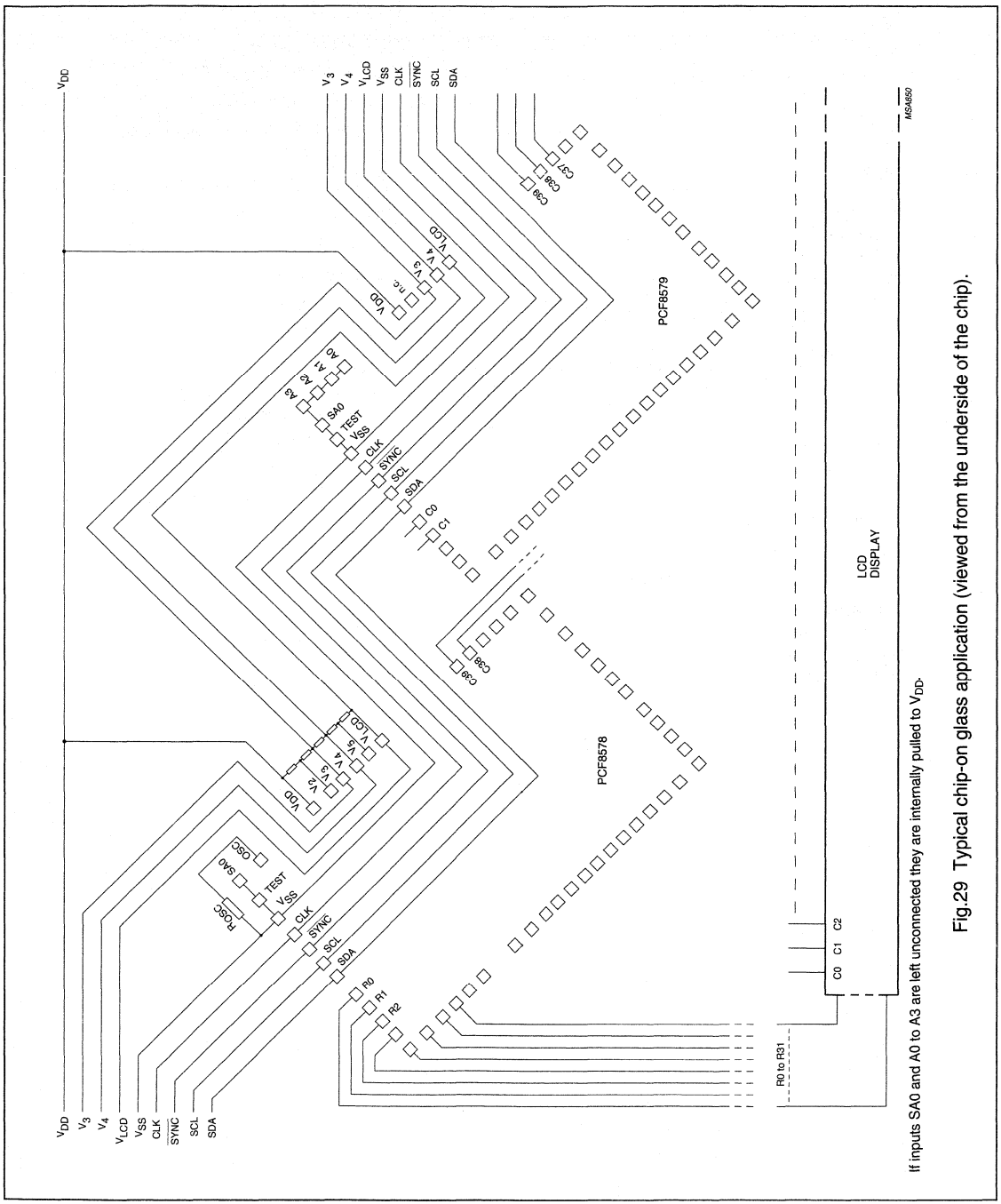


Fig.29 Typical chip-on glass application (viewed from the underside of the chip).

LCD column driver for dot matrix graphic displays

PCF8579

CONTENTS

LCD column driver for dot matrix graphic displays

PCF8579

1 FEATURES

- LCD column driver
- Used in conjunction with the PCF8578, this device forms part of a chip set capable of driving up to 40960 dots
- 40 column outputs
- Selectable multiplex rates; 1 : 8, 1 : 16, 1 : 24 or 1 : 32
- Externally selectable bias configuration, 5 or 6 levels
- Easily cascadable for large applications (up to 32 devices)
- 1280-bit RAM for display data storage
- Display memory bank switching
- Auto-incremented data loading across hardware subaddress boundaries (with PCF8578)
- Power-on reset blanks display
- Logic voltage supply range 2.5 to 6 V
- Maximum LCD supply voltage 9 V
- Low power consumption
- I²C-bus interface
- TTL/CMOS compatible
- Compatible with most microcontrollers
- Optimized pinning for single plane wiring in multiple device applications (with PCF8578)
- Space saving 56-lead plastic mini-pack and 64-pin plastic low profile quad flat package
- Compatible with chip-on-glass technology
- I²C-bus address: 011110 SA0.

2 APPLICATIONS

- Automotive information systems
- Telecommunication systems
- Point-of-sale terminals
- Computer terminals
- Instrumentation.

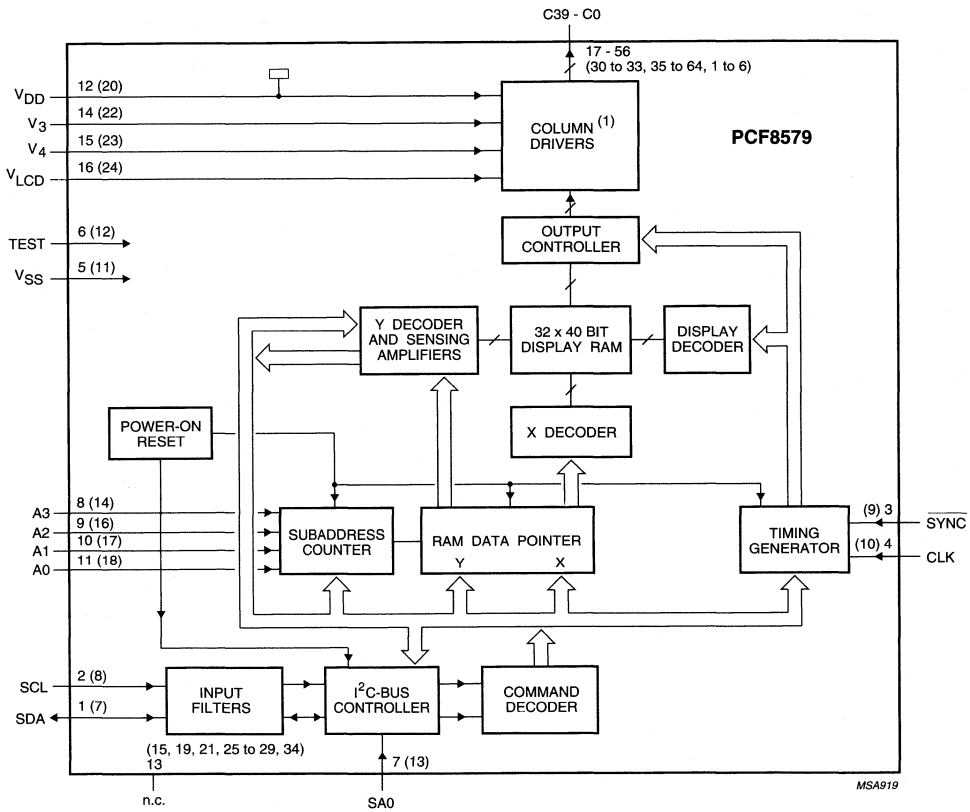
3 GENERAL DESCRIPTION

The PCF8579 is a low power CMOS LCD column driver, designed to drive dot matrix graphic displays at multiplex rates of 1 : 8, 1 : 16, 1 : 24 or 1 : 32. The device has 40 outputs and can drive 32 × 40 dots in a 32 row multiplexed LCD. Up to 16 PCF8579s can be cascaded and up to 32 devices may be used on the same I²C-bus (using the two slave addresses). The device is optimized for use with the PCF8578 LCD row/column driver. Together these two devices form a general purpose LCD dot matrix driver chip set, capable of driving displays of up to 40960 dots. The PCF8579 is compatible with most microcontrollers and communicates via a two-line bidirectional bus (I²C-bus). To allow partial V_{DD} shutdown the ESD protection system of the SCL and SDA pins does not use a diode connected to V_{DD}. Communication overheads are minimized by a display RAM with auto-incremented addressing and display bank switching.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8579T	VSO56	plastic very small outline package; 56 leads	SOT190
PCF8579U7	–	chip with bumps on tape	–
PCF8579H	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2

5 BLOCK DIAGRAM



(1) Operates at LCD voltage levels, all other blocks operate at logic levels.
The pin numbers given in parenthesis refer to the LQFP64 package.

Fig.1 Block diagram.

6 PINNING

SYMBOL	PINS		DESCRIPTION
	VSO56	LQFP64	
SDA	1	7	I²C-bus serial data input/output
SCL	2	8	I²C-bus serial clock input
$\overline{SYNC}$	3	9	cascade synchronization input
CLK	4	10	external clock input
V_{SS}	5	11	ground (logic)
TEST	6	12	test pin (connect to V_{SS})
SA0	7	13	I²C-bus slave address input (bit 0)
A3 to A0	8 to 11	14, 16 to 18	I²C-bus subaddress inputs
V_{DD}	12	20	supply voltage
n.c.	13(1)	15, 19, 21,25 to 29, 34	not connected
V_3, V_4	14 and 15	22 and 23	LCD bias voltage inputs
V_{LCD}	16	24	LCD supply voltage
C39 to C0	17 to 56	30 to 33, 35 to 64 and 1 to 6	LCD column driver outputs

Note

1. Do not connect, this pin is reserved.

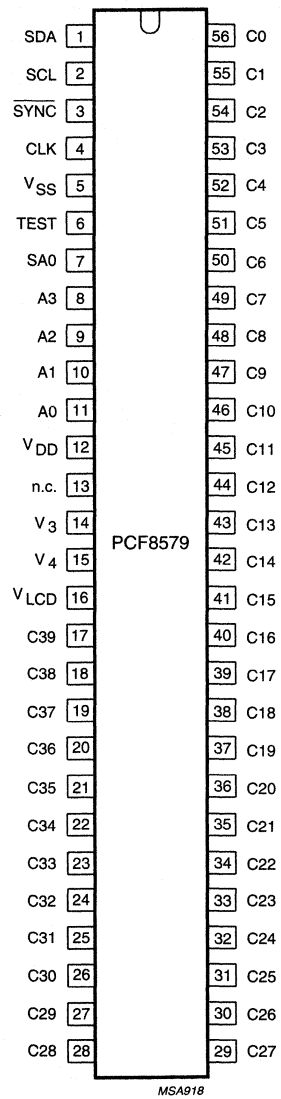


Fig.2 Pin configuration (VSO56).

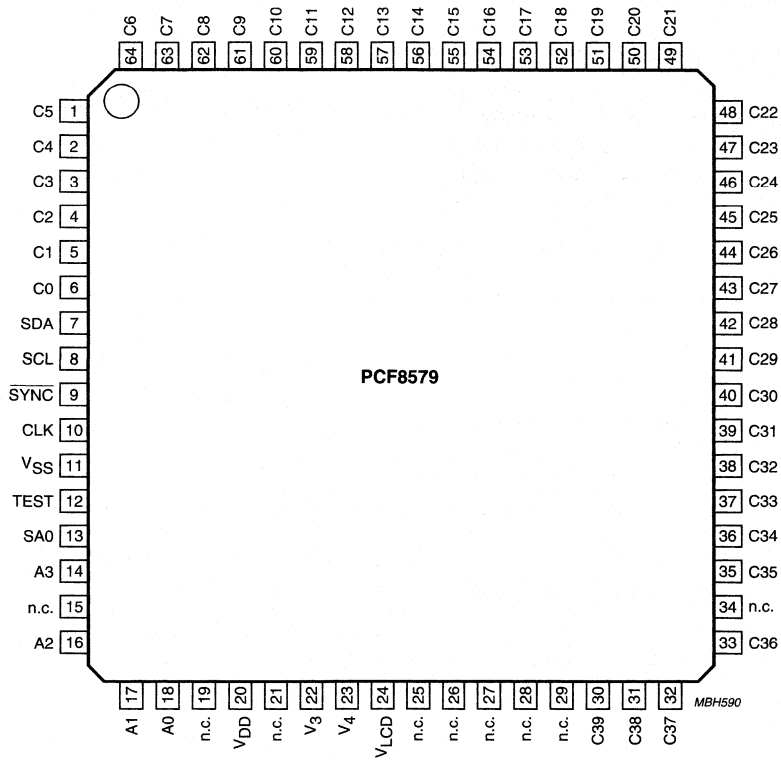


Fig.3 Pin configuration (LQFP64).

7 FUNCTIONAL DESCRIPTION

The PCF8579 column driver is designed for use with the PCF8578. Together they form a general purpose LCD dot matrix chip set.

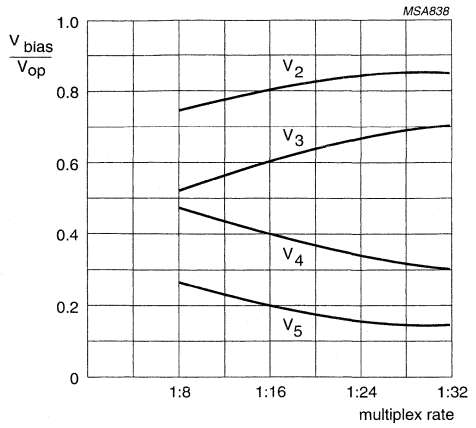
Typically up to 16 PCF8579s may be used with one PCF8578. Each of the PCF8579s is identified by a unique 4-bit hardware subaddress, set by pins A0 to A3. The PCF8578 can operate with up to 32 PCF8579s when using two I²C-bus slave addresses. The two slave addresses are set by the logic level on input SA0.

7.1 Multiplexed LCD bias generation

The bias levels required to produce maximum contrast depend on the multiplex rate and the LCD threshold voltage (V_{th}). V_{th} is typically defined as the RMS voltage at which the LCD exhibits 10% contrast. Table 1 shows the optimum voltage bias levels for the PCF8578/PCF8579 chip set as functions of V_{op} ($V_{op} = V_{DD} - V_{LCD}$), together with the discrimination ratios (D) for the different multiplex rates. A practical value for V_{op} is obtained by equating $V_{off(rms)}$ with V_{th}. Figure 4 shows the first 4 rows of Table 1 as graphs.

Table 1 Optimum LCD bias voltages

PARAMETER	MULTIPLEX RATE			
	1 : 8	1 : 16	1 : 24	1 : 32
$\frac{V_2}{V_{op}}$	0.739	0.800	0.830	0.850
$\frac{V_3}{V_{op}}$	0.522	0.600	0.661	0.700
$\frac{V_4}{V_{op}}$	0.478	0.400	0.339	0.300
$\frac{V_5}{V_{op}}$	0.261	0.200	0.170	0.150
$\frac{V_{off(rms)}}{V_{op}}$	0.297	0.245	0.214	0.193
$\frac{V_{on(rms)}}{V_{op}}$	0.430	0.316	0.263	0.230
$D = \frac{V_{on(rms)}}{V_{off(rms)}}$	1.447	1.291	1.230	1.196
$\frac{V_{op}}{V_{th}}$	3.370	4.080	4.680	5.190



$V_{bias} = V_2, V_3, V_4, V_5$. See Table 1.

Fig.4 V_{bias}/V_{op} as a function of the multiplex rate.

7.2 Power-on reset

At power-on the PCF8579 resets to a defined starting condition as follows:

1. Display blank (in conjunction with PCF8578)
2. 1 : 32 multiplex rate
3. Start bank, 0 selected
4. Data pointer is set to X, Y address 0, 0
5. Character mode
6. Subaddress counter is set to 0
7. I²C-bus is initialized.

Data transfers on the I²C-bus should be avoided for 1 ms following power-on, to allow completion of the reset action.

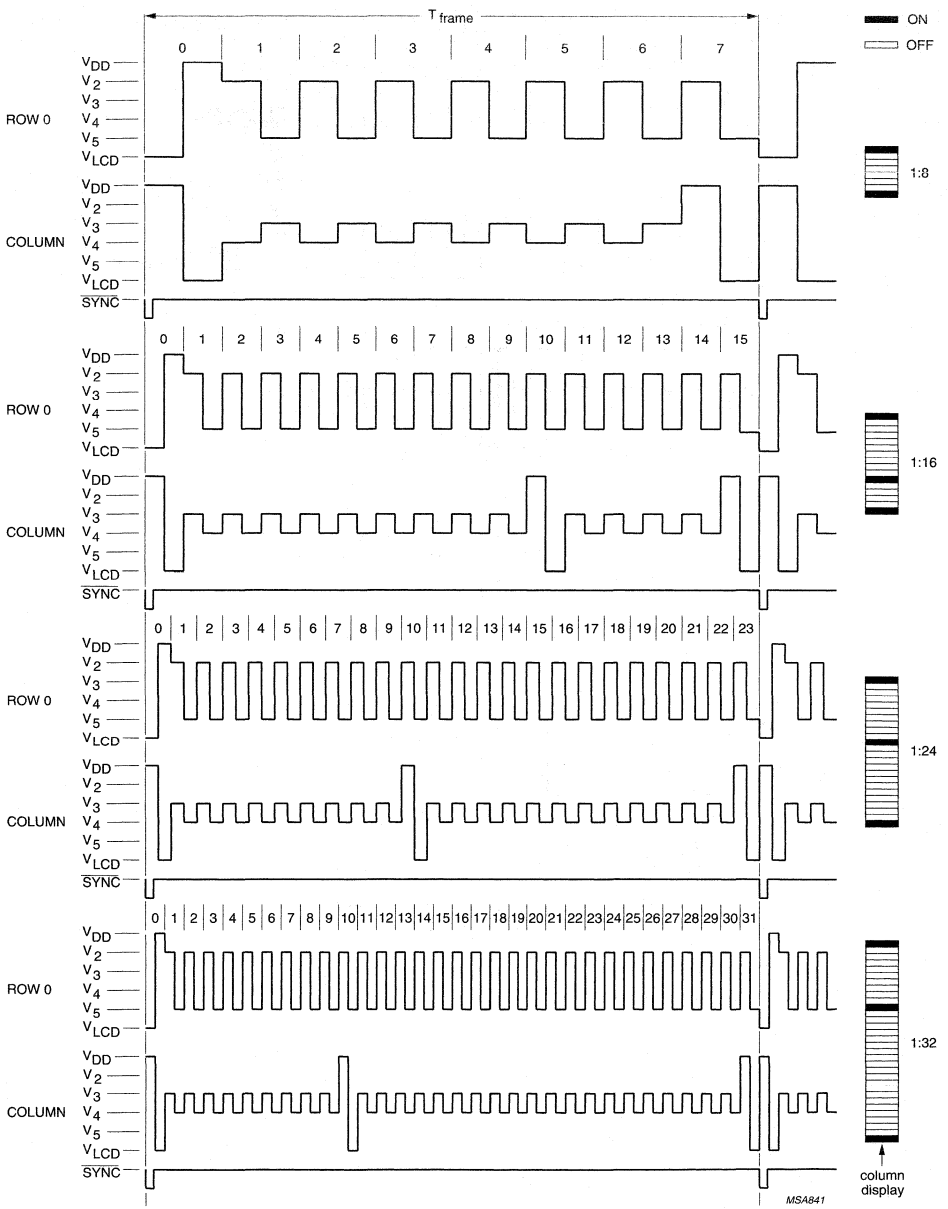
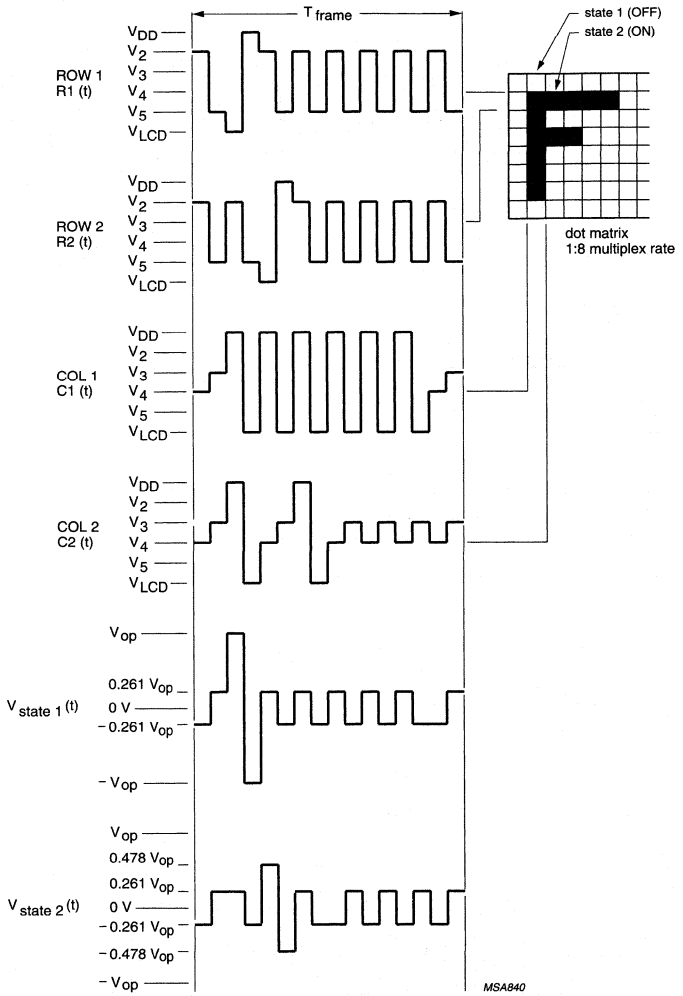


Fig.5 LCD row/column waveforms.



$V_{state\ 1}(t) = C1(t) - R1(t)$:

$$\frac{V_{on(rms)}}{V_{op}} = \sqrt{\frac{1}{8} + \frac{\sqrt{8}-1}{8(\sqrt{8}+1)}} = 0.430$$

$V_{state\ 2}(t) = C2(t) - R2(t)$:

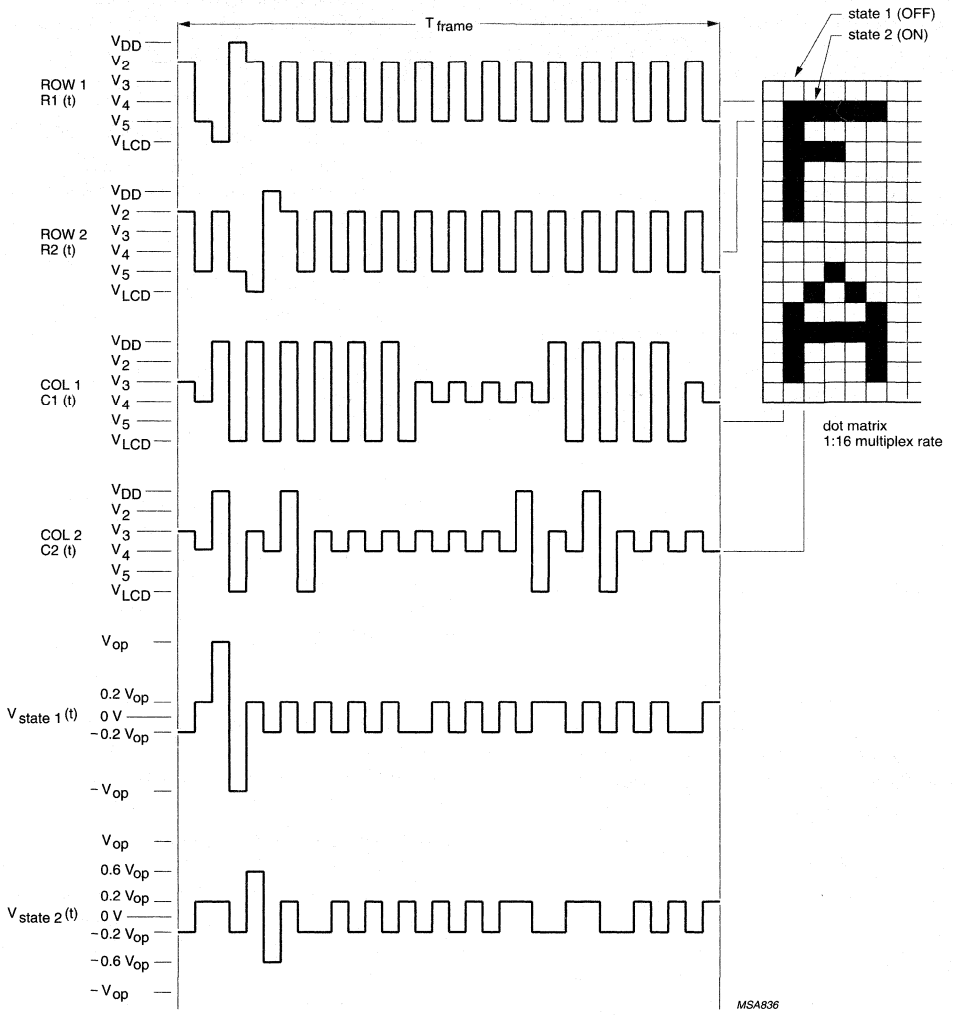
$$\frac{V_{off(rms)}}{V_{op}} = \sqrt{\frac{2(\sqrt{8}-1)}{\sqrt{8}(\sqrt{8}+1)^2}} = 0.297$$

general relationship (n = multiplex rate)

$$\frac{V_{on(rms)}}{V_{op}} = \sqrt{\frac{1}{n} + \frac{\sqrt{n}-1}{n(\sqrt{n}+1)}}$$

$$\frac{V_{off(rms)}}{V_{op}} = \sqrt{\frac{2(\sqrt{n}-1)}{\sqrt{n}(\sqrt{n}+1)^2}}$$

Fig.6 LCD drive mode waveforms for 1 : 8 multiplex rate.



$V_{state\ 1}(t) = C1(t) - R1(t)$:

$$\frac{V_{on(rms)}}{V_{op}} = \sqrt{\frac{1}{16} + \frac{\sqrt{16}-1}{16(\sqrt{16}+1)}} = 0.316$$

$V_{state\ 2}(t) = C2(t) - R2(t)$:

$$\frac{V_{off(rms)}}{V_{op}} = \sqrt{\frac{2(\sqrt{16}-1)}{\sqrt{16}(\sqrt{16}+1)^2}} = 0.254$$

general relationship (n = multiplex rate)

$$\frac{V_{on(rms)}}{V_{op}} = \sqrt{\frac{1}{n} + \frac{\sqrt{n}-1}{n(\sqrt{n}+1)}}$$

$$\frac{V_{off(rms)}}{V_{op}} = \sqrt{\frac{2(\sqrt{n}-1)}{\sqrt{n}(\sqrt{n}+1)^2}}$$

Fig.7 LCD drive mode waveforms for 1 : 16 multiplex rate.sa.

7.3 Timing generator

The timing generator of the PCF8579 organizes the internal data flow from the RAM to the display drivers. An external synchronization pulse $\overline{SYNC}$ is received from the PCF8578. This signal maintains the correct timing relationship between cascaded devices.

7.4 Column drivers

Outputs C0 to C39 are column drivers which must be connected to the LCD. Unused outputs should be left open-circuit.

7.5 Display RAM

The PCF8579 contains a 32×40-bit static RAM which stores the display data. The RAM is divided into 4 banks of 40 bytes ($4 \times 8 \times 40$ bits). During RAM access, data is transferred to/from the RAM via the I^2C-bus.

7.6 Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows an individual data byte or a series of data bytes to be written into, or read from, the display RAM, controlled by commands sent on the I^2C-bus.

7.7 Subaddress counter

The storage and retrieval of display data is dependent on the content of the subaddress counter. Storage and retrieval take place only when the contents of the subaddress counter agree with the hardware subaddress at pins A0, A1, A2 and A3.

7.8 I^2C-bus controller

The I^2C-bus controller detects the I^2C-bus protocol, slave address, commands and display data bytes. It performs the conversion of the data input (serial-to-parallel) and the data output (parallel-to-serial). The PCF8579 acts as an I^2C-bus slave transmitter/receiver. Device selection depends on the I^2C-bus slave address, the hardware subaddress and the commands transmitted.

7.9 Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

7.10 RAM access

There are three RAM ACCESS modes:

- Character
- Half-graphic
- Full-graphic.

These modes are specified by bits G1 and G0 of the RAM ACCESS command. The RAM ACCESS command controls the order in which data is written to or read from the RAM (see Fig.8).

To store RAM data, the user specifies the location into which the first byte will be loaded (see Fig.9):

- Device subaddress (specified by the DEVICE SELECT command)
- RAM X-address (specified by the LOAD X-ADDRESS command)
- RAM bank (specified by bits Y1 and Y0 of the RAM ACCESS command).

Subsequent data bytes will be written or read according to the chosen RAM access mode. Device subaddresses are automatically incremented between devices until the last device is reached. If the last device has subaddress 15, further display data transfers will lead to a wrap-around of the subaddress to 0.

7.11 Display control

The display is generated by continuously shifting rows of RAM data to the dot matrix LCD via the column outputs. The number of rows scanned depends on the multiplex rate set by bits M1 and M0 of the SET MODE command.

The display status (all dots on/off and normal/inverse video) is set by bits E1 and E0 of the SET MODE command. For bank switching, the RAM bank corresponding to the top of the display is set by bits B1 and B0 of the SET START BANK command. This is shown in Fig.10 This feature is useful when scrolling in alphanumeric applications.

7.12 TEST pin

The TEST pin must be connected to V_{SS}.

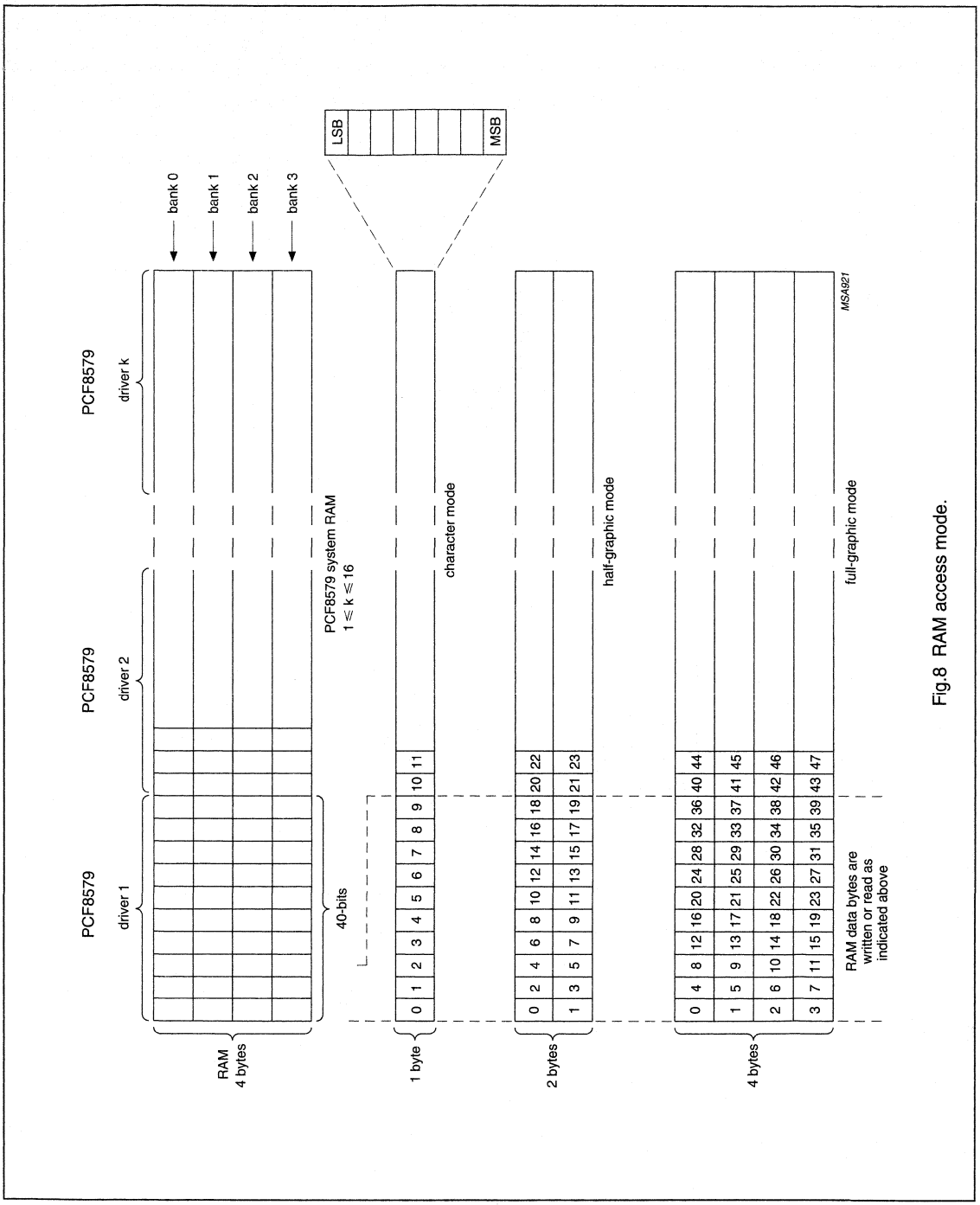


Fig.8 RAM access mode.

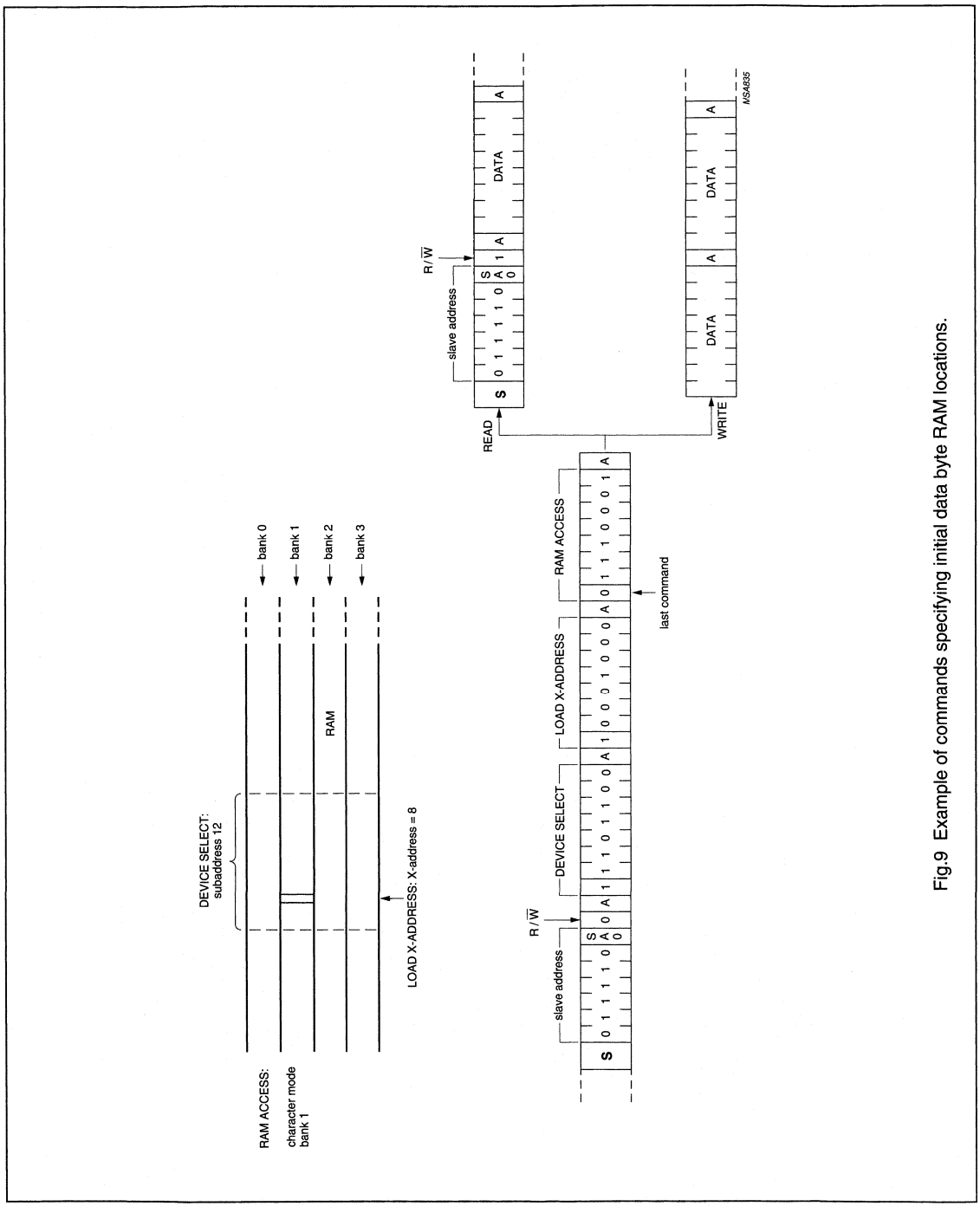


Fig.9 Example of commands specifying initial data byte RAM locations.

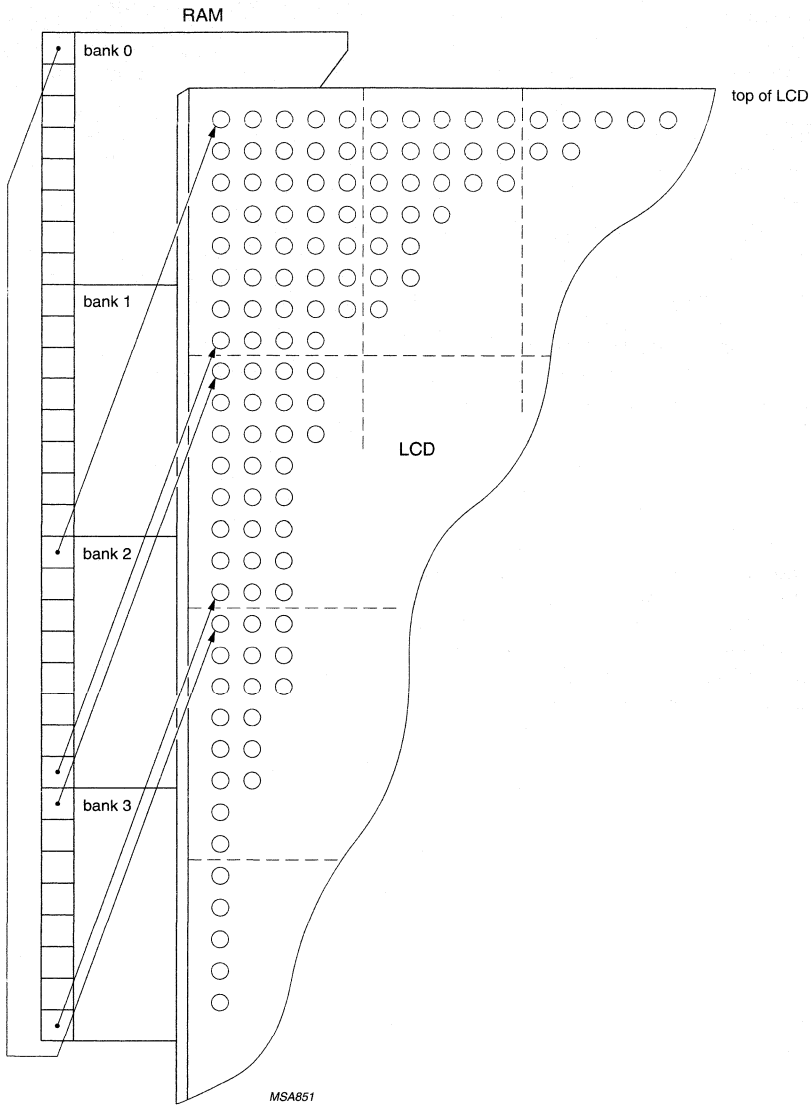


Fig.10 Relationship between display and SET START BANK; 1 : 32 multiplex rate and start bank = 2.

8 I²C-BUS PROTOCOL

Two 7-bit slave addresses (0111100 and 0111101) are reserved for both the PCF8578 and PCF8579. The least significant bit of the slave address is set by connecting input SA0 to either logic 0 (V_{SS}) or logic 1 (V_{DD}). Therefore, two types of PCF8578 or PCF8579 can be distinguished on the same I²C-bus which allows:

1. One PCF8578 to operate with up to 32 PCF8579s on the same I²C-bus for very large applications.
2. The use of two types of LCD multiplex schemes on the same I²C-bus.

In most applications the PCF8578 will have the same slave address as the PCF8579.

The I²C-bus protocol is shown in Fig.11.
All communications are initiated with a start condition (S) from the I²C-bus master, which is followed by the desired slave address and read/write bit. All devices with this slave address acknowledge in parallel. All other devices ignore the bus transfer.

In WRITE mode (indicated by setting the read/write bit LOW) one or more commands follow the slave address acknowlegement. The commands are also acknowledged by all addressed devices on the bus.
The last command must clear the continuation bit C. After the last command a series of data bytes may follow.
The acknowlegement after each byte is made only by the (A0, A1, A2 and A3) addressed PCF8579 or PCF8578 with its implicit subaddress 0. After the last data byte has been acknowledged, the I²C-bus master issues a stop condition (P).

In READ mode, indicated by setting the read/write bit HIGH, data bytes may be read from the RAM following the slave address acknowlegement. After this acknowlegement the master transmitter becomes a master receiver and the PCF8579 becomes a slave transmitter. The master receiver must acknowledge the reception of each byte in turn. The master receiver must signal an end of data to the slave transmitter, by **not** generating an acknowledge on the last byte clocked out of the slave. The slave transmitter then leaves the data line HIGH, enabling the master to generate a stop condition (P).

Display bytes are written into, or read from, the RAM at the address specified by the data pointer and subaddress counter. Both the data pointer and subaddress counter are automatically incremented, enabling a stream of data to be transferred either to, or from, the intended devices.

In multiple device applications, the hardware subaddress pins of the PCF8579s (A0 to A3) are connected to V_{SS} or V_{DD} to represent the desired hardware subaddress code. If two or more devices share the same slave address, then each device **must** be allocated a unique hardware subaddress.

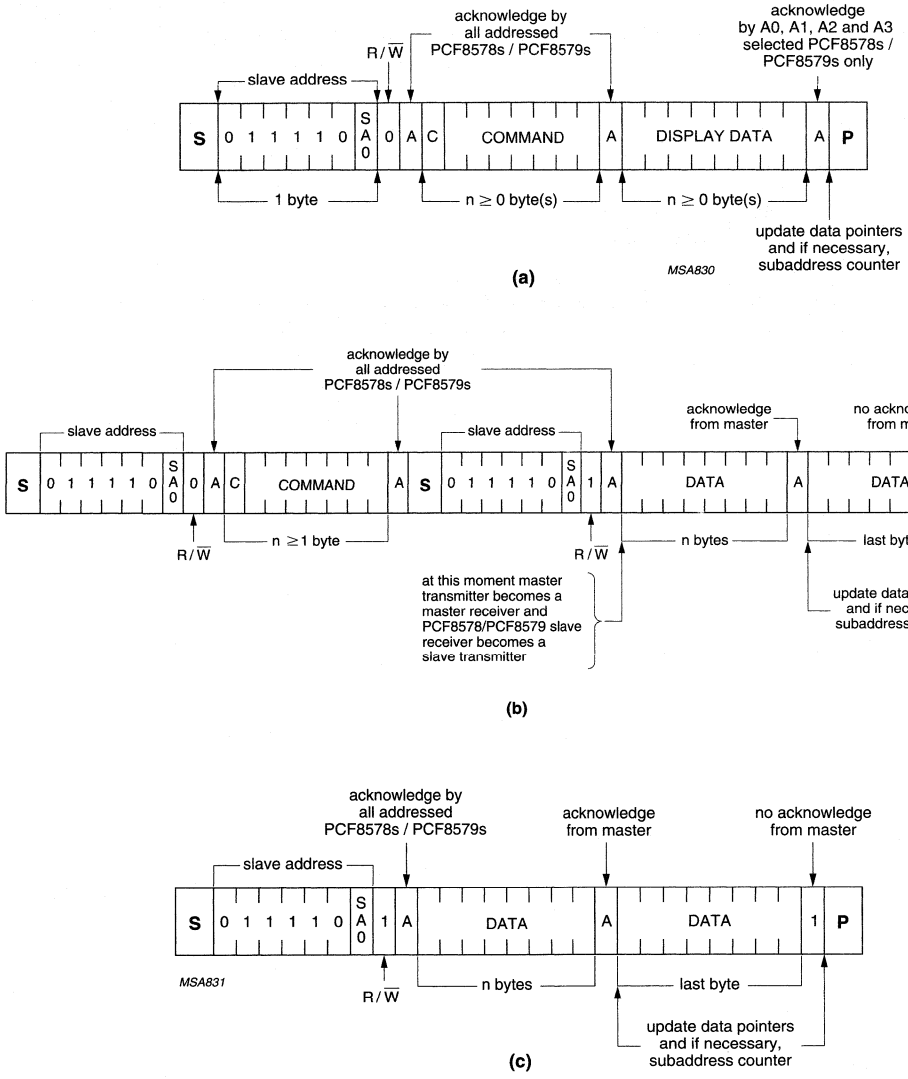
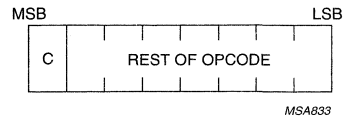


Fig.11 (a) Master transmits to slave receiver (WRITE mode); (b) Master reads after sending command string (WRITE commands; READ data); (c) Master reads slave immediately after sending slave address (READ mode).

8.1 Command decoder

The command decoder identifies command bytes that arrive on the I²C-bus. The most significant bit of a command is the continuation bit C (see Fig.12). When this bit is set, it indicates that the next byte to be transferred will also be a command. If the bit is reset, it indicates the conclusion of the command transfer. Further bytes will be regarded as display data. Commands are transferred in WRITE mode only.

The five commands available to the PCF8579 are defined in Tables 2 and 3.



C = 0; last command.
C = 1; commands continue.

Fig.12 General format of command byte.

Table 2 Summary of commands

COMMAND	OPCODE(1)								DESCRIPTION
SET MODE	C	1	0	D	D	D	D	D	multiplex rate, display status, system type
SET START BANK	C	1	1	1	1	1	D	D	defines bank at top of LCD
DEVICE SELECT	C	1	1	0	D	D	D	D	defines device subaddress
RAM ACCESS	C	1	1	1	D	D	D	D	graphic mode, bank select (D D D D ≥ 12 is not allowed; see SET START BANK opcode)
LOAD X-ADDRESS	C	0	D	D	D	D	D	D	0 to 39

Note

1. C = command continuation bit. D = may be a logic 1 or 0.

Table 3 Definition of PCF8578/PCF8579 commands

COMMAND	OPCODE								OPTIONS	DESCRIPTION
SET MODE	C	1	0	T	E1	E0	M1	M0	see Table 4	defines LCD drive mode
									see Table 5	defines display status
									see Table 6	defines system type
SET START BANK	C	1	1	1	1	1	B1	B0	see Table 7	defines pointer to RAM bank corresponding to the top of the LCD; useful for scrolling, pseudo motion and background preparation of new display
DEVICE SELECT	C	1	1	0	A3	A2	A1	A0	see Table 8	four bits of immediate data, bits A0 to A3, are transferred to the subaddress counter to define one of sixteen hardware subaddresses
RAM ACCESS	C	1	1	1	G1	G0	Y1	Y0	see Table 9	defines the auto-increment behaviour of the address for RAM access
									see Table 10	two bits of immediate data, bits Y0 to Y1, are transferred to the X-address pointer to define one of forty display RAM columns
LOAD X-ADDRESS	C	0	X5	X4	X3	X2	X1	X0	see Table 11	six bits of immediate data, bits X0 to X5, are transferred to the X-address pointer to define one of forty display RAM columns

Table 4 Set mode option 1

LCD DRIVE MODE		BITS	
		M1	M0
1 : 8	MUX (8 rows)	0	1
1 : 16	MUX (16 rows)	1	0
1 : 24	MUX (24 rows)	1	1
1 : 32	MUX (32 rows)	0	0

Table 5 Set mode option 2

DISPLAY STATUS	BITS	
	E1	E0
Blank	0	0
Normal	0	1
All segments on	1	0
Inverse video	1	1

Table 6 Set mode option 3

SYSTEM TYPE	BIT T
PCF8578 row only	0
PCF8578 mixed mode	1

Table 7 Set start bank option 1

START BANK POINTER	BITS	
	B1	B0
Bank 0	0	0
Bank 1	0	1
Bank 2	1	0
Bank 3	1	1

Table 8 Device select option 1

DESCRIPTION	BITS			
Decimal value of 0 to 15	A3	A2	A1	A0

Table 9 RAM access option 1

RAM ACCESS MODE	BITS	
	G1	G0
Character	0	0
Half-graphic	0	1
Full-graphic	1	0
Not allowed (note 1)	1	1

Note

1. See opcode for SET START BANK in Table 3.

Table 10 RAM access option 2

DESCRIPTION	BITS	
Decimal value of 0 to 3	Y1	Y0

Table 11 Load X-address option 1

DESCRIPTION	BITS					
Decimal value of 0 to 39	X5	X4	X3	X2	X1	X0

9 CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL) which must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

9.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this moment will be interpreted as control signals.

9.2 Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the start condition (S).
A LOW-to-HIGH transition of the data line while the clock is HIGH, is defined as the stop condition (P).

9.3 System configuration

A device transmitting a message is a 'transmitter', a device receiving a message is the 'receiver'. The device that controls the message flow is the 'master' and the devices which are controlled by the master are the 'slaves'.

9.4 Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is unlimited. Each data byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse.
A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal the end of a data transmission to the transmitter by **not** generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

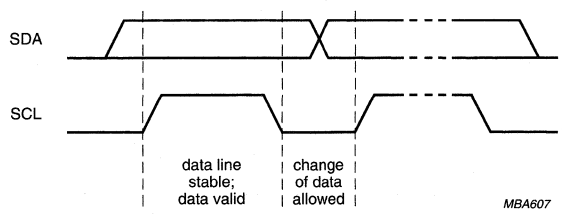


Fig.13 Bit transfer.

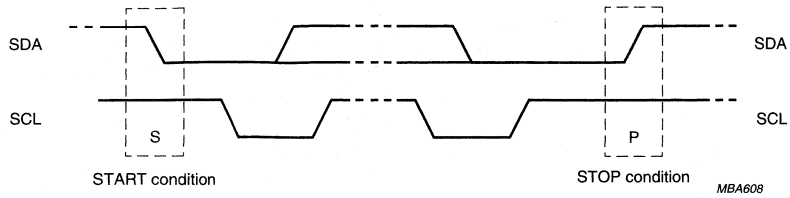


Fig.14 Definition of start and stop condition.

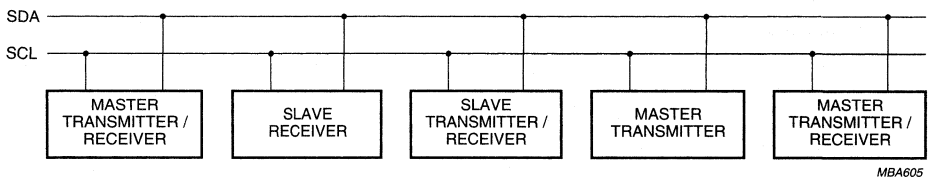
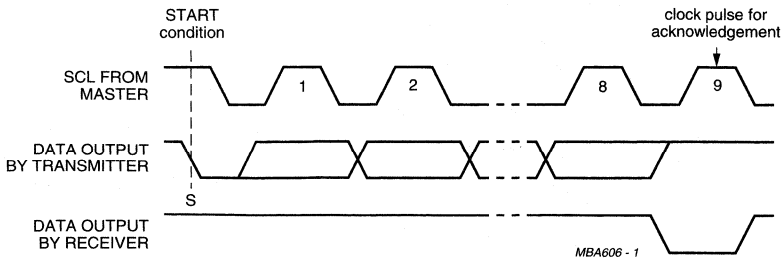


Fig.15 System configuration.



The general characteristics and detailed specification of the I²C-bus are available on request.

Fig.16 Acknowledgement on the I²C-bus.

10 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.5	+8.0	V
V_{LCD}	LCD supply voltage	V_{DD} − 11	V_{DD}	V
V_{i1}	input voltage pins SDA, SCL, $\overline{SYNC}$, CLK, TEST, SA0, A0, A1, A2 and A3	V_{SS} − 0.5	V_{DD} + 0.5	V
V_{i2}	input voltage pins V_3 and V_4	V_{LCD} − 0.5	V_{DD} + 0.5	V
V_{o1}	output voltage pin SDA	V_{SS} − 0.5	V_{DD} + 0.5	V
V_{o2}	output voltage pins C0 to C39	V_{LCD} − 0.5	V_{DD} + 0.5	V
I_I	DC input current	−10	+10	mA
I_O	DC output current	−10	+10	mA
I_{DD}, I_{SS}, I_{LCD}	current at pins V_{DD}, V_{SS} or V_{LCD}	−50	+50	mA
P_{tot}	total power dissipation per package	−	400	mW
P_o	power dissipation per output	−	100	mW
T_{stg}	storage temperature	−65	+150	°C

11 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe it is desirable to take normal precautions appropriate to handling MOS devices. Advice can be found in Data Handbook IC12 under *"Handling MOS Devices"*.

12 DC CHARACTERISTICS

V_{DD} = 2.5 to 6 V; V_{SS} = 0 V; V_{LCD} = V_{DD} − 3.5 V to V_{DD} − 9 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage		2.5	–	6.0	V
V_{LCD}	LCD supply voltage		V_{DD} − 9	–	V_{DD} − 3.5	V
I_{DD}	supply current	f_{CLK} = 2 kHz; note 1	–	9	20	μA
V_{POR}	power-on reset level	note 2	–	1.3	1.8	V
Logic						
V_{IL}	LOW level input voltage		V_{SS}	–	0.3V_{DD}	V
V_{IH}	HIGH level input voltage		0.7V_{DD}	–	V_{DD}	V
I_{LI1}	leakage current at pins SDA, SCL, $\overline{SYNC}$, CLK, TEST, SA0, A0, A1, A2 and A3	V_i = V_{DD} or V_{SS}	−1	–	+1	μA
I_{OL}	LOW level output current at pin SDA	V_{OL} = 0.4 V; V_{DD} = 5 V	3	–	–	mA
C_i	input capacitance	note 3	–	–	5	pF
LCD outputs						
I_{LI2}	leakage current at pins V_3 to V_4	V_i = V_{DD} or V_{LCD}	−2	–	+2	μA
V_{DC}	DC component of LCD drivers pins C0 to C39		–	±20	–	mV
R_{COL}	output resistance at pins C0 to C39	note 4	–	3	6	kΩ

Notes

1. Outputs are open; inputs at V_{DD} or V_{SS}; I²C-bus inactive; clock with 50% duty factor.
2. Resets all logic when V_{DD} < V_{POR}.
3. Periodically sampled; not 100% tested.
4. Resistance measured between output terminal (C0 to C39) and bias input (V_3, V_4, V_{DD} and V_{LCD}) when the specified current flows through one output under the following conditions (see Table 1):
   a) $-V_{op} = V_{DD} - V_{LCD}$ = 9 V;
   b) $-V_3 - V_{LCD} \geq 4.70$ V; $V_4 - V_{LCD} \leq 4.30$ V; I_{LOAD} = 100 μA.

13 AC CHARACTERISTICS

All timing values are referred to V_{IH} and V_{IL} levels with an input voltage swing of V_{SS} to V_{DD}.
V_{DD} = 2.5 to 6 V; V_{SS} = 0 V; V_{LCD} = V_{DD} − 3.5 V to V_{DD} − 9 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{clk}	clock frequency	50% duty factor	–	note 1	10	kHz
t_{PLCD}	driver delays	V_{DD} − V_{LCD} = 9 V; with test loads	–	–	100	µs
I²C-bus						
f_{SCL}	SCL clock frequency		–	–	100	kHz
t_{SW}	tolerable spike width on bus		–	–	100	ns
t_{BUF}	bus free time		4.7	–	–	µs
$t_{SU;STA}$	START condition set-up time	repeated start codes only	4.7	–	–	µs
$t_{HD;STA}$	START condition hold time		4.0	–	–	µs
t_{LOW}	SCL LOW time		4.7	–	–	µs
t_{HIGH}	SCL HIGH time		4.0	–	–	µs
t_r	SCL and SDA rise time		–	–	1.0	µs
t_f	SCL and SDA fall time		–	–	0.3	µs
$t_{SU;DAT}$	data set-up time		250	–	–	ns
$t_{HD;DAT}$	data hold time		0	–	–	ns
$t_{SU;STO}$	STOP condition set-up time		4.0	–	–	µs

Note

1. Typically 0.9 to 3.3 kHz.

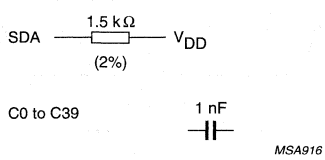


Fig.17 AC test loads.

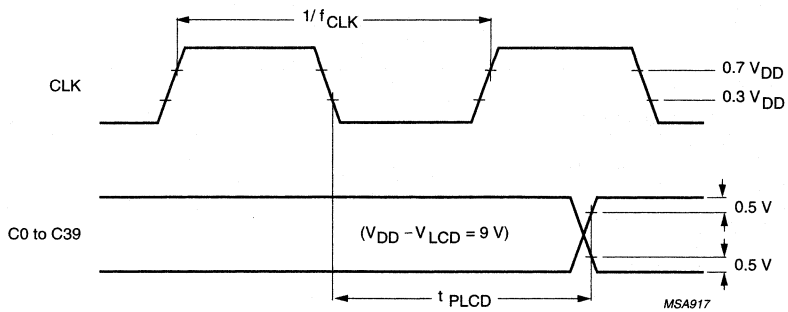


Fig.18 Driver timing waveforms.

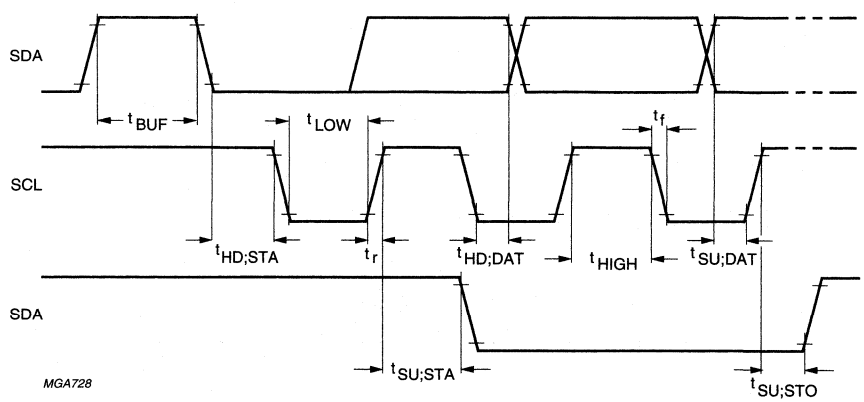


Fig.19 I²C-bus timing waveforms.

14 APPLICATION INFORMATION

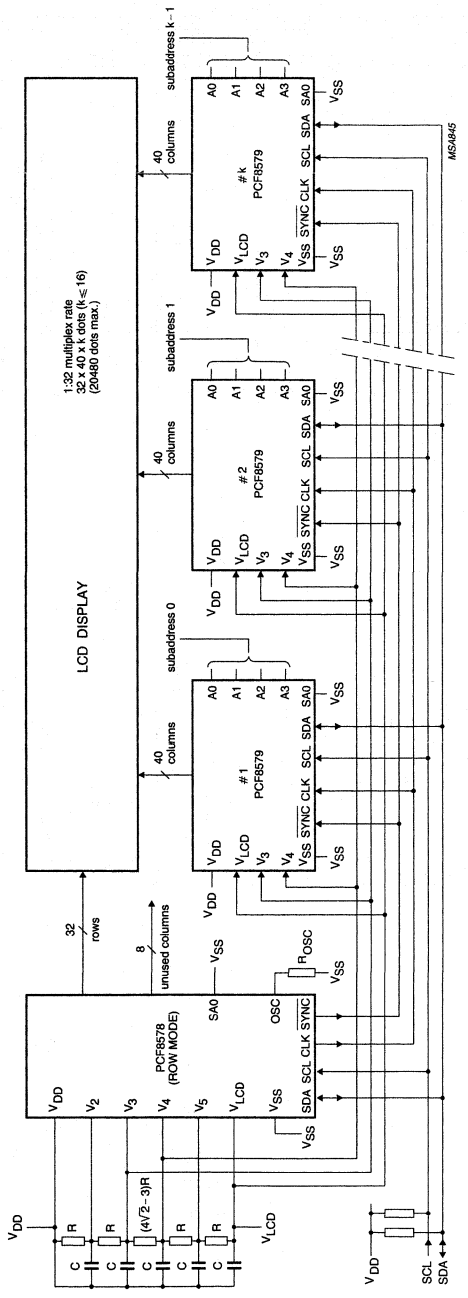


Fig.20 Typical LCD driver system with 1 : 32 multiplex rate.

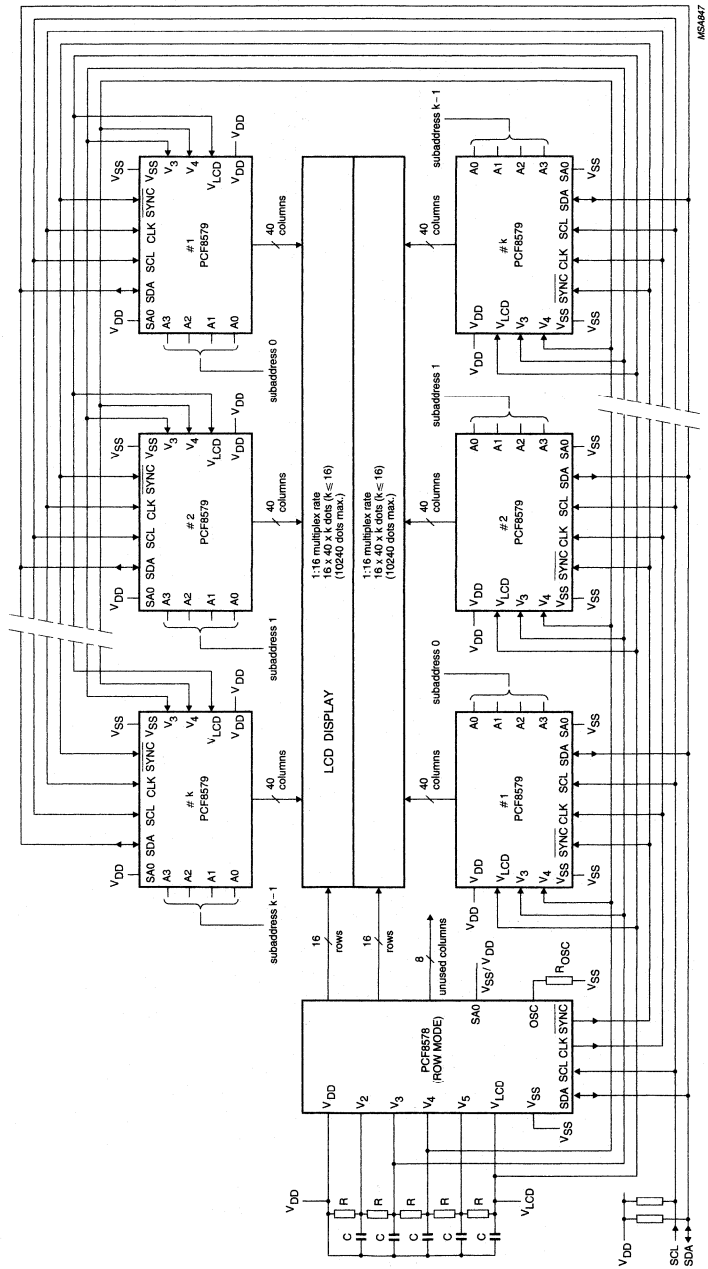


Fig.21 Split screen application with 1 : 16 multiplex rate for improved contrast.

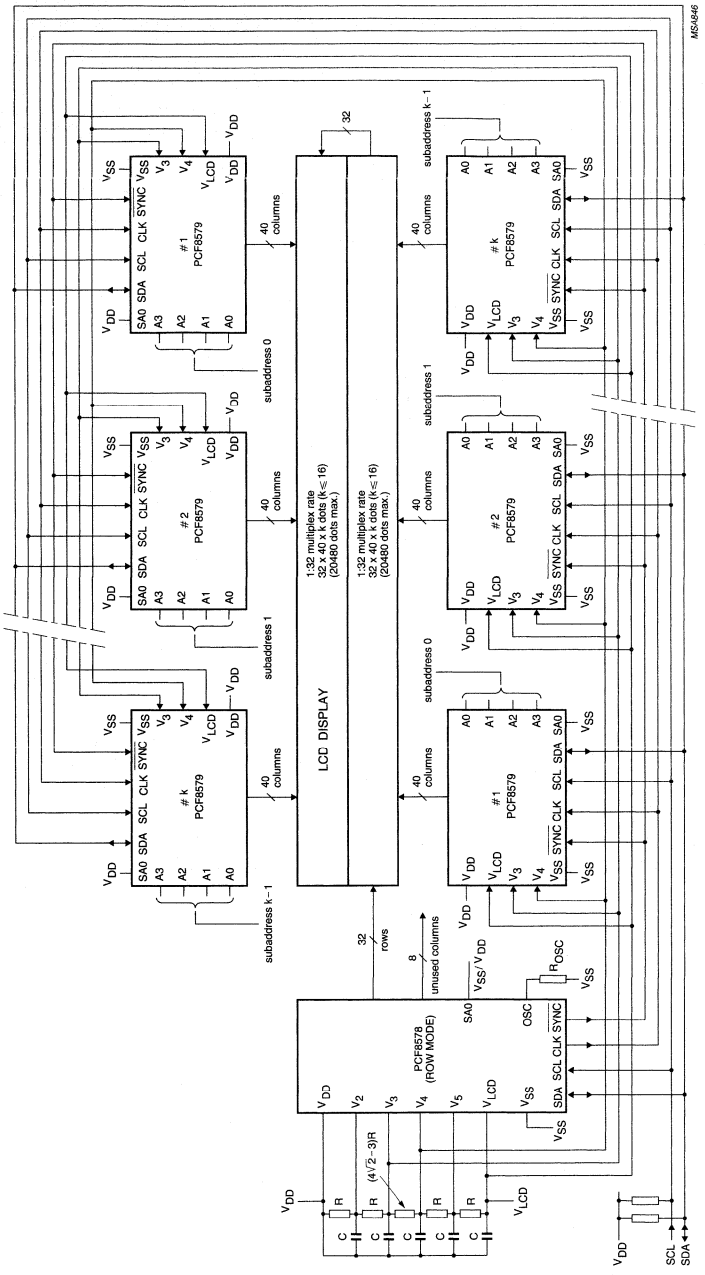


Fig.22 Split screen application with 1 : 32 multiplex rate.

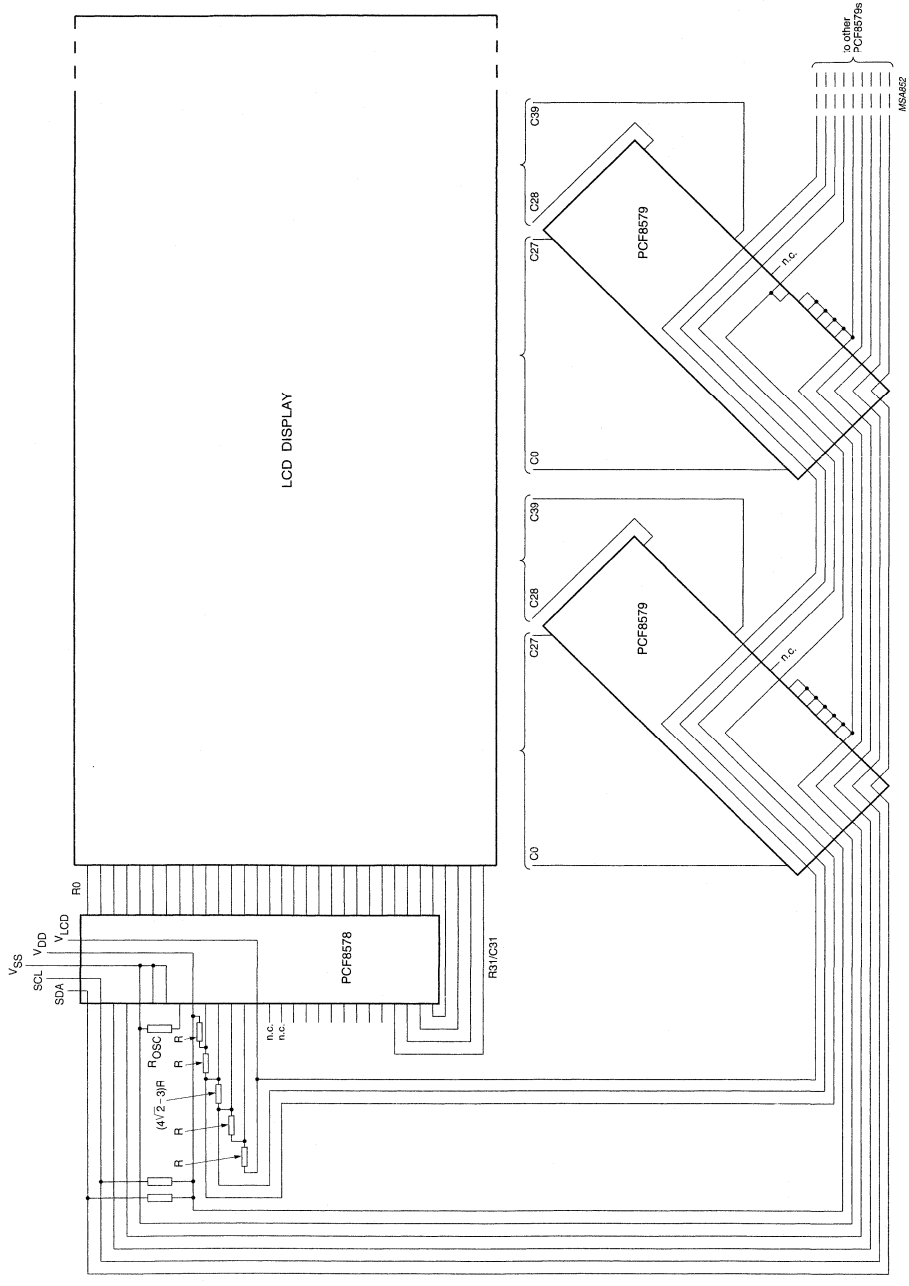
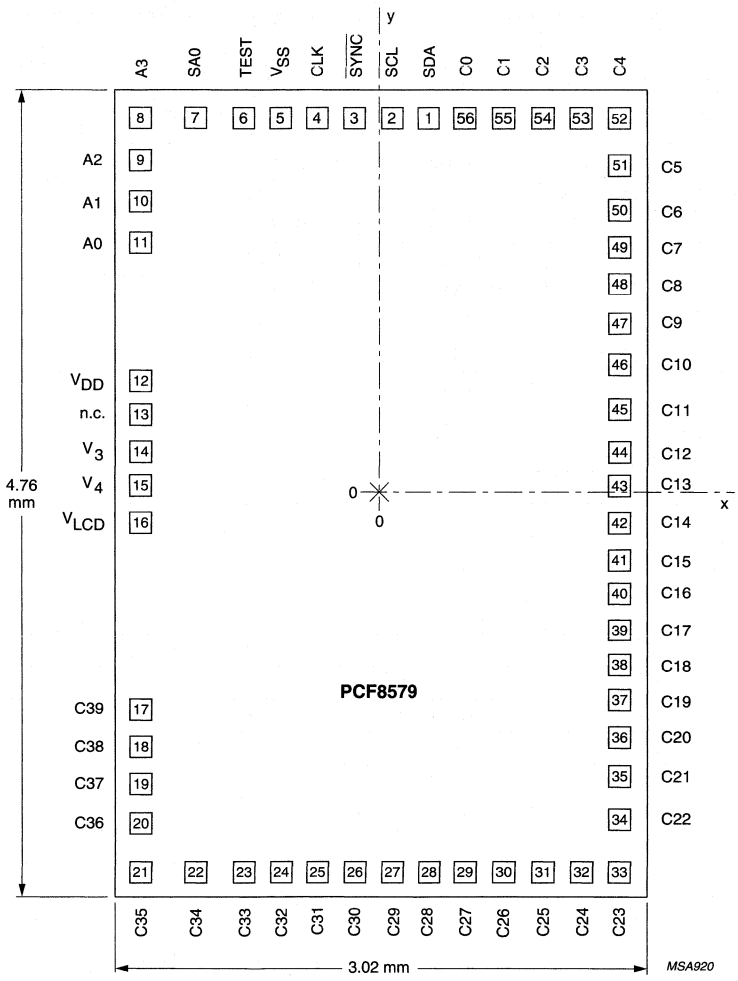


Fig.23 Example of single plane wiring, single screen with 1 : 32 multiplex rate (PCF8578 in row driver mode).

15 CHIP DIMENSIONS AND BONDING PAD LOCATIONS



Chip area: 14.37 mm^2.
Bonding pad dimensions: 120 µm × 120 µm.
Gold bump dimensions (if ordered): 94 × 94 × 25 µm.
The numbers given in the square boxes refer to the pad number.

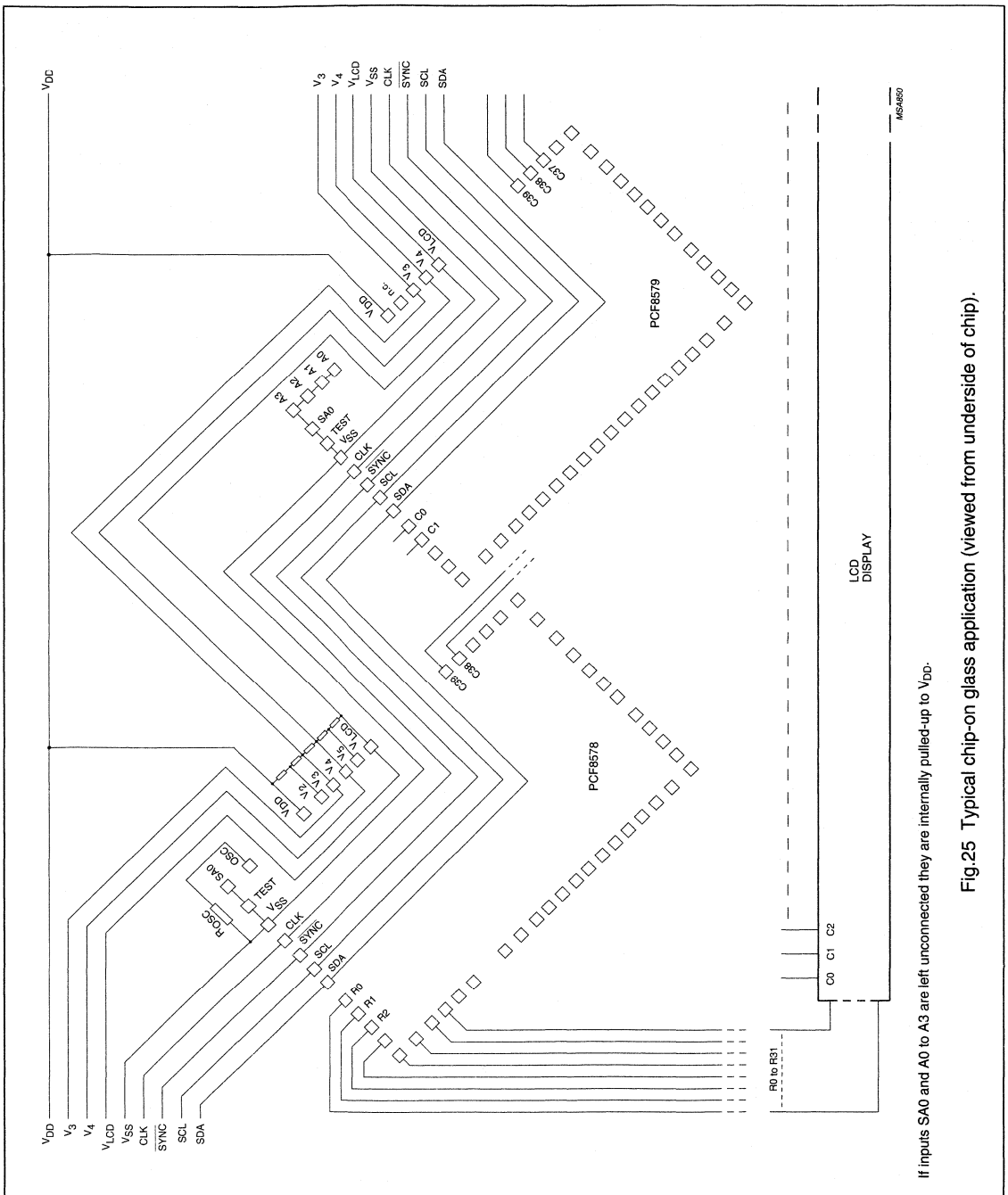
Fig.24 Bonding pad locations.

Table 12 Bonding pad locations (dimensions in μm); all x/y coordinates are referenced to centre of chip, see Fig.24.

PAD NUMBER	SYMBOL	x	y	PINS	
				VSO56	LQFP64
1	SDA	252	2142	1	7
2	SCL	48	2142	2	8
3	$\overline{SYNC}$	−156	2142	3	9
4	CLK	−360	2142	4	10
5	V_{SS}	−564	2142	5	11
6	TEST	−786	2142	6	12
7	SA0	−1032	2142	7	13
8	A3	−1314	2142	8	14
9	A2	−1314	1920	9	16
10	A1	−1314	1716	10	17
11	A0	−1314	1512	11	18
12	V_{DD}	−1314	708	12	20
13	n.c.	−1314	504	13	21
14	V_3	−1314	300	14	22
15	V_4	−1314	96	15	23
16	V_{LCD}	−1314	−108	16	24
17	C39	−1314	−1308	17	30
18	C38	−1314	−1512	18	31
19	C37	−1314	−1716	19	32
20	C36	−1314	−1920	20	33
21	C35	−1314	−2142	21	35
22	C34	−1032	−2142	22	36
23	C33	−786	−2142	23	37
24	C32	−564	−2142	24	38
25	C31	−360	−2142	25	39
26	C30	−156	−2142	26	40
27	C29	48	−2142	27	41
28	C28	252	−2142	28	42
29	C27	498	−2142	29	43
30	C26	702	−2142	30	44
31	C25	906	−2142	31	45
32	C24	1110	−2142	32	46
33	C23	1314	−2142	33	47
34	C22	1314	−1830	34	48
35	C21	1314	−1570	35	49
36	C20	1314	−1326	36	50
37	C19	1314	−1122	37	51
38	C18	1314	−918	38	52

PAD NUMBER	SYMBOL	x	y	PINS	
				VSO56	LQFP64
39	C17	1314	−714	39	53
40	C16	1314	−510	40	54
41	C15	1314	−306	41	55
42	C14	1314	−102	42	56
43	C13	1314	102	43	57
44	C12	1314	306	44	58
45	C11	1314	510	45	59
46	C10	1314	714	46	60
47	C9	1314	918	47	61
48	C8	1314	1122	48	62
49	C7	1314	1326	49	63
50	C6	1314	1566	50	64
51	C5	1314	1830	51	1
52	C4	1314	2142	52	2
53	C3	1110	2142	53	3
54	C2	906	2142	54	4
55	C1	702	2142	55	5
56	C0	498	2142	56	6
–	n.c.	–	–	–	15, 19, 21, 25 to 29, 34

16 CHIP-ON GLASS INFORMATION



If inputs SA0 and A0 to A3 are left unconnected they are internally pulled-up to V_{DD}.

Fig.25 Typical chip-on glass application (viewed from underside of chip).

Clock/calendar with 240 × 8-bit RAM PCF8583

CONTENTS

Clock/calendar with 240 × 8-bit RAM PCF8583

1 FEATURES

- I²C-bus interface operating supply voltage: 2.5 V to 6 V
- Clock operating supply voltage (0 to +70 °C): 1.0 V to 6.0 V
- 240 × 8-bit low-voltage RAM
- Data retention voltage: 1.0 V to 6 V
- Operating current (at f_{SCL} = 0 Hz): max. 50 µA
- Clock function with four year calendar
- Universal timer with alarm and overflow indication
- 24 or 12 hour format
- 32.768 kHz or 50 Hz time base
- Serial input/output bus (I²C)
- Automatic word address incrementing
- Programmable alarm, timer and interrupt function
- Slave address:
  - READ: A1 or A3
  - WRITE: A0 or A2.

2 GENERAL DESCRIPTION

The PCF8583 is a clock/calendar circuit based on a 2048-bit static CMOS RAM organized as 256 words by 8 bits. Addresses and data are transferred serially via the two-line bidirectional I²C-bus. The built-in word address register is incremented automatically after each written or read data byte. Address pin A0 is used for programming the hardware address, allowing the connection of two devices to the bus without additional hardware.

The built-in 32.768 kHz oscillator circuit and the first 8 bytes of the RAM are used for the clock/calendar and counter functions. The next 8 bytes may be programmed as alarm registers or used as free RAM space.
The remaining 240 bytes are free RAM locations.

3 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage operating mode	I²C-bus active	2.5	–	6.0	V
		I²C-bus inactive	1.0	–	6.0	V
I_{DD}	supply current operating mode	f_{SCL} = 100 kHz	–	–	200	µA
I_{DDO}	supply current clock mode	f_{SCL} = 0 Hz; V_{DD} = 5 V	–	10	50	µA
		f_{SCL} = 0 Hz; V_{DD} = 1 V	–	2	10	µA
T_{amb}	operating ambient temperature range		−40	–	+85	°C
T_{stg}	storage temperature range		−65	–	+150	°C

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8583P	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1
PCF8583T	SO8	plastic small outline package; 8 leads; body width 7.5 mm	SOT176-1

5 BLOCK DIAGRAM

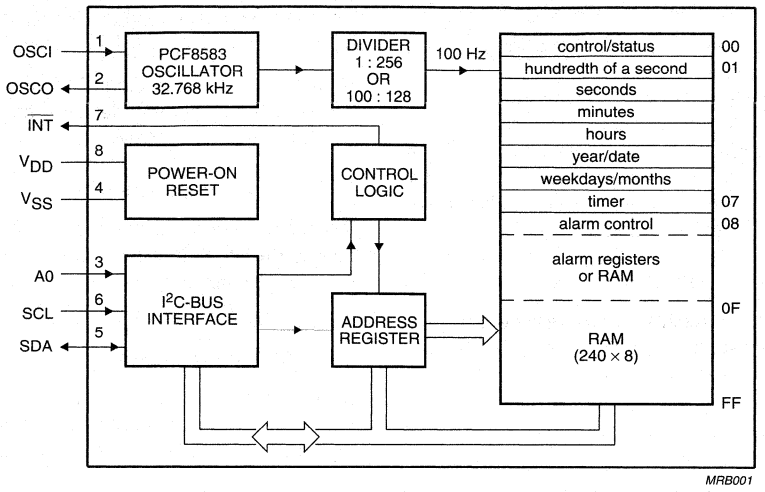


Fig.1 Block diagram.

6 PINNING

SYMBOL	PIN	DESCRIPTION
OSCI	1	oscillator input, 50 Hz or event-pulse input
OSCO	2	oscillator output
A0	3	address input
V_{SS}	4	negative supply
SDA	5	serial data line
SCL	6	serial clock line
$\overline{INT}$	7	open drain interrupt output (active LOW)
V_{DD}	8	positive supply

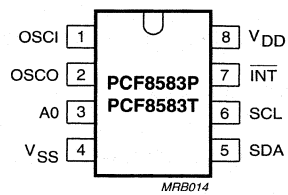


Fig.2 Pinning diagram.

7 FUNCTIONAL DESCRIPTION

The PCF8583 contains a 256 by 8-bit RAM with an 8-bit auto-increment address register, an on-chip 32.768 kHz oscillator circuit, a frequency divider, a serial two-line bidirectional I²C-bus interface and a power-on reset circuit.

The first 16 bytes of the RAM (memory addresses 00 to 0F) are designed as addressable 8-bit parallel special function registers. The first register (memory address 00) is used as a control/status register. The memory addresses 01 to 07 are used as counters for the clock function. The memory addresses 08 to 0F may be programmed as alarm registers or used as free RAM locations, when the alarm is disabled.

7.1 Counter function modes

When the control/status register is programmed, a 32.768 kHz clock mode, a 50 Hz clock mode or an event-counter mode can be selected.

In the clock modes the hundredths of a second, seconds, minutes, hours, date, month (four year calendar) and weekday are stored in a BCD format. The timer register stores up to 99 days. The event counter mode is used to count pulses applied to the oscillator input (OSCO left open-circuit). The event counter stores up to 6 digits of data.

When one of the counters is read (memory locations 01 to 07), the contents of all counters are strobed into capture latches at the beginning of a read cycle. Therefore, faulty reading of the count during a carry condition is prevented.

When a counter is written, other counters are not affected.

7.2 Alarm function modes

By setting the alarm enable bit of the control/status register the alarm control register (address 08) is activated.

By setting the alarm control register a dated alarm, a daily alarm, a weekday alarm or a timer alarm may be programmed. In the clock modes, the timer register (address 07) may be programmed to count hundredths of a second, seconds, minutes, hours or days. Days are counted when an alarm is not programmed.

Whenever an alarm event occurs the alarm flag of the control/status register is set. A timer alarm event will set the alarm flag and an overflow condition of the timer will set the timer flag. The open drain interrupt output is switched on (active LOW) when the alarm or timer flag is set (enabled). The flags remain set until directly reset by a write operation.

When the alarm is disabled (Bit 2 of control/status register = 0) the alarm registers at addresses 08 to 0F may be used as free RAM.

7.3 Control/status register

The control/status register is defined as the memory location 00 with free access for reading and writing via the I²C-bus. All functions and options are controlled by the contents of the control/status register (see Fig.3).

7.4 Counter registers

In the clock modes 24 h or 12 h format can be selected by setting the most significant bit of the hours counter register. The format of the hours counter is shown in Fig.5.

The year and date are packed into memory location 05 (see Fig.6). The weekdays and months are packed into memory location 06 (see Fig.7). When reading these memory locations the year and weekdays are masked out when the mask flag of the control/status register is set. This allows the user to read the date and month count directly.

In the event-counter mode events are stored in BCD format. D5 is the most significant and D0 the least significant digit. The divider is by-passed.

In the different modes the counter registers are programmed and arranged as shown in Fig.4. Counter cycles are listed in Table 1.

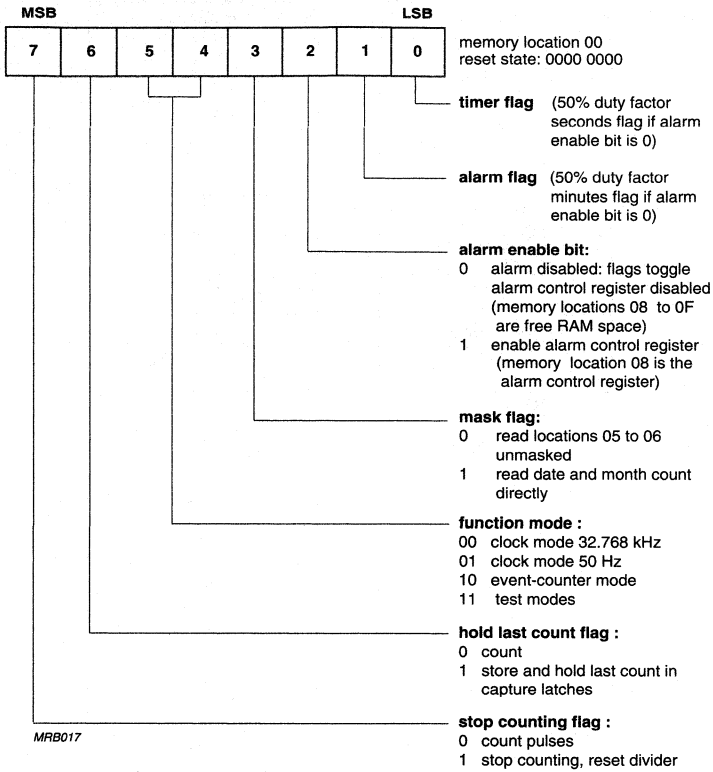


Fig.3 Control/status register.

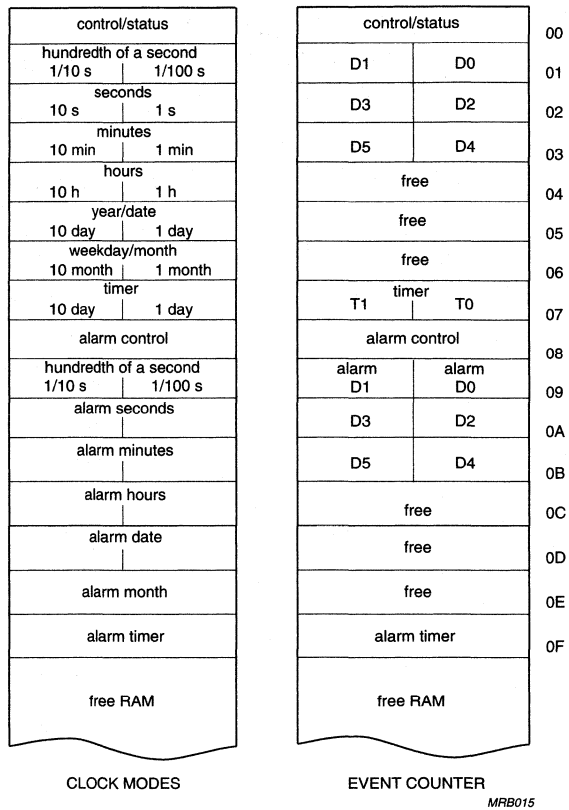


Fig.4 Register arrangement.

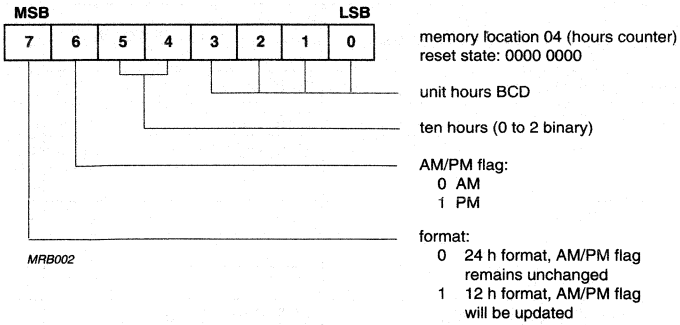


Fig.5 Format of the hours counter.

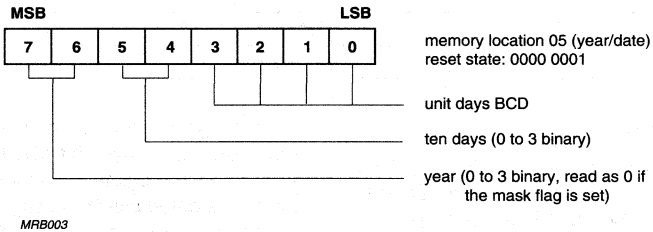


Fig.6 Format of the year/date counter.

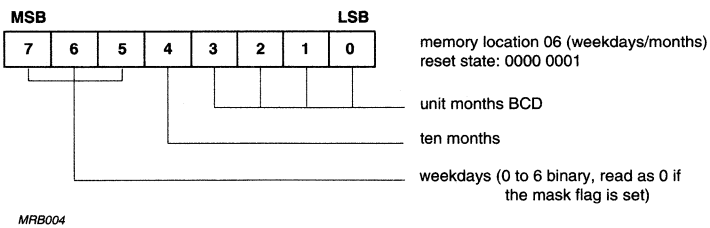


Fig.7 Format of the weekdays/month counter.

Table 1 Cycle length of the time counters, clock modes

UNIT	COUNTING CYCLE	CARRY TO NEXT UNIT	CONTENTS OF THE MONTH COUNTER
Hundredths of a second	00 to 99	99 to 00	–
Seconds	00 to 59	59 to 00	–
Minutes	00 to 59	59 to 00	–
Hours (24 h)	00 to 23	23 to 00	–
Hours (12 h)	12 AM	–	–
	01 AM to 11 AM	–	–
	12 PM	–	–
	01 PM to 11 PM	11 PM to 12 AM	–
Date	01 to 31	31 to 01	1, 3, 5, 7, 8, 10 and 12
	01 to 30	30 to 01	4, 6, 9 and 11
	01 to 29	29 to 01	2, year = 0
	01 to 28	28 to 01	2, year = 1, 2 and 3
Months	01 to 12	12 to 01	–
Year	0 to 3	–	–
Weekdays	0 to 6	6 to 0	–
Timer	00 to 99	no carry	–

7.5 Alarm control register

When the alarm enable bit of the control/status register is set (address 00, bit 2) the alarm control register (address 08) is activated. All alarm, timer, and interrupt output functions are controlled by the contents of the alarm control register (see Fig.8).

7.6 Alarm registers

All alarm registers are allocated with a constant address offset of hexadecimal 08 to the corresponding counter registers (see Fig.4, Register arrangement).

An alarm signal is generated when the contents of the alarm registers matches bit-by-bit the contents of the involved counter registers. The year and weekday bits are ignored in a dated alarm. A daily alarm ignores the month and date bits. When a weekday alarm is selected, the contents of the alarm weekday/month register will select the weekdays on which an alarm is activated (see Fig.9).

Remark: In the 12 h mode, bits 6 and 7 of the alarm hours register must be the same as the hours counter.

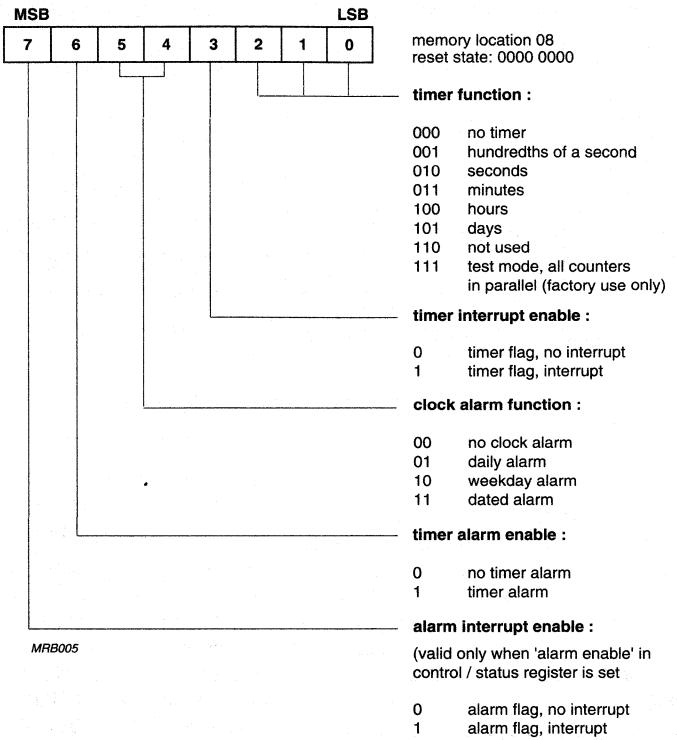


Fig.8 Alarm control register; clock mode.

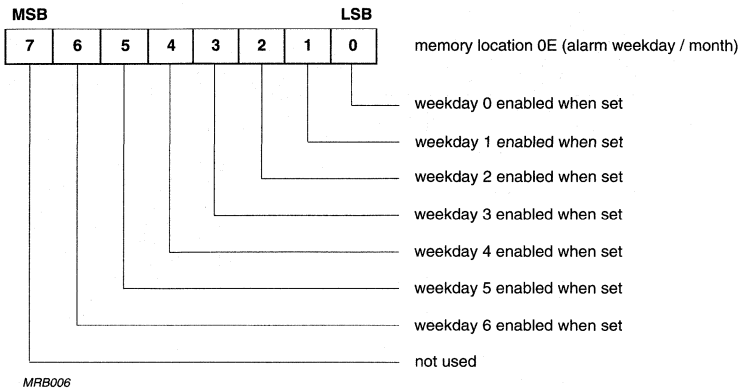


Fig.9 Selection of alarm weekdays.

7.7 Timer

The timer (location 07) is enabled by setting the control/status register = XX0X X1XX. The timer counts up from 0 (or a programmed value) to 99. On overflow, the timer resets to 0. The timer flag (LSB of control/status register) is set on overflow of the timer. This flag must be reset by software. The inverted value of this flag can be transferred to the external interrupt by setting bit 3 of the alarm control register.

Additionally, a timer alarm can be programmed by setting the timer alarm enable (bit 6 of the alarm control register). When the value of the timer equals a pre-programmed value in the alarm timer register (location 0F), the alarm flag is set (bit 1 of the control/status register). The inverted value of the alarm flag can be transferred to the external interrupt by enabling the alarm interrupt (bit 6 of the alarm control register).

Resolution of the timer is programmed via the 3 LSBs of the alarm control register (see Fig.11, Alarm and timer Interrupt logic diagram).

7.8 Event counter mode

Event counter mode is selected by bits 4 and 5 which are logic 1, 0 in the control/status register. The event counter mode is used to count pulses externally applied to the oscillator input (OSCO left open-circuit).

The event counter stores up to 6 digits of data, which are stored as 6 hexadecimal values located in locations 1, 2, and 3. Thus, up to 1 million events may be recorded.

An event counter alarm occurs when the event counter registers match the value programmed in locations 9, A, and B, and the event alarm is enabled (bits 4 and 5 which are logic 0, 1 in the alarm control register). In this event, the alarm flag (bit 1 of the control/status register) is set. The inverted value of this flag can be transferred to the interrupt pin (pin 7) by setting the alarm interrupt enable in the alarm control register. In this mode, the timer (location 07) increments once for every one, one-hundred, ten thousand, or 1 million events, depending on the value programmed in bits 0, 1 and 2 of the alarm control register. In all other events, the timer functions are as in the clock mode.

7.9 Interrupt output

The conditions for activating the open-drain n-channel interrupt output $\overline{INT}$ (active LOW) are determined by appropriate programming of the alarm control register. These conditions are clock alarm, timer alarm, timer overflow, and event counter alarm. An interrupt occurs when the alarm flag or the timer flag is set, and the corresponding interrupt is enabled. In all events, the interrupt is cleared only by software resetting of the flag which initiated the interrupt.

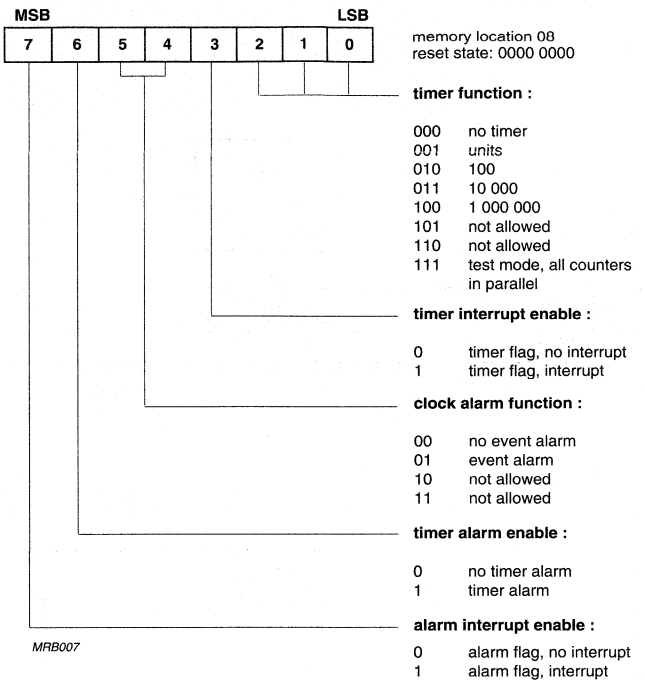


Fig.10 Alarm control register, event-counter mode.

In the clock mode, if the alarm enable is not activated (alarm enable bit of control/status register is logic 0), the interrupt output toggles at 1 Hz with a 50% duty cycle (may be used for calibration). This is the default power-on state of the device. The OFF voltage of the interrupt output may exceed the supply voltage, up to a maximum of 6.0 V. A logic diagram of the interrupt output is shown in Fig.11.

7.10 Oscillator and divider

A 32.768 kHz quartz crystal has to be connected to OSCI (pin 1) and OSCO (pin 2). A trimmer capacitor between OSCI and V_{DD} is used for tuning the oscillator (see quartz frequency adjustment). A 100 Hz clock signal is derived from the quartz oscillator for the clock counters.

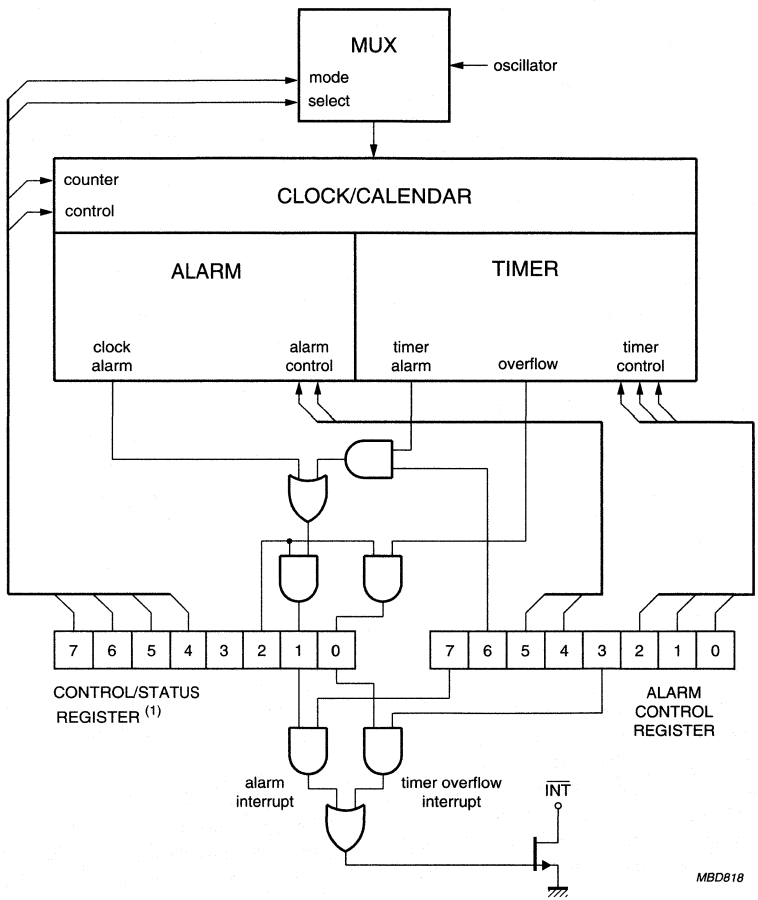
In the 50 Hz clock mode or event-counter mode the oscillator is disabled and the oscillator input is switched to a high impedance state.

This allows the user to feed the 50 Hz reference frequency or an external high speed event signal into the input OSCI.

7.11 Initialization

When power-up occurs the I^2C-bus interface, the control/status register and all clock counters are reset. The device starts time-keeping in the 32.768 kHz clock mode with the 24 h format on the first of January at 0.00.00: 00. A 1 Hz square wave with 50% duty cycle appears at the interrupt output pin (starts HIGH).

It is recommended to set the stop counting flag of the control/status register before loading the actual time into the counters. Loading of illegal states may lead to a temporary clock malfunction.



(1) If the alarm enable bit of the control/status register is reset (logic 0), a 1 Hz signal can be observed on the interrupt pin $\overline{INT}$.

Fig.11 Alarm and timer interrupt logic diagram.

8 CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

8.1 Bit transfer (see Fig.12)

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

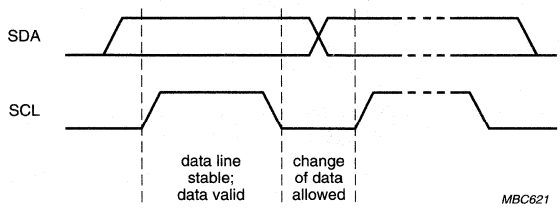


Fig.12 Bit transfer.

8.2 Start and stop conditions (see Fig.13)

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

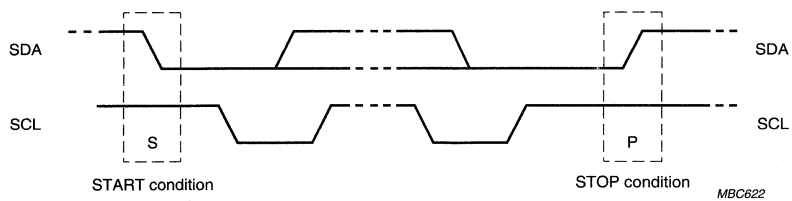


Fig.13 Definition of start and stop conditions.

8.3 System configuration (see Fig.14)

A device generating a message is a 'transmitter', a device receiving a message is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves'.

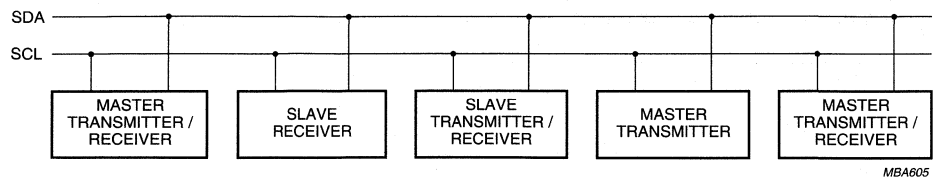


Fig.14 System configuration.

8.4 Acknowledge (see Fig.15)

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by **not** generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

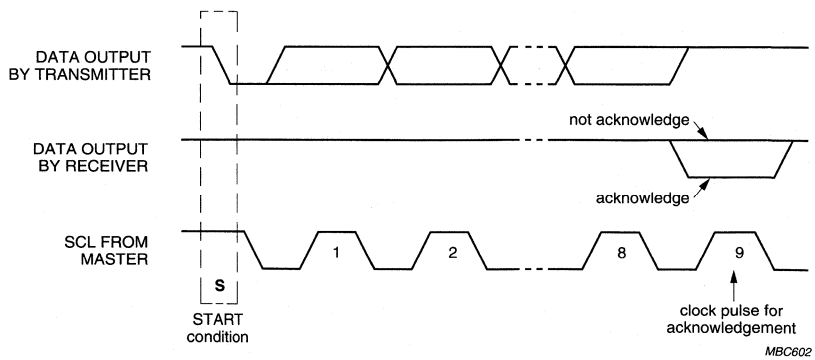


Fig.15 Acknowledgment on the I²C-bus.

9 I²C-BUS PROTOCOL

9.1 Addressing

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always carried out with the first byte transmitted after the start procedure.

The clock/calendar acts as a slave receiver or slave transmitter. Therefore the clock signal SCL is only an input signal, but the data signal SDA is a bidirectional line.

The clock/calendar slave address is shown in Fig.16. Bit A0 corresponds to hardware address pin A0. Connecting this pin to V_{DD} or V_{SS} allows the device to have one of two different addresses.

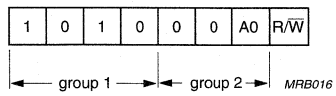


Fig.16 Slave address.

9.2 Clock/calendar READ/WRITE cycles

The I²C-bus configuration for the different PCF8583 READ and WRITE cycles is shown in Figs 17, 18 and 19.

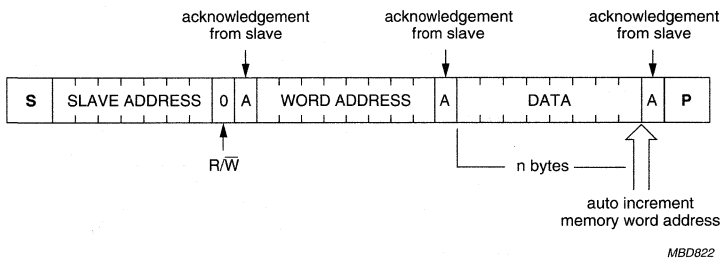


Fig.17 Master transmits to slave receiver (WRITE) mode.

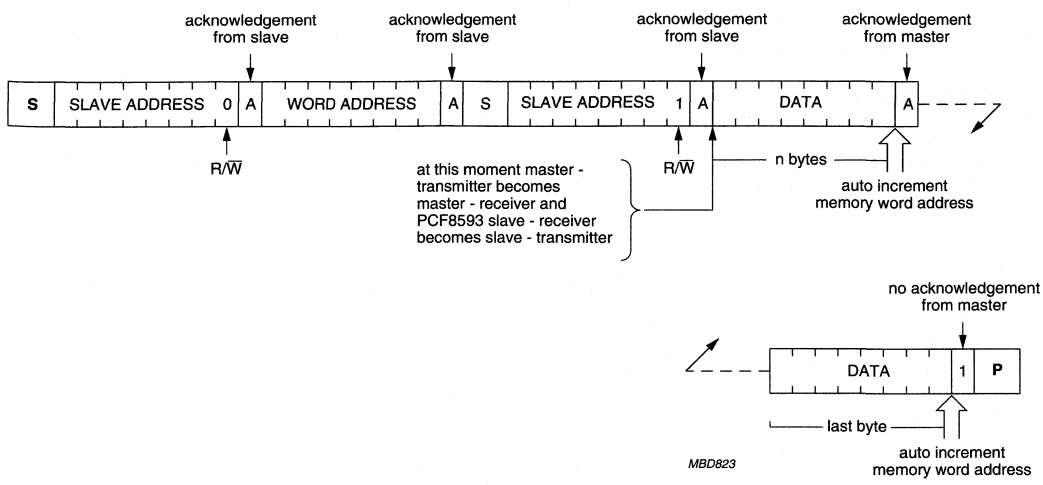


Fig.18 Master reads after setting word address (write word address; READ data).

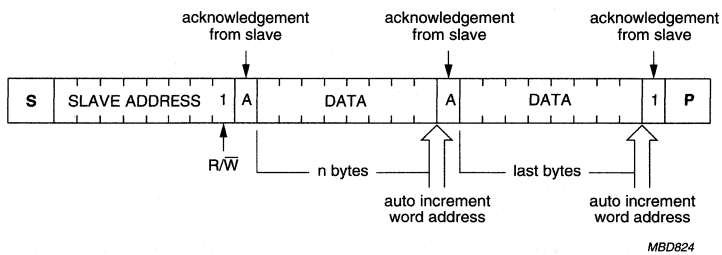


Fig.19 Master reads slave immediately after first byte (READ mode).

10 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage (pin 8)	−0.8	+7.0	V
I_{DD}	supply current (pin 8)	–	50	mA
I_{SS}	supply current (pin 4)	–	50	mA
V_I	input voltage	−0.8	V_{DD} + 0.8	V
I_I	DC input current	–	10	mA
I_O	DC output current	–	10	mA
P_{tot}	total power dissipation per package	–	300	mW
P_O	power dissipation per output	–	50	mW
T_{amb}	operating ambient temperature	−40	+85	°C
T_{stg}	storage temperature	−65	+150	°C

11 HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices. Advice can be found in Data Handbook IC12 under *"Handling MOS Devices"*.

12 DC CHARACTERISTICS

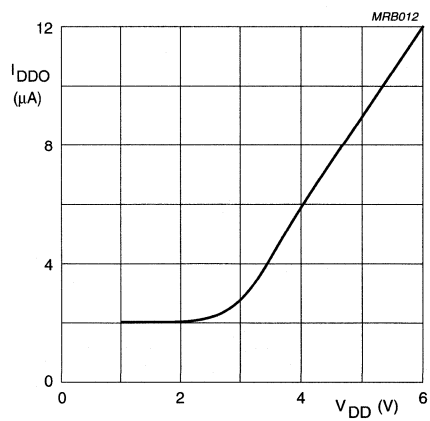
V_{DD} = 2.5 to 6.0 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.(1)	MAX.	UNIT
V_{DD}	supply voltage (operating mode)	I²C-bus active	2.5	–	6.0	V
		I²C-bus inactive	1.0	–	6.0	V
V_{DDosc}	supply voltage (quartz oscillator)	T_{amb} = 0 to 70 °C; note 2	1.0	–	6.0	V
I_{DD}	supply current (operating mode)	f_{SCL} = 100 kHz; clock mode; note 3	–	–	200	µA
I_{DDO}	supply current (clock mode)	see Fig.20				
		f_{SCL} = 0 Hz; V_{DD} = 5 V	–	10	50	µA
		f_{SCL} = 0 Hz; V_{DD} = 1 V	–	2	10	µA
I_{DDR}	data retention	f_{OSCI} = 0 Hz; V_{DD} = 1 V				
		T_{amb} = −40 to + 85 °C	–	–	5	µA
		T_{amb} = −25 to + 70 °C	–	–	2	µA
V_{EN}	I²C-bus enable level	note 4	1.5	1.9	2.3	V
SDA						
V_{IL}	LOW level input voltage	note 5	−0.8	–	0.3V_{DD}	V
V_{IH}	HIGH level input voltage	note 5	0.7V_{DD}	–	V_{DD} +0.8	V
I_{OL}	LOW level output current	V_{OL} = 0.4 V	3	–	–	mA
I_{LI}	input leakage current	V_I = V_{DD} or V_{SS}	−1	–	+1	µA
C_i	input capacitance	note 6	–	–	7	pF
A0; OSCI						

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.(1)	MAX.	UNIT
I_{LI}	input leakage current	$V_I = V_{DD}$ or V_{SS}	−250	–	+250	nA
$\overline{INT}$						
I_{OL}	LOW level output current	V_{OL} = 0.4 V	3	–	–	mA
I_{LI}	input leakage current	$V_I = V_{DD}$ or V_{SS}	−1	–	+1	µA
SCL						
C_i	input capacitance	note 6	–	–	7	pF
I_{LI}	input leakage current	$V_I = V_{DD}$ or V_{SS}	−1	–	+1	µA

Notes

1. Typical values measured at T_{amb} = 25 °C.
2. When powering-up the device, V_{DD} must exceed 1.5 V until stable operation of the oscillator is established.
3. Event counter mode: supply current dependant upon input frequency.
4. The I^2C-bus logic is disabled if $V_{DD} < V_{EN}$.
5. When the voltages are above or below the supply voltages V_{DD} or V_{SS}, an input current may flow; this current must not exceed ±0.5 mA.
6. Tested on sample basis.



f_{SCL} = 32 kHz; T_{amb} = 25 °C.

Fig.20 Typical supply current in clock mode as a function of supply voltage.

13 AC CHARACTERISTICS

V_{DD} = 2.5 to 6.0 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Oscillator						
C_{osc}	integrated oscillator capacitance		–	40	–	pF
Δf_{osc}	oscillator stability	for ΔV_{DD} = 100 mV; T_{amb} = 25 °C; V_{DD} = 1.5 V	–	2×10^{-7}	–	
f_i	input frequency	note 1	–	–	1	MHz
Quartz crystal parameters (f = 32.768 kHz)						
R_s	series resistance		–	–	40	kΩ
C_L	parallel load capacitance		–	10	–	pF
C_T	trimmer capacitance		5	–	25	pF
I²C-bus timing (see Fig.21; notes 2 and 3)						
f_{SCL}	SCL clock frequency		–	–	100	kHz
t_{SP}	tolerable spike width on bus		–	–	100	ns
t_{BUF}	bus free time		4.7	–	–	µs
$t_{SU;STA}$	START condition set-up time		4.7	–	–	µs
$t_{HD;STA}$	START condition hold time		4.0	–	–	µs
t_{LOW}	SCL LOW time		4.7	–	–	µs
t_{HIGH}	SCL HIGH time		4.0	–	–	µs
t_r	SCL and SDA rise time		–	–	1.0	µs
t_f	SCL and SDA fall time		–	–	0.3	µs
$t_{SU;DAT}$	data set-up time		250	–	–	ns
$t_{HD;DAT}$	data hold time		0	–	–	ns
$t_{VD;DAT}$	SCL LOW to data out valid		–	–	3.4	µs
$t_{SU;STO}$	STOP condition set-up time		4.0	–	–	µs

Notes

1. Event counter mode only.
2. All timing values are valid within the operating supply voltage and ambient temperature range and reference to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.
3. A detailed description of the I²C-bus specification, with applications, is given in brochure *"The I²C-bus and how to use it"*. This brochure may be ordered using the code 9398 393 40011.

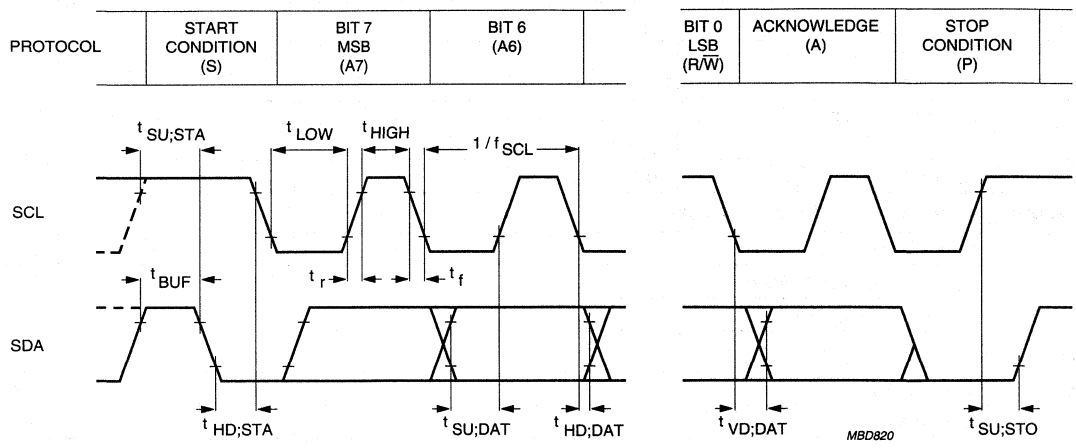


Fig.21 I²C-bus timing diagram; rise and fall times refer to V_{IL} and V_{IH}.

14 APPLICATION INFORMATION

14.1 Quartz frequency adjustment

14.1.1 METHOD 1: FIXED OSCI CAPACITOR

By evaluating the average capacitance necessary for the application layout a fixed capacitor can be used. The frequency is best measured via the 1 Hz signal available after power-on at the interrupt output (pin 7). The frequency tolerance depends on the quartz crystal tolerance, the capacitor tolerance and the device-to-device tolerance (on average $\pm 5 \times 10^{-6}$). Average deviations of ±5 minutes per year can be achieved.

14.1.2 METHOD 2: OSCI TRIMMER

Using the alarm function (via the I²C-bus) a signal faster than 1 Hz can be generated at the interrupt output for fast setting of a trimmer.

Procedure:

- Power-on
- Initialization (alarm functions).

Routine:

- Set clock to time T and set alarm to time T + dT
- At time T + dT (interrupt) repeat routine.

14.1.3 METHOD 3:

Direct measurement of OSC out (accounting for test probe capacitance).

The PCF8583 slave address has a fixed combination 1010 as group 1.

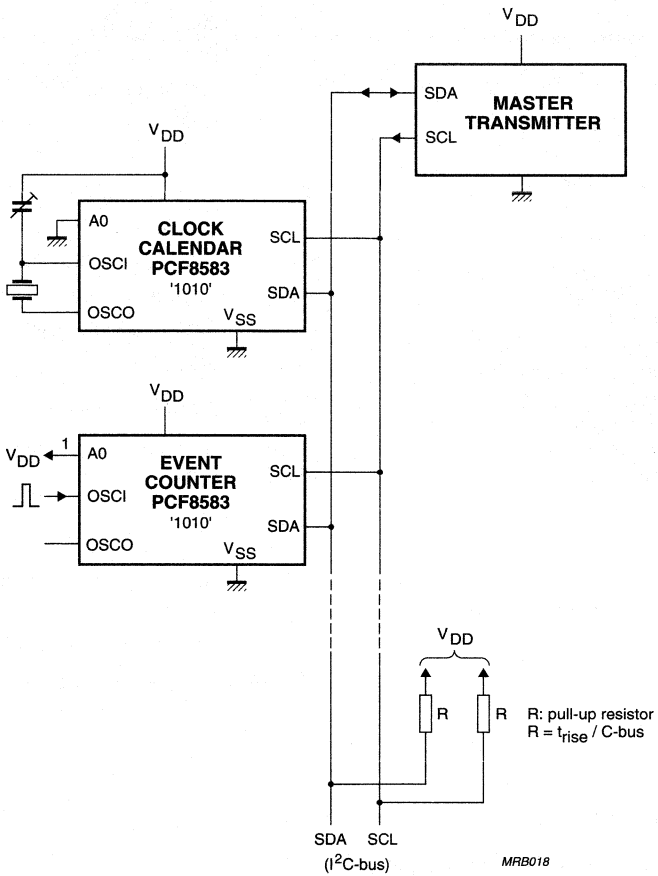


Fig.22 Application diagram.

I²C-bus controller PCF8584

CONTENTS

I²C-bus controller PCF8584

1 FEATURES

- Parallel-bus to I²C-bus protocol converter and interface
- Compatible with most parallel-bus microcontrollers/microprocessors including 8049, 8051, 6800, 68000 and Z80
- Both master and slave functions
- Automatic detection and adaption to bus interface type
- Programmable interrupt vector
- Multi-master capability
- I²C-bus monitor mode
- Long-distance mode (4-wire)
- Operating supply voltage 4.5 to 5.5 V
- Operating temperature range: −40 to +85 °C.

2 GENERAL DESCRIPTION

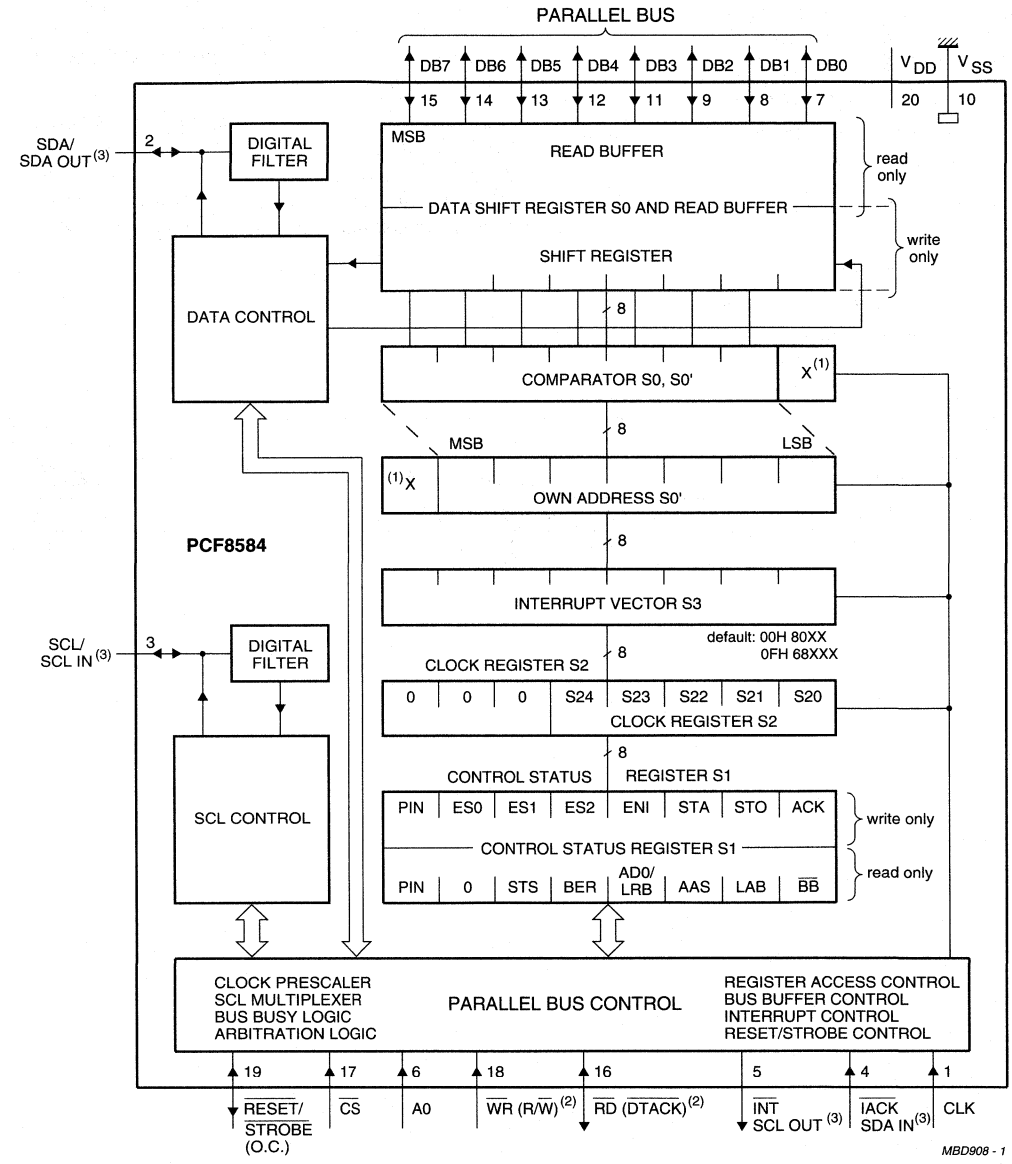
The PCF8584 is an integrated circuit designed in CMOS technology which serves as an interface between most standard parallel-bus microcontrollers/microprocessors and the serial I²C-bus. The PCF8584 provides both master and slave functions.

Communication with the I²C-bus is carried out on a byte-wise basis using interrupt or polled handshake. It controls all the I²C-bus specific sequences, protocol, arbitration and timing. The PCF8584 allows parallel-bus systems to communicate bidirectionally with the I²C-bus.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8584P	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1
PCF8584T	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1

4 BLOCK DIAGRAM



(1) X = don't care.

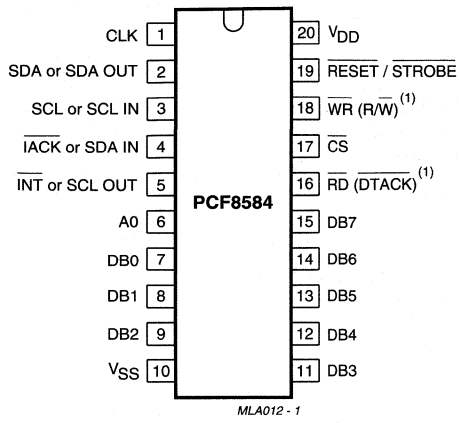
(2) Pin mnemonics between parenthesis indicate the 68000 mode pin designations.

(3) These pin mnemonics represent the long-distance mode pin designations.

Fig.1 Block diagram.

5 PINNING

SYMBOL	PIN	I/O	DESCRIPTION
CLK	1	I	clock input from microcontroller clock generator (internal pull-up)
SDA or SDA OUT	2	I/O	I²C-bus serial data input/output (open-drain). Serial data output in long-distance mode.
SCL or SCL IN	3	I/O	I²C-serial clock input/output (open-drain). Serial clock input in long-distance mode.
$\overline{IACK}$ or SDA IN	4	I	Interrupt acknowledge input (internal pull-up); when this signal is asserted the interrupt vector in register S3 will be available at the bus Port if the ENI flag is set. Serial data input in long-distance mode.
$\overline{INT}$ or SCL OUT	5	O	Interrupt output (open-drain); this signal is enabled by the ENI flag in register S1. It is asserted when the PIN flag is reset. (PIN is reset after 1 byte is transmitted or received over the I²C-bus). Serial clock output in long-distance mode.
A0	6	I	Register select input (internal pull-up); this input selects between the control/status register and the other registers. Logic 1 selects register S1, logic 0 selects one of the other registers depending on bits loaded in ESO, ES1 and ES2 of register S1.
DB0	7	I/O	bidirectional 8-bit bus Port 0
DB1	8	I/O	bidirectional 8-bit bus Port 1
DB2	9	I/O	bidirectional 8-bit bus Port 2
V_{SS}	10	–	ground
DB3	11	I/O	bidirectional 8-bit bus Port 3
DB4	12	I/O	bidirectional 8-bit bus Port 4
DB5	13	I/O	bidirectional 8-bit bus Port 5
DB6	14	I/O	bidirectional 8-bit bus Port 6
DB7	15	I/O	bidirectional 8-bit bus Port 7
$\overline{RD}$ ($\overline{DTACK}$)	16	I/(O)	$\overline{RD}$ is the read control input for MAB8049, MAB8051 or Z80-types. $\overline{DTACK}$ is the data transfer control output for 68000-types (open-drain).
$\overline{CS}$	17	I	chip select input (internal pull-up)
$\overline{WR}$ (R/$\overline{W}$)	18	I	$\overline{WR}$ is the write control input for MAB8048, MAB8051, or Z80-types (internal pull-up). R/$\overline{W}$ control input for 68000-types.
$\overline{RESET}$/ $\overline{STROBE}$	19	I/O	Reset input (open-drain); this input forces the I²C-bus controller into a predefined state; all flags are reset, except PIN, which is set. Also functions as strobe output.
V_{DD}	20	–	supply voltage



(1) *Pin mnemonics between parenthesis indicate the 68000 mode pin designations.*

Fig.2 Pin configuration.

6 FUNCTIONAL DESCRIPTION

6.1 General

The PCF8584 acts as an interface device between standard high-speed parallel buses and the serial I²C-bus. On the I²C-bus, it can act either as master or slave. Bidirectional data transfer between the I²C-bus and the parallel-bus microcontroller is carried out on a byte-wise basis, using either an interrupt or polled handshake. Interface to either 80XX-type (e.g. 8048, 8051, Z80) or 68000-type buses is possible. Selection of bus type is automatically performed (see Section 6.2).

Table 1 Control signals utilized by the PCF8584 for microcontroller/microprocessor interfacing

TYPE	R/$\overline{W}$	$\overline{WR}$	$\overline{R}$	$\overline{DTACK}$	$\overline{IACK}$
8048/ 8051	no	yes	yes	no	no
68000	yes	no	no	yes	yes
Z80	no	yes	yes	no	yes

The structure of the PCF8584 is similar to that of the I²C-bus interface section of the Philips' MABXXXX/PCF84(C)XX-series of microcontrollers, but with a modified control structure. The PCF8584 has five internal register locations. Three of these (own address register S0', clock register S2 and interrupt vector S3) are used for initialization of the PCF8584. Normally they are only written once directly after resetting of the PCF8584.

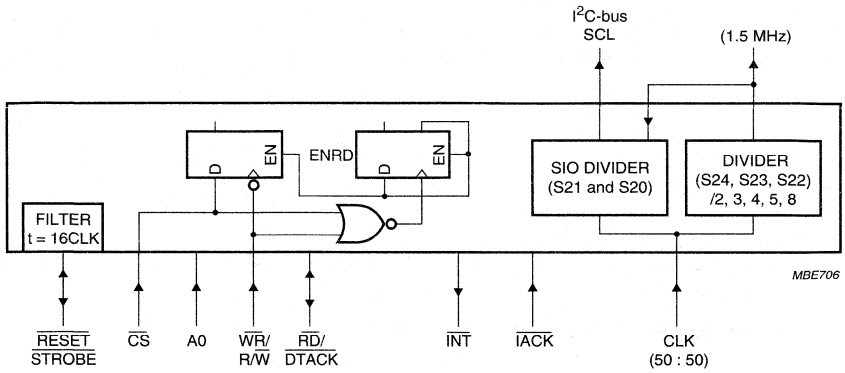
The remaining two registers function as double registers (data buffer/shift register S0, and control/status register S1) which are used during actual data transmission/reception. By using these double registers, which are separately write and read accessible, overhead for register access is reduced. Register S0 is a combination of a shift register and data buffer.

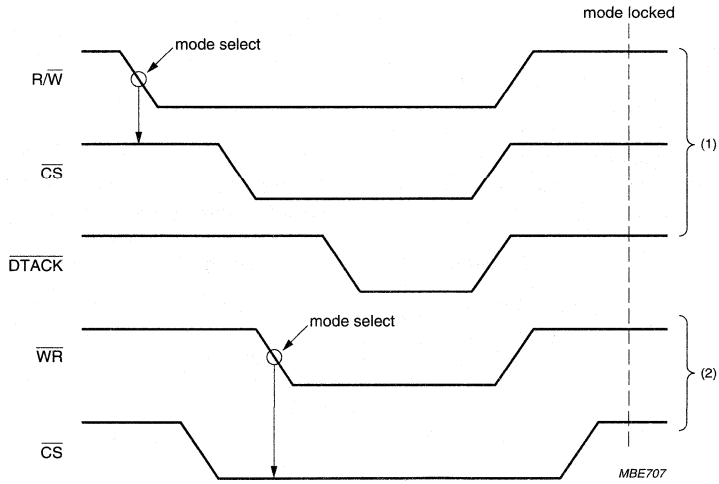
Register S0 performs all serial-to-parallel interfacing with the I²C-bus.

Register S1 contains I²C-bus status information required for bus access and/or monitoring.

6.2 Interface Mode Control (IMC)

Selection of either an 80XX mode or 68000 mode interface is achieved by detection of the first $\overline{WR}$-$\overline{CS}$ signal sequence. The concept takes advantage of the fact that the write control input is common for both types of interfaces. An 80XX-type interface is default. If a HIGH-to-LOW transition of $\overline{WR}$ (R/$\overline{W}$) is detected while $\overline{CS}$ is HIGH, the 68000-type interface mode is selected and the $\overline{DTACK}$ output is enabled. Care must be taken that $\overline{WR}$ and $\overline{CS}$ are stable after reset.





(1) Bus timing; 68000 mode write cycle.
(2) Bus timing; 80XX mode.

Fig.3 68000/80XX timing sequence utilized by the Interface Mode Control (IMC).

6.3 Set-up registers S0', S2 and S3

Registers S0', S2 and S3 are used for initialization of the PCF8584 (see Fig.5 'Initialization sequence' flowchart).

6.4 Own address register S0'

When the PCF8584 is addressed as slave, this register must be loaded with the 7-bit I²C-bus address to which the PCF8584 is to respond. During initialization, the own address register S0' must be written to, regardless whether it is later used. The Addressed As Slave (AAS) bit in status register S1 is set when this address is received (the value in S0 is compared with the value in S0'). Note that the S0 and S0' registers are offset by one bit; hence, programming the own address register S0' with a value of 55H will result in the value AAH being recognized as the PCF8584's slave address (see Fig.1).

Programming of S0' is accomplished via the parallel-bus when A0 is LOW, with the appropriate bit combinations set in control status register S1 (S1 is written when pin A0 = HIGH). Bit combinations for accessing all registers are given in Table 5. After reset, S0' has default address 00H (PCF8584 is thus initially in monitor mode, see Section 6.12.3).

6.5 Clock register S2

Register S2 provides control over chip clock frequency and SCL clock frequency. S20 and S21 provide a selection of 4 different I²C-bus SCL frequencies which are shown in Table 2. Note that these SCL frequencies are only obtained when bits S24, S23 and S22 are programmed to the correct input clock frequency (f_{clk}).

Table 2 Register S2 selection of SCL frequency

BIT		APPROXIMATE SCL FREQUENCY f_{SCL} (kHz)
S21	S20	
0	0	90
0	1	45
1	0	11
1	1	1.5

S22, S23 and S24 are used for control of the internal clock prescaler. Due to the possibility of varying microcontroller clock signals, the prescaler can be programmed to adapt to 5 different clock rates, thus providing a constant internal clock. This is required to provide a stable time base for the SCL generator and the digital filters associated with the I²C-bus signals SCL and SDA. Selection for adaption to external clock rates is shown in Table 3.

Programming of S2 is accomplished via the parallel-bus when A0 = LOW, with the appropriate bit combinations set in control status register S1 (S1 is written when A0 = HIGH). Bit combinations for accessing all registers are given in Table 5.

Table 3 Register S2 selection of clock frequency

INTERNAL CLOCK FREQUENCY			
S24	S23	S22	f_{clk} (MHz)
0	X[1]	X[1]	3
1	0	0	4.43
1	0	1	6
1	1	0	8
1	1	1	12

Note

1. X = don't care.

6.6 Interrupt vector S3

The interrupt vector register provides an 8-bit user-programmable vector for vectored-interrupt microcontrollers. The vector is sent to the bus port (DB7 to DB0) when an interrupt acknowledge signal is asserted and the ENI (enable interrupt) flag is set. Default vector values are:

- Vector is '00H' in 80XX mode
- Vector is '0FH' in 68000 mode.

On reset the PCF8584 is in the 80XX mode, thus the default interrupt vector is '00H'.

6.7 Data shift register/read buffer S0

Register S0 acts as serial shift register and read buffer interfacing to the I²C-bus. All read and write operations to/from the I²C-bus are done via this register. S0 is a combination of a shift register and a data buffer; parallel data is always written to the shift register, and read from the data buffer. I²C-bus data is always shifted in or out of shift register S0.

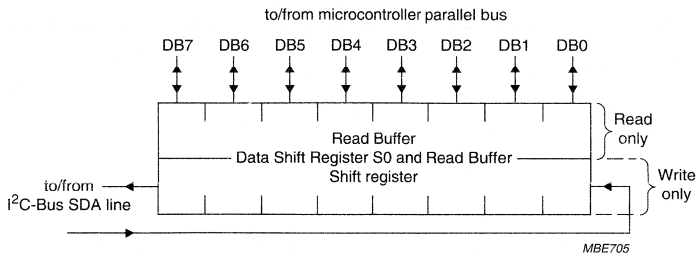


Fig.4 Data shift register/bus buffer S0.

In receiver mode the data from the shift register is copied to the read buffer during the acknowledge phase. Further reception of data is inhibited (SCL held LOW) until the S0 read buffer is read (see Section 6.8.1.1).

In the transmitter mode data is transmitted to the I²C-bus as soon as it is written to the S0 shift register if the serial I/O is enabled (ESO = 1).

Remarks:

1. A minimum of 6 clock cycles must elapse between consecutive parallel-bus accesses to the PCF8584 when the I²C-bus controller operates at 8 or 12 MHz. This may be reduced to 3 clock cycles for lower operating frequencies.
2. To start a read operation immediately after a write, it is necessary to read the S0 read buffer in order to invoke reception of the first byte ('dummy read' of the address). Immediately after the acknowledgement, this first byte will be transferred from the shift register to the read buffer. The **next** read will then transfer the correct value of the first byte to the microcontroller bus (see Fig.7).

6.8 Control/status register S1

Register S1 controls I²C-bus operation and provides I²C-bus status information. Register S1 is accessed by a HIGH signal on register select input A0. For more efficient communication between microcontroller/processor and the I²C-bus, register S1 has separate read and write functions for all bit positions (see Fig.3). The write-only section provides register access control and control over I²C-bus signals, while the read-only section provides I²C-bus status information.

Table 4 Control/status register S1

CONTROL/STATUS	BITS								MODE
Control[1]	PIN	ESO	ES1	ES2	ENI	STA	STO	ACK	write only
Status[2]	PIN	0[3]	STS	BER	AD0/LRB	AAS	LAB	$\overline{BB}$	read only

Notes

1. For further information see Section 6.8.1.
2. For further information see Section 6.8.2.
3. Logic 1 if not-initialized.

6.8.1 REGISTER S1 CONTROL SECTION

The write-only section of S1 enables access to registers S0, S0', S1, S2 and S3, and controls I²C-bus operation; see Table 4.

6.8.1.1 PIN (Pending Interrupt Not)

When the PIN bit is written with a logic 1, all status bits are reset to logic 0. This may serve as a software reset function (see Figs 5 to 9). PIN is the only bit in S1 which may be both read and written to. PIN is mostly used as a status bit for synchronizing serial communication, see Section 6.8.2.

6.8.1.2 ESO (Enable Serial Output)

ESO enables or disables the serial I²C-bus I/O. When ESO is LOW, register access for initialization is possible. When ESO is HIGH, I²C-bus communication is enabled; communication with serial shift register S0 is enabled and the S1 bus status bits are made available for reading.

Table 5 Register access control; ESO = 0 (serial interface off) and ESO = 1 (serial interface on)

INTERNAL REGISTER ADDRESSING 2-WIRE MODE				
A0	**ES1**	**ES2**	**$\overline{\text{IACK}}$**	**FUNCTION**
ESO = 0; serial interface off (see note 1)				
1	0	X	1(2)	R/W S1: control
0	0	0	1(2)	R/W S0': (own address)
0	0	1	1(2)	R/W S3: (interrupt vector)
0	1	0	1(2)	R/W S2: (clock register)
ESO = 1; serial interface on				
1	0	X	1	W S1: control
1	0	X	1	R S1; status
0	0	0	1	R/W S0: (data)
0	0	1	1	R/W S3: (interrupt vector)
X	0	X	0	R S3: (interrupt vector ACK cycle))

Notes

1. With ESO = 0, bits ENI, STA, STO and ACK of S1 can be read for test purposes.
2. 'X' if ENI = 0.

6.8.1.3 ES1 and ES2

ES1 and ES2 control selection of other registers for initialization and control of normal operation. After these bits are programmed for access to the desired register (shown in Table 5), the register is selected by a logic LOW level on register select pin A0.

6.8.1.4 ENI

This bit enables the external interrupt output $\overline{\text{INT}}$, which is generated when the PIN bit is active (logic 0).

This bit must be set to logic 0 before entering the long-distance mode, and remain at logic 0 during operation in long-distance mode.

6.8.1.5 STA and STO

These bits control the generation of the I²C-bus START condition and transmission of slave address and R/$\overline{W}$ bit, generation of repeated START condition, and generation of the STOP condition (see Table 7).

Table 6 Register access control; ESO = 1 (serial interface on) and ES1 = 1; long-distance (4-wire) mode; note 1

INTERNAL REGISTER ADDRESSING: LONG-DISTANCE (4-WIRE) MODE				
A0	**ES1**	**ES2**	**$\overline{IACK}$**	**FUNCTION**
1	1	X	1	W S1: control
1	1	X	X	R S1; status
0	1	X	X	R/W S0; (data)

Note

1. Trying to read from or write to registers other than S0 and S1 (setting ESO = 0) brings the PCF8584 out of the long-distance mode.

Table 7 Instruction table for serial bus control

STA	STO	PRESENT MODE	FUNCTION	OPERATION
1	0	SLV/REC	START	transmit START + address, remain MST/TRM if R/$\overline{W}$ = 0; go to MST/REC if R/$\overline{W}$ = 1
1	0	MST/TRM	REPEAT START	same as for SLV/REC
0	1	MST/REC; MST/TRM	STOP READ; STOP WRITE	transmit STOP go to SLV/REC mode; note 1
1	1	MST	DATA CHAINING	send STOP, START and address after last master frame without STOP sent; note 2
0	0	ANY	NOP	no operation; note 3

Notes

1. In master receiver mode, the last byte must be terminated with ACK bit HIGH ('negative acknowledge').
2. If both STA and STO are set HIGH simultaneously in master mode, a STOP condition followed by a START condition + address will be generated. This allows 'chaining' of transmissions without relinquishing bus control.
3. All other STA and STO mode combinations not mentioned in Table 7 are NOPs.

6.8.1.6 ACK

This bit must be set normally to a logic 1. This causes the I²C-bus controller to send an acknowledge automatically after each byte (this occurs during the 9th clock pulse). The bit must be reset (to logic 0) when the I²C-bus controller is operating in master/receiver mode and requires no further data to be sent from the slave transmitter. This causes a negative acknowledge on the I²C-bus, which halts further transmission from the slave device.

6.8.2 REGISTER S1 STATUS SECTION

The read-only section of S1 enables access to I²C-bus status information; see Table 4.

6.8.2.1 PIN bit

'Pending Interrupt Not' (MSB of register S1) is a status flag which is used to synchronize serial communication and is set to logic 0 whenever the PCF8584 requires servicing. The PIN bit is normally read in polled applications to determine when an I²C-bus byte transmission/reception is completed. The PIN bit may also be written, see Section 6.8.1.

Each time a serial data transmission is initiated (by setting the STA bit in the same register), the PIN bit will be set to logic 1 automatically (inactive). When acting as transmitter, PIN is also set to logic 1 (inactive) each time S0 is written. In receiver mode, the PIN bit is automatically set to logic 1 (inactive) each time the data register S0 is read.

After transmission or reception of one byte on the I²C-bus (9 clock pulses, including acknowledge), the PIN bit will be automatically reset to logic 0 (active) indicating a complete byte transmission/reception. When the PIN bit is subsequently set to logic 1 (inactive), all status bits will be reset to logic 0. PIN is also set to zero on a BER (bus error) condition.

In polled applications, the PIN bit is tested to determine when a serial transmission/reception has been completed. When the ENI bit (bit 4 of write-only section of register S1) is also set to logic 1 the hardware interrupt is enabled. In this case, the PIN flag also triggers an external interrupt (active LOW) via the $\overline{INT}$ output each time PIN is reset to logic 0 (active).

When acting as slave transmitter or slave receiver, while PIN = 0, the PCF8584 will suspend I²C-bus transmission by holding the SCL line LOW until the PIN bit is set to logic 1 (inactive). This prevents further data from being transmitted or received until the current data byte in S0 has been read (when acting as slave receiver) or the next data byte is written to S0 (when acting as slave transmitter).

PIN bit summary:

- The PIN bit can be used in polled applications to test when a serial transmission has been completed. When the ENI bit is also set, the PIN flag sets the external interrupt via the $\overline{INT}$ output.
- Setting the STA bit (start bit) will set PIN = 1 (inactive).
- In transmitter mode, after successful transmission of one byte on the I²C-bus the PIN bit will be automatically reset to logic 0 (active) indicating a complete byte transmission.
- In transmitter mode, PIN is set to logic 1 (inactive) each time register S0 is written.
- In receiver mode, PIN is set to logic 0 (active) on completion of each received byte. Subsequently, the SCL line will be held LOW until PIN is set to logic 1.
- In receiver mode, when register S0 is read, PIN is set to logic 1 (inactive).
- In slave receiver mode, an I²C-bus STOP condition will set PIN = 0 (active).
- PIN = 0 if a bus error (BER) occurs.

6.8.2.2 STS

When in slave receiver mode, this flag is asserted when an externally generated STOP condition is detected (used only in slave receiver mode).

6.8.2.3 BER

Bus error; a misplaced START or STOP condition has been detected. Resets $\overline{BB}$ (to logic 1; inactive), sets PIN = 0 (active).

6.8.2.4 LRB/AD0

'Last Received Bit' or 'Address 0 (General Call) bit'. This status bit serves a dual function, and is valid only while PIN = 0:

1. LRB holds the value of the last received bit over the I²C-bus while AAS = 0 (not addressed as slave). Normally this will be the value of the slave acknowledgement; thus checking for slave acknowledgement is done via testing of the LRB.
2. AD0; when AAS = 1 ('Addressed As Slave' condition), the I²C-bus controller has been addressed as a slave. Under this condition, this bit becomes the 'AD0' bit and will be set to logic 1 if the slave address received was the 'general call' (00H) address, or logic 0 if it was the I²C-bus controller's own slave address.

6.8.2.5 AAS

'Addressed As Slave' bit. Valid only when PIN = 0. When acting as slave receiver, this flag is set when an incoming address over the I²C-bus matches the value in own address register S0' (shifted by one bit, see Section 6.4), or if the I²C-bus 'General Call' address (00H) has been received ('General Call' is indicated when AD0 status bit is also set to logic 1, see Section 6.8.2.4).

6.8.2.6 LAB

'Lost Arbitration' Bit. This bit is set when, in multi-master operation, arbitration is lost to another master on the I²C-bus.

6.8.2.7 $\overline{BB}$

'Bus Busy' bit. This is a read-only flag indicating when the I²C-bus is in use. A zero indicates that the bus is busy, and access is not possible. This bit is set/reset (logic 1/logic 0) by STOP/START conditions.

6.9 Multi-master operation

To avoid conflict between data and repeated START and STOP operations, multi-master systems have some limitations:

- When powering up multiple PCF8584s in multi-master systems, the possibility exists that one node may power up slightly after another node has already begun an I²C-bus transmission; the Bus Busy condition will thus not have been detected. To avoid this condition, a delay should be introduced in the initialization sequence of each PCF8584 equal to the longest I²C-bus transmission, see flowchart 'PCF8584 initialization' (Fig.5).

6.10 Reset

A LOW level pulse on the $\overline{RESET}$ (CLK must run) input forces the I²C-bus controller into a well-defined state. All flags in S1 are reset to logic 0, except the PIN flag and the $\overline{BB}$ flag, which are set to logic 1. S0' and S3 are set to 00H.

The $\overline{RESET}$ pin is also used for the $\overline{STROBE}$ output signal. Both functions are separated on-chip by a digital filter. The reset input signal has to be sufficiently long (minimum 30 clock cycles) to pass through the filter. The $\overline{STROBE}$ output signal is sufficiently short (8 clock cycles) to be blocked by the filter. For more detailed information on the strobe function see Section 6.12.

6.11 Comparison to the MAB8400 I²C-bus interface

The structure of the PCF8584 is similar to that of the MAB8400 series of microcontrollers, but with a modified control structure. Access to all I²C-bus control and status registers is done via the parallel-bus port in conjunction with register select input A0, and control bits ESO, ES1 and ES2.

6.11.1 DELETED FUNCTIONS

The following functions are not available in the PCF8584:

- Always selected (ALS flag)
- Access to the bit counter (BC0 to BC2)
- Full SCL frequency selection (2 bits instead of 5 bits)
- The non-acknowledge mode (ACK flag)
- Asymmetrical clock (ASC flag).

6.11.2 ADDED FUNCTIONS

The following functions either replace the deleted functions or are completely new:

- Chip clock prescaler
- Assert acknowledge bit (ACK flag)
- Register selection bits (ES1 and ES2 flags)
- Additional status flags (BER, 'bus error')
- Automatic interface control between 80XX and 68000-type microcontrollers
- Programmable interrupt vector
- Strobe generator
- Bus monitor function
- Long-distance mode [non-I²C-bus mode (4-wire); only for communication between parallel-bus processors using the PCF8584 at each interface point].

6.12 Special function modes

6.12.1 STROBE

When the I²C-bus controller receives its own address (or the '00H' general call address) followed immediately by a STOP condition (i.e. no further data transmitted after the address), a strobe output signal is generated at the $\overline{RESET}/\overline{STROBE}$ pin (pin 19). The $\overline{STROBE}$ signal consists of a monostable output pulse (active LOW), 8 clock cycles long (see Fig.9). It is generated after the STOP condition is received, preceded by the correct slave address. This output can be used as a bus access controller for multi-master parallel-bus systems.

6.12.2 LONG-DISTANCE MODE

The long-distance mode provides the possibility of longer-distance serial communication between parallel processors via two I²C-bus controllers. This mode is selected by setting ES1 to logic 1 while the serial interface is enabled (ESO = 1).

In this mode the I²C-bus protocol is transmitted over 4 unidirectional lines, SDA OUT, SCL IN, SDA IN and SCL IN (pins 2, 3, 4 and 5). These communication lines should be connected to line drivers/receivers (example: RS422) for long-distance applications. Hardware characteristics for long-distance transmission are then given by the chosen standard. Control of data transmission is the same as in normal I²C-bus mode. After reading or writing data to shift register S0, long-distance mode must be initialized by setting ESO and ES1 to logic 1. Because the interrupt output $\overline{INT}$ is not available in this operating mode, synchronization of data transmission/reception must be polled via the PIN bit.

Remarks:

Before entering the long-distance mode, ENI must be set to logic 0.

When powering up an PCF8584-node in long-distance mode, the PCF8584 must be isolated from the 4-wire bus via 3-state line drivers/receivers until the PCF8584 is properly initialized for long-distance mode. Failure to implement this precaution will result in system malfunction.

6.12.3 MONITOR MODE

When the 7-bit own address register S0' is loaded with all zeros, the I²C-bus controller acts as a passive I²C monitor. The main features of the monitor mode are:

- The controller is always selected.
- The controller is always in the slave receiver mode.
- The controller never generates an acknowledge.
- The controller never generates an interrupt request.
- A pending interrupt condition does not force SCL LOW.
- $\overline{BB}$ is set to logic 0 after detection of a START condition, and reset to logic 1 after a STOP condition.
- Received data is automatically transferred to the read buffer.
- Bus traffic is monitored by the PIN bit, which is reset to logic 0 after the acknowledge bit of an incoming byte has been received, and is set to logic 1 as soon as the first bit of the next incoming byte is detected. Reading the data buffer S0 sets the PIN bit to logic 1. Data in the read buffer is valid from PIN = 0 and during the next 8 clock pulses (until next acknowledge).
- AAS is set to logic 1 at every START condition, and reset at every 9th clock pulse.

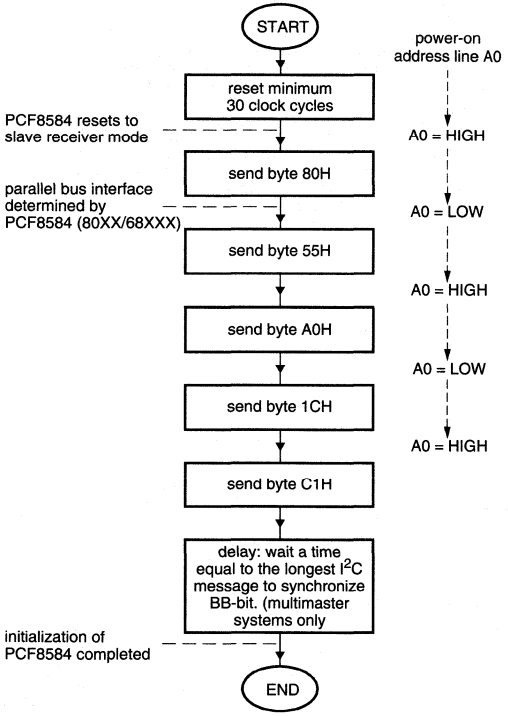
7 SOFTWARE FLOWCHART EXAMPLES

7.1 Initialization

The flowchart of Fig.5 gives an example of a proper initialization sequence of the PCF8584.

7.2 Implementation

The flowcharts (Figs 6 to 9) illustrate proper programming sequences for implementing master transmitter, master receive, and master transmitter, repeated start and master receiver modes in polled applications.



A0 = HIGH	enables data transfer to/from register S1
A0 = LOW	Access to all other registers defined by the bit pattern in register S1

Loads byte 80H into register S1'
i.e. next byte will be loaded into register S0'
(own address register); serial interface off.

Loads byte 55H into register S0';
effective own address becomes AAH.

Loads byte A0H into register S1, i.e. next byte will be loaded into the clock control register S2.

Loads byte 1CH into register S2;
system clock is 12 MHz; SCL = 90 kHz.

Loads byte C1H into register S1; register enable serial interface, set I²C-bus into idle mode; SDA and SCL are HIGH. The next write or read operation will be to/from data transfer register S0 if A0 = LOW.

On power-on, if an PCF8584 node is powered-up slightly after another node has already begun an I²C-bus transmission, the bus busy condition will not have been detected. Thus, introducing this delay will insure that this condition will not occur.

MBE714

Fig.5 PCF8584 initialization sequence.

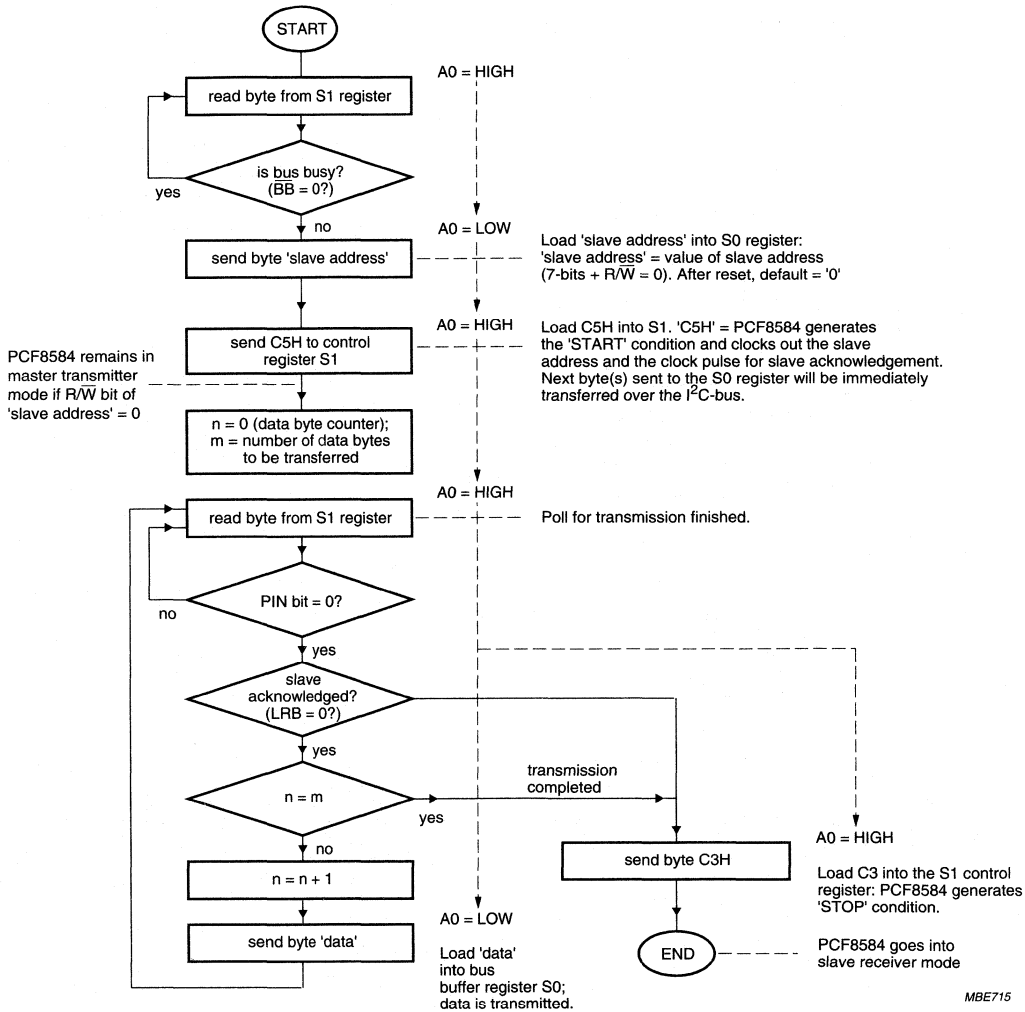
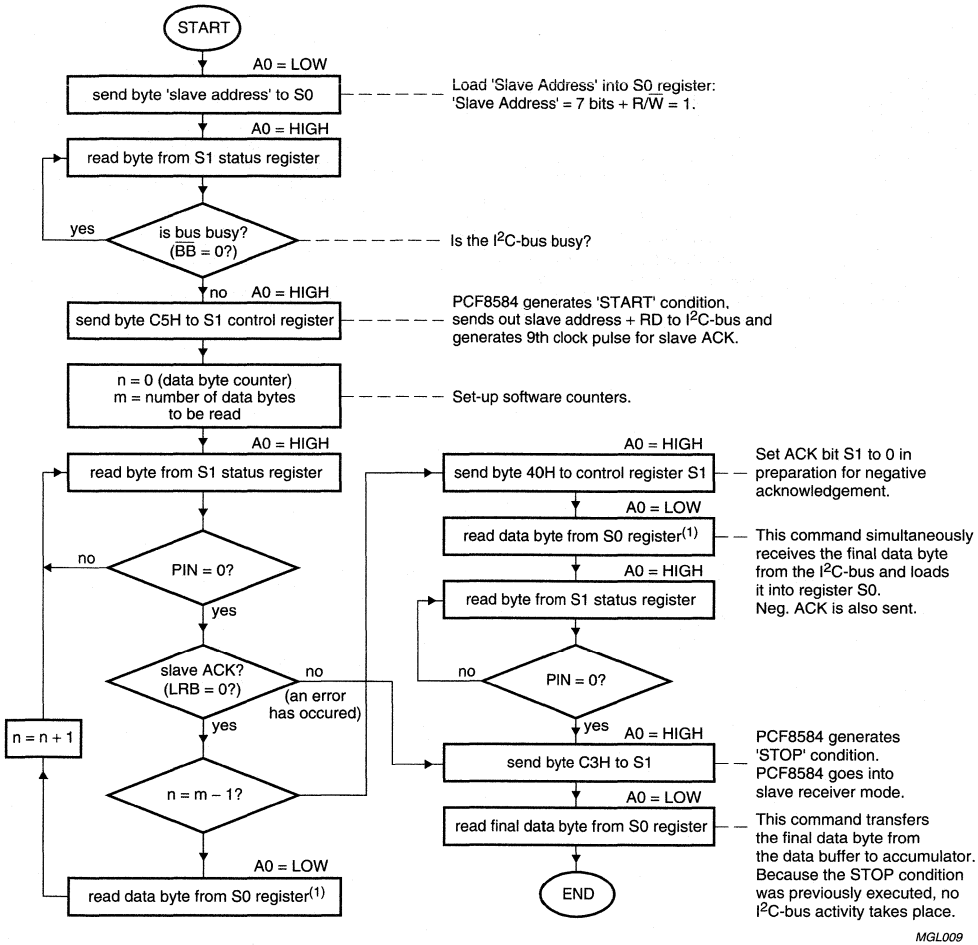


Fig.6 PCF8584 master transmitter mode.



(1) The first read of the S0 register is a 'dummy read' of the slave address which should be discarded. The first read of the S0 register simultaneously reads the current value of S0 and then transfers the first valid data byte from the I²C-bus to S0.

Fig.7 PCF8584 master receiver mode.

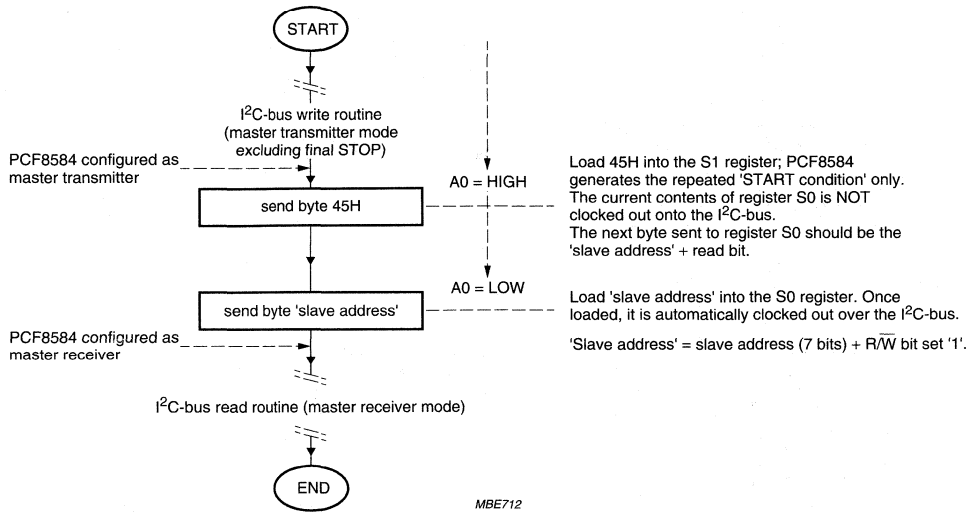


Fig.8 Master transmitter followed by repeated START and becoming master receiver.

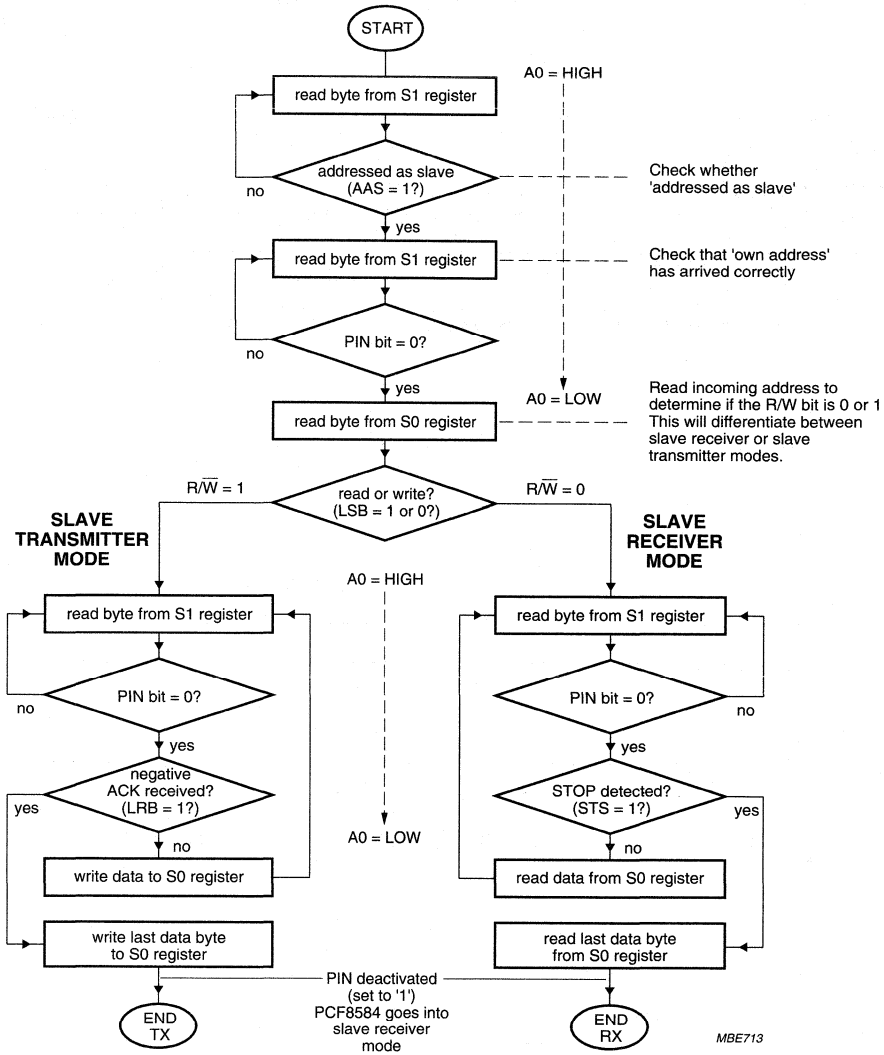
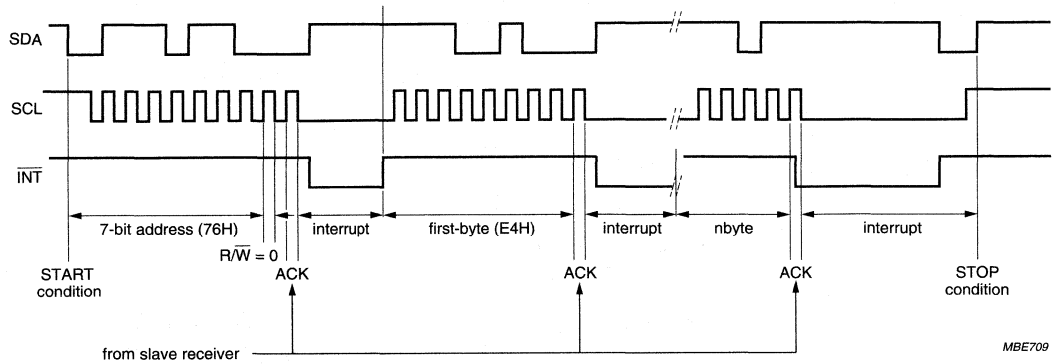


Fig.9 Slave receiver/slave transmitter modes.

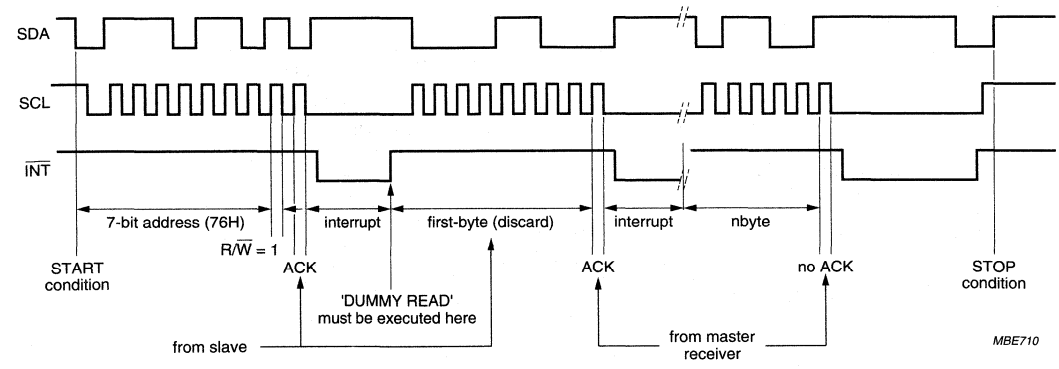
8 I²C-BUS TIMING DIAGRAMS

The diagrams (Figs 10 to 13) illustrate typical timing diagrams for the PCF8584 in master/slave functions. For detailed description of the I²C-bus protocol, please refer to *"The I²C-bus and how to use it"*; Philips document ordering number 9398 393 40011.



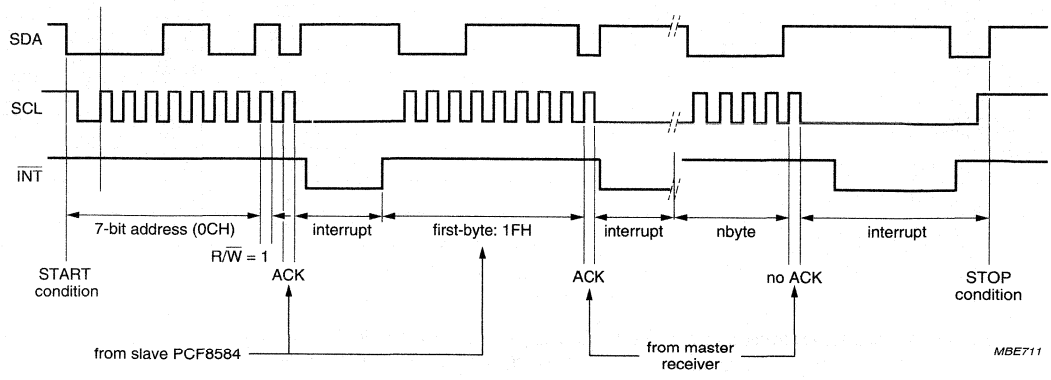
Master PCF8584 writes data to slave transmitter.

Fig.10 Bus timing diagram; master transmitter mode.



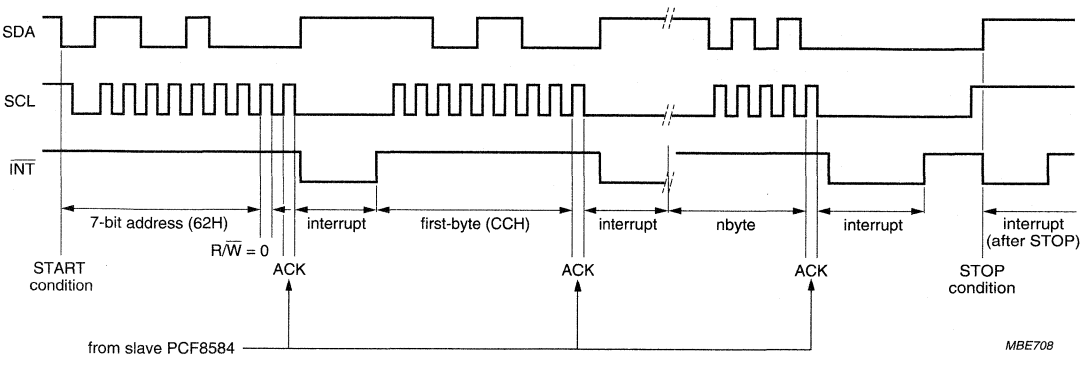
Master PCF8584 reads data from slave transmitter.

Fig.11 Bus timing diagram; master receiver mode.



External master receiver reads data from PCF8584.

Fig.12 Bus timing diagram; slave transmitter mode.



Slave PCF8584 is written to by external master transmitter.

Fig.13 Bus timing diagram; slave receiver mode.

9 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.3	+7.0	V
V_I	voltage range (any input)	−0.8	V_{DD} + 0.5	V
I_I	DC input current (any input)	−10	+10	mA
I_O	DC output current (any output)	−10	+10	mA
P_{tot}	total power dissipation	−	300	mW
P_O	power dissipation per output	−	50	mW
T_{amb}	operating ambient temperature	−40	+85	°C
T_{stg}	storage temperature	−65	+150	°C

10 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is good practice to take normal precautions appropriate to handling MOS devices (see *"Handling MOS Devices"*).

11 DC CHARACTERISTICS

V_{DD} = 5 V ±10%; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		4.5	5.0	5.5	V
I_{DD}	supply current	standby; note 1	–	–	2.5	μA
		operating; notes 1 and 2	–	–	1.5	mA
Inputs						
CLK, $\overline{IACK}$, A0, $\overline{CS}$, $\overline{WR}$, $\overline{RD}$, $\overline{RESET}$ AND D0 to D7						
V_{IL}	LOW level input voltage	note 3	0	–	0.8	V
V_{IH}	HIGH level input voltage	note 3	2.0	–	V_{DD}	V
SDA AND SCL						
V_{IL}	LOW level input voltage	note 4	0	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage	note 4	$0.7V_{DD}$	–	V_{DD}	V
R_i	resistance to V_{DD}	T_{amb} = 25 °C; note 5	25	–	100	kΩ
Outputs						
I_{OH}	HIGH level output current	V_{OH} = 2.4 V; note 6 and 7	−2.4	–	–	mA
I_{OL}	LOW level output current	V_{OL} = 0.4 V; note 6	3.0	–	–	mA
I_{OL}	leakage current	note 8	−1	–	+1	μA

Notes

1. Test conditions: 22 kΩ pull-up resistors on D0 to D7; 10 kΩ pull-up resistors on SDA, SCL, $\overline{RD}$; $\overline{RESET}$ connected to V_{SS}; remaining pins open-circuit.
2. CLK waveform of 12 MHz with 50% duty factor.
3. CLK, $\overline{IACK}$, A0, $\overline{CS}$, $\overline{WR}$, $\overline{RD}$, $\overline{RESET}$ and D0 to D7 are TTL level inputs.
4. SDA and SCL are CMOS level inputs.
5. CLK, $\overline{IACK}$, A0, $\overline{CS}$ and $\overline{WR}$.
6. D0 to D7.
7. $\overline{DTACK}$, $\overline{STROBE}$.
8. D0 to D7 3-state, SDA, SCL, $\overline{INT}$, $\overline{RD}$, $\overline{RESET}$.

12 I²C-BUS TIMING SPECIFICATIONS

All the timing limits are valid within the operating supply voltage and ambient temperature range; V_{DD} = 5 V ±10%; T_{amb} = −40 to +85 °C; and refer to V_{IL} and V_{IH} with an input voltage of V_{SS} to V_{DD}.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
f_{SCL}	SCL clock frequency	–	–	100	kHz
t_{SW}	tolerable spike width on bus	–	–	100	ns
t_{BUF}	bus free time	4.7	–	–	µs
$t_{SU;STA}$	START condition set-up time	4.7	–	–	µs
$t_{HD;STA}$	START condition hold time	4.0	–	–	µs
t_{LOW}	SCL LOW time	4.7	–	–	µs
t_{HIGH}	SCL HIGH time	4.0	–	–	µs
t_r	SCL and SDA rise time	–	–	1.0	µs
t_f	SCL and SDA fall time	–	–	0.3	µs
$t_{SU;DAT}$	data set-up time	250	–	–	ns
$t_{HD;DAT}$	data hold time	0	–	–	ns
$t_{VD;DAT}$	SCL LOW to data out valid	–	–	3.4	µs
$t_{SU;STO}$	STOP condition set-up time	4.0	–	–	µs

13 PARALLEL INTERFACE TIMING

All the timing limits are valid within the operating supply voltage and ambient temperature range: V_{DD} = 5 V ±10%; T_{amb} = −40 to +85 °C; and refer to V_{IL} and V_{IH} with an input voltage of V_{SS} to V_{DD}. C_L = 100 pF; R_L = 1.5 kΩ (connected to V_{DD}) for open-drain and high-impedance outputs, where applicable (for measurement purposes only).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_r	clock rise time	see Fig.14	–	–	6	ns
t_f	clock fall time	see Fig.14	–	–	6	ns
t_{CLK}	input clock period (50% ±5% duty factor)	see Fig.14	83	–	333	ns
t_{CLRL}	$\overline{CS}$ set-up to $\overline{RD}$ LOW	see Fig.16 and note 1	20	–	–	ns
t_{CLWL}	$\overline{CS}$ set-up to $\overline{WR}$ LOW	see Fig.15 and note 1	20	–	–	ns
t_{RHCH}	$\overline{CS}$ hold from $\overline{RD}$ HIGH	see Fig.16	0	–	–	ns
t_{WHCH}	$\overline{CS}$ hold from $\overline{WR}$ HIGH	see Fig.15	0	–	–	ns
t_{AVWL}	A0 set-up to $\overline{WR}$ LOW	see Fig.15	10	–	–	ns
t_{AVRL}	A0 set-up to $\overline{RD}$ LOW	see Fig.16	10	–	–	ns
t_{WHAI}	A0 hold from $\overline{WR}$ HIGH	see Fig.15	20	–	–	ns
t_{RHAI}	A0 hold from $\overline{RD}$ HIGH	see Fig.16	10	–	–	ns
t_{WLWH}	WR pulse width	see Fig.15	230	–	1000	ns
t_{RLRH}	$\overline{RD}$ pulse width	see Fig.16	230	–	1000	ns
t_{DVWH}	data set-up before $\overline{WR}$ HIGH	see Fig.15	150	–	–	ns
t_{RLDV}	data valid after $\overline{RD}$ LOW	see Fig.16	–	160	180	ns
t_{WHDI}	data hold after $\overline{WR}$ HIGH	see Fig.15	20	–	–	ns
t_{RHDF}	data bus floating after $\overline{RD}$ HIGH	see Fig.16	–	–	150	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{AVCL}	A0 set-up to $\overline{CS}$ LOW	see Figs 17 and 18	10	–	–	ns
t_{WLCL}	R/$\overline{WR}$ set-up to $\overline{CS}$ LOW	see Fig.17	10	–	–	ns
t_{RHCL}	$\overline{R}$/WR set-up to $\overline{CS}$ LOW	see Fig.18	10	–	–	ns
t_{CLDV}	data valid after $\overline{CS}$ LOW	see Fig.18 and note 2	–	160	180	ns
t_{CLDL}	$\overline{DTACK}$ LOW after $\overline{CS}$ LOW	see Figs 17 and 18	–	$2t_{CLK}$ + 75	$3t_{CLK}$ + 150	ns
t_{CHAI}	A0 hold from $\overline{CS}$ HIGH	see Fig.18	0	–	–	ns
t_{CHRL}	R/$\overline{WR}$ hold from $\overline{CS}$ HIGH	see Fig.18	0	–	–	ns
t_{CHWH}	$\overline{R}$/WR hold from $\overline{CS}$ HIGH	see Fig.17	0	–	–	ns
t_{CHDF}	data bus float after $\overline{CS}$ HIGH	see Fig.18	–	–	150	ns
t_{CHDE}	$\overline{DTACK}$ HIGH from $\overline{CS}$ HIGH	see Figs 17 and 18	–	100	120	ns
t_{CHDI}	data hold after $\overline{CS}$ HIGH	see Fig.17	0	–	–	ns
t_{DVCL}	data set-up to $\overline{CS}$ LOW	see Fig.17	0	–	–	ns
t_{ALIE}	$\overline{INT}$ HIGH from $\overline{IACK}$ LOW	see Figs 19 and 20	–	130	180	ns
t_{ALDV}	data valid after $\overline{IACK}$ LOW	see Figs 19 and 20	–	200	250	ns
t_{ALAE}	$\overline{IACK}$ pulse width	see Fig.20	230	–	–	ns
t_{AHDI}	data hold after $\overline{IACK}$ HIGH	see Fig.20	–	–	30	ns
t_{ALDL}	$\overline{DTACK}$ LOW from $\overline{IACK}$ LOW	see Fig.20	–	$2t_{CLK}$ + 75	$3t_{CLK}$ + 150	ns
t_{AHDE}	$\overline{DTACK}$ HIGH from $\overline{IACK}$ HIGH	see Fig.20	–	120	140	ns
t_{W4}	$\overline{RESET}$ pulse width	see Fig.21	$30t_{CLK}$	–	–	ns
t_{W5}	$\overline{STROBE}$ pulse width	see Fig.22	$8t_{CLK}$	$8t_{CLK}$ + 90	–	ns
t_{CLCL}	$\overline{CS}$ LOW	see Figs 17 and 18	–	t_{CLDL} + t_{CHDE}	–	ns

Notes

1. A minimum of 6 clock cycles must elapse between consecutive parallel-bus accesses when the I²C-bus controller operates at 8 or 12 MHz. This may be reduced to 3 clock cycles for lower operating frequencies.
2. Not for S1.

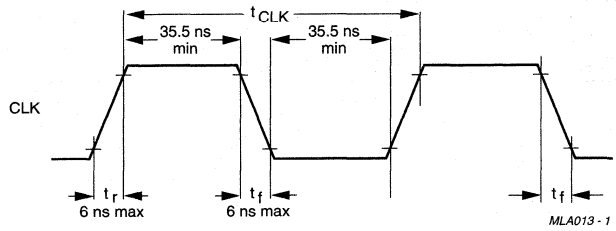


Fig.14 Clock input timing.

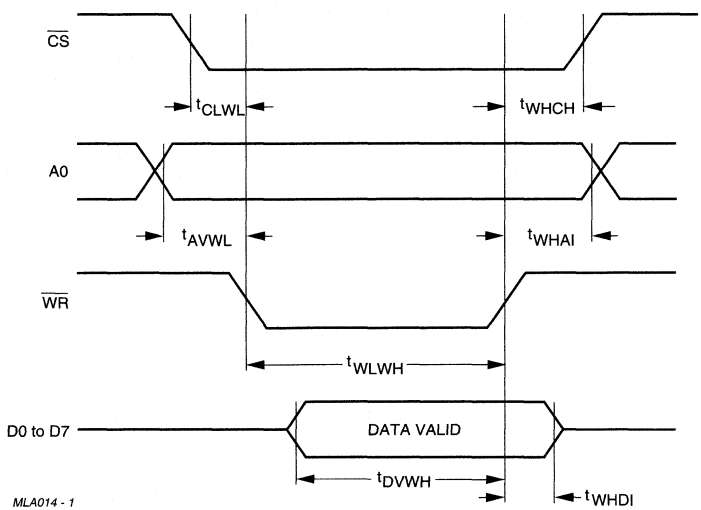


Fig.15 Bus timing (80XX mode); write cycle.

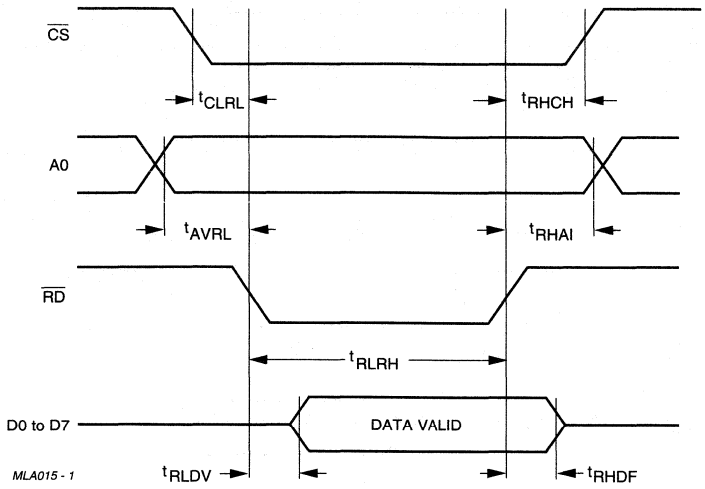


Fig.16 Bus timing (80XX mode); read cycle.

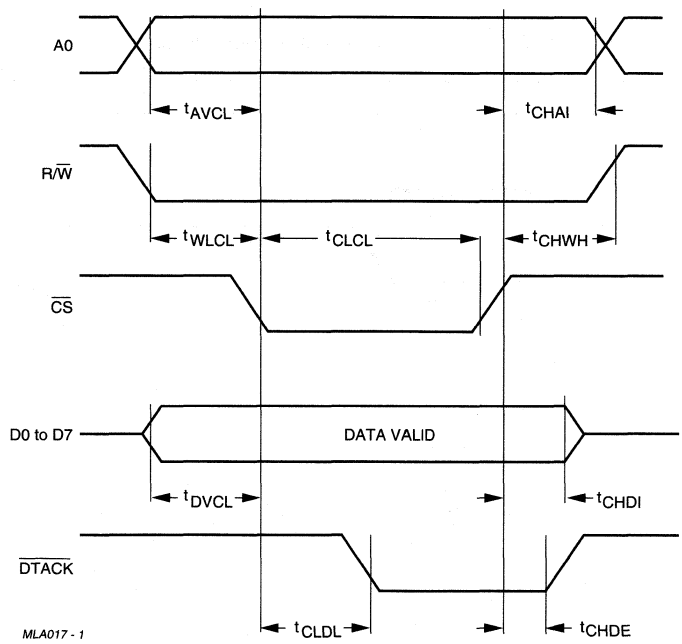


Fig.17 Bus timing (68000 mode); write cycle.

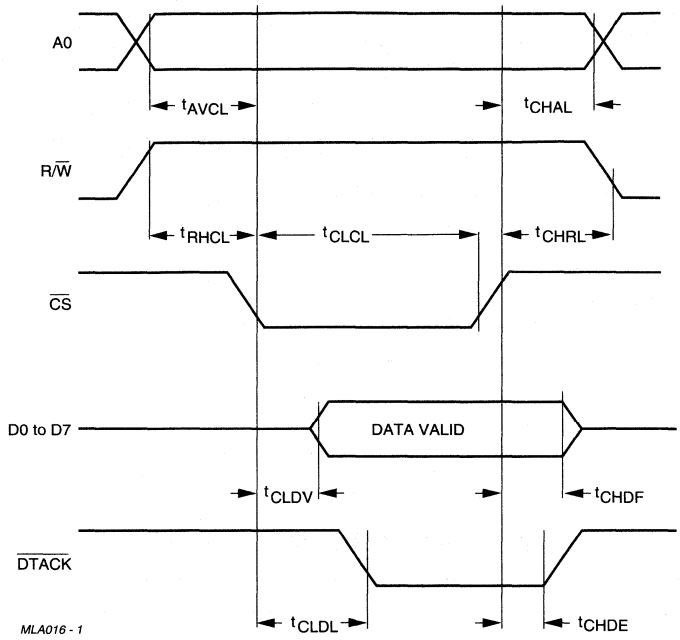


Fig.18 Bus timing (68000 mode); read cycle.

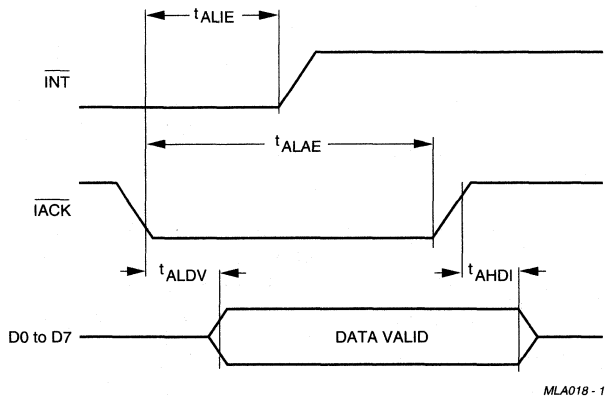


Fig.19 Interrupt timing (80XX mode).

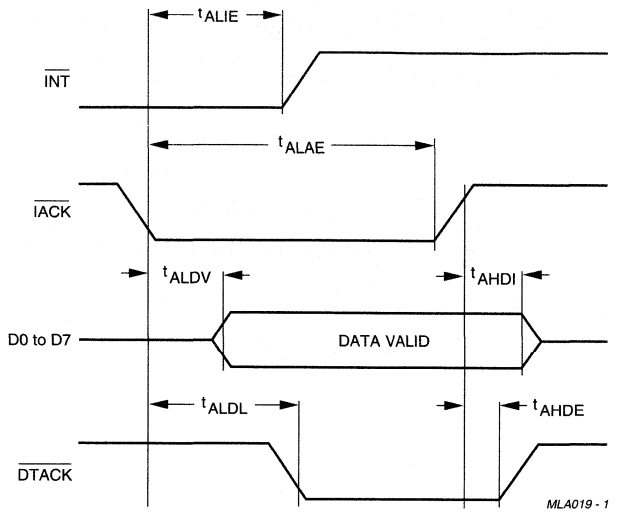


Fig.20 Interrupt timing (68000 mode).

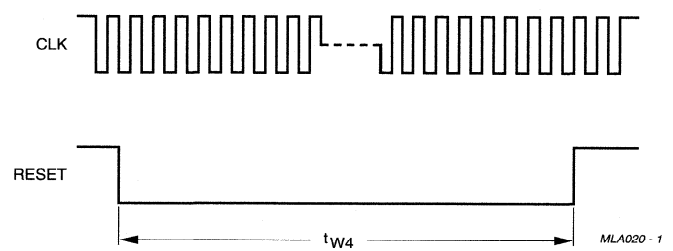


Fig.21 Reset timing.

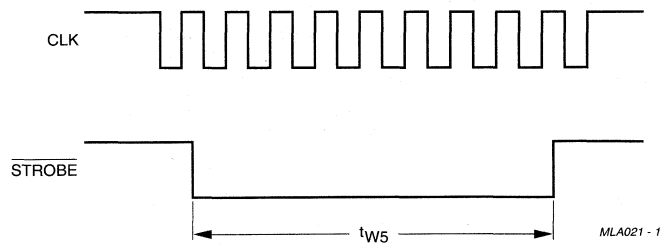


Fig.22 Strobe timing.

14 APPLICATION INFORMATION

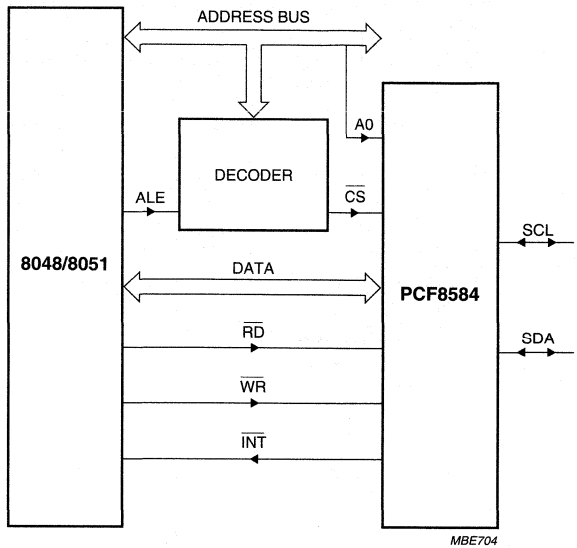


Fig.23 Application diagram using the 8048/8051.

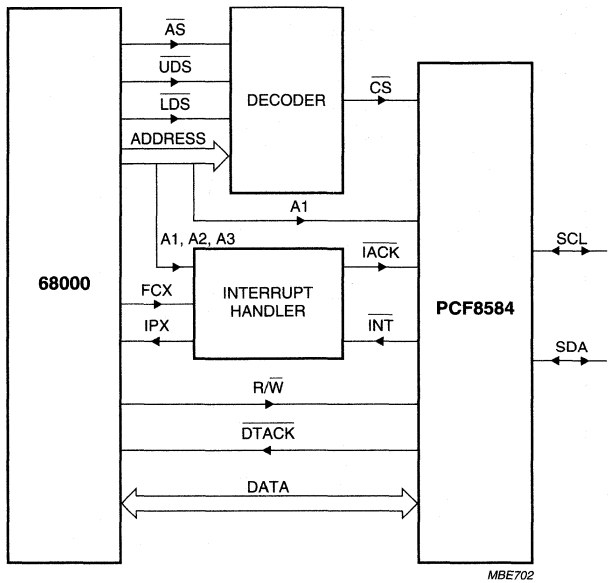


Fig.24 Application diagram using the 68000.

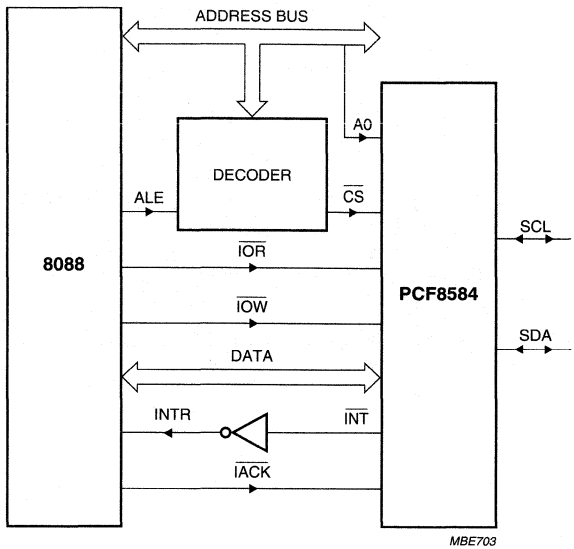
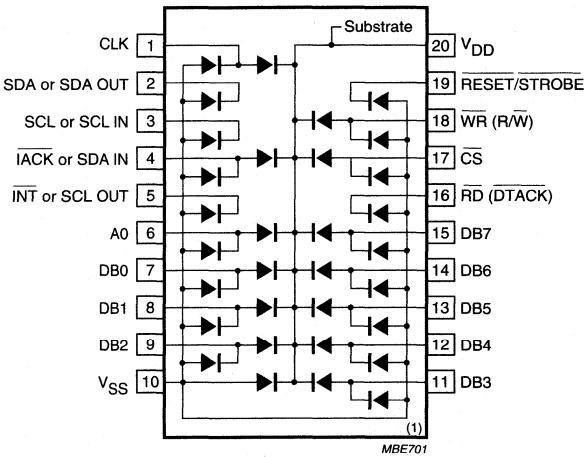


Fig.25 Application diagram using the 8088.



Maximum forward current: 5 mA; maximum reverse voltage: 5 V.

Fig.26 PCF8584 diode protection.

14.1 Application notes

Additional application notes are available from Philips Semiconductors:

1. AN95068: *"C Routines for the PCF8584"*.
2. AN96040: *"Using the PCF8584 with non-specified timings and other frequently asked questions"*.
3. AN90001: *"Interfacing PCF8584 I²C-bus controller to 80(C)51 family of microcontrollers"*.

CONTENTS

8-bit A/D and D/A converter PCF8591

1 FEATURES

- Single power supply
- Operating supply voltage 2.5 V to 6 V
- Low standby current
- Serial input/output via I^2C-bus
- Address by 3 hardware address pins
- Sampling rate given by I^2C-bus speed
- 4 analog inputs programmable as single-ended or differential inputs
- Auto-incremented channel selection
- Analog voltage range from V_{SS} to V_{DD}
- On-chip track and hold circuit
- 8-bit successive approximation A/D conversion
- Multiplying DAC with one analog output.

2 APPLICATIONS

- Closed loop control systems
- Low power converter for remote data acquisition
- Battery operated equipment
- Acquisition of analog values in automotive, audio and TV applications.

3 GENERAL DESCRIPTION

The PCF8591 is a single-chip, single-supply low power 8-bit CMOS data acquisition device with four analog inputs, one analog output and a serial I^2C-bus interface. Three address pins A0, A1 and A2 are used for programming the hardware address, allowing the use of up to eight devices connected to the I^2C-bus without additional hardware. Address, control and data to and from the device are transferred serially via the two-line bidirectional I^2C-bus.

The functions of the device include analog input multiplexing, on-chip track and hold function, 8-bit analog-to-digital conversion and an 8-bit digital-to-analog conversion. The maximum conversion rate is given by the maximum speed of the I^2C-bus.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCA8591P	DIP16	plastic dual in-line package; 16 leads (300 mil); long body	SOT38-1
PCA8591T	SO16	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1

5 BLOCK DIAGRAM

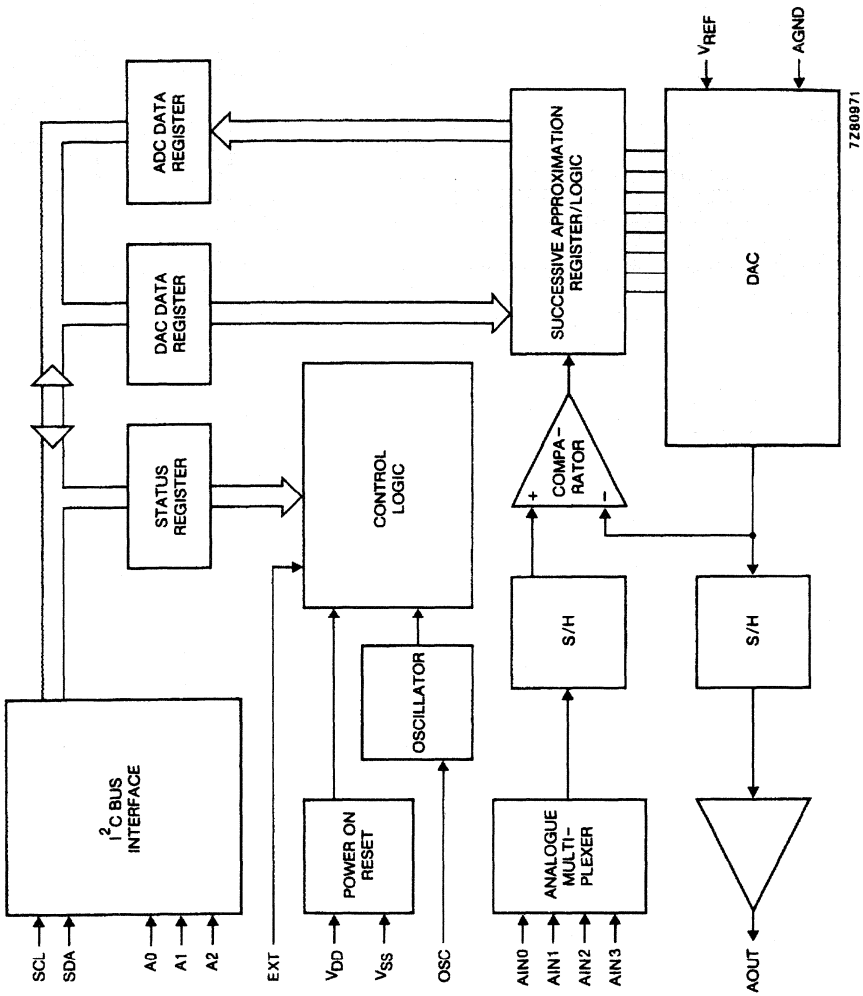


Fig.1 Block diagram.

6 PINNING

SYMBOL	PIN	DESCRIPTION
AINO	1	analog inputs (A/D converter)
AIN1	2	
AIN2	3	
AIN3	4	
A0	5	hardware address
A1	6	
A2	7	
V_{SS}	8	negative supply voltage
SDA	9	I^2C-bus data input/output
SCL	10	I^2C-bus clock input
OSC	11	oscillator input/output
EXT	12	external/internal switch for oscillator input
AGND	13	analog ground
V_{REF}	14	voltage reference input
AOUT	15	analog output (D/A converter)
V_{DD}	16	positive supply voltage

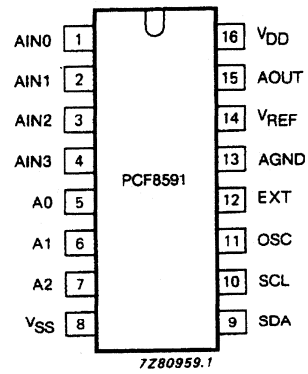


Fig.2 Pinning diagram.

7 FUNCTIONAL DESCRIPTION

7.1 Addressing

Each PCF8591 device in an I²C-bus system is activated by sending a valid address to the device. The address consists of a fixed part and a programmable part. The programmable part must be set according to the address pins A0, A1 and A2. The address always has to be sent as the first byte after the start condition in the I²C-bus protocol. The last bit of the address byte is the read/write-bit which sets the direction of the following data transfer (see Figs 3, 15 and 16).

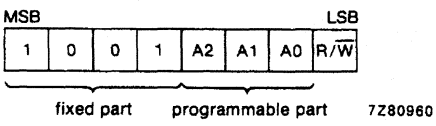


Fig.3 Address byte.

7.2 Control byte

The second byte sent to a PCF8591 device will be stored in its control register and is required to control the device function.

The upper nibble of the control register is used for enabling the analog output, and for programming the analog inputs as single-ended or differential inputs. The lower nibble selects one of the analog input channels defined by the upper nibble (see Fig.4). If the auto-increment flag is set the channel number is incremented automatically after each A/D conversion.

If the auto-increment mode is desired in applications where the internal oscillator is used, the analog output enable flag in the control byte (bit 6) should be set. This allows the internal oscillator to run continuously, thereby preventing conversion errors resulting from oscillator start-up delay. The analog output enable flag may be reset at other times to reduce quiescent power consumption.

The selection of a non-existing input channel results in the highest available channel number being allocated. Therefore, if the auto-increment flag is set, the next selected channel will be always channel 0. The most significant bits of both nibbles are reserved for future functions and have to be set to 0. After a Power-on reset condition all bits of the control register are reset to 0. The D/A converter and the oscillator are disabled for power saving. The analog output is switched to a high-impedance state.

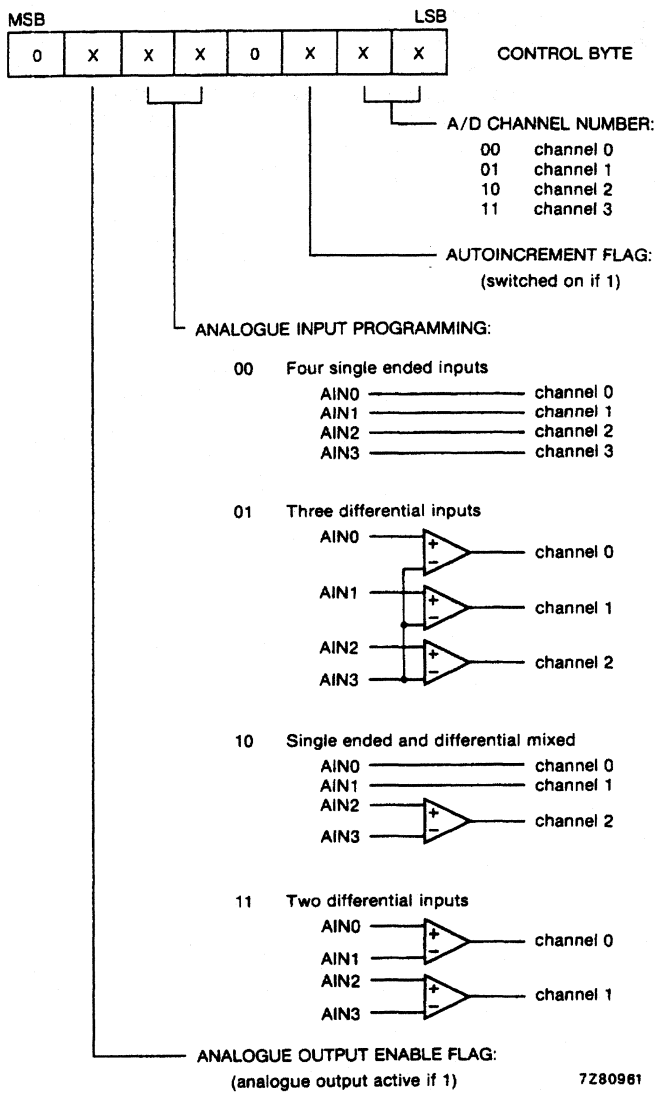


Fig.4 Control byte.

7.3 D/A conversion

The third byte sent to a PCF8591 device is stored in the DAC data register and is converted to the corresponding analog voltage using the on-chip D/A converter. This D/A converter consists of a resistor divider chain connected to the external reference voltage with 256 taps and selection switches. The tap-decoder switches one of these taps to the DAC output line (see Fig.5).

The analog output voltage is buffered by an auto-zeroed unity gain amplifier. This buffer amplifier may be switched on or off by setting the analog output enable flag of the control register. In the active state the output voltage is held until a further data byte is sent.

The on-chip D/A converter is also used for successive approximation A/D conversion. In order to release the DAC for an A/D conversion cycle the unity gain amplifier is equipped with a track and hold circuit. This circuit holds the output voltage while executing the A/D conversion.

The output voltage supplied to the analog output AOUT is given by the formula shown in Fig.6. The waveforms of a D/A conversion sequence are shown in Fig.7.

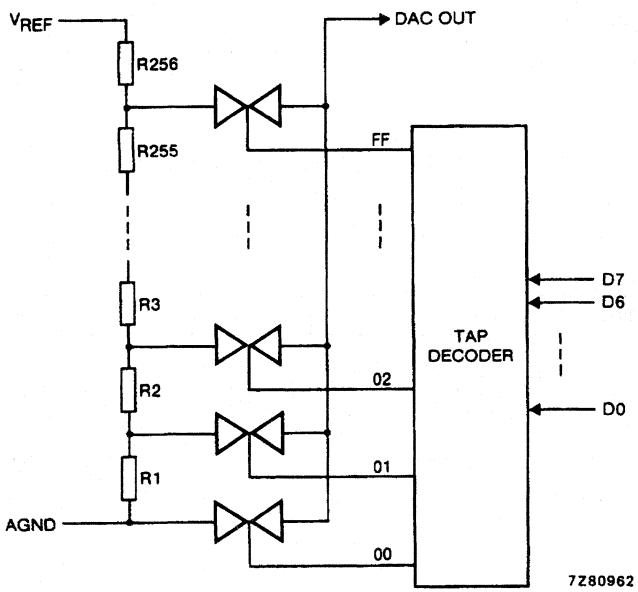


Fig.5 DAC resistor divider chain.

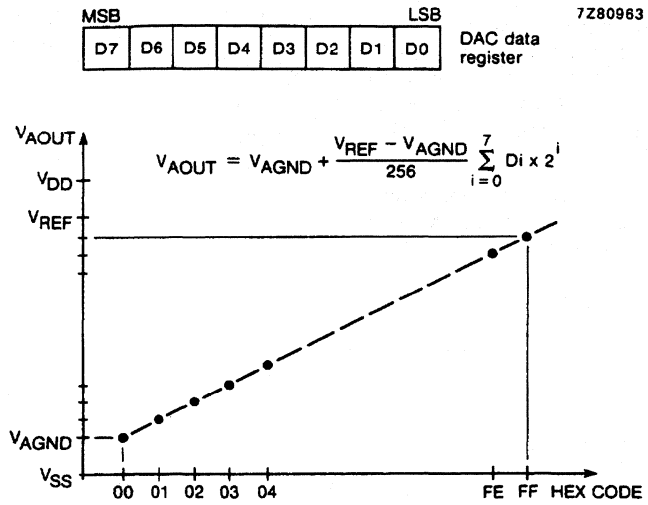


Fig.6 DAC data and DC conversion characteristics.

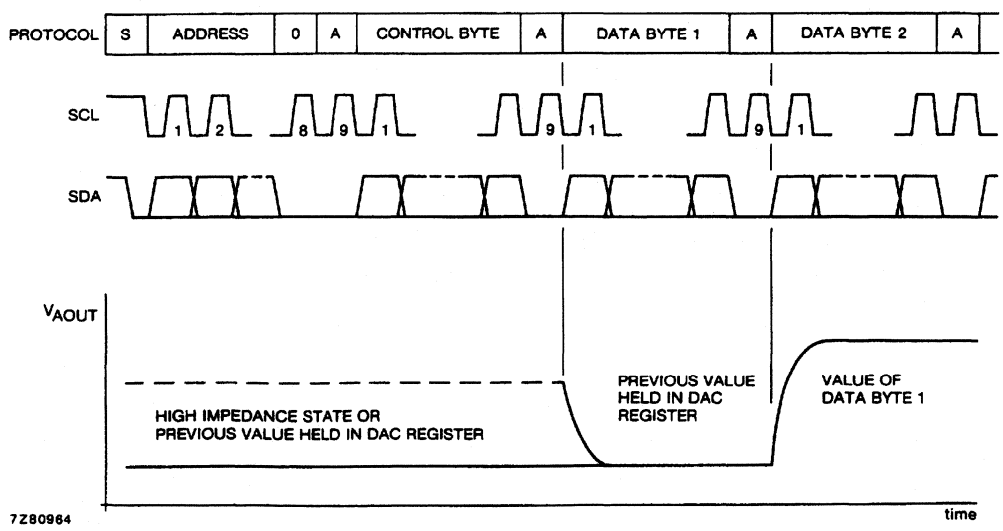


Fig.7 D/A conversion sequence.

7.4 A/D conversion

The A/D converter makes use of the successive approximation conversion technique. The on-chip D/A converter and a high-gain comparator are used temporarily during an A/D conversion cycle.

An A/D conversion cycle is always started after sending a valid read mode address to a PCF8591 device. The A/D conversion cycle is triggered at the trailing edge of the acknowledge clock pulse and is executed while transmitting the result of the previous conversion (see Fig.8).

Once a conversion cycle is triggered an input voltage sample of the selected channel is stored on the chip and is converted to the corresponding 8-bit binary code. Samples picked up from differential inputs are converted to an 8-bit two's complement code (see Figs 9 and 10).

The conversion result is stored in the ADC data register and awaits transmission. If the auto-increment flag is set the next channel is selected.

The first byte transmitted in a read cycle contains the conversion result code of the previous read cycle. After a Power-on reset condition the first byte read is a hexadecimal 80. The protocol of an I^2C-bus read cycle is shown in Chapter 8, Figs 15 and 16.

The maximum A/D conversion rate is given by the actual speed of the I^2C-bus.

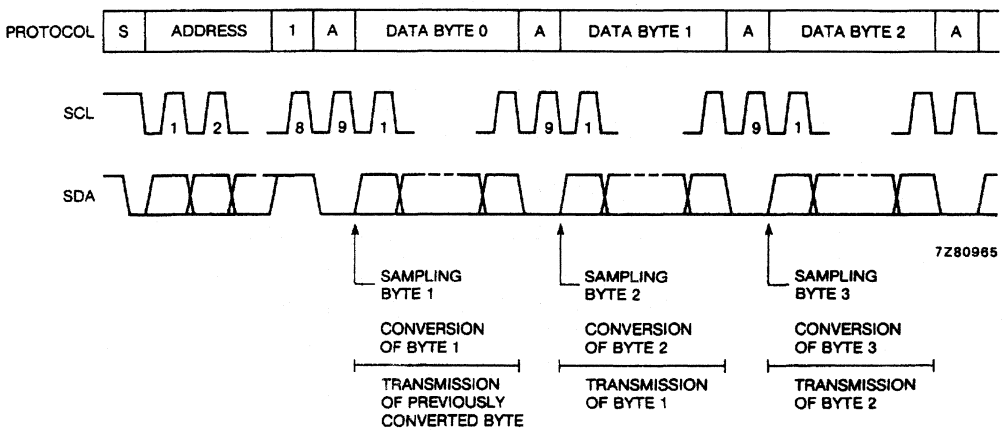


Fig.8 A/D conversion sequence.

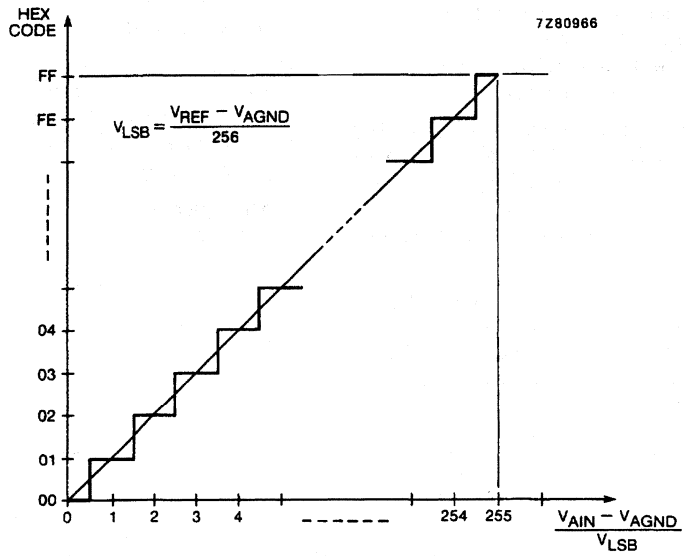


Fig.9 A/D conversion characteristics of single-ended inputs.

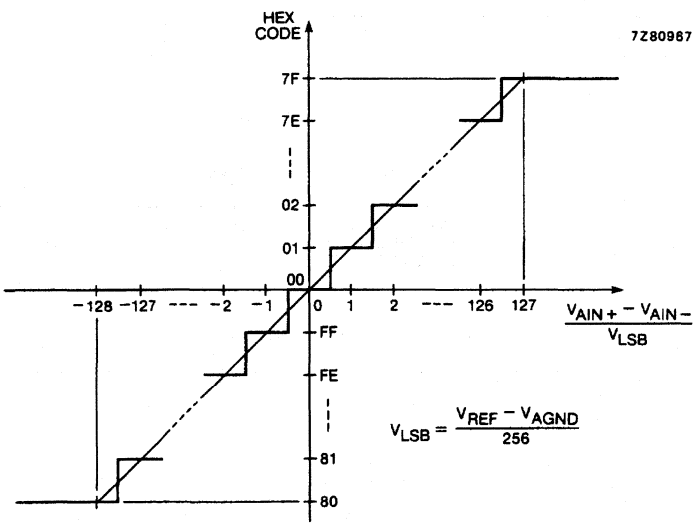


Fig.10 A/D conversion characteristics of differential inputs.

7.5 Reference voltage

For the D/A and A/D conversion either a stable external voltage reference or the supply voltage has to be applied to the resistor divider chain (pins V_{REF} and AGND). The AGND pin has to be connected to the system analog ground and may have a DC off-set with reference to V_{SS}.

A low frequency may be applied to the V_{REF} and AGND pins. This allows the use of the D/A converter as a one-quadrant multiplier; see Chapter 15 and Fig.6.

The A/D converter may also be used as a one or two quadrant analog divider. The analog input voltage is divided by the reference voltage. The result is converted to a binary code. In this application the user has to keep the reference voltage stable during the conversion cycle.

7.6 Oscillator

An on-chip oscillator generates the clock signal required for the A/D conversion cycle and for refreshing the auto-zeroed buffer amplifier. When using this oscillator the EXT pin has to be connected to V_{SS}. At the OSC pin the oscillator frequency is available.

If the EXT pin is connected to V_{DD} the oscillator output OSC is switched to a high-impedance state allowing the user to feed an external clock signal to OSC.

8 CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

8.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

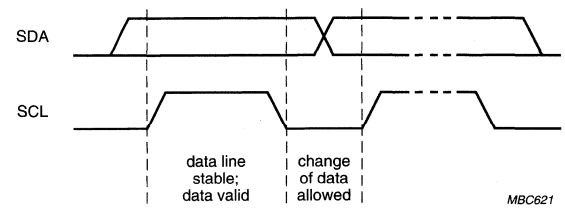


Fig.11 Bit transfer.

8.2 Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH, is defined as the stop condition (P).

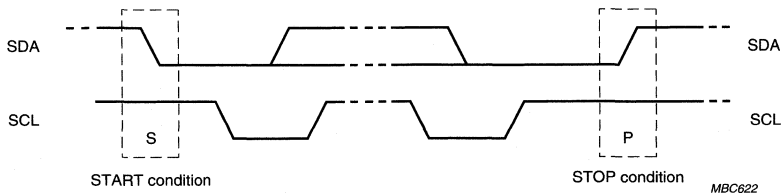


Fig.12 Definition of START and STOP condition.

8.3 System configuration

A device generating a message is a 'transmitter', a device receiving a message is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves'.

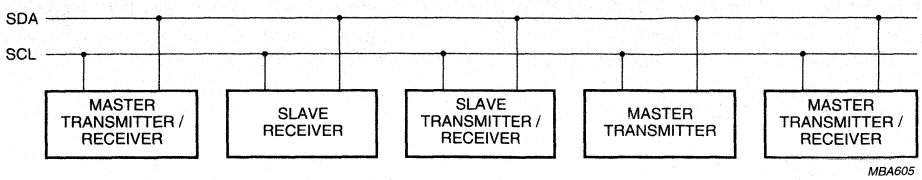


Fig.13 System configuration.

8.4 Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each data byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master also generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. A master receiver must signal an end of data to the transmitter by **not** generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

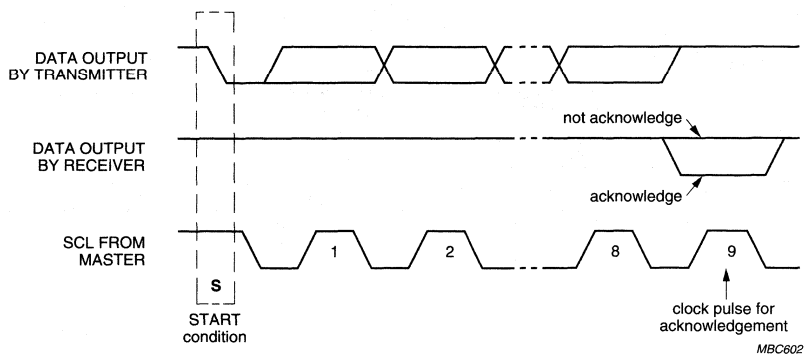


Fig.14 Acknowledgement on the I^2C-bus.

8.5 I²C-bus protocol

After a start condition a valid hardware address has to be sent to a PCF8591 device. The read/write bit defines the direction of the following single or multiple byte data transfer. For the format and the timing of the start condition (S), the stop condition (P) and the acknowledge bit (A) refer to the I²C-bus characteristics. In the write mode a data transfer is terminated by sending either a stop condition or the start condition of the next data transfer.

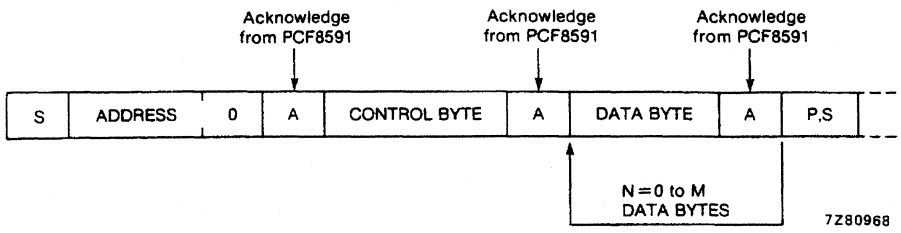


Fig.15 Bus protocol for write mode, D/A conversion.

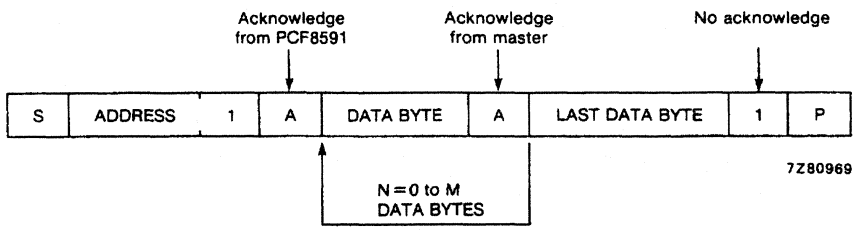


Fig.16 Bus protocol for read mode, A/D conversion.

9 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage (pin 16)	−0.5	+8.0	V
V_I	input voltage (any input)	−0.5	V_{DD} + 0.5	V
I_I	DC input current	–	±10	mA
I_O	DC output current	–	±20	mA
I_{DD}, I_{SS}	V_{DD} or V_{SS} current	–	±50	mA
P_{tot}	total power dissipation per package	–	300	mW
P_O	power dissipation per output	–	100	mW
T_{amb}	operating ambient temperature	−40	+85	°C
T_{stg}	storage temperature	−65	+150	°C

10 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take precautions appropriate to handling MOS devices. Advice can be found in Data Handbook IC12 under *"Handling MOS Devices"*.

11 DC CHARACTERISTICS

V_{DD} = 2.5 V to 6 V; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage (operating)		2.5	–	6.0	V
I_{DD}	supply current					
	standby	$V_I = V_{SS}$ or V_{DD}; no load	–	1	15	μA
	operating, AOUT off	f_{SCL} = 100 kHz	–	125	250	μA
	operating, AOUT active	f_{SCL} = 100 kHz	–	0.45	1.0	mA
V_{POR}	Power-on reset level	note 1	0.8	–	2.0	V
Digital inputs/output: SCL, SDA, A0, A1, A2						
V_{IL}	LOW level input voltage		0	–	$0.3 \times V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7 \times V_{DD}$	–	V_{DD}	V
I_L	leakage current					
	A0, A1, A2	$V_I = V_{SS}$ to V_{DD}	−250	–	+250	nA
	SCL, SDA	$V_I = V_{SS}$ to V_{DD}	−1	–	+1	μA
C_i	input capacitance		–	–	5	pF
I_{OL}	LOW level SDA output current	V_{OL} = 0.4 V	3.0	–	–	mA
Reference voltage inputs						
V_{REF}	reference voltage	$V_{REF} > V_{AGND}$; note 2	V_{SS} + 1.6	–	V_{DD}	V
V_{AGND}	analog ground voltage	$V_{REF} > V_{AGND}$; note 2	V_{SS}	–	V_{DD} − 0.8	V
I_{LI}	input leakage current		−250	–	+250	nA
R_{REF}	input resistance	pins V_{REF} and AGND	–	100	–	kΩ
Oscillator: OSC, EXT						
I_{LI}	input leakage current		–	–	250	nA
f_{OSC}	oscillator frequency		0.75	–	1.25	MHz

Notes

1. The power on reset circuit resets the I^2C-bus logic when V_{DD} is less than V_{POR}.
2. A further extension of the range is possible, if the following conditions are fulfilled:

$$\frac{V_{REF} + V_{AGND}}{2} \geq 0.8V, V_{DD} - \frac{V_{REF} + V_{AGND}}{2} \geq 0.4V$$

12 D/A CHARACTERISTICS

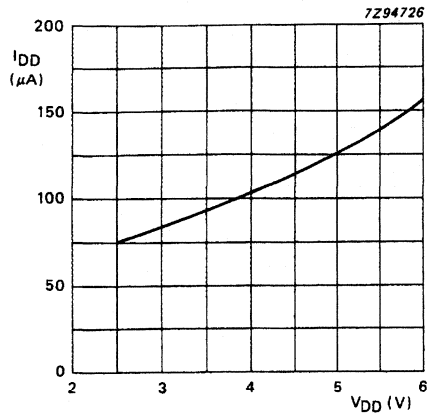
V_{DD} = 5.0 V; V_{SS} = 0 V; V_{REF} = 5.0 V; V_{AGND} = 0 V; R_L = 10 kΩ; C_L = 100 pF; T_{amb} = −40 °C to +85 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Analog output						
V_{OA}	output voltage	no resistive load	V_{SS}	–	V_{DD}	V
		R_L = 10 kΩ	V_{SS}	–	0.9 × V_{DD}	V
I_{LO}	output leakage current	AOUT disabled	–	–	250	nA
Accuracy						
OS_e	offset error	T_{amb} = 25 °C	–	–	50	mV
L_e	linearity error		–	–	±1.5	LSB
G_e	gain error	no resistive load	–	–	1	%
t_{DAC}	settling time	to ½ LSB full scale step	–	–	90	µs
f_{DAC}	conversion rate		–	–	11.1	kHz
SNRR	supply noise rejection ratio	f = 100 Hz; V_{DDN} = 0.1 × V_{PP}	–	40	–	dB

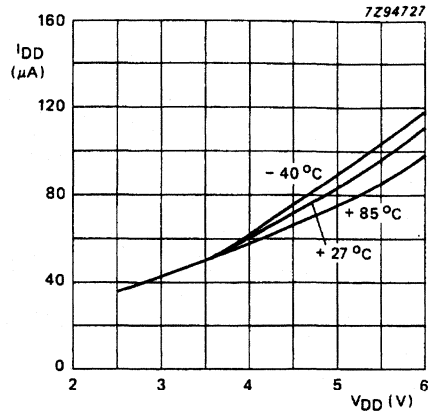
13 A/D CHARACTERISTICS

V_{DD} = 5.0 V; V_{SS} = 0 V; V_{REF} = 5.0 V; V_{AGND} = 0 V; R_S = 10 kΩ; T_{amb} = −40 °C to +85 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Analog inputs						
V_{IA}	analog input voltage		V_{SS}	–	V_{DD}	V
I_{LIA}	analog input leakage current		–	–	100	nA
C_{IA}	analog input capacitance		–	10	–	pF
C_{ID}	differential input capacitance		–	10	–	pF
V_{IS}	single-ended voltage	measuring range	V_{AGND}	–	V_{REF}	V
V_{ID}	differential voltage	measuring range; $V_{FS} = V_{REF} - V_{AGND}$	$\frac{-V_{FS}}{2}$	–	$\frac{+V_{FS}}{2}$	V
Accuracy						
OS_e	offset error	T_{amb} = 25 °C	–	–	20	mV
L_e	linearity error		–	–	±1.5	LSB
G_e	gain error		–	–	1	%
GS_e	small-signal gain error	ΔV_i = 16 LSB	–	–	5	%
CMRR	common-mode rejection ratio		–	60	–	dB
SNRR	supply noise rejection ratio	f = 100 Hz; V_{DDN} = 0.1 × V_{PP}	–	40	–	dB
t_{ADC}	conversion time		–	–	90	µs
f_{ADC}	sampling/conversion rate		–	–	11.1	kHz

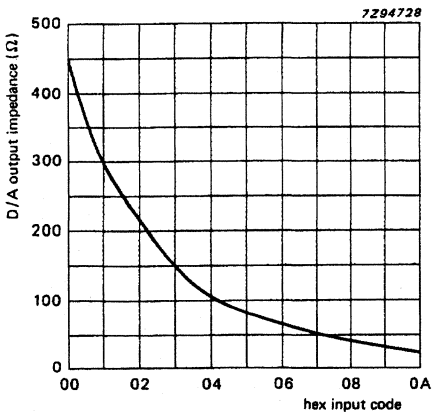


(a) Internal oscillator; T_{amb} = +27 °C.

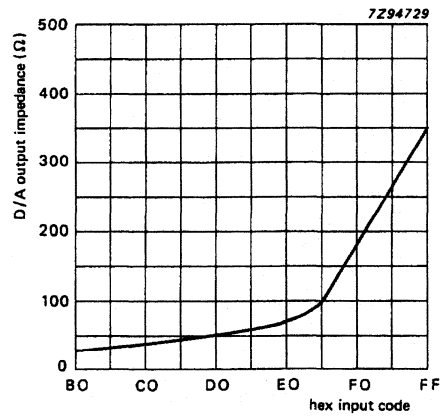


(b) External oscillator.

Fig.17 Operating supply current as a function of supply voltage (analog output disabled).



(a) Output impedance near negative power rail; T_{amb} = +27 °C.



(b) Output impedance near positive power rail; T_{amb} = +27 °C.

The x-axis represents the hex input-code equivalent of the output voltage.

Fig.18 Output impedance of analog output buffer (near power rails).

14 AC CHARACTERISTICS

All timing values are valid within the operating supply voltage and ambient temperature range and reference to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
I²C-bus timing (see Fig.19; note 1)					
f_{SCL}	SCL clock frequency	–	–	100	kHz
t_{SP}	tolerable spike width on bus	–	–	100	ns
t_{BUF}	bus free time	4.7	–	–	µs
$t_{SU;STA}$	START condition set-up time	4.7	–	–	µs
$t_{HD;STA}$	START condition hold time	4.0	–	–	µs
t_{LOW}	SCL LOW time	4.7	–	–	µs
t_{HIGH}	SCL HIGH time	4.0	–	–	µs
t_r	SCL and SDA rise time	–	–	1.0	µs
t_f	SCL and SDA fall time	–	–	0.3	µs
$t_{SU;DAT}$	data set-up time	250	–	–	ns
$t_{HD;DAT}$	data hold time	0	–	–	ns
$t_{VD;DAT}$	SCL LOW-to-data out valid	–	–	3.4	µs
$t_{SU;STO}$	STOP condition set-up time	4.0	–	–	µs

Note

1. A detailed description of the I²C-bus specification, with applications, is given in brochure *"The I²C-bus and how to use it"*. This brochure may be ordered using the code 9398 393 40011.

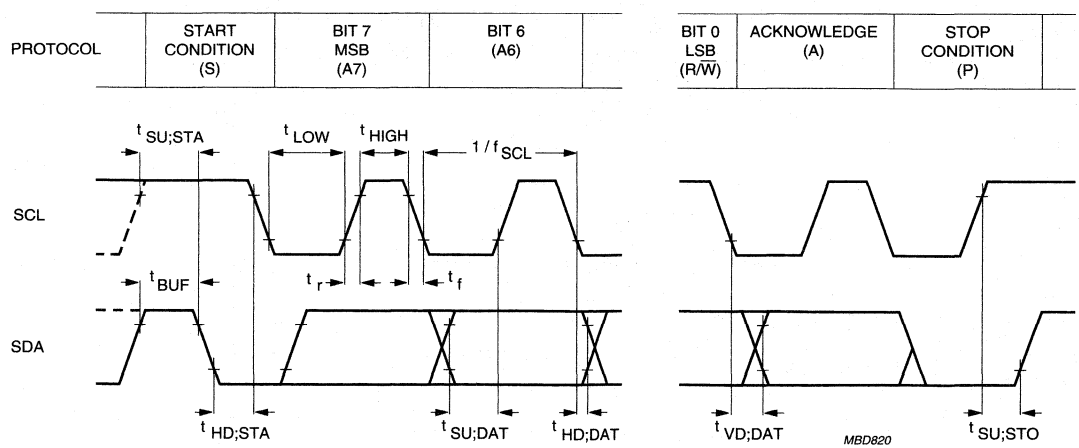


Fig.19 I²C-bus timing diagram; rise and fall times refer to V_{IL} and V_{IH}.

15 APPLICATION INFORMATION

Inputs must be connected to V_{SS} or V_{DD} when not in use. Analog inputs may also be connected to AGND or V_{REF}.

In order to prevent excessive ground and supply noise and to minimize cross-talk of the digital to analog signal paths the user has to design the printed-circuit board layout very carefully. Supply lines common to a PCF8591 device and noisy digital circuits and ground loops should be avoided. Decoupling capacitors (>10 μF) are recommended for power supply and reference voltage inputs.

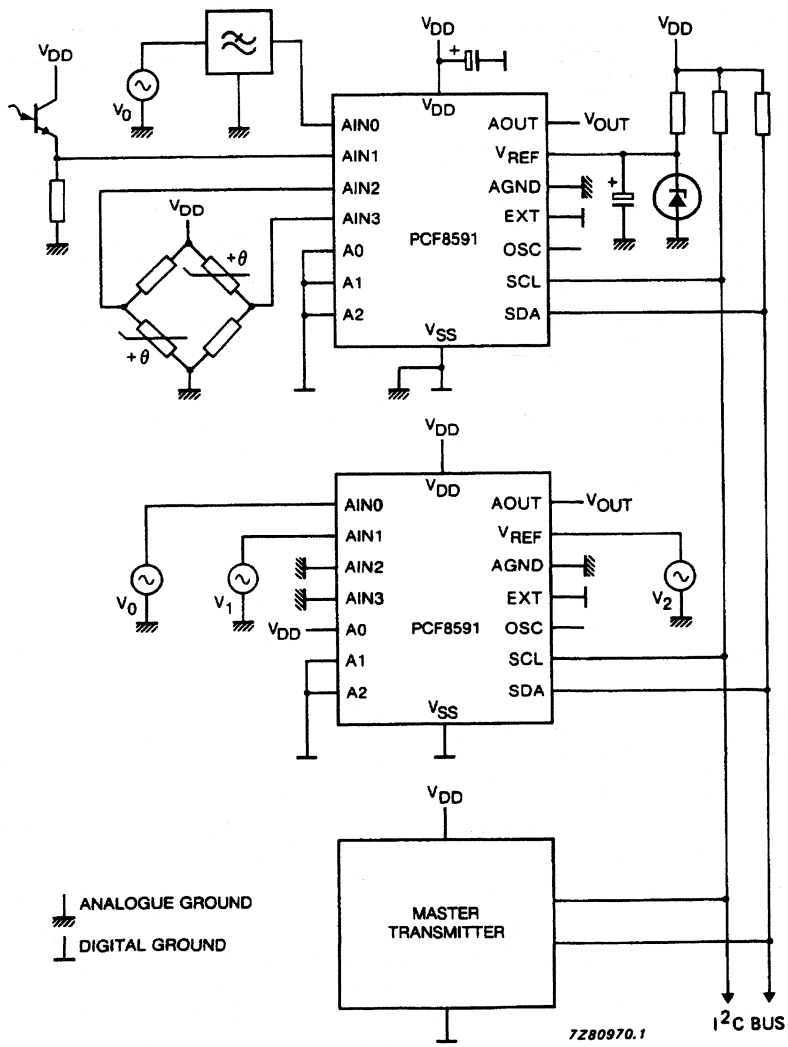
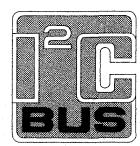


Fig.20 Application diagram.

Low power clock/calendar PCF8593

CONTENTS



Low power clock/calendar PCF8593

1 FEATURES

- I²C-bus interface operating supply voltage: 2.5 to 6.0 V
- Clock operating supply voltage (T_{amb} = 0 to +70 °C): 1.0 to 6.0 V
- 8 bytes scratchpad RAM (when alarm not used)
- Data retention voltage: 1.0 to 6.0 V
- External $\overline{\text{RESET}}$ input resets I²C interface (only)
- Operating current (f_{scl} = 0 Hz, 32 kHz time base, V_{DD} = 2.0 V): typ. 1 µA
- Clock function with four year calendar
- Universal timer with alarm and overflow indication
- 24 or 12 hour format
- 32.768 kHz or 50 Hz time base
- Serial input/output bus (I²C-bus)
- Automatic word address incrementing
- Programmable alarm, timer and interrupt function
- Space-saving SO8 package available
- Slave address:
  - READ A3
  - WRITE A2.

2 GENERAL DESCRIPTION

The PCF8593 is a CMOS clock/calendar circuit, optimized for low power consumption. Addresses and data are transferred serially via the two-line bidirectional I²C-bus. The built-in word address register is incremented automatically after each written or read data byte.
The built-in 32.768 kHz oscillator circuit and the first 8 bytes of RAM are used for the clock/calendar and counter functions. The next 8 bytes may be programmed as alarm registers or used as free RAM space.

3 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage operating mode	I²C-bus active	2.5	–	6.0	V
		I²C-bus inactive	1.0	–	6.0	V
I_{DD}	supply current operating mode	f_{scl} = 100 kHz	–	–	200	µA
I_{DD}	supply current clock mode	f_{scl} = 0 Hz; V_{DD} = 5 V	–	4.0	15.0	µA
		f_{scl} = 0 Hz; V_{DD} = 2 V	–	1.0	8.0	µA
T_{amb}	operating ambient temperature		−40	–	+85	°C
T_{stg}	storage temperature		−65	–	+150	°C

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8593P	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1
PCF8593T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

5 BLOCK DIAGRAM

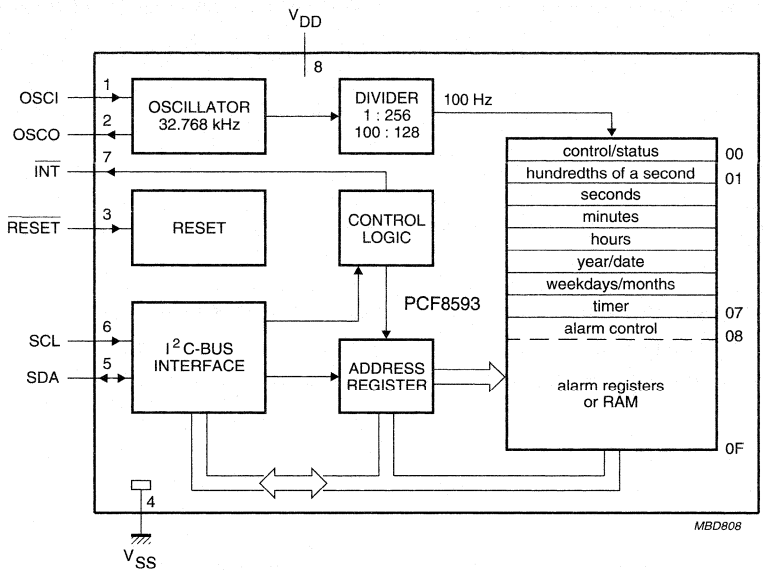


Fig.1 Block diagram.

6 PINNING

SYMBOL	PIN	DESCRIPTION
OSCI	1	oscillator input, 50 Hz or event-pulse input
OSCO	2	oscillator output
$\overline{RESET}$	3	reset input (active LOW)
V_{SS}	4	negative supply
SDA	5	serial data input/output
SCL	6	serial clock input
$\overline{INT}$	7	open drain interrupt output (active LOW)
V_{DD}	8	positive supply

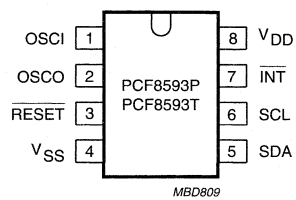


Fig.2 Pin configuration.

7 FUNCTIONAL DESCRIPTION

The PCF8593 contains sixteen 8-bit registers with an 8-bit auto-incrementing address register, an on-chip 32.768 kHz oscillator circuit, a frequency divider and a serial two-line bidirectional I^2C-bus interface.

The first 8 registers (memory addresses 00 to 07) are designed as addressable 8-bit parallel registers. The first register (memory address 00) is used as a control/status register. The memory addresses 01 to 07 are used as counters for the clock function. The memory addresses 08 to 0F may be programmed as alarm registers or used as free RAM locations.

7.1 Counter function modes

When the control/status register is programmed, a 32.768 kHz clock mode, a 50 Hz clock mode or an event-counter mode can be selected.

In the clock modes the hundredths of a second, seconds, minutes, hours, date, month (four year calendar) and weekday are stored in a BCD format. The timer register stores up to 99 days. The event counter mode is used to count pulses applied to the oscillator input (OSCO left open-circuit). The event counter stores up to 6 digits of data.

When one of the counters is read (memory locations 01 to 07), the contents of all counters are strobed into capture latches at the beginning of a read cycle. Therefore, faulty reading of the count during a carry condition is prevented.

When a counter is written, other counters are not affected.

7.2 Alarm function modes

By setting the alarm enable bit of the control/status register the alarm control register (address 08) is activated.

By setting the alarm control register a dated alarm, a daily alarm, a weekday alarm or a timer alarm may be programmed. In the clock modes, the timer register (address 07) may be programmed to count hundredths of a second, seconds, minutes, hours or days. Days are counted when an alarm is not programmed.

Whenever an alarm event occurs the alarm flag of the control/status register is set. A timer alarm event will set the alarm flag and an overflow condition of the timer will set the timer flag. The open-drain interrupt output is switched on (active LOW) when the alarm or timer flag is set (enabled). The flags remain set until directly reset by a write operation.

When the alarm is disabled (Bit 2 of control/status register = 0) the alarm registers at addresses 08 to 0F may be used as free RAM.

7.3 Control/status register

The control/status register is defined as the memory location 00 with free access for reading and writing via the I^2C-bus. All functions and options are controlled by the contents of the control/status register (see Fig.3).

7.4 Counter registers

In the clock modes 24 h or 12 h format can be selected by setting the most significant bit of the hours counter register. The format of the hours counter is shown in Fig.5.

The year and date are packed into memory location 05 (see Fig 6). The weekdays and months are packed into memory location 06 (see Fig.7). When reading these memory locations the year and weekdays are masked out when the mask flag of the control/status register is set. This allows the user to read the date and month count directly.

In the event-counter mode events are stored in BCD format. D5 is the most significant and D0 the least significant digit. The divider is by-passed.

In the different modes the counter registers are programmed and arranged as shown in Fig.4. Counter cycles are listed in Table 1.

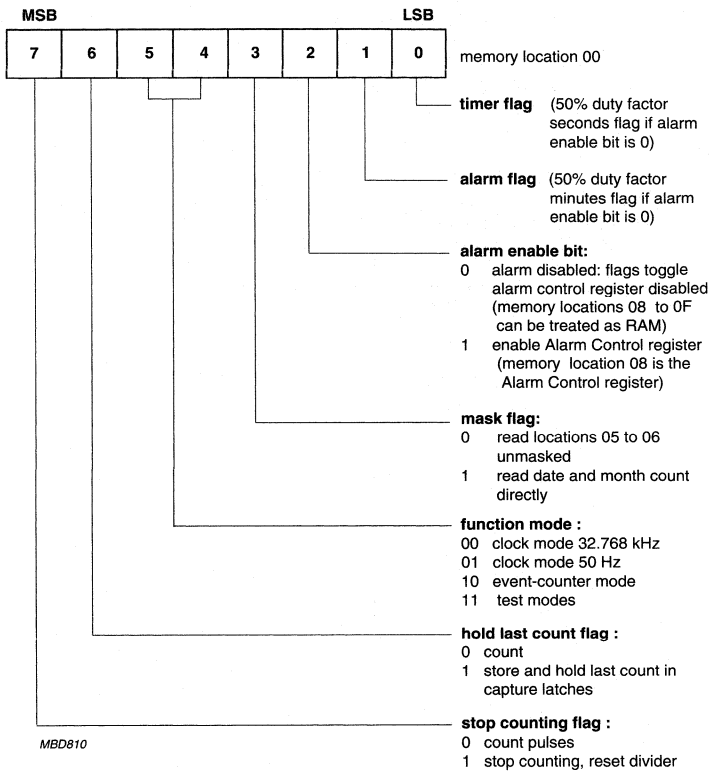


Fig.3 Control/status register.

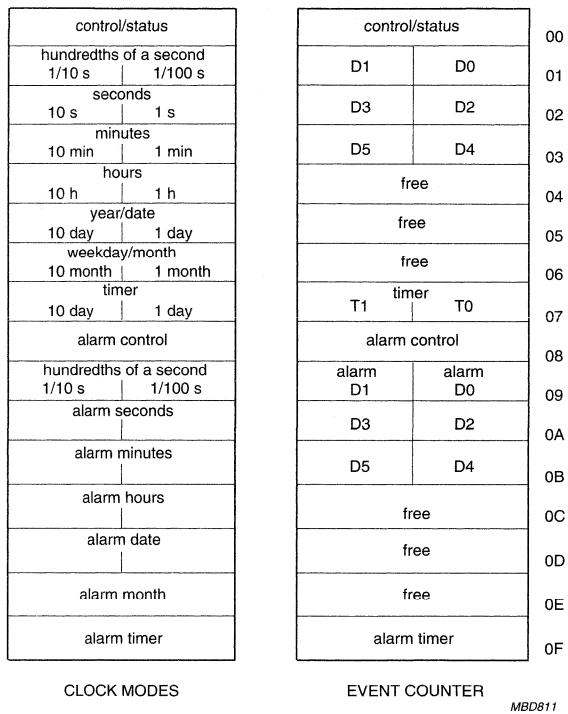


Fig.4 Register arrangement.

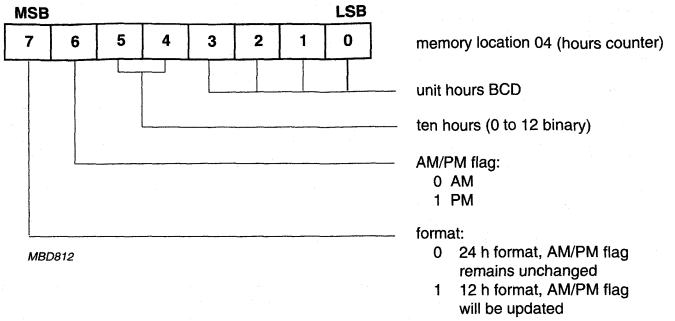


Fig.5 Format of the hours counter.

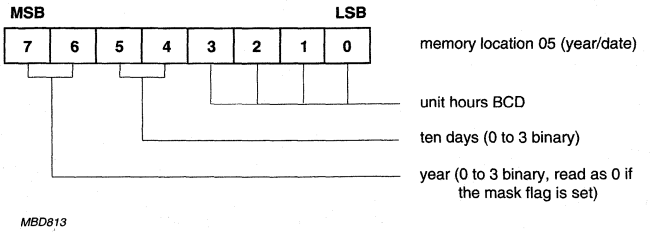


Fig.6 Format of the year/date counter.

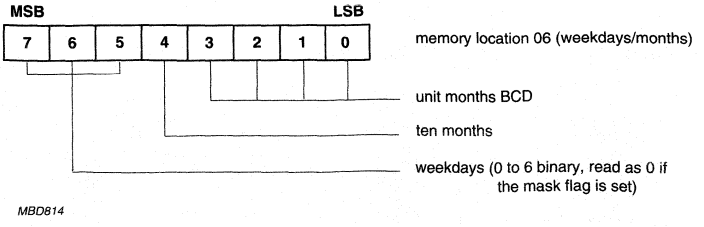


Fig.7 Format of the weekdays/months counter.

Table 1 Cycle length of the time counters, clock modes.

UNIT	COUNTING CYCLE	CARRY TO NEXT UNIT	CONTENTS OF THE MONTH COUNTER
Hundredths of a second	00 to 99	99 to 00	–
Seconds	00 to 59	59 to 00	–
Minutes	00 to 59	59 to 00	–
Hours (24 h)	00 to 23	23 to 00	–
Hours (12 h)	12 AM	–	–
	01 AM to 11 AM	–	–
	12 PM	–	–
	01 PM to 11 PM	11 PM to 12 AM	–
Date	01 to 31	31 to 01	1, 3, 5, 7, 8, 10 and 12
	01 to 30	30 to 01	4, 6, 9 and 11
	01 to 29	29 to 01	2, year = 0
	01 to 28	28 to 01	2, year = 1, 2 and 3
Months	01 to 12	12 to 01	–
Year	0 to 3	–	–
Weekdays	0 to 6	6 to 0	–
Timer	00 to 99	no carry	–

7.5 Alarm control register

When the alarm enable bit of the control/status register is set (address 00, bit 2) the alarm control register (address 08) is activated. All alarm, timer, and interrupt output functions are controlled by the contents of the alarm control register (see Fig.8).

7.6 Alarm registers

All alarm registers are allocated with a constant address offset of hexadecimal 08 to the corresponding counter registers (see Fig.4,Register arrangement).

An alarm signal is generated when the contents of the alarm registers matches bit-by-bit the contents of the involved counter registers. The year and weekday bits are ignored in a dated alarm. A daily alarm ignores the month and date bits. When a weekday alarm is selected, the contents of the alarm weekday/month register will select the weekdays on which an alarm is activated (see Fig.9).

Remark: in the 12 h mode, bits 6 and 7 of the alarm hours register must be the same as the hours counter.

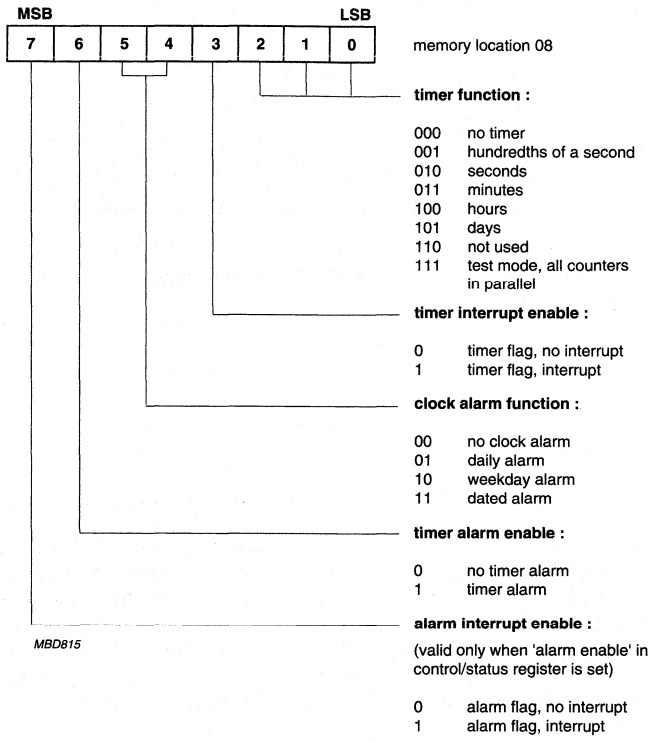


Fig.8 Alarm control register, clock mode.

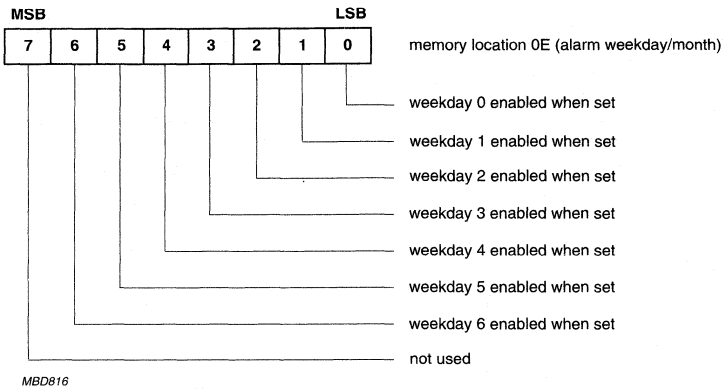


Fig.9 Selection of alarm weekdays.

7.7 Timer

The timer (location 07) is enabled by setting the control/status register = XX0X X1XX. The timer counts up from 0 (or a programmed value) to 99. On overflow, the timer resets to 0. The timer flag (LSB of control/status register) is set on overflow of the timer. This flag must be reset by software. The inverted value of this flag can be transferred to the external interrupt by setting bit 3 of the alarm control register.

Additionally, a timer alarm can be programmed by setting the timer alarm enable (bit 6 of the alarm control register). When the value of the timer equals a pre-programmed value in the alarm timer register (location 0F), the alarm flag is set (bit 1 of the control/status register). The inverted value of the alarm flag can be transferred to the external interrupt by enabling the alarm interrupt (bit 6 of the alarm control register).

Resolution of the timer is programmed via the 3 LSBs of the alarm control register (see Fig.11, Alarm and timer Interrupt logic diagram).

7.8 Event counter mode

Event counter mode is selected by bits 4 and 5 which are logic 1, 0 in the control/status register. The event counter mode is used to count pulses externally applied to the oscillator input (OSCO left open-circuit). The event counter stores up to 6 digits of data, which are stored as 6 hexadecimal values located in locations 1, 2, and 3. Thus, up to 1 million events may be recorded.

An event counter alarm occurs when the event counter registers match the value programmed in locations 9, A, and B, and the event alarm is enabled (bits 4 and 5 which are logic 0, 1 in the alarm control register). In this event, the alarm flag (bit 1 of the control/status register) is set. The inverted value of this flag can be transferred to the interrupt pin (pin 7) by setting the alarm interrupt enable in the alarm control register. In this mode, the timer (location 07) increments once for every one, one-hundred, ten thousand, or 1 million events, depending on the value programmed in bits 0,1 and 2 of the alarm control register. In all other events, the timer functions are as in the clock mode.

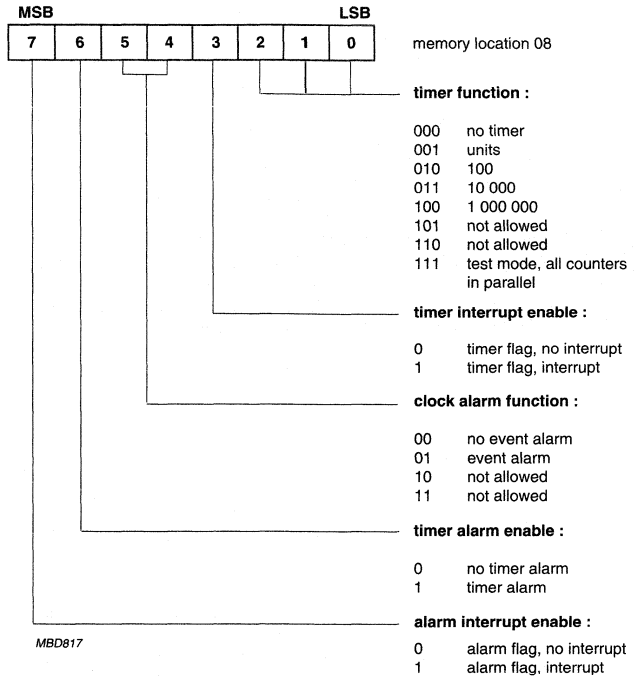
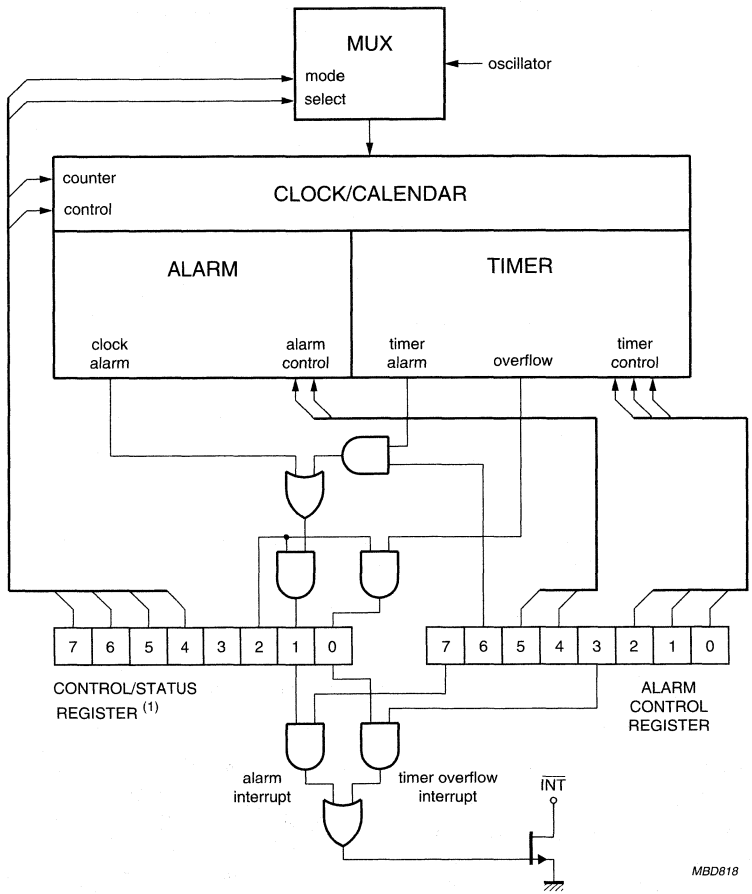


Fig.10 Alarm control register, event-counter mode.

7.9 Interrupt output

The conditions for activating the open-drain n-channel interrupt output $\overline{INT}$ (active LOW) are determined by appropriate programming of the alarm control register. These conditions are clock alarm, timer alarm, timer overflow, and event counter alarm. An interrupt occurs when the alarm flag or the timer flag is set, and the corresponding interrupt is enabled. In all events, the interrupt is cleared only by software resetting of the flag which initiated the interrupt.

In the clock mode, if the alarm enable is not activated (alarm enable bit of control/status register is logic 0), the interrupt output toggles at 1 Hz with a 50% duty cycle (may be used for calibration). The OFF voltage of the interrupt output may exceed the supply voltage, up to a maximum of 6.0 V. A logic diagram of the interrupt output is shown in Fig.11.



(1) If the alarm enable bit of the control/status register is reset (logic 0), a 1 Hz signal can be observed on the interrupt pin $\overline{INT}$.

Fig.11 Alarm and timer interrupt logic diagram.

7.10 Oscillator and divider

A 32.768 kHz quartz crystal has to be connected to OSCI (pin 1) and OSCO (pin 2). A trimmer capacitor between OSCI and V_{DD} is used for tuning the oscillator (see Chapter 14, Section 14.1). A 100 Hz clock signal is derived from the quartz oscillator for the clock counters.

In the 50 Hz clock mode or event-counter mode the oscillator is disabled and the oscillator input is switched to a high-impedance state. This allows the user to feed the 50 Hz reference frequency or an external high-speed event signal into the input OSCI.

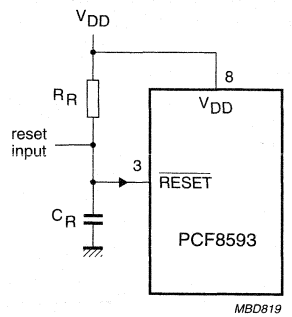
7.10.1 DESIGNING

When designing the printed-circuit board layout, keep the oscillator components as close to the IC package as possible, and keep all other signal lines as far away as possible. In applications involving tight packing of components, shielding of the oscillator may be necessary. AC coupling of extraneous signals can introduce oscillator inaccuracy.

7.11 Initialization (see Fig.12)

Note that immediately following power-on, all internal registers are undefined and, following a $\overline{\text{RESET}}$ pulse on pin 3, must be defined via software. Attention should be paid to the possibility that the device may be initially in event-counter mode, in which event the oscillator will not operate. Over-ride can be achieved via software.

Reset is accomplished by applying an external $\overline{\text{RESET}}$ pulse (active LOW) at pin 3. When reset occurs only the I^2C-bus interface is reset. The control/status register and all clock counters are not affected by $\overline{\text{RESET}}$. $\overline{\text{RESET}}$ must return HIGH during device operation.



To avoid overload of the internal diode by falling V_{DD}, an external diode should be added in parallel to R_R if $C_R \geq 0.2\ \mu F$. Note that RC must be evaluated with the actual V_{DD} of the application, as their value will be V_{DD} rise-time dependent.

Fig.12 RC reset.

An RC combination can also be utilized to provide a power-on $\overline{\text{RESET}}$ signal at pin 3. In this event, the values of the RC must fulfil the following relationship to guarantee power-on reset (see Fig.12).

$\overline{\text{RESET}}$ input must be $\leq 0.3V_{DD}$ when V_{DD} reaches V_{DDmin} (or higher).

It is recommended to set the stop counting flag of the control/status register before loading the actual time into the counters. Loading of illegal states may lead to a temporary clock malfunction.

8 CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

8.1 Bit transfer (see Fig.13)

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

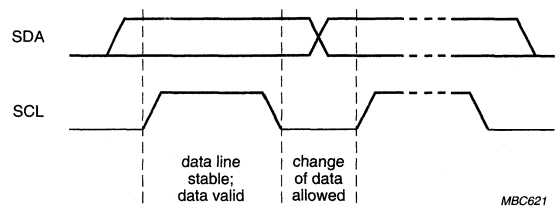


Fig.13 Bit transfer.

8.2 Start and stop conditions (see Fig.14)

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

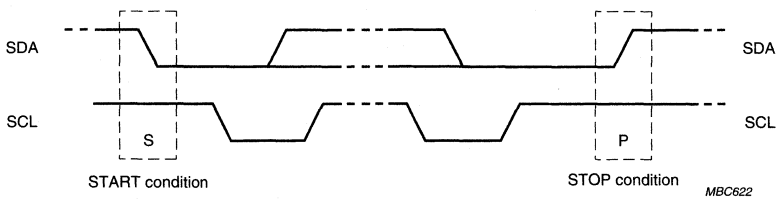


Fig.14 Definition of start and stop conditions.

8.3 System configuration (see Fig.15)

A device generating a message is a 'transmitter', a device receiving a message is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves'.

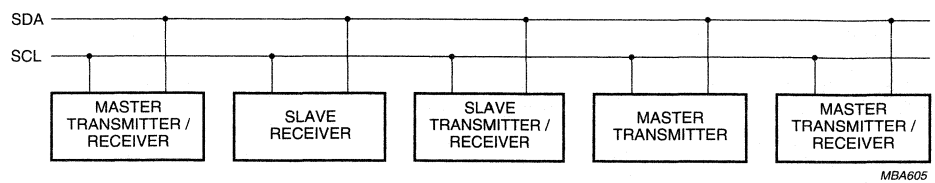


Fig.15 System configuration.

8.4 Acknowledge (see Fig.16)

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by **not** generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

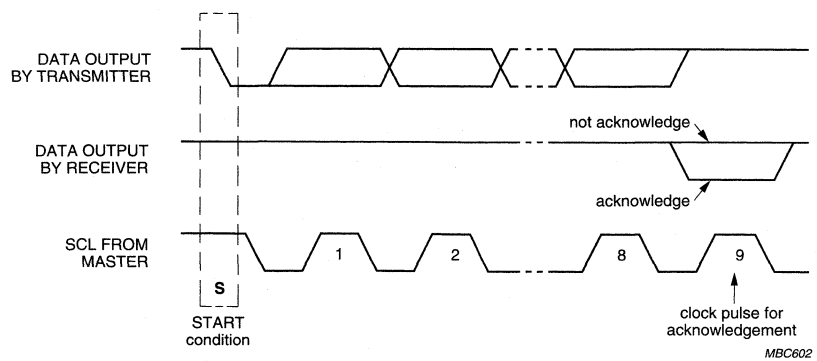


Fig.16 Acknowledgment on the I^2C-bus.

9 I²C-BUS PROTOCOL

9.1 Addressing

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always carried out with the first byte transmitted after the start procedure.

The clock/calendar acts as a slave receiver or slave transmitter. Therefore the clock signal SCL is only an input signal, but the data signal SDA is a bidirectional line. The clock/calendar slave address is shown in Fig.17.

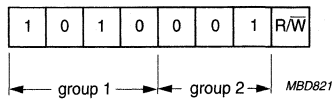


Fig.17 Slave address.

9.2 Clock/calendar READ/WRITE cycles

The I²C-bus configuration for the different PCF8593 READ and WRITE cycles is shown in Figs 18, 19 and 20.

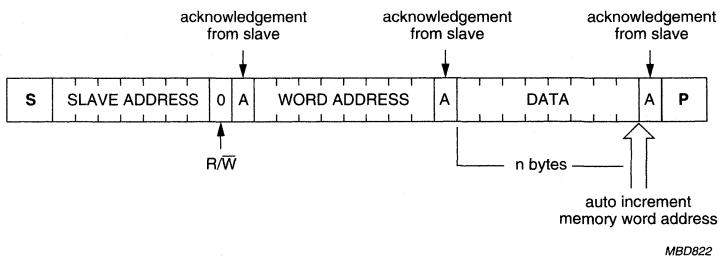


Fig.18 Master transmits to slave receiver (WRITE) mode.

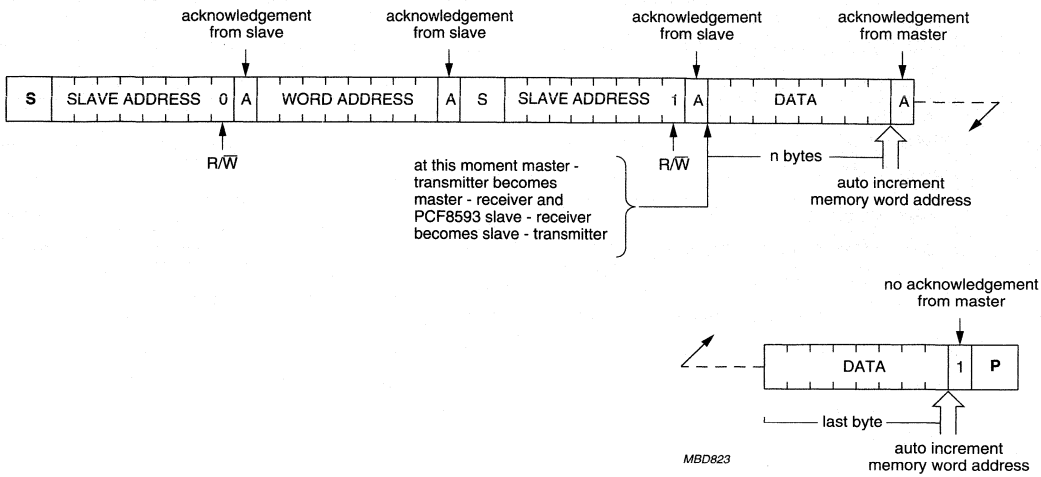


Fig.19 Master reads after setting word address (write word address, READ data).

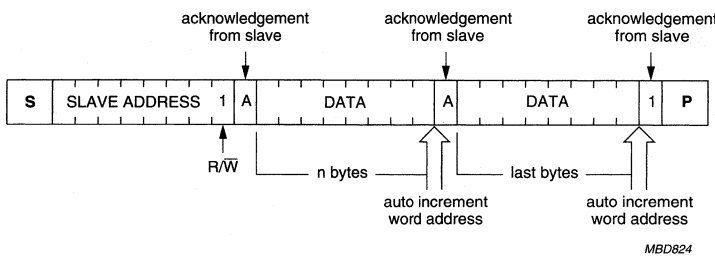


Fig.20 Master reads slave immediately after first byte (READ mode).

10 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage (pin 8)	−0.8	+7.0	V
I_{DD}	supply current (pin 8)	−	50	mA
I_{SS}	supply current (pin 4)	−	50	mA
V_I	input voltage	−0.8	V_{DD} + 0.8	V
I_I	input current	−	10	mA
I_O	DC output current	−	10	mA
P_{tot}	total power dissipation per package	−	300	mW
P_O	power dissipation per output	−	50	mW
T_{amb}	operating ambient temperature	−40	+85	°C
T_{stg}	storage temperature	−65	+150	°C

11 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take precautions appropriate to handling MOS devices Advice can be found in Data Handbook IC12 under *"Handling MOS Devices"*.

12 DC CHARACTERISTICS

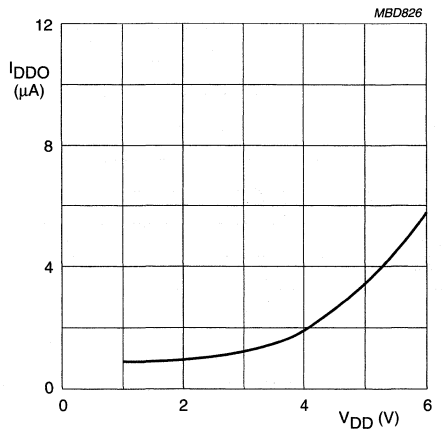
V_{DD} = 2.5 to 6.0 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; f_{osc} = 32 kHz; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.(1)	MAX.	UNIT
Supply						
V_{DD}	supply voltage (operating mode)	I^2C-bus active	2.5	−	6.0	V
		I^2C-bus inactive	1.0	−	6.0	V
V_{DDosc}	supply voltage (quartz oscillator)	note 2				
		T_{amb} = 0 to 70 °C	1.0	−	6.0	V
		T_{amb} = −40 to 85 °C	1.2	−	6.0	V
I_{DD}	supply current (operating mode)	f_{scl} = 100 kHz; clock mode; note 3	−	−	200	µA
I_{DDO}	supply current (clock mode with I^2C-bus inactive)	f_{scl} = 0 Hz; inputs at V_{DD} or V_{SS}				
		V_{DD} = 2 V	−	1.0	8.0	µA
		V_{DD} = 5 V	−	4.0	15	µA
SDA, SCL, $\overline{INT}$ and RESET						
V_{IL}	LOW level input voltage		0	−	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	−	V_{DD}	V
I_{OL}	LOW level output current	V_{OL} = 0.4 V	3	−	−	mA
I_{LI}	input leakage current	V_I = V_{DD} or V_{SS}	−1	−	+1	µA
C_i	input capacitance	note 4	−	−	7	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.(1)	MAX.	UNIT
OSCI and $\overline{\text{RESET}}$						
I_{LI}	input leakage current	$V_I = V_{DD}$ or V_{SS}	−250	–	+250	nA
$\overline{\text{INT}}$						
I_{OL}	LOW level output current	V_{OL} = 0.4 V	1	–	–	mA
I_{LI}	input leakage current	$V_I = V_{DD}$ or V_{SS}	−1	–	+1	μA
SCL						
C_i	input capacitance	note 4	–	–	7	pF
I_{LI}	input leakage current	$V_I = V_{DD}$ or V_{SS}	−1	–	+1	μA

Notes

1. Typical values measured at T_{amb} = 25 °C.
2. When powering up the device, V_{DD} must exceed the specified minimum value by 300 mV to guarantee correct start-up of the oscillator.
3. Event counter mode: supply current dependent upon input frequency.
4. Tested on sample basis.



f_{SCL} = 32 kHz; T_{amb} = 25 °C.

Fig.21 Typical supply current in clock mode as a function of supply voltage.

13 AC CHARACTERISTICS

V_{DD} = 2.5 to 6.0 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Oscillator						
C_{osc}	integrated oscillator capacitance		20	25	30	pF
Δf_{osc}	oscillator stability	for ΔV_{DD} = 100 mV; T_{amb} = 25 °C; V_{DD} = 1.5 V	–	2×10^{-7}	–	
f_i	input frequency	note 1	–	–	1	MHz
Quartz crystal parameters (f = 32.768 kHz)						
R_s	series resistance		–	–	40	kΩ
C_L	parallel load capacitance		–	10	–	pF
C_T	trimmer capacitance		5	–	25	pF
I²C-bus timing (see Fig.22; notes 2 and 3)						
f_{SCL}	SCL clock frequency		–	–	100	kHz
t_{SP}	tolerable spike width on bus		–	–	100	ns
t_{BUF}	bus free time		4.7	–	–	µs
$t_{SU;STA}$	START condition set-up time		4.7	–	–	µs
$t_{HD;STA}$	START condition hold time		4.0	–	–	µs
t_{LOW}	SCL LOW time		4.7	–	–	µs
t_{HIGH}	SCL HIGH time		4.0	–	–	µs
t_r	SCL and SDA rise time		–	–	1.0	µs
t_f	SCL and SDA fall time		–	–	0.3	µs
$t_{SU;DAT}$	data set-up time		250	–	–	ns
$t_{HD;DAT}$	data hold time		0	–	–	ns
$t_{VD;DAT}$	SCL LOW to data out valid		–	–	3.4	µs
$t_{SU;STO}$	STOP condition set-up time		4.0	–	–	µs

Notes

1. Event counter mode only.
2. All timing values are valid within the operating supply voltage and ambient temperature range and reference to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.
3. A detailed description of the I²C-bus specification, with applications, is given in brochure *"The I²C-bus and how to use it"*. This brochure may be ordered using the code 9398 393 40011.

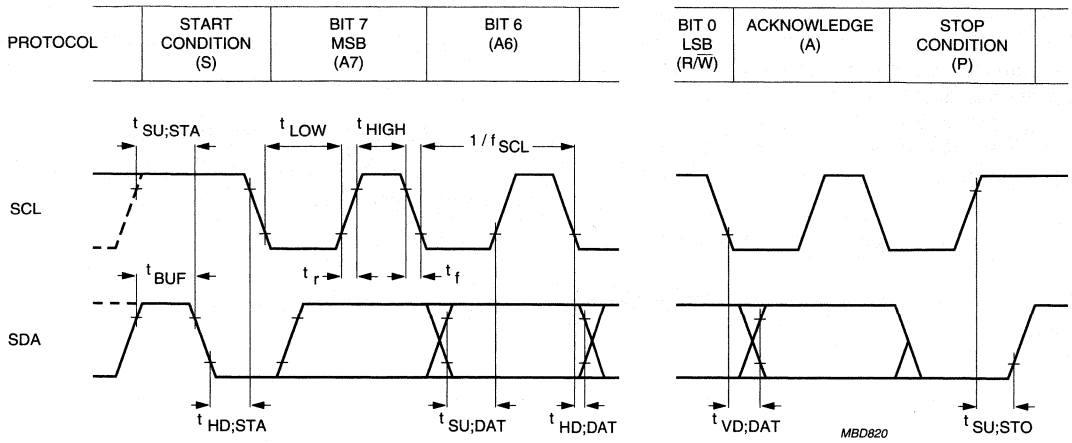


Fig.22 I^2C-bus timing diagram; rise and fall times refer to V_{IL} and V_{IH}.

14 APPLICATION INFORMATION

14.1 Quartz frequency adjustment

14.1.1 METHOD 1: FIXED OSCI CAPACITOR

By evaluating the average capacitance necessary for the application layout a fixed capacitor can be used. The frequency is best measured via the 1 Hz signal which can be programmed to occur at the interrupt output (pin 7). The frequency tolerance depends on the quartz crystal tolerance, the capacitor tolerance and the device-to-device tolerance (on average $\pm 5 \times 10^{-6}$). Average deviations of ±5 minutes per year can be achieved.

14.1.2 METHOD 2: OSCI TRIMMER

Using the alarm function (via the I²C-bus) a signal faster than 1 Hz can be generated at the interrupt output for fast setting of a trimmer.

Procedure:

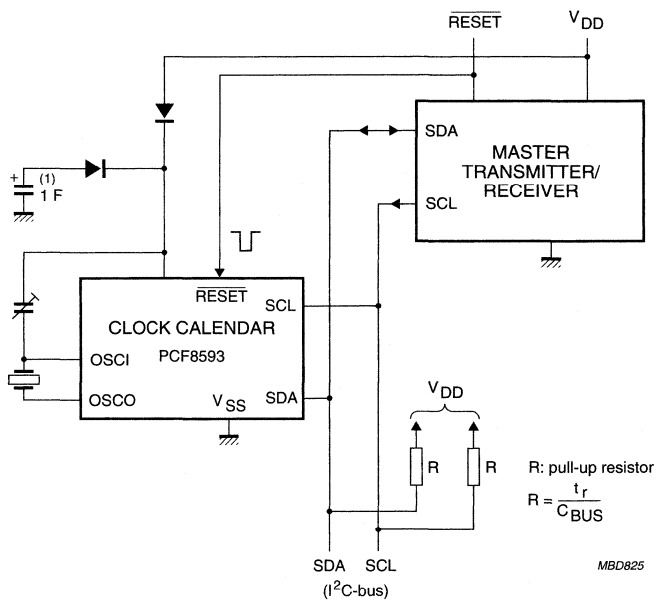
- Power-on
- Apply $\overline{\text{RESET}}$
- Initialization (alarm functions).

Routine:

- Set clock to time T and set alarm to time T + ΔT
- At time T + ΔT (interrupt) repeat routine.

14.1.3 METHOD 3: DIRECT OUTPUT

Direct measurement of oscillator output (accounting for test probe capacitance).



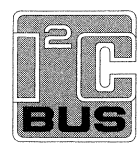
(1) Example Philips DLC 196 Double-Layer Capacitor family.

Fig.23 Application diagram.

256 to 1024 × 8-bit CMOS EEPROMs with I²C-bus interface

PCF85xxC-2 family

CONTENTS



256 to 1024 × 8-bit CMOS EEPROMs with I²C-bus interface

PCF85xxC-2 family

1 FEATURES

- Low power CMOS:
  - maximum operating current:
    2.0 mA (PCF8582C-2)
    2.5 mA (PCF8594C-2)
    4.0 mA (PCF8598C-2)
  - maximum standby current 10 μA (at 6.0 V), typical 4 μA
- Non-volatile storage of:
  - 2 kbits organized as 256 × 8-bit (PCF8582C-2)
  - 4 kbits organized as 512 × 8-bit (PCF8594C-2)
  - 8 kbits organized as 1024 × 8-bit (PCF8598C-2)
- Single supply with full operation down to 2.5 V
- On-chip voltage multiplier
- Serial input/output I²C-bus
- Write operations:
  - byte write mode
  - 8-byte page write mode (minimizes total write time per byte)
- Read operations:
  - sequential read
  - random read
- Internal timer for writing (no external components)
- Power-on-reset
- High reliability by using a redundant storage code
- Endurance: 1000000 Erase/Write (E/W) cycles at T_{amb} = 22 °C
- 10 years non-volatile data retention time
- Pin and address compatible to: PCF8570, PCF8571, PCF8572 and PCF8581.

2 GENERAL DESCRIPTION

The PCF85xxC-2 is a family of floating gate Electrically Erasable Programmable Read Only Memories (EEPROMs) with 2, 4 and 8 kbits (256, 512 and 1024 × 8-bit). By using an internal redundant storage code it is fault tolerant to single bit errors. This feature dramatically increases the reliability compared to conventional EEPROMs. Power consumption is low due to the full CMOS technology used. The programming voltage is generated on-chip, using a voltage multiplier.

As data bytes are received and transmitted via the serial I²C-bus, a package using eight pins is sufficient. Up to eight PCF85xxC-2 devices may be connected to the I²C-bus. Chip select is accomplished by three address inputs (A0, A1 and A2).

Timing of the E/W cycle is carried out internally, thus no external components are required. Pin 7 (PTC) must be connected to either V_{DD} or left open-circuit. There is an option of using an external clock for timing the length of an E/W cycle.

3 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		2.5	6.0	V
I_{DDR}	supply current read	f_{SCL} = 100 kHz			
		V_{DD} = 2.5 V	–	60	μA
		V_{DD} = 6 V	–	200	μA
I_{DDW}	supply current E/W	f_{SCL} = 100 kHz			
	PCF8582C-2	V_{DD} = 2.5 V	–	0.6	mA
		V_{DD} = 6 V	–	2.0	mA
	PCF8594C-2	V_{DD} = 2.5 V	–	0.8	mA
		V_{DD} = 6 V	–	2.5	mA
	PCF8598C-2	V_{DD} = 2.5 V	–	1.0	mA
		V_{DD} = 6 V	–	4.0	mA
$I_{DD(stb)}$	standby supply current	V_{DD} = 2.5 V	–	3.5	μA
		V_{DD} = 6 V	–	10	μA

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8582C-2P	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1
PCF8594C-2P			
PCF8598C-2P			
PCF8582C-2T	SO8	plastic small outline package; 8 leads (straight); body width 3.9 mm	SOT96-1
PCF8594C-2T			
PCF8598C-2T	SO8	plastic small outline package; 8 leads; body width 7.5 mm	SOT176-1

5 DEVICE SELECTION

Table 1 Device selection code

SELECTION	DEVICE CODE				CHIP ENABLE			R/$\overline{W}$
Bit	b7[1]	b6	b5	b4	b3	b2	b1	b0
Device	1	0	1	0	A2	A1	A0	R/$\overline{W}$

Note

1. The Most Significant Bit (MSB) 'b7' is sent first.

6 BLOCK DIAGRAM

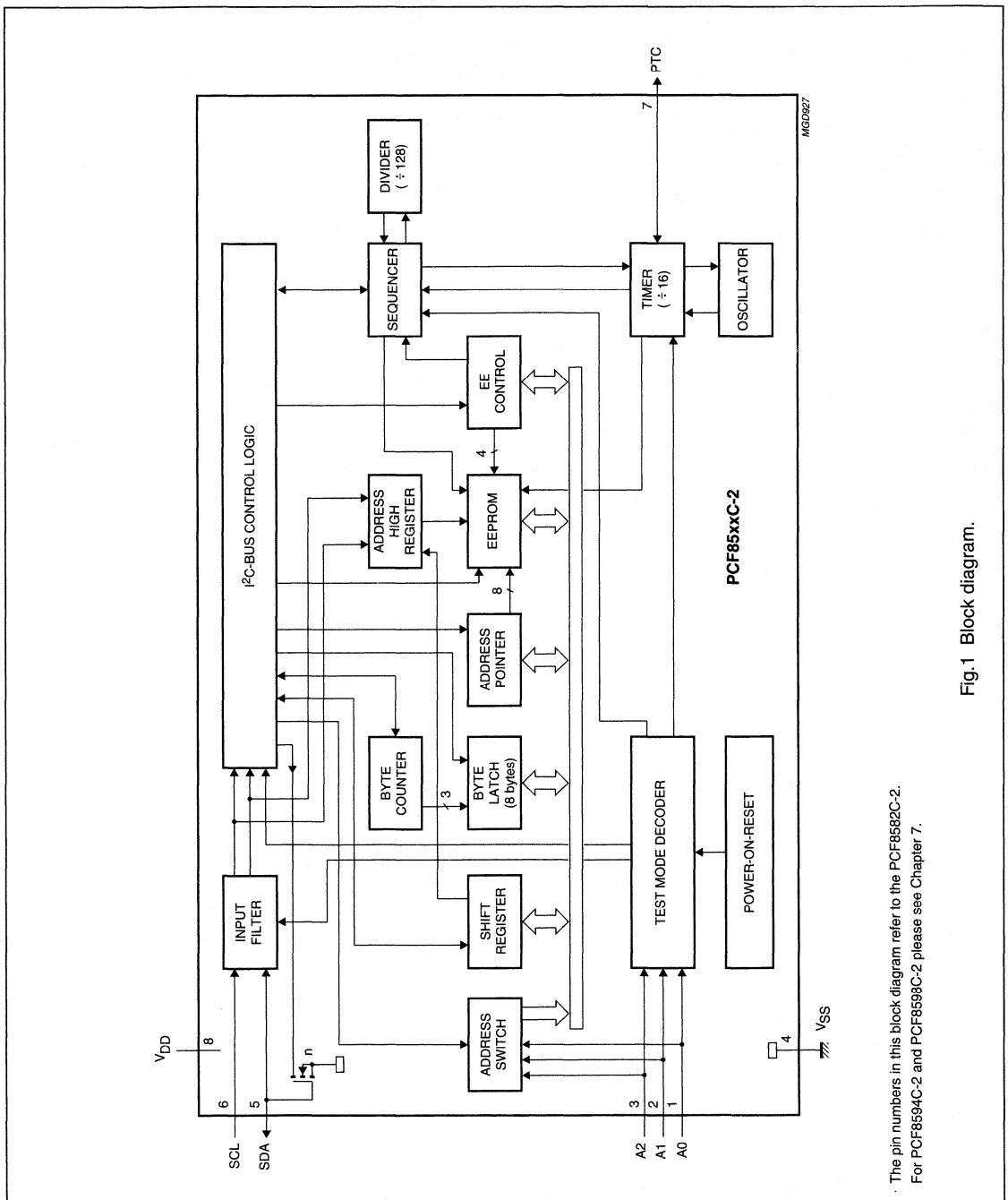


Fig.1 Block diagram.

The pin numbers in this block diagram refer to the PCF8582C-2.
For PCF8594C-2 and PCF8598C-2 please see Chapter 7.

7 PINNING

7.1 Pin description PCF8582C-2

SYMBOL	PIN	DESCRIPTION
A0	1	address input 0
A1	2	address input 1
A2	3	address input 2
V_{SS}	4	negative supply voltage
SDA	5	serial data input/output (I²C-bus)
SCL	6	serial clock input (I²C-bus)
PTC	7	programming time control output
V_{DD}	8	positive supply voltage

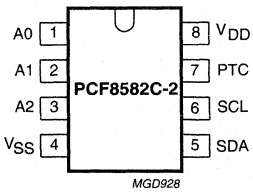


Fig.2 Pin configuration PCF8582C-2.

7.2 Pin description PCF8594C-2

SYMBOL	PIN	DESCRIPTION
WP	1	write-protection input
A1	2	address input 1
A2	3	address input 2
V_{SS}	4	negative supply voltage
SDA	5	serial data input/output (I²C-bus)
SCL	6	serial clock input (I²C-bus)
PTC	7	programming time control output
V_{DD}	8	positive supply voltage

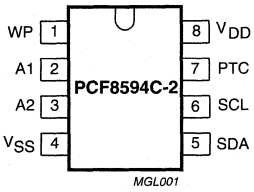


Fig.3 Pin configuration PCF8594C-2.

7.3 Pin description PCF8598C-2

SYMBOL	PIN	DESCRIPTION
WP	1	write-protection input
n.c.	2	not connected
A2	3	address input 2
V_{SS}	4	negative supply voltage
SDA	5	serial data input/output (I²C-bus)
SCL	6	serial clock input (I²C-bus)
PTC	7	programming time control output
V_{DD}	8	positive supply voltage

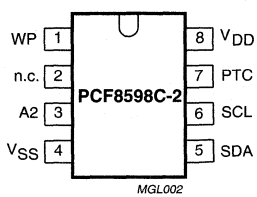


Fig.4 Pin configuration PCF8598C-2.

8 I²C-BUS PROTOCOL

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The serial bus consists of two bidirectional lines: one for data signals (SDA), and one for clock signals (SCL).

Both the SDA and SCL lines must be connected to a positive supply voltage via a pull-up resistor.

The following protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as control signals.

8.1 Bus conditions

The following bus conditions have been defined:

- **Bus not busy**: both data and clock lines remain HIGH.
- **Start data transfer**: a change in the state of the data line, from HIGH-to-LOW, while the clock is HIGH, defines the START condition.
- **Stop data transfer**: a change in the state of the data line, from LOW-to-HIGH, while the clock is HIGH, defines the STOP condition.
- **Data valid**: the state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. There is one clock pulse per bit of data.

8.2 Data transfer

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes, transferred between the START and STOP conditions is limited to 7 bytes in the E/W mode and 8 bytes in the page E/W mode.

Data transfer is unlimited in the read mode.
The information is transmitted in bytes and each receiver acknowledges with a ninth bit.

Within the I²C-bus specifications a low-speed mode (2 kHz clock rate) and a high speed mode (100 kHz clock rate) are defined. The PCF85xxC-2 operates in both modes.

By definition a device that sends a signal is called a 'transmitter', and the device which receives the signal is called a 'receiver'. The device which controls the signal is called the 'master'. The devices that are controlled by the master are called 'slaves'.

Each byte is followed by one acknowledge bit. This acknowledge bit is a HIGH level, put on the bus by the transmitter. The master generates an extra acknowledge related clock pulse. The slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte.

The master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse.

Set-up and hold times must be taken into account.
A master receiver must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master generation of the STOP condition.

8.3 Device addressing

Following a START condition the bus master must output the address of the slave it is accessing. The 4 MSBs of the slave address are the device type identifier (see Fig.5). For the PCF85xxC-2 this is fixed to '1010'.

The next three significant bits address a particular device or memory page (page = 256 bytes of memory). A system could have up to eight PCF8582C-2 (or four PCF8594C-2 containing two memory pages each or two PCF8598C-2 containing four memory pages each, respectively) devices on the bus. The eight addresses are defined by the state of the A0, A1 and A2 inputs.

The last bit of the slave address defines the operation to be performed. When set to logic 1 a read operation is selected.

Address bits must be connected to either V_{DD} or V_{SS}.

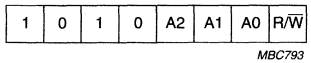


Fig.5 Slave address.

8.4 Write operations

8.4.1 BYTE/WORD WRITE

For a write operation the PCF85xxC-2 requires a second address field. This address field is a word address providing access to the 256 words of memory. Upon receipt of the word address the PCF85xxC-2 responds with an acknowledge and awaits the next eight bits of data, again responding with an acknowledge. Word address is automatically incremented. The master can now terminate the transfer by generating a STOP condition or transmit up to six more bytes of data and then terminate by generating a STOP condition.

After this STOP condition the E/W cycle starts and the bus is free for another transmission. Its duration is 10 ms per byte.

During the E/W cycle the slave receiver does not send an acknowledge bit if addressed via the I²C-bus.

8.4.2 PAGE WRITE

The PCF85xxC-2 is capable of an eight-byte page write operation. It is initiated in the same manner as the byte write operation. The master can transmit eight data bytes within one transmission. After receipt of each byte the PCF85xxC-2 will respond with an acknowledge.
The typical E/W time in this mode is 9 × 3.5 ms = 31.5 ms. Erasing a block of 8 bytes in page mode takes typical 3.5 ms and sequential writing of these 8 bytes another typical 28 ms.

After the receipt of each data byte the three low order bits of the word address are internally incremented. The high order five bits of the address remain unchanged. The slave acknowledges the reception of each data byte with an ACK. The I²C-bus data transfer is terminated by the master after the 8th byte with a STOP condition. If the master transmits more than eight bytes prior to generating the STOP condition, no acknowledge will be given on the ninth (and following) data bytes and the whole transmission will be ignored and no programming will be done. As in the byte write operation, all inputs are disabled until completion of the internal write cycles.

8.4.3 REMARK

A write to the EEPROM is always performed if the pin WP is LOW (not on PCF8582C-2). If WP is HIGH, then the upper half of the EEPROM is write-protected and no acknowledge will be given by the PCF85xxC-2 when one of the upper 256 EEPROM bytes (PCF8594C-2) or 512 EEPROM bytes (PCF8598C-2) is addressed. However, an acknowledge will be given after the slave address and the word address.

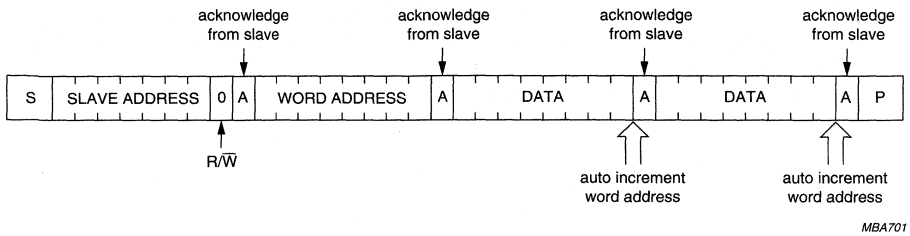


Fig.6 Auto increment memory word address; two byte write.

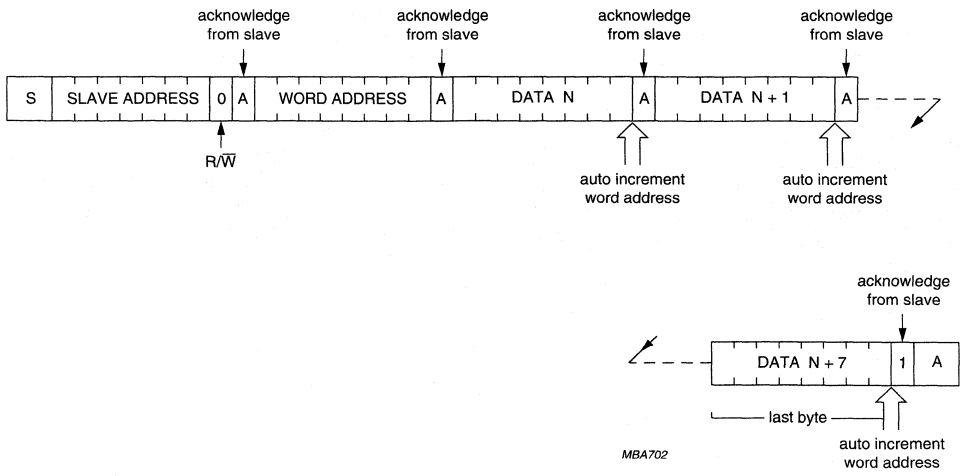


Fig.7 Page write operation; eight bytes.

8.5 Read operations

Read operations are initiated in the same manner as write operations with the exception that the LSB of the slave address is set to logic 1.

There are three basic read operations; current address read, random read and sequential read sequential read.

8.5.1 REMARK

The lower 8 bits of the word address are incremented after each transmission of a data byte (read or write). The MSB of the word address, which is defined in the slave address, is not changed when the word address count overflows. Thus, the word address overflows from 255 to 0 and from 511 to 256.

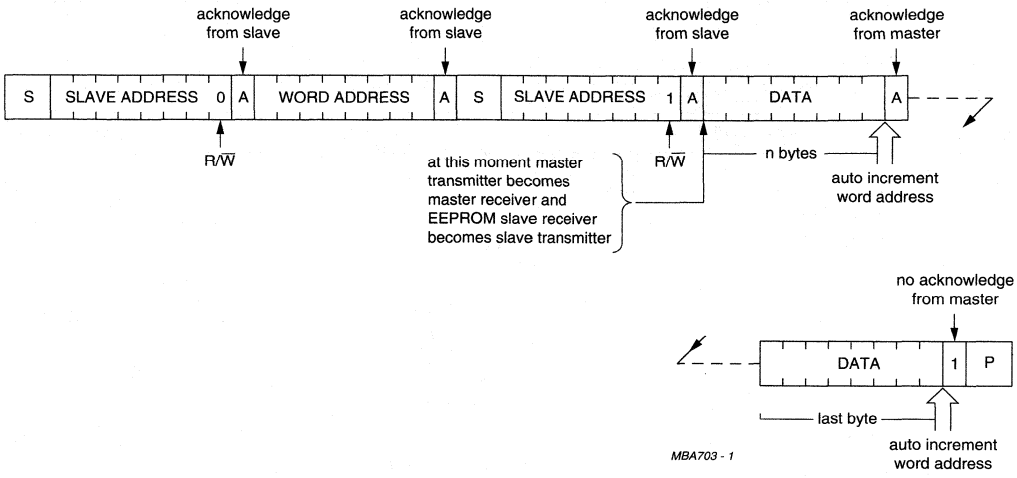


Fig.8 Master reads PCF85xxC-2 slave after setting word address (write word address; read data).

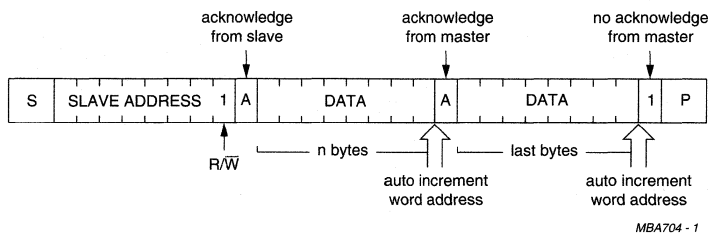


Fig.9 Master reads PCF85xxC-2 immediately after first byte (read mode).

9 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		−0.3	+6.5	V
V_I	input voltage on any input pin	$\|Z_i\| > 500\ \Omega$	$V_{SS} - 0.8$	+6.5	V
I_I	input current on any input pin		−	1	mA
I_O	output current		−	10	mA
T_{stg}	storage temperature		−65	+150	°C
T_{amb}	operating ambient temperature		−40	+85	°C

10 CHARACTERISTICS

V_{DD} = 2.5 to 6.0 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Supplies					
V_{DD}	supply voltage		2.5	6.0	V
I_{DDR}	supply current read	f_{SCL} = 100 kHz			
		V_{DD} = 2.5 V	−	60	µA
		V_{DD} = 6.0 V	−	200	µA
I_{DDW}	supply current E/W	f_{SCL} = 100 kHz			
	PCF8582C-2	V_{DD} = 2.5 V	−	0.6	mA
		V_{DD} = 6.0 V	−	2.0	mA
	PCF8594C-2	V_{DD} = 2.5 V	−	0.8	mA
		V_{DD} = 6.0 V	−	2.5	mA
	PCF8598C-2	V_{DD} = 2.5 V	−	1.0	mA
		V_{DD} = 6.0 V	−	4.0	mA
$I_{DD(stb)}$	standby supply current	V_{DD} = 2.5 V	−	3.5	µA
		V_{DD} = 6.0 V	−	10	µA
PTC output (pin 7)					
V_{IL}	LOW level input voltage		−0.8	$0.1V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.9V_{DD}$	$V_{DD} + 0.8$	V
SCL input (pin 6)					
V_{IL}	LOW level input voltage		−0.8	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	+6.5	V
I_{LI}	input leakage current	$V_I = V_{DD}$ or V_{SS}	−	±1	µA
f_{SCL}	clock input frequency		0	100	kHz
C_I	input capacitance	$V_I = V_{SS}$	−	7	pF
SDA input/output (pin 5)					
V_{IL}	LOW level input voltage		−0.8	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	+6.5	V
V_{OL}	LOW level output voltage	I_{OL} = 3 mA; $V_{DD(min)}$	−	0.4	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{LO}	output leakage current	$V_{OH} = V_{DD}$	–	1	μA
C_I	input capacitance	$V_I = V_{SS}$	–	7	pF
Data retention time					
t_S	data retention time	T_{amb} = 55 °C	10	–	years

11 I²C-BUS CHARACTERISTICS

All of the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing from V_{SS} to V_{DD}; see Fig.10.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
f_{SCL}	clock frequency		0	100	kHz
t_{BUF}	bus free time between a STOP and START condition		4.7	–	μs
$t_{HD;STA}$	START condition hold time after which first clock pulse is generated		4.0	–	μs
t_{LOW}	LOW level clock period		4.7	–	μs
t_{HIGH}	HIGH level clock period		4.0	–	μs
$t_{SU;STA}$	set-up time for STARt condition	repeated start	4.7	–	μs
$t_{HD;DAT}$	data hold time				
	for bus compatible masters		5	–	μs
	for bus devices	note 1	0	–	ns
$t_{SU;DAT}$	data set-up time		250	–	ns
t_r	SDA and SCL rise time		–	1	μs
t_f	SDA and SCL fall time		–	300	ns
$t_{SU;STO}$	set-up time for STOP condition		4.0	–	μs

Note

1. The hold time required (not greater than 300 ns) to bridge the undefined region of the falling edge of SCL must be internally provided by a transmitter.

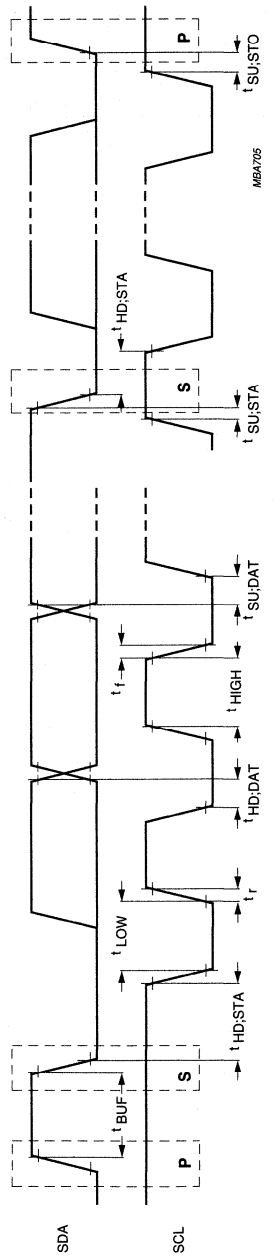


Fig.10 Timing requirements for the I²C-bus.

P = STOP condition; **S** = START condition.

12 WRITE CYCLE LIMITS

Selection of the chip address is achieved by connecting the A0, A1 and A2 inputs to either V_{SS} or V_{DD}.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
E/W cycle timing						
$t_{E/W}$	E/W cycle time	internal oscillator	–	7	–	ms
		external clock	4	–	10	ms
Endurance						
$N_{E/W}$	E/W cycle per byte	T_{amb} = −40 to +85 °C	100000	–	–	cycles
		T_{amb} = 22 °C	–	1000000	–	cycles

13 EXTERNAL CLOCK TIMING

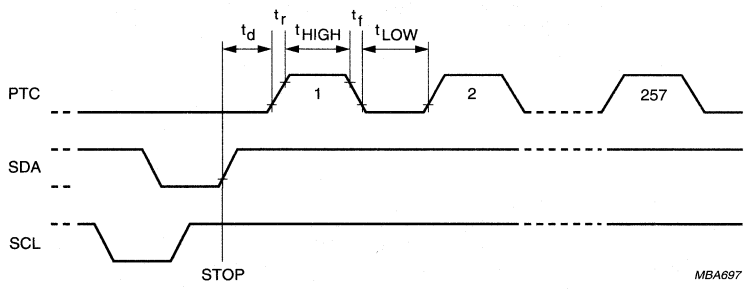


Fig.11 One byte E/W cycle.

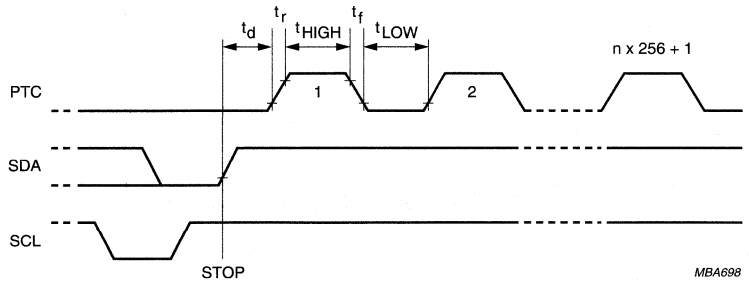


Fig.12 n bytes E/W cycle (n = 2 to 7).

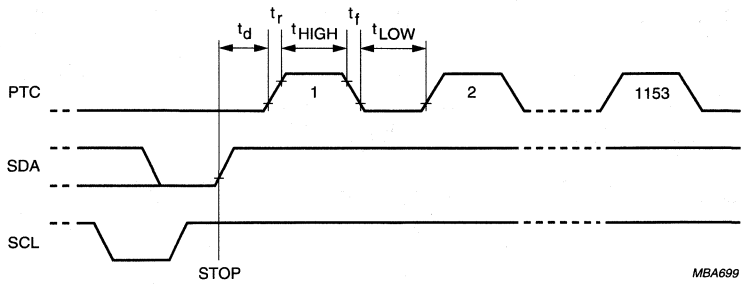
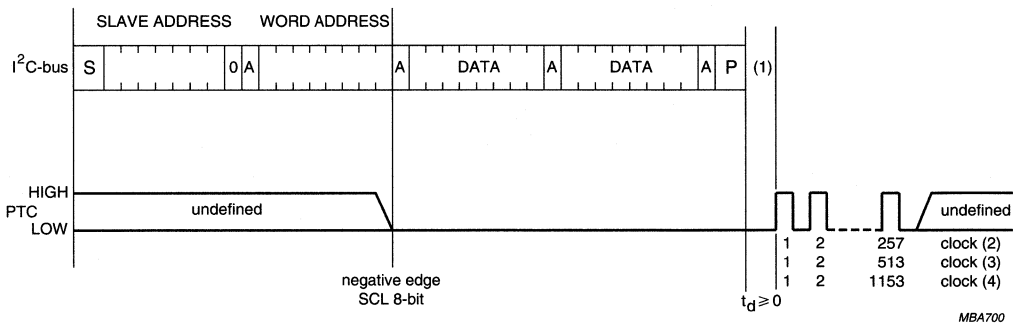


Fig.13 Page mode.



(1) If an external clock is chosen, this information is latched internally by setting pin 7 (PTC) LOW after transmission of the eighth bits of the word address (negative edge of SCL). Thus the state of pin 7 may be previously undefined. Leaving pin 7 LOW causes a higher standby current.

(2) 1-byte programming.

(3) 2-byte programming.

(4) One page (8 bytes) programming.

Fig.14 External clock.

14.318–150 MHz I²C 1:18 Clock Buffer — PCK2001

FEATURES

- HIGH speed, LOW noise non-inverting 1–18 buffer
- Typically used to support four SDRAM DIMMs
- Multiple V_{DD}, V_{SS} pins for noise reduction
- 3.3V operation
- Separate 3-State pin for testing
- ESD protection exceeds 2000V per Standard 801.2
- Optimized for 66MHz, 100MHz and 133MHz operation
- 175 ps skew outputs
- Available in 48-pin SSOP package
- See PCK2001M for mobile (reduced pincount) 28-pin 1-10 buffer version
- Individual clock output enable/disable via I²C

DESCRIPTION

The PCK2001 is a 1–18 fanout buffer used for 133/100 MHz CPU, 66/33 MHz PCI, 14.318 MHz REF, or 133/100/66 MHz SDRAM clock distribution. 18 outputs are typically used to support up to 4 SDRAM DIMMS commonly found in desktop, workstation or server applications.

All clock outputs meet Intel's drive, rise/fall time, accuracy, and skew requirements. An I²C interface is included to allow each output to be enabled/disabled individually. An output disabled via the I²C interface will be held in the LOW state. In addition, there is an OE input which 3-States all outputs.

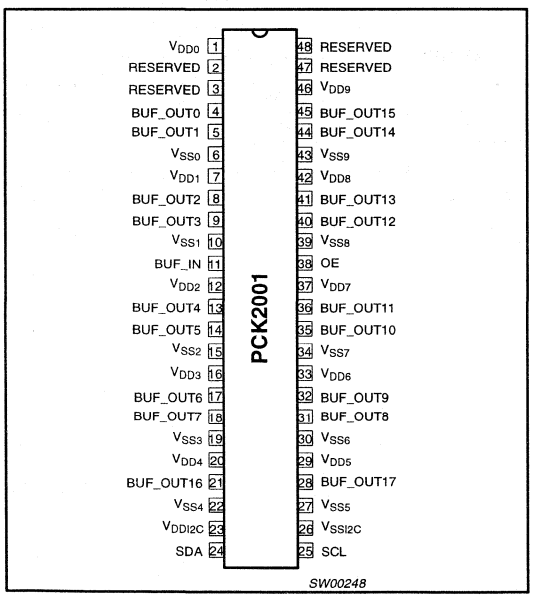
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay BUF_IN to BUF_OUT$_n$	V_{CC} = 3.3V, CL = 30pF	2.5 2.5	ns
t_r	Rise time	V_{CC} = 3.3V, CL = 30pF	1.0	ns
t_f	Fall time	V_{CC} = 3.3V, CL = 20pF	700	ps
I_{CC}	Total supply current	V_{CC} = 3.465V	50	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
48-Pin Plastic SSOP	0°C to +70°C	PCK2001 DL	SOT370-1

PIN CONFIGURATION



I²C is a trademark of Philips Semiconductors Corporation.

PIN DESCRIPTION

PIN NUMBER	I/O TYPE	SYMBOL	FUNCTION
4, 5, 8, 9	Output	BUF_OUT (0–3)	Buffered clock outputs
13, 14, 17, 18	Output	BUF_OUT (4–7)	Buffered clock outputs
31, 32, 35, 36	Output	BUF_OUT (8–11)	Buffered clock outputs
40, 41, 44, 45	Output	BUF_OUT (12–15)	Buffered clock outputs
21, 28	Output	BUF_OUT (16–17)	Buffered clock outputs
11	Input	BUF_IN	Buffered clock input
38	Input	OE	Active high output enable
24	I/O	SDA	I²C serial data
25	Input	SCL	I²C serial clock
3, 7, 12, 16, 20, 29, 33, 37, 42, 46	Input	$V_{DD\ (0–9)}$	3.3V Power supply
6, 10, 15, 19, 22, 27, 30, 34, 39, 43	Input	$V_{SS\ (0–9)}$	Ground
23	Input	V_{DDI2C}	3.3V I²C Power supply
26	Input	V_{SSI2C}	I²C Ground

FUNCTION TABLE

OE	BUF_IN	I²CEN	BUF_OUTn
L	X	X	Z
H	L	X	L
H	H	H	H
H	H	L	L

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to V_{SS} (V_{SS} = 0V)

SYMBOL	PARAMETER	CONDITION	LIMITS		UNIT
			MIN	MAX	
V_{DD}	DC 3.3V supply voltage		–0.5	+4.6	V
I_{IK}	DC input diode current	V_I < 0		–50	mA
V_I	DC input voltage	Note 2	–0.5	5.5	V
I_{OK}	DC output diode current	V_O > V_{DD} or V_O < 0		±50	mA
V_O	DC output voltage	Note 2	–0.5	V_{CC} + 0.5	V
I_O	DC output source or sink current	V_O >= 0 to V_{DD}		±50	mA
T_{STG}	Storage temperature range		–65	+150	°C
P_{TOT}	Power dissipation per package plastic medium-shrink SO (SSOP)	For temperature range: 0 to +70°C above +55°C derate linearly with 11.3mW/K		850	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{DD}	DC 3.3V supply voltage		3.135	3.465	V
C_L	Capacitive load		20	30	pF
V_I	DC input voltage range		0	V_{DD}	V
V_O	DC output voltage range		0	V_{DD}	V
T_{amb}	Operating ambient temperature range in free air		0	+70	°C

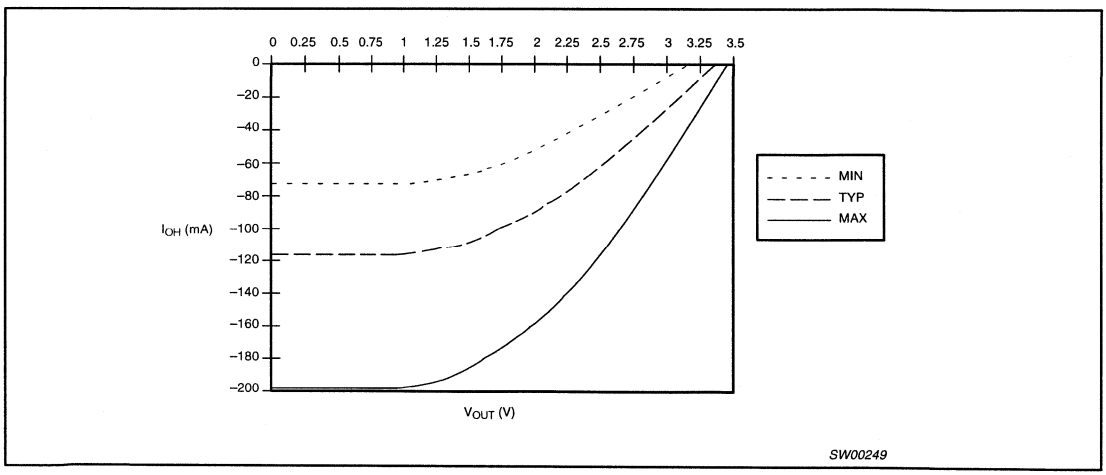
DC CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS			LIMITS		UNIT
					T_{amb} = 0°C to +70°C		
		V_{DD} (V)	OTHER		MIN	MAX	
V_{IH}	HIGH level input voltage	3.135 to 3.465			2.0	V_{DD} + 0.3	V
V_{IL}	LOW level input voltage	3.135 to 3.465			V_{SS} – 0.3	0.8	V
V_{OH}	3.3V output HIGH voltage	3.135 to 3.465	I_{OH} = –1mA		2.4	–	V
V_{OL}	3.3V output LOW voltage	3.135 to 3.465	I_{OL}= 1mA		–	0.4	V
I_{OH}	Output HIGH current	3.135 to 3.465	V_{OUT} = 2.0V		–54	–	mA
		3.135 to 3.465	V_{OUT} = 3.135V		–	–46	
I_{OL}	Output LOW current	3.135 to 3.465	V_{OUT} = 1.0V		54	–	mA
		3.135 to 3.465	V_{OUT} = 0.4V		–	53	
$\pm I_I$	Input leakage current	3.465			–	5	µA
$\pm I_{OZ}$	3-State output OFF-State current	3.465	V_{OUT} = V_{DD}or GND	I_O = 0	–	10	µA
I_{CC}	Quiescent supply current	3.465	V_I = V_{DD} or GND	I_O = 0	–	100	µA
ΔI_{CC}	Additional quiescent supply current given per control pin	3.135 to 3.465	V_I = V_{DD}– 0.6V	I_O = 0	–	500	µA

SDRAM CLOCK OUTPUT BUFFER PULL-UP CHARACTERISTICS

PULL-UP			
VOLTAGE (V)	I (mA)		
	MIN	TYP	MAX
0	–72	–116	–198
1	–72	–116	–198
1.40	–68	–110	–188
1.50	–67	–107	–184
1.65	–64	–103	–177
1.80	–60	–98	–170
2.00	–54	–90	–157
2.40	–39	–69	–126
2.60	–30	–56	–107
3.135	0	–15	–46
3.30		0	–23
3.465			0

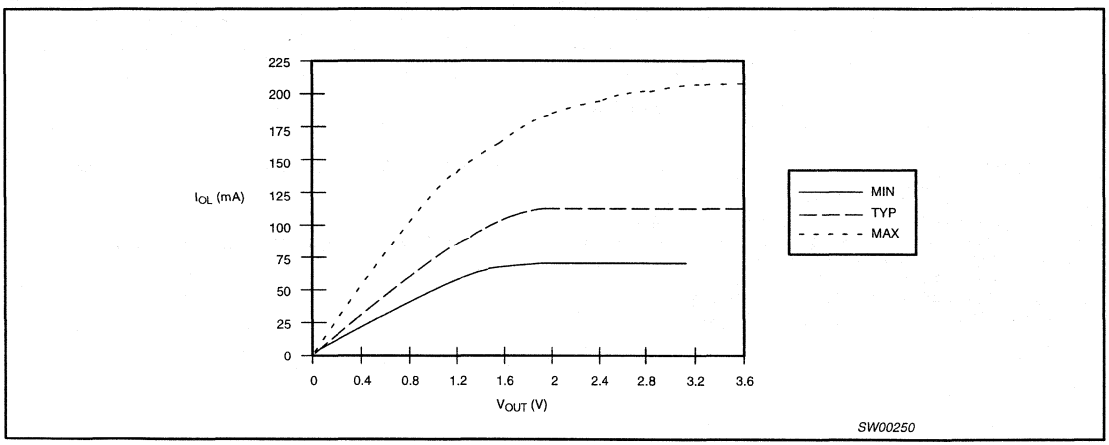
SDRAM PULL-UP



SDRAM CLOCK OUTPUT BUFFER PULL-DOWN CHARACTERISTICS

PULL-UP			
VOLTAGE (V)	I (mA)		
	MIN	TYP	MAX
0	0	0	0
0.4	23	34	53
0.65	35	52	83
0.85	43	65	104
1.00	49	74	118
1.4	61	93	152
1.5	64	98	159
1.65	67	103	168
1.8	70	108	177
1.95	72	112	184
3.135	72	112	204
3.6		112	204

SDRAM PULL-DOWN



AC CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS T_{amb} = 0°C to +70°C			UNIT
			NOTES	MIN	TYP[9]	MAX	
T_{SDKP}	SDRAM CLK period	66MHz	1, 6	15.0	15.2	15.5	ns
T_{SDKH}	SDRAM CLK HIGH time		2, 6, 8	5.6	7.8	8.4	
T_{SDKL}	SDRAM CLK LOW time		3, 6, 8	5.3	7.4	8.0	
T_{SDKP}	SDRAM CLK period	100MHz	1, 6	10.0	10.01	10.5	ns
T_{SDKH}	SDRAM CLK HIGH time		2, 6, 8	3.3	5.1	5.7	
T_{SDKL}	SDRAM CLK LOW time		3, 6, 8	3.1	4.9	5.5	
T_{SDKP}	SDRAM clock period	133MHz	1, 6	7.4	7.5	7.7	ns
T_{SDKH}	SDRAM CLK HIGH time		2, 6, 8	2.6	3.2	3.8	
T_{SDKL}	SDRAM CLK LOW time		3, 6, 8	2.1	2.8	3.5	
T_{SDRISE}	SDRAM rise time		4, 6, 10	1.5	2.0	4.0	V/ns
T_{SDFALL}	SDRAM fall time		4, 6, 11	1.5	2.9	4.0	V/ns
T_{PLH}	SDRAM buffer LH propagation delay		6, 7	1.0	2.5	3.5	ns
T_{PHL}	SDRAM buffer HL propagation delay		6, 7	1.0	2.5	3.5	ns
T_{PZL}, T_{PZH}	SDRAM buffer enable time		6, 7	1.0	2.6	5.0	ns
T_{PLZ}, T_{PHZ}	SDRAM buffer disable time		6, 7	1.0	2.7	5.0	ns
DUTY CYCLE	Output Duty Cycle	Measured at 1.5V	5, 6, 7	45	52	55	%
T_{SDSKW}	SDRAM Bus CLK skew		1, 6		150	250	ps
T_{DDSKW}	Device to device skew					250	ps

NOTES:
1. Clock period and skew are measured on the rising edge at 1.5V.
2. T_{SDKH} is measured at 2.4V as shown in Figure 4.
3. T_{SDKL} is measured at 0.4V as shown in Figure 4.
4. T_{SDRISE} and T_{SDFALL} are measured as a transition through the threshold region V_{OL} = 0.4V and V_{OH} = 2.4V (1mA) JEDEC specification.
5. Duty cycle should be tested with a 50/50% input.
6. Over MIN (20pF) to MAX (30pF) discrete load, process, voltage, and temperature.
7. Input edge rate for these tests must be faster than 1 V/ns.
8. Calculated at minimum edge rate (1.5ns) to guarantee 45/55% duty cycle at 1.5V. Pulsewidth is required to be wider at the faster edge to ensure duty cycle specification is met.
9. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
10. Typical is measured with MAX (30pf) discrete load.
11. Typical is measured with MIN (20pf) discrete load.

I²C CONSIDERATIONS

I²C has been chosen as the serial bus interface to control the PCK2001. I²C was chosen to support the JEDEC proposal JC-42.5 168 Pin Unbuffered SDRAM DIMM. All vendors are required to determine the legal issues associated with the manufacture of I²C devices.

1) Address assignment: The clock driver in this specification uses the single, 7-bit address shown below. All devices can use the address if only one master clock driver is used in a design. The address can be re-used for the CKBF device if no other conflicting I²C clock driver is used in the system.

The following address was confirmed by Philips on 09/04/96.

A6	A5	A4	A3	A2	A1	A0	R/W#
1	1	0	1	0	0	1	0

NOTE: The R/W# bit is used by the I²C controller as a data direction bit. A 'zero' indicates a transmission (WRITE) to the clock device. A 'one' indicates a request for data (READ) from the clock driver. Since the definition of the clock buffer only allows the controller to WRITE data; the R/W# bit of the address will always be seen as 'zero'. Optimal address decoding of this bit is left to the vendor.

2) Options: It is our understanding that metal mask options and other pinouts of this type of clock driver will be allowed to use the same address as the original CKBF device. I²C addresses are defined in terms of function (master clock driver) rather than form (pinout, and option).

3) Slave/Receiver: The clock driver is assumed to require only slave/receiver functionality. Slave/transmitter functionality is optional.

4) Data Transfer Rate: 100 kbits/s (standard mode) is the base functionality required. Fast mode (400 kbits/s) functionality is optional.

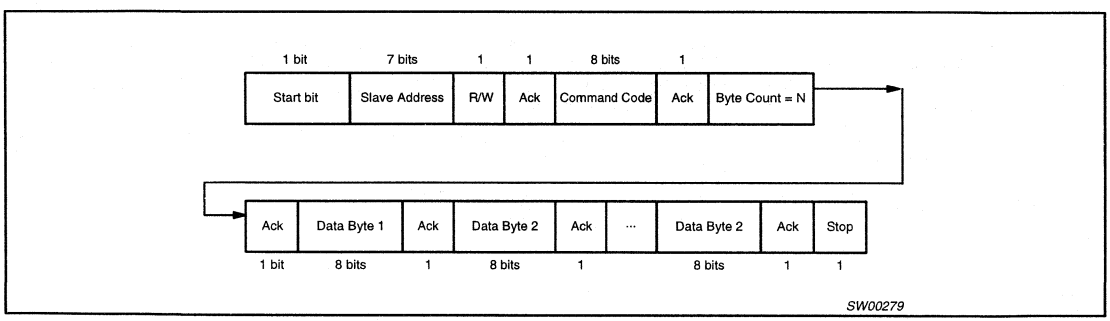
5) Logic Levels: I²C logic levels are based on a percentage of V_{DD} for the controller and other devices on the bus. Assume all devices are based on a 3.3 Volt supply.

6) Data Byte Format: Byte format is 8 Bits as described in the following appendices.

7) Data Protocol: To simplify the clock I²C interface, the clock driver serial protocol was specified to use only block writes from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. Indexed bytes are not allowed. However, the SMBus controller has a more specific format than the generic I²C protocol.

The clock driver must meet this protocol which is more rigorous than previously stated I²C protocol. Treat the description from the viewpoint of controller. The controller "writes" to the clock driver and if possible would "read" from the clock driver (the clock driver is a slave/receiver only and is incapable of this transaction.)

"The block write begins with a slave address and a write condition. After the command code the host (controller) issues a byte count which describes how many more bytes will follow in the message. If the host had 20 bytes to send, the first byte would be the number 20 (14h), followed by the 20 bytes of data. The byte count may not be 0. A block write command is allowed to transfer a maximum of 32 data bytes."



NOTE: The acknowledgement bit is returned by the slave/receiver (the clock driver).

Consider the command code and the byte count bytes required as the first two bytes of any transfer. The command code is software programmable via the controller, but will be specified as 0000 0000 in the clock specification. The byte count byte is the number of additional bytes required to transfer, not counting the command code and byte count bytes. Additionally, the byte count byte is required to be a minimum of 1 byte and a maximum of 32 bytes to satisfy the above requirement.

For example:

Byte count byte		Notes:
MSB	LSB	
0000	0000	Not allowed. Must have at least one byte.
0000	0001	Data for functional and frequency select register (currently byte 0 in spec)
0000	0010	Reads first two bytes of data. (byte 0 then byte 1)
0000	0011	Reads first three bytes (byte 0, 1, 2 in order)
0000	0100	Reads first four bytes (byte 0, 1, 2, 3 in order)
0000	0101	Reads first five bytes (byte 0, 1, 2, 3, 4 in order)
0000	0110	Reads first six bytes (byte 0, 1, 2, 3, 4, 5 in order)
0000	0111	Reads first seven bytes (byte 0, 1, 2, 3, 4, 5, 6 in order)
0010	0000	Max byte count supported = 32

A transfer is considered valid after the acknowledge bit corresponding to the byte count is read by the controller. The serial controller interface can be simplified by discarding the information in both the command code and the byte count bytes and simply reading all the bytes that are sent to the clock driver after being addressed by the controller. It is expected that the controller will not provide more bytes than the clock driver can handle. A clock vendor may choose to discard any number of bytes that exceed the defined byte count.

8) Clock stretching: The clock device must not hold/stretch the SCLOCK or SDATA lines low for more than 10 mS. Clock stretching is discouraged and should only be used as a last resort. Stretching the clock/data lines for longer than this time puts the device in an error/time-out mode and may not be supported in all platforms. It is assumed that all data transfers can be completed as specified without the use of clock/data stretching.

9) General Call: It is assumed that the clock driver will not have to respond to the "general call."

10) Electrical Characteristics: All electrical characteristics must meet the standard mode specifications found in section 15 of the I²C specification.

a) Pull-Up Resistors: Any internal resistors pull-ups on the SDATA and SCLOCK inputs must be stated in the individual datasheet. The use of internal pull-ups on these pins of below 100K is discouraged. Assume that the board designer will use a single external pull-up resistor for each line and that these values are in the 5 - 6K Ohm range. Assume one I²C device per DIMM (serial presence detect), one I²C controller, one clock driver plus one/two more I²C devices on the platform for capacitive loading purposes.

(b) Input Glitch Filters: Only fast mode I²C devices require input glitch filters to suppress bus noise. The clock driver is specified as a standard mode device and is not required to support this feature.

11) PWR DWN#: If a clock driver is placed in PWR DWN# mode, the SDATA and SCLK inputs must be Tri-Stated and the device must retain all programming information. I_{dd} current due to the I²C circuitry must be characterized and in the data sheet.

For specific I²C information consult the Philips I²C Peripherals Data Handbook IC12 (1997)

SERIAL CONFIGURATION MAP

The serial bits will be read by the clock buffer in the following order:

Byte 0 – Bits 7, 6, 5, 4, 3, 2, 1, 0
Byte 1 – Bits 7, 6, 5, 4, 3, 2, 1, 0
Byte 2 – Bits 7, 6, 5, 4, 3, 2, 1, 0

All unused register bits (Reserved and N/A) should be desined as "Dont Care". It is expected that the controller will force all of these bits to a "0" level.

All register bits labeled "Initialize to 0" must be written to zero during intialization. Failure to do so may result in a higher than normal operating current. The controller will read back the last written value.

Byte 0: Output active/inactive register

1 = enable; 0 = disable

BIT	PIN#	NAME	DESCRIPTION
7	18	BUF_OUT7	Active/Inactive
6	17	BUF_OUT6	Active/Inactive
5	14	BUF_OUT5	Active/Inactive
4	13	BUF_OUT4	Active/Inactive
3	9	BUF_OUT3	Active/Inactive
2	8	BUF_OUT2	Active/Inactive
1	5	BUF_OUT1	Active/Inactive
0	4	BUF_OUT0	Active/Inactive

NOTE:
1. Inactive means outputs are held LOW and are disabled from switching. These outputs are designed to be configured at power-on and are not expected to be configured during the normal modes of operation.

Byte 1: Output active/inactive register

1 = enable; 0 = disable

BIT	PIN#	NAME	DESCRIPTION
7	45	BUF_OUT15	Active/Inactive
6	44	BUF_OUT14	Active/Inactive
5	41	BUF_OUT13	Active/Inactive
4	40	BUF_OUT12	Active/Inactive
3	36	BUF_OUT11	Active/Inactive
2	35	BUF_OUT10	Active/Inactive
1	32	BUF_OUT9	Active/Inactive
0	31	BUF_OUT8	Active/Inactive

NOTE:
1. Inactive means outputs are held LOW and are disabled from switching. These outputs are designed to be configured at power-on and are not expected to be configured during the normal modes of operation.

Byte 2: Optional register for possible future requirments

BIT	PIN#	NAME	DESCRIPTION
7	28	BUF_OUT17	Active/Inactive
6	21	BUF_OUT16	Active/Inactive
5	—	(reserved)	(reserved)
4	—	(reserved)	(reserved)
3	—	(reserved)	(reserved)
2	—	(reserved)	(reserved)
1	—	(reserved)	(reserved)
0	—	(reserved)	(reserved)

NOTE:
1. Inactive means outputs are held LOW and are disabled from switching. These outputs are designed to be configured at power-on and are not expected to be configured during the normal modes of operation.

AC WAVEFORMS

$V_M = 1.5V$
$V_X = V_{OL} + 0.3V$
$V_Y = V_{OH} - 0.3V$
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

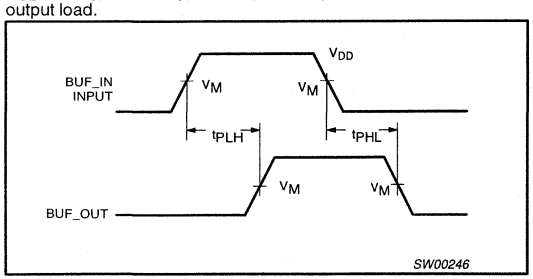


Figure 1. Load circuitry for switching times.

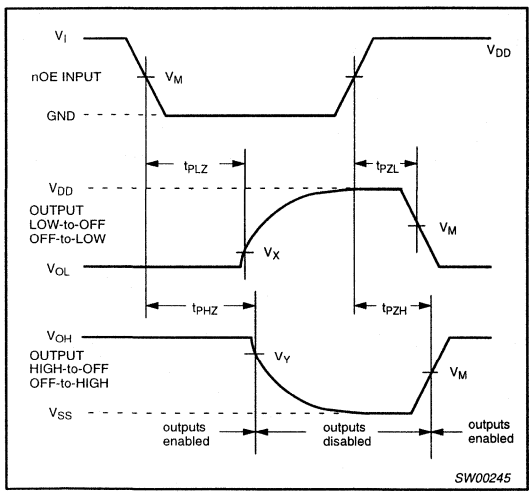


Figure 2. 3-State enable and disable times

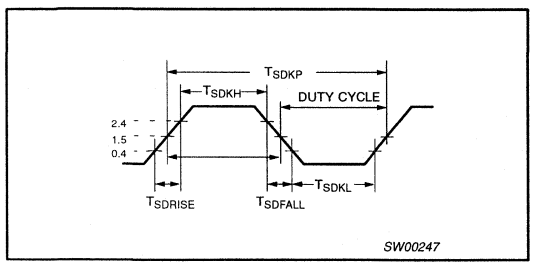


Figure 3. Buffer Output clock

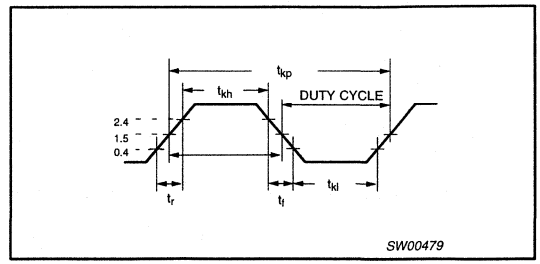
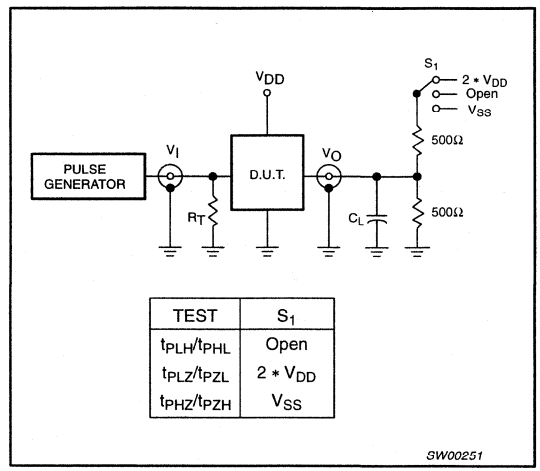


Figure 4. SDRAM Output clock

TEST CIRCUIT



TEST	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 * V_{DD}$
t_{PHZ}/t_{PZH}	V_{SS}

Figure 5. Load circuitry for switching times

14.318–150 MHz I²C 1:10 Clock Buffer — PCK2001M

FEATURES

- Mobile (reduced pincount) version of PCK2001
- Typically used to two SDRAM DIMMs
- 28 pin SSOP package
- Same general features as PCK2001
- See PCK2001 for 48-pin 1-18 buffer part supporting up to 4 SDRAM DIMMs
- Optimized for 66MHz, 100MHz and 133MHz operation
- 175 ps skew outputs
- Individual clock output enable/disable via I²C

DESCRIPTION

The PCK2001M is a 1–10 fanout buffer used for 133/100 MHz CPU, 66/33 MHz PCI, 14.318 MHz REF, or 133/100/66 MHz SDRAM clock distribution. 10 outputs are typically used to support up to 2 SDRAM DIMMs commonly found in laptop or mobile applications. The PCK2001M has the same features and operating characteristics of the PCK2001 and is available in the SSOP 28 pin package.

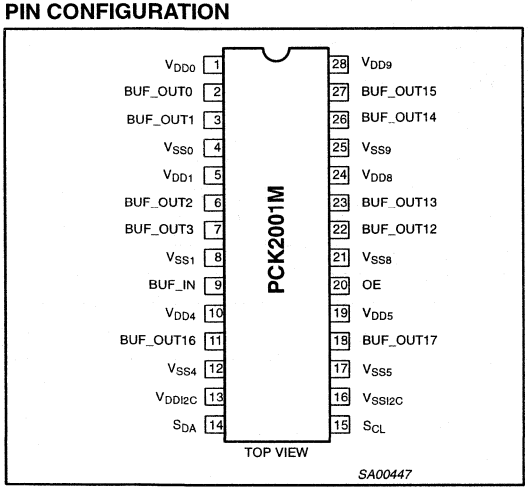
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay BUF_IN to BUF_OUT$_n$	V_{CC} = 3.3V, CL = 30pF	2.5 2.5	ns
t_r	Rise time	V_{CC} = 3.3V, CL = 30pF	1.0	ns
t_f	Fall time	V_{CC} = 3.3V, CL = 20pF	700	ps
I_{CC}	Total supply current	V_{CC} = 3.465V	50	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
28-Pin Plastic SSOP	0°C to +70°C	PCK2001M DB	SOT341–1

PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	I/O TYPE	SYMBOL	FUNCTION
2, 3, 6, 7	Output	BUF_OUT (0–3)	Buffered clock outputs
22, 23, 26, 27	Output	BUF_OUT (12–15)	Buffered clock outputs
11, 18	Output	BUF_OUT (16–17)	Buffered clock outputs
9	Input	BUF_IN	Buffered clock input
20	Input	OE	Active high ouput enable
14	I/O	SDA	I²C serial data
15	Input	SCL	I²C serial clock
1, 5, 10, 19, 24, 28	Input	$V_{DD\ (0–9)}$	3.3V power supply
4, 8, 12, 17, 21, 25	Input	$V_{SS\ (0–9)}$	Ground
13	Input	V_{DDI2C}	3.3V I²C power supply
16	Input	V_{DDI2C}	I²C ground

FUNCTION TABLE

OE	BUF_IN	I²CEN	BUF_OUTn
L	X	X	Z
H	L	X	L
H	H	H	H
H	H	L	L

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to V_{SS} (V_{SS} = 0V)

SYMBOL	PARAMETER	CONDITION	LIMITS		UNIT
			MIN	MAX	
V_{DD}	DC 3.3V supply voltage		–0.5	+4.6	V
I_{IK}	DC input diode current	V_I < 0		–50	mA
V_I	DC input voltage	Note 2	–0.5	5.5	V
I_{OK}	DC output diode current	V_O > V_{DD} or V_O < 0		±50	mA
V_O	DC output voltage	Note 2	–0.5	V_{CC} + 0.5	V
I_O	DC output source or sink current	V_O >= 0 to V_{DD}		±50	mA
T_{STG}	Storage temperature range		–65	+150	°C
P_{TOT}	Power dissipation per package plastic medium-shrink SO (SSOP)	For temperature range: 0 to +70°C above +55°C derate linearly with 11.3mW/K		850	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{DD}	DC 3.3V supply voltage		3.135	3.465	V
C_L	Capacitive load		20	30	pF
V_I	DC input voltage range		0	V_{DD}	V
V_O	DC output voltage range		0	V_{DD}	V
T_{amb}	Operating ambient temperature range in free air		0	+70	°C

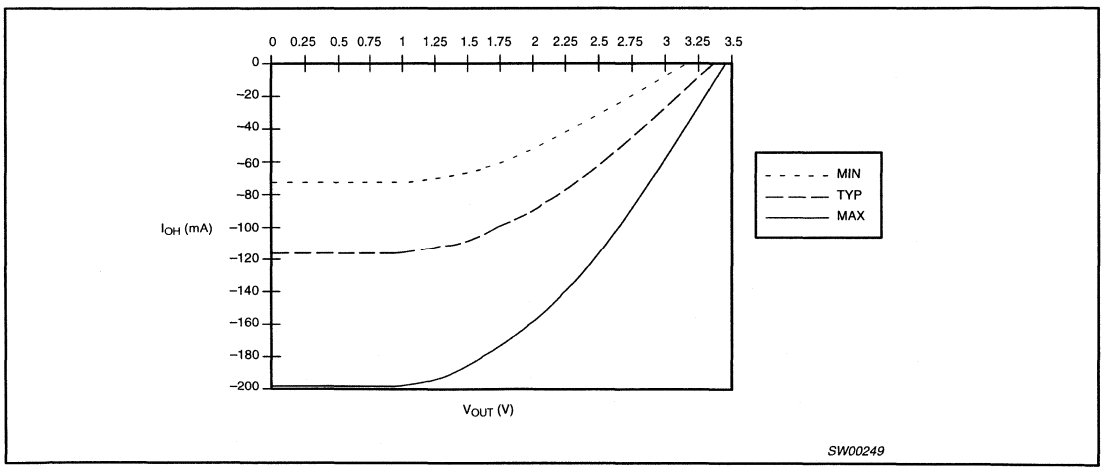
DC CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS			LIMITS T_{amb} = 0°C to +70°C		UNIT
		V_{DD} (V)	OTHER		MIN	MAX	
V_{IH}	HIGH level input voltage	3.135 to 3.465			2.0	V_{DD} + 0.3	V
V_{IL}	LOW level input voltage	3.135 to 3.465			V_{SS} – 0.3	0.8	V
V_{OH}	3.3V output HIGH voltage	3.135 to 3.465	I_{OH} = –1mA		2.4	–	V
V_{OL}	3.3V output LOW voltage	3.135 to 3.465	I_{OL}= 1mA		–	0.4	V
I_{OH}	Output HIGH current	3.135 to 3.465	V_{OUT} = 2.0V		–54	–	mA
		3.135 to 3.465	V_{OUT} = 3.135V		–	–46	
I_{OL}	Output LOW current	3.135 to 3.465	V_{OUT} = 1.0V		54	–	mA
		3.135 to 3.465	V_{OUT} = 0.4V		–	53	
$\pm I_I$	Input leakage current	3.465			–	5	µA
$\pm I_{OZ}$	3-State output OFF-State current	3.465	V_{OUT} = V_{DD}or GND	I_O = 0	–	10	µA
I_{CC}	Quiescent supply current	3.465	V_I = V_{DD} or GND	I_O = 0	–	100	µA
ΔI_{CC}	Additional quiescent supply current given per control pin	3.135 to 3.465	V_I = V_{DD}– 0.6V	I_O = 0	–	500	µA

SDRAM CLOCK OUTPUT BUFFER PULL-UP CHARACTERISTICS

PULL-UP			
VOLTAGE (V)	I (mA)		
	MIN	TYP	MAX
0	–72	–116	–198
1	–72	–116	–198
1.40	–68	–110	–188
1.50	–67	–107	–184
1.65	–64	–103	–177
1.80	–60	–98	–170
2.00	–54	–90	–157
2.40	–39	–69	–126
2.60	–30	–56	–107
3.135	0	–15	–46
3.30		0	–23
3.465			0

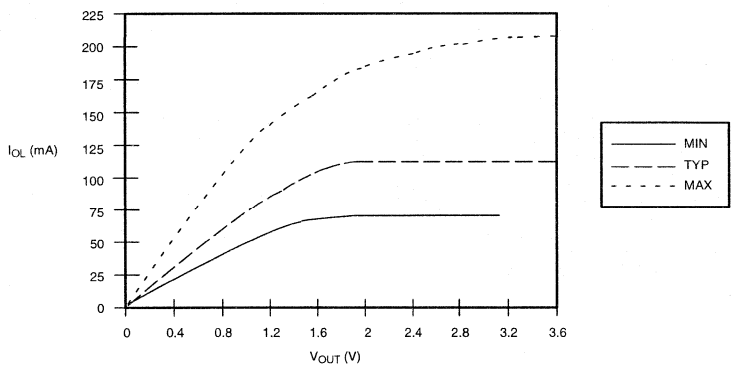
SDRAM PULL-UP



SDRAM CLOCK OUTPUT BUFFER PULL-DOWN CHARACTERISTICS

PULL-UP			
VOLTAGE (V)	I (mA)		
	MIN	TYP	MAX
0	0	0	0
0.4	23	34	53
0.65	35	52	83
0.85	43	65	104
1.00	49	74	118
1.4	61	93	152
1.5	64	98	159
1.65	67	103	168
1.8	70	108	177
1.95	72	112	184
3.135	72	112	204
3.6		112	204

SDRAM PULL-DOWN



AC CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS T_{amb} = 0°C to +70°C			UNIT
			NOTES	MIN	TYP[9]	MAX	
T_{SDKP}	SDRAM CLK period	66MHz	1, 6	15.0	15.2	15.5	ns
T_{SDKH}	SDRAM CLK HIGH time		2, 6, 8	5.6	7.8	8.4	
T_{SDKL}	SDRAM CLK LOW time		3, 6, 8	5.3	7.4	8.0	
T_{SDKP}	SDRAM CLK period	100MHz	1, 6	10.0	10.01	10.5	ns
T_{SDKH}	SDRAM CLK HIGH time		2, 6, 8	3.3	5.1	5.7	
T_{SDKL}	SDRAM CLK LOW time		3, 6, 8	3.1	4.9	5.5	
T_{SDKP}	SDRAM CLK period	133MHz	1, 6	7.4	7.5	7.7	ns
T_{SDKH}	SDRAM CLK HIGH time		2, 6, 8	2.6	3.2	3.8	
T_{SDKL}	SDRAM CLK LOW time		3, 6, 8	2.1	2.8	3.5	
T_{SDRISE}	SDRAM rise time		4, 6, 10	1.5	2.0	4.0	V/ns
T_{SDFALL}	SDRAM fall time		4, 6, 11	1.5	2.9	4.0	V/ns
T_{PLH}	SDRAM buffer LH propagation delay		6, 7	1.0	2.5	3.5	ns
T_{PHL}	SDRAM buffer HL propagation delay		6, 7	1.0	2.5	3.5	ns
T_{PZL}, T_{PZH}	SDRAM buffer enable time		6, 7	1.0	2.6	5.0	ns
T_{PLZ}, T_{PHZ}	SDRAM buffer disable time		6, 7	1.0	2.7	5.0	ns
DUTY CYCLE	Output Duty Cycle	Measured at 1.5V	5, 6, 7	45	52	55	%
T_{SDSKW}	SDRAM Bus CLK skew		1, 6		150	250	ps
T_{DDSKW}	Device to device skew					250	ps

NOTES:
1. Clock period and skew are measured on the rising edge at 1.5V.
2. T_{SDKH} is measured at 2.4V as shown in Figure 4.
3. T_{SDKL} is measured at 0.4V as shown in Figure 4.
4. T_{SDRISE} and T_{SDFALL} are measured as a transition through the threshold region V_{OL} = 0.4V and V_{OH} = 2.4V (1mA) JEDEC specification.
5. Duty cycle should be tested with a 50/50% input.
6. Over MIN (20pF) to MAX (30pF) discrete load, process, voltage, and temperature.
7. Input edge rate for these tests must be faster than 1 V/ns.
8. Calculated at minimum edge rate (1.5ns) to guarantee 45/55% duty cycle at 1.5V. Pulsewidth is required to be wider at the faster edge to ensure duty cycle specification is met.
9. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
10. Typical is measured with MAX (30pf) discrete load.
11. Typical is measured with MIN (20pf) discrete load.

I²C CONSIDERATIONS

I²C has been chosen as the serial bus interface to control the PCK2001M. I²C was chosen to support the JEDEC proposal JC-42.5 168 Pin Unbuffered SDRAM DIMM. All vendors are required to determine the legal issues associated with the manufacture of I²C devices.

1) Address assignment: The clock driver in this specification uses the single, 7-bit address shown below. All devices can use the address if only one master clock driver is used in a design. The address can be re-used for the CKBF device if no other conflicting I²C clock driver is used in the system.

The following address was confirmed by Philips on 09/04/96.

A6	A5	A4	A3	A2	A1	A0	R/W#
1	1	0	1	0	0	1	0

NOTE: The R/W# bit is used by the I²C controller as a data direction bit. A 'zero' indicates a transmission (WRITE) to the clock device. A 'one' indicates a request for data (READ) from the clock driver. Since the definition of the clock buffer only allows the controller to WRITE data; the R/W# bit of the address will always be seen as 'zero'. Optimal address decoding of this bit is left to the vendor.

2) Options: It is our understanding that metal mask options and other pinouts of this type of clock driver will be allowed to use the same address as the original CKBF device. I²C addresses are defined in terms of function (master clock driver) rather than form (pinout, and option).

3) Slave/Receiver: The clock driver is assumed to require only slave/receiver functionality. Slave/transmitter functionality is optional.

4) Data Transfer Rate: 100 kbits/s (standard mode) is the base functionality required. Fast mode (400 kbits/s) functionality is optional.

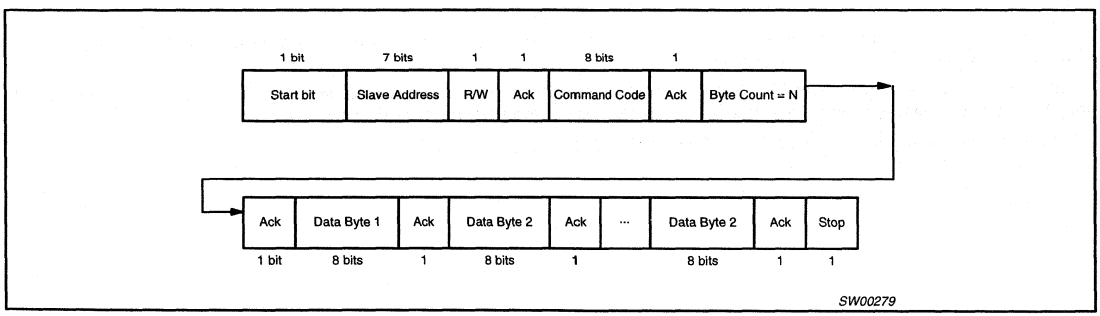
5) Logic Levels: I²C logic levels are based on a percentage of V_{DD} for the controller and other devices on the bus. Assume all devices are based on a 3.3 Volt supply.

6) Data Byte Format: Byte format is 8 Bits as described in the following appendices.

7) Data Protocol: To simplify the clock I²C interface, the clock driver serial protocol was specified to use only block writes from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. Indexed bytes are not allowed. However, the SMBus controller has a more specific format than the generic I²C protocol.

The clock driver must meet this protocol which is more rigorous than previously stated I²C protocol. Treat the description from the viewpoint of controller. The controller "writes" to the clock driver and if possible would "read" from the clock driver (the clock driver is a slave/receiver only and is incapable of this transaction.)

"The block write begins with a slave address and a write condition. After the command code the host (controller) issues a byte count which describes how many more bytes will follow in the message. If the host had 20 bytes to send, the first byte would be the number 20 (14h), followed by the 20 bytes of data. The byte count may not be 0. A block write command is allowed to transfer a maximum of 32 data bytes."



NOTE: The acknowledgement bit is returned by the slave/receiver (the clock driver).

Consider the command code and the byte count bytes required as the first two bytes of any transfer. The command code is software programmable via the controller, but will be specified as 0000 0000 in the clock specification. The byte count byte is the number of additional bytes required to transfer, not counting the command code and byte count bytes. Additionally, the byte count byte is required to be a minimum of 1 byte and a maximum of 32 bytes to satisfy the above requirement.

For example:

Byte count byte		Notes:
MSB	LSB	
0000	0000	Not allowed. Must have at least one byte.
0000	0001	Data for functional and frequency select register (currently byte 0 in spec)
0000	0010	Reads first two bytes of data. (byte 0 then byte 1)
0000	0011	Reads first three bytes (byte 0, 1, 2 in order)
0000	0100	Reads first four bytes (byte 0, 1, 2, 3 in order)
0000	0101	Reads first five bytes (byte 0, 1, 2, 3, 4 in order)
0000	0110	Reads first six bytes (byte 0, 1, 2, 3, 4, 5 in order)
0000	0111	Reads first seven bytes (byte 0, 1, 2, 3, 4, 5, 6 in order)
0010	0000	Max byte count supported = 32

A transfer is considered valid after the acknowledge bit corresponding to the byte count is read by the controller. The serial controller interface can be simplified by discarding the information in both the command code and the byte count bytes and simply reading all the bytes that are sent to the clock driver after being addressed by the controller. It is expected that the controller will not provide more bytes than the clock driver can handle. A clock vendor may choose to discard any number of bytes that exceed the defined byte count.

8) Clock stretching: The clock device must not hold/stretch the SCLOCK or SDATA lines low for more than 10 mS. Clock stretching is discouraged and should only be used as a last resort. Stretching the clock/data lines for longer than this time puts the device in an error/time-out mode and may not be supported in all platforms. It is assumed that all data transfers can be completed as specified without the use of clock/data stretching.

9) General Call: It is assumed that the clock driver will not have to respond to the "general call."

10) Electrical Characteristics: All electrical characteristics must meet the standard mode specifications found in section 15 of the I²C specification.

a) Pull-Up Resistors: Any internal resistors pull-ups on the SDATA and SCLOCK inputs must be stated in the individual datasheet. The use of internal pull-ups on these pins of below 100K is discouraged. Assume that the board designer will use a single external pull-up resistor for each line and that these values are in the 5 - 6K Ohm range. Assume one I²C device per DIMM (serial presence detect), one I²C controller, one clock driver plus one/two more I²C devices on the platform for capacitive loading purposes.

(b) Input Glitch Filters: Only fast mode I²C devices require input glitch filters to suppress bus noise. The clock driver is specified as a standard mode device and is not required to support this feature.

11) PWR DWN#: If a clock driver is placed in PWR DWN# mode, the SDATA and SCLK inputs must be Tri-Stated and the device must retain all programming information. I_{dd} current due to the I²C circuitry must be characterized and in the data sheet.

For specific I²C information consult the Philips I²C Peripherals Data Handbook IC12 (1997)

SERIAL CONFIGURATION MAP

The serial bits will be read by the clock buffer in the following order:

Byte 0 – Bits 7, 6, 5, 4, 3, 2, 1, 0
Byte 1 – Bits 7, 6, 5, 4, 3, 2, 1, 0
Byte 2 – Bits 7, 6, 5, 4, 3, 2, 1, 0

All unused register bits (Reserved and N/A) should be desined as "Dont Care". It is expected that the controller will force all of these bits to a "0" level.

All register bits labeled "Initialize to 0" must be written to zero during intialization. Failure to do so may result in a higher than normal operating current. The controller will read back the last written value.

Byte 0: Output active/inactive register

1 = enable; 0 = disable

BIT	PIN#	NAME	DESCRIPTION
7	—	BUF_OUT7	Initialize to 0
6	—	BUF_OUT6	Initialize to 0
5	—	BUF_OUT5	Initialize to 0
4	—	BUF_OUT4	Initialize to 0
3	7	BUF_OUT3	Active/Inactive
2	6	BUF_OUT2	Active/Inactive
1	3	BUF_OUT1	Active/Inactive
0	2	BUF_OUT0	Active/Inactive

NOTE:
1. Inactive means outputs are held LOW and are disabled from switching. These outputs are designed to be configured at power-on and are not expected to be configured during the normal modes of operation.

Byte 1: Output active/inactive register

1 = enable; 0 = disable

BIT	PIN#	NAME	DESCRIPTION
7	27	BUF_OUT15	Active/Inactive
6	26	BUF_OUT14	Active/Inactive
5	23	BUF_OUT13	Active/Inactive
4	22	BUF_OUT12	Active/Inactive
3	—	BUF_OUT11	Initialize to 0
2	—	BUF_OUT10	Initialize to 0
1	—	BUF_OUT9	Initialize to 0
0	—	BUF_OUT8	Initialize to 0

NOTE:
1. Inactive means outputs are held LOW and are disabled from switching. These outputs are designed to be configured at power-on and are not expected to be configured during the normal modes of operation.

Byte 2: Optional register for possible future requirments

BIT	PIN#	NAME	DESCRIPTION
7	18	BUF_OUT17	Active/Inactive
6	11	BUF_OUT16	Active/Inactive
5	—	(reserved)	(reserved)
4	—	(reserved)	(reserved)
3	—	(reserved)	(reserved)
2	—	(reserved)	(reserved)
1	—	(reserved)	(reserved)
0	—	(reserved)	(reserved)

NOTE:
1. Inactive means outputs are held LOW and are disabled from switching. These outputs are designed to be configured at power-on and are not expected to be configured during the normal modes of operation.

AC WAVEFORMS

V_M = 1.5V
$V_X = V_{OL}$ + 0.3V
$V_Y = V_{OH}$ –0.3V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

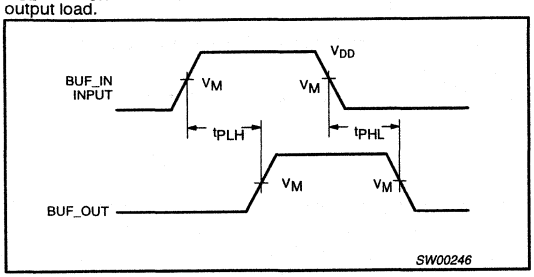


Figure 1. Load circuitry for switching times.

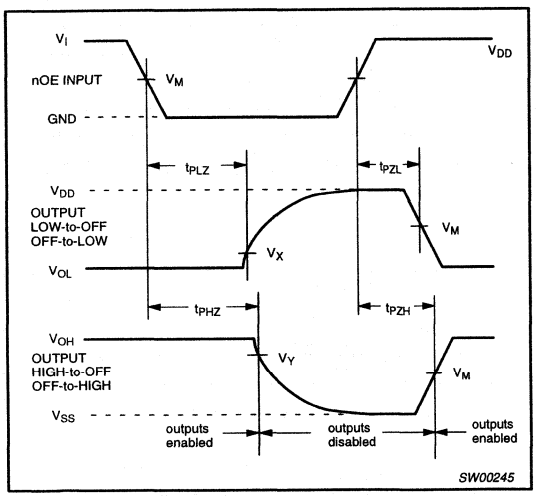


Figure 2. 3-State enable and disable times

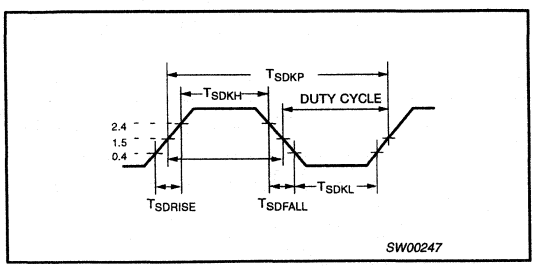


Figure 3. SDRAM Output clock

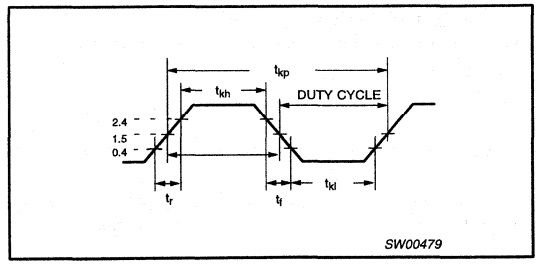
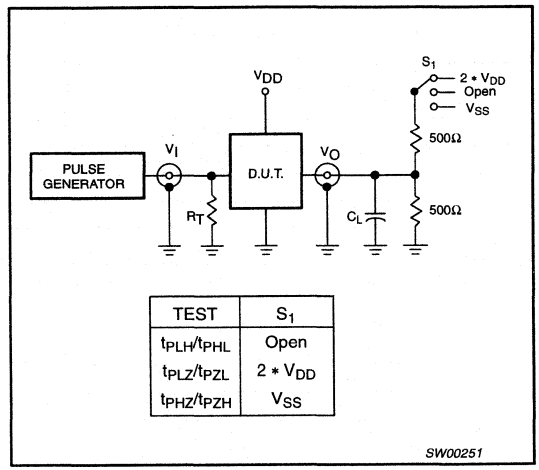


Figure 4. Buffer Output clock

TEST CIRCUIT



TEST	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 * V_{DD}
t_{PHZ}/t_{PZH}	V_{SS}

Figure 5. Load circuitry for switching times

4-digit LED-driver with I²C-Bus interface SAA1064

GENERAL DESCRIPTION

The LED-driver is a bipolar integrated circuit made in an I²L compatible 18 volts process. The circuit is especially designed to drive four 7-segment LED displays with decimal point by means of multiplexing between two pairs of digits. It features an I²C-Bus slave transceiver interface with the possibility to program four different SLAVE ADDRESSES, a POWER RESET flag, 16 current sink OUTPUTS, controllable by software up to 21 mA, two multiplex drive outputs for common anode segments, an on-chip multiplex oscillator, control bits to select static, dynamic and blank mode, and one bit for segment test.

QUICK REFERENCE DATA

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{EE} = 0 V	V_{CC}	4.5	5	15	V
Supply current all outputs OFF	V_{CC} = 5 V	I_{CC}(1)	7	9.5	14	mA
Total power dissipation						
24-lead DIL (SOT101B)		P_{tot}	–	–	1000	mW
24-lead DIL SO (SOT137A)		P_{tot}	–	–	500	mW
Operating ambient						
temperature range		T_{amb}	–40	–	+85	°C

Note

1. The positive current is defined as the conventional current flow into a device (sink current).

PACKAGE OUTLINE

SAA1064: 24-lead DIL; plastic with internal heat spreader (SOT101B); SOT101-1; 1996 August 30.

SAA1064T: 24-lead mini-pack; plastic (SO-24; SOT137A); SOT137-1; 1996 August 30.

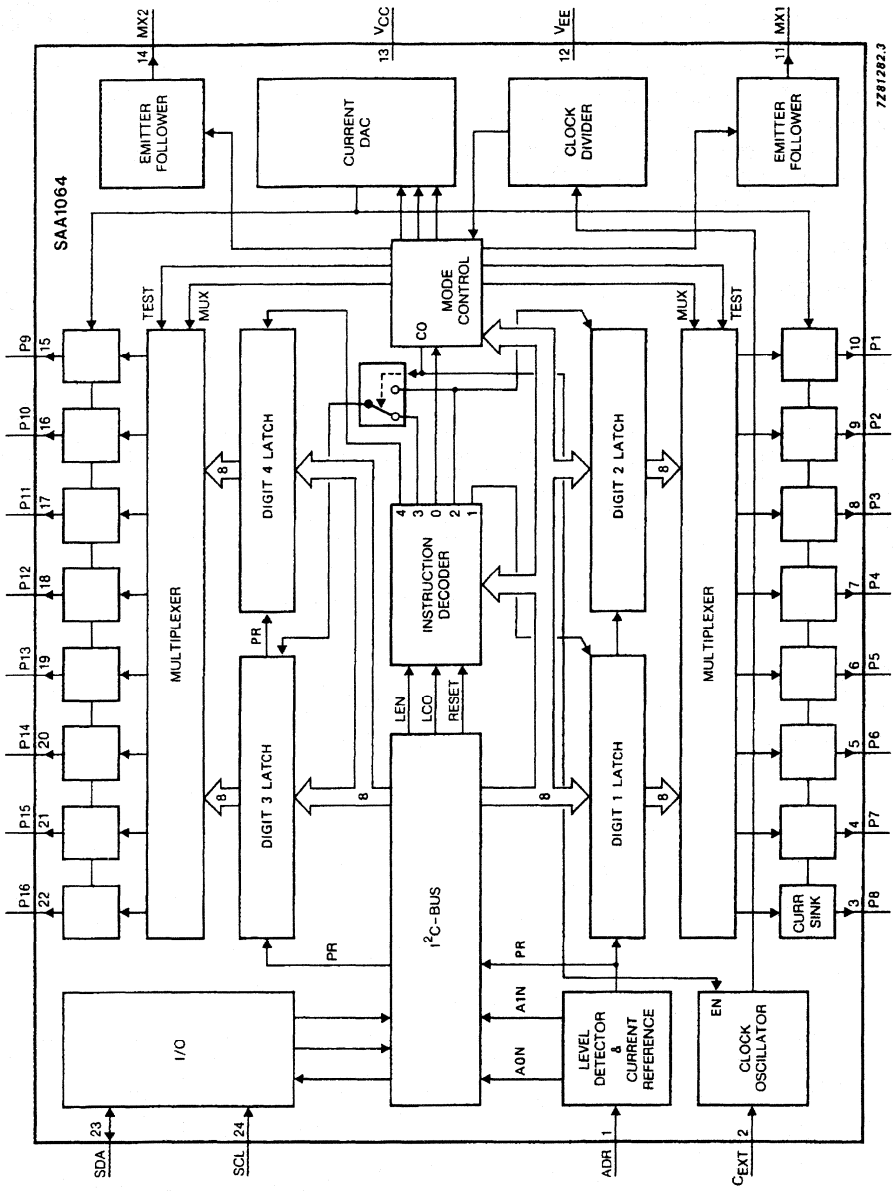


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
ADR	1	I²C-Bus slave address input
C_{EXT}	2	external control
P8 to P1	3-10	segment output
MX1	11	multiplex output
V_{EE}	12	ground
V_{CC}	13	positive supply
MX2	14	multiplex output
P9 to P16	15-22	segment output
SDA	23	I²C-Bus serial data line
SCL	24	I²C-Bus serial clock line

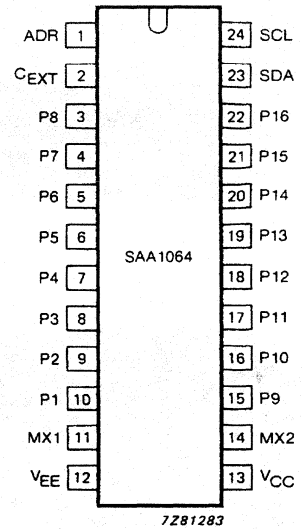
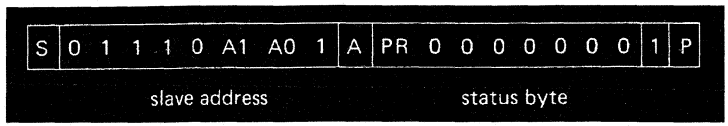
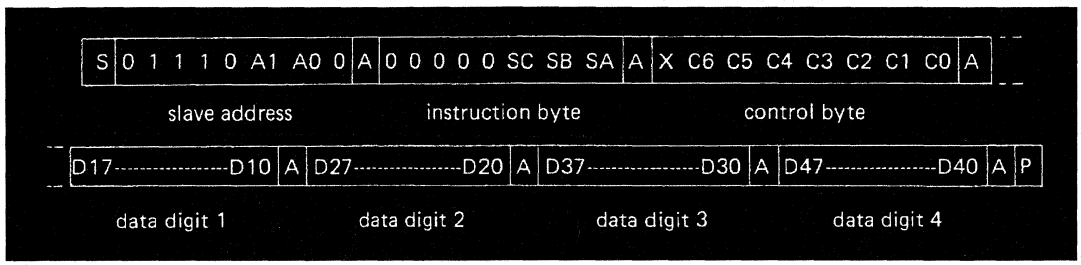


Fig.2 Pinning diagram.

FUNCTIONAL DESCRIPTION



a. READ mode.



b. WRITE mode.

S = start condition
P = stop condition
A = acknowledge
X = don't care

A1, A0 = programmable address bits
SC SB SA = subaddress bits
C6 to C0 = control bits
PR = POWER RESET flag

Fig.3 I²C-Bus format.

Address pin ADR

Four different slave addresses can be chosen by connecting ADR either to V_{EE}, 3/8 V_{CC}, 5/8 V_{CC} or V_{CC}. This results in the corresponding valid addresses HEX 70, 72, 74 and 76 for writing and 71, 73, 75 and 77 for reading. All other addresses cannot be acknowledged by the circuit.

Status byte

Only one bit is present in the status byte, the POWER RESET flag. A logic 1 indicates the occurence of a power failure since the last time it was read out. After completion of the READ action this flag will be set to logic 0.

Subaddressing

The bits SC, SB and SA form a pointer and determine to which register the data byte following the instruction byte will be written. All other bytes will then be stored in the registers with consecutive subaddresses. This feature is called Auto-Increment (AI) of the subaddress and enables a quick initialization by the master.
The subaddress pointer will wrap around from 7 to 0.
The subaddresses are given as follows:

SC	SB	SA	SUB-ADDRESS	FUNCTION
0	0	0	00	control register
0	0	1	01	digit 1
0	1	0	02	digit 2
0	1	1	03	digit 3
1	0	0	04	digit 4
1	0	1	05	reserved, not used
1	1	0	06	reserved, not used
1	1	1	07	reserved, not used

Control bits (see Fig.4)
The control bits C0 to C6 have the following meaning:

C0 = 0	static mode, i.e. continuous display of digits 1 and 2
C0 = 1	dynamic mode, i.e. alternating display of digit 1 + 3 and 2 + 4
C1 = 0/1	digits 1 + 3 are blanked/not blanked
C2 = 0/1	digits 2 + 4 are blanked/not blanked
C3 = 1	all segment outputs are switched-on for segment test[1]
C4 = 1	adds 3 mA to segment output current
C5 = 1	adds 6 mA to segment output current
C6 = 1	adds 12 mA to segment output current

Note

1. At a current determined by C4, C5 and C6.

Data

A segment is switched ON if the corresponding data bit is logic 1. Data bits D17 to D10 correspond with digit 1, D27 to D20 with digit 2, D37 to D30 with digit 3 and D47 to D40 with digit 4.

The MSBs correspond with the outputs P8 and P16, the LSBs with P1 and P9. Digit numbers 1 to 4 are equal to their subaddresses (hex) 1 to 4.

SDA, SCL

The SDA and SCL I/O meet the I²C-Bus specification. For protection against positive voltage pulses on these inputs voltage regulator diodes are connected to V_{EE}. This means that normal line voltage should not exceed 5,5 volt. Data will be latched on the positive-going edge of the acknowledge related clock pulse.

Power-on reset

The power-on reset signal is generated internally and sets all bits to zero, resulting in a completely blanked display. Only the POWER RESET flag is set.

External Control (C_{EXT})

With a capacitor connected to pin 2 the multiplex frequency can be set (see Fig.5). When static this pin can be connected to V_{EE} or V_{CC} or left floating since the oscillator will be switched off.

Segment outputs

The segment outputs P1 to P16 are controllable current-sink sources. They are switched on by the corresponding data bits and their current is adjusted by control bits C4, C5 and C6.

Multiplex outputs

The multiplex outputs MX1 and MX2 are switched alternately in dynamic mode with a frequency derived from the clock-oscillator. In static mode MX1 is switched on. The outputs consist of an emitter-follower, which can be used to drive the common anodes of two displays directly provided that the total power dissipation of the circuit is not exceeded. If this occurs external transistors should be connected to pins 11 and 14 as shown in Fig.5.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

PARAMETER	CONDITIONS	SYMBOL	MIN.	MAX.	UNIT
Supply voltage (pin 13)	V_{EE} = 0 V	V_{CC}	−0.5	18	V
Supply current (pin 13)		I_{CC}	−50	200	mA
Total power dissipation					
24-lead DIL (SOT101B)		P_{tot}		1000	mW
24-lead SO (SO137A)		P_{tot}		500	mW
SDA, SCL voltages	V_{EE} = 0 V	$V_{23, 24}$	−0.5	5.9	V
Voltages ADR-MX1 and MX2-P16	V_{EE} = 0 V	V_{1-11}, V_{14-22}	−0.5	V_{CC} + 0.5	V
Input/output current all pins	outputs OFF	$\pm I_{I/O}$	–	10	mA
Operating ambient					
temperature range		T_{amb}	−40	+85	°C
Storage temperature range		T_{stg}	−55	+150	°C

THERMAL RESISTANCE

From crystal to ambient		
24-lead DIL	$R_{th\ j\text{-}a}$	35 K/W
24-lead SO (on ceramic substrate)	$R_{th\ j\text{-}a}$	75 K/W
24-lead SO (on printed circuit board)	$R_{th\ j\text{-}a}$	105 K/W

CHARACTERISTICS

V_{CC} = 5 V; T_{amb} = 25 °C; voltages are referenced to ground (V_{EE} = 0 V); unless otherwise specified

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply						
Supply voltage (pin 13)		V_{CC}	4,5	5,0	15	V
Supply current	all outputs OFF					
	V_{CC} = 5 V	I_{CC}	7,0	9,5	14,0	mA
Power dissipation	all outputs OFF	P_d	–	50	–	mW
SDA; SCL (pins 23 and 24)						
Input voltages		$V_{23,24}$	0	–	5,5	V
Logic input voltage LOW		$V_{IL(L)}$	–	–	1,5	V
Logic input voltage HIGH		$V_{IH(L)}$	3,0	–	–	V
Input current LOW	$V_{23,24} = V_{EE}$	$-I_{IL}$	–	–	10	µA
Input current HIGH	$V_{23,24} = V_{CC}$	I_{IH}	–	–	10	µA
SDA						
Logic output voltage LOW	I_O = 3 mA	$V_{OL(L)}$	–	–	0,4	V
Output sink current		I_{SDA}	3	–	–	mA
Address input (pin 1)						
Input voltage						
programmable address bits:						
A0 = 0; A1 = 0		V_1	V_{EE}	–	$3/16V_{CC}$	V
A0 = 1; A1 = 0		V_1	$5/16V_{CC}$	$3/8V_{CC}$	$7/16V_{CC}$	V
A0 = 0; A1 = 1		V_1	$9/16V_{CC}$	$5/8V_{CC}$	$11/16V_{CC}$	V
A0 = 1; A1 = 1		V_1	$13/16V_{CC}$	–	V_{CC}	V
Input current LOW	$V_1 = V_{EE}$	$-I_1$	–	–	10	µA
Input current HIGH	$V_1 = V_{CC}$	I_1	–	–	10	µA
External control (C_{EXT}) pin 2						
Switching level input						
Input voltage LOW		V_{IL}	–	–	V_{CC}–3,3	V
Input voltage HIGH		V_{IH}	V_{CC}–1,5	–	–	V
Input current	V_2 = 2 V	I_2	–140	–160	–180	µA
	V_2 = 4 V	I_2	140	160	180	µA

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Segment outputs						
(P8 to P1; pins 3 to 10)						
P9 to P16; pins 15 to 22)						
Output voltages	I_O = 15 mA	V_O	–	–	0.5	V
Output leakage current HIGH	$V_O = V_{CC}$ = 15 V	I_{LO}	–	–	± 10	μA
Output current LOW						
All control bits (C4, C5						
and C6) are HIGH	V_{OL} = 5 V	I_{OL}	17.85	21	25.2	mA
Contribution of:						
control bit C4		I_O	2.55	3.0	3.6	mA
control bit C5		I_O	5.1	6.0	7.2	mA
control bit C6		I_O	10.2	12.0	14.4	mA
Relative segment output current accuracy						
with respect to highest value		ΔI_O	–	–	7.5	%
Multiplex 1 and 2 (pins 11 and 14)						
Maximum output voltage						
(when ON)	$-I_{MPX}$ = 50 mA	V_{MPX}	V_{CC}–1.5	–	–	V
Maximum output current HIGH						
(when ON)	V_{MPX} = 2 V	$-I_{MPX}$	50	–	110	mA
Maximum output current LOW						
(when OFF)	V_O = 2 V	$+I_{MPX}$	50	70	110	μA
Multiplex output period	C_{EXT} = 2.7 nF	T_{MPX}	5	–	10	ms
Multiplexed duty factor			–	48.4	–	%

* Value to be fixed.

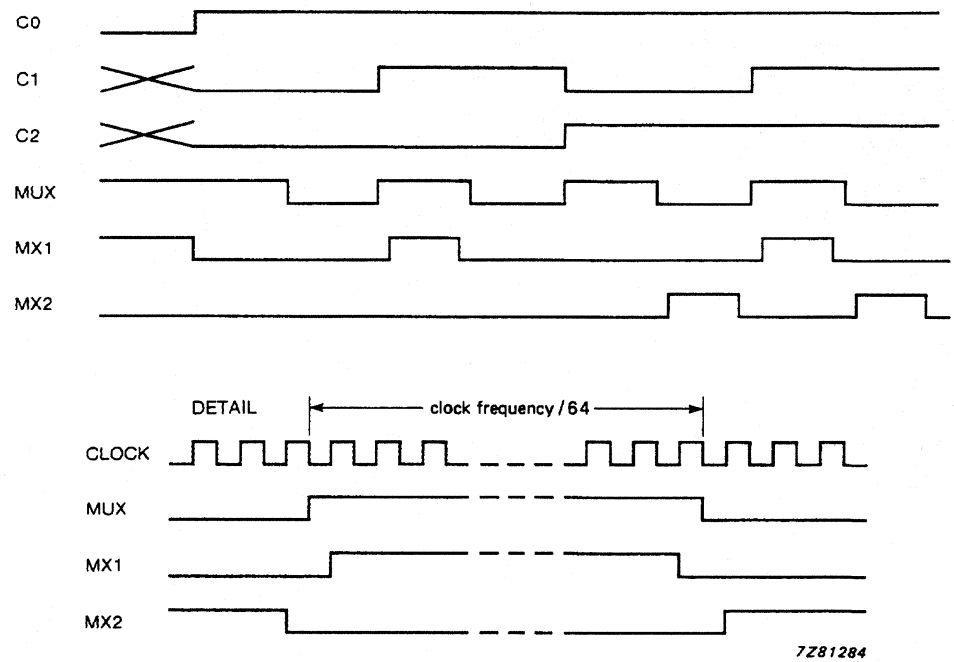


Fig.4 Timing diagram.

APPLICATION INFORMATION

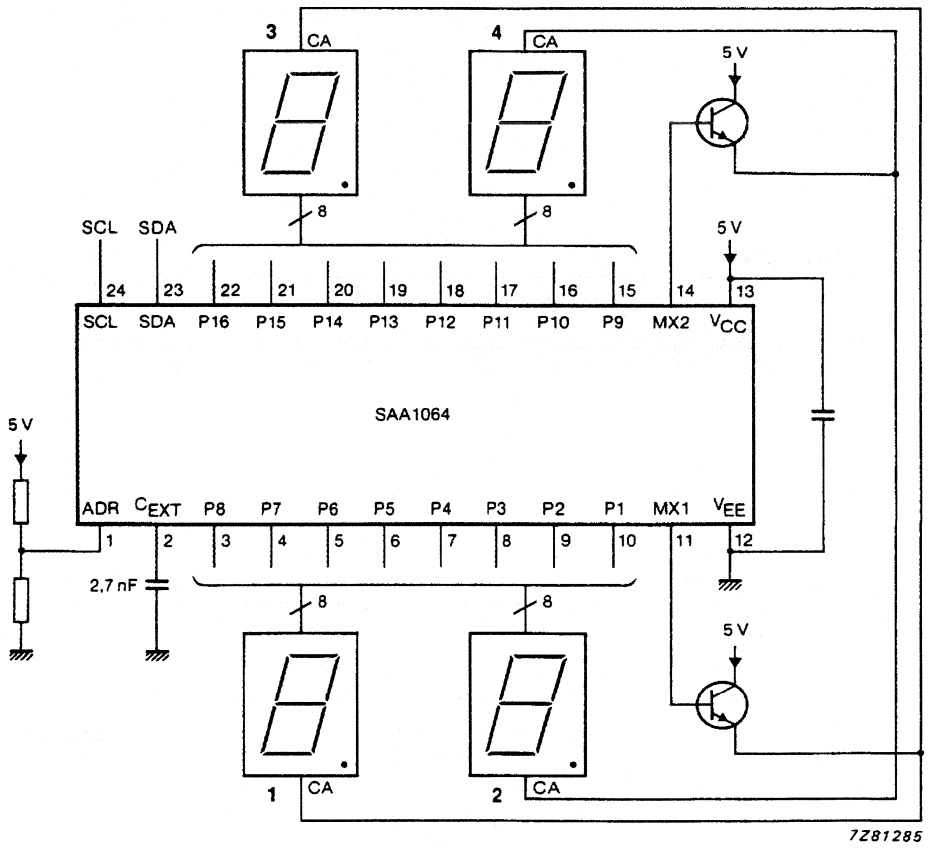


Fig.5 Dynamic mode application diagram.

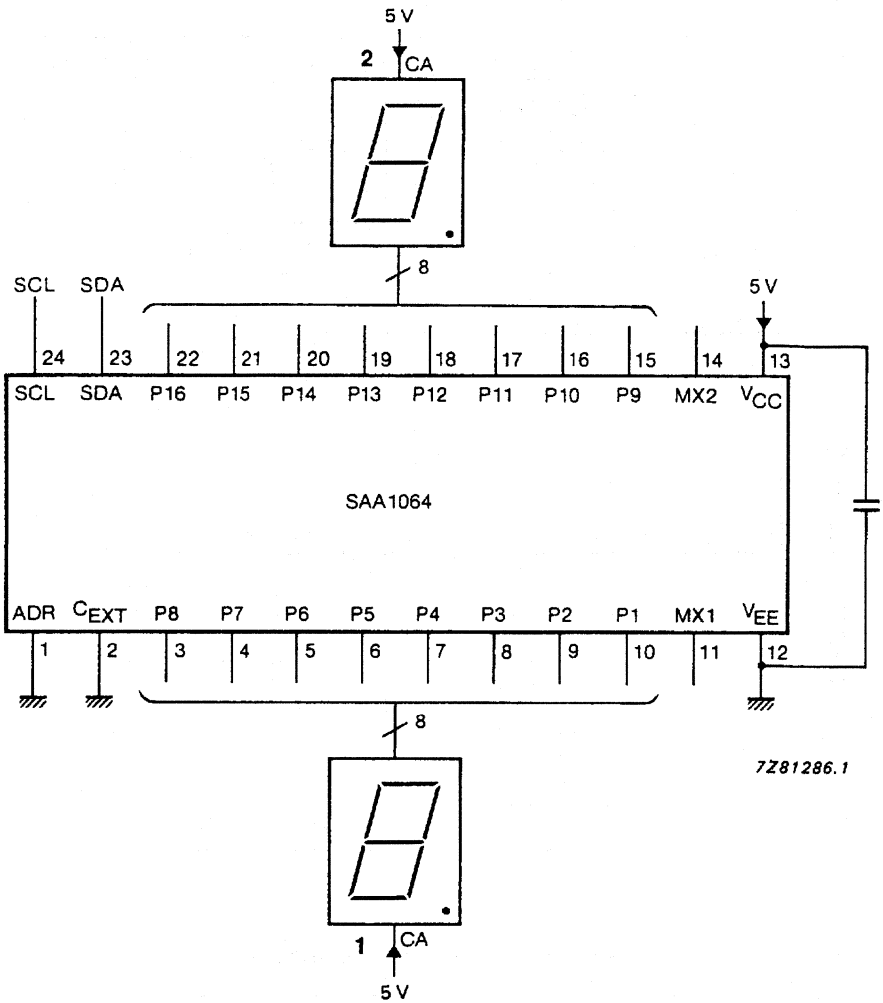


Fig.6 Static mode application diagram.

POWER DISSIPATION

The total maximum power dissipation of the SAA1064 is made up by the following parts:

1. Maximum dissipation when none of the outputs are programmed (continuous line in Fig.7).
2. Maximum dissipation of each programmed output. The dashed line in Fig.7 visualises the dissipation when **all** the segments are programmed (max. 16 in the static, and max. 32 in the dynamic mode). When less segments are programmed one should take a proportional part of the maximum value.
3. Maximum dissipation of the programmed segment drivers which can be expressed as: $P_{add} = V_O \times I_O \times N$.

Where:

P_{add} = The additional power dissipation of the segment drivers

V_O = The low state segment driver output voltage

I_O = The programmed segment output current

N = The number of programmed segments in the static mode, or half the number of programmed segment drivers in the dynamic mode.

Under no conditions the total maximum dissipation (500 mW for the SO and 1000 mW for the DIL package) should be exceeded.

Example: V_{CC} = 5 V

V_O = 0.25 V

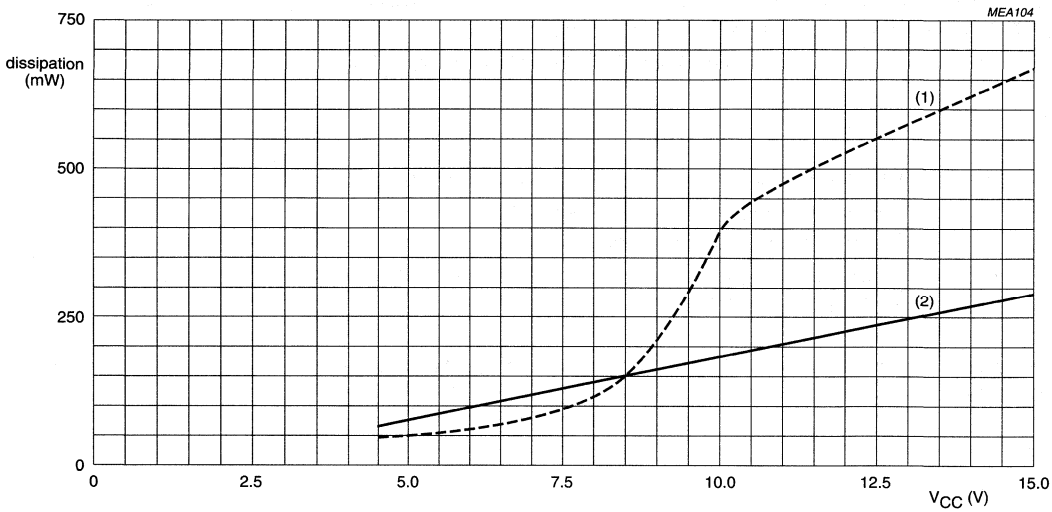
I_O = 12 mA

24 programmed segments in dynamic mode

$P_{tot} = P_1 + P_2 + P_3$

$= 75\ mW + (50 * 24/32)\ mW + (0.25 * 12.10^{-3} * 12)\ mW$

$= 148.5\ mW$



(1) All outputs programmed (no segment current sink).
(2) Outputs not programmed.

Fig.7 SAA1064 power dissipation as a function of supply voltage.

Tuner switching circuit SAA1300

The SAA1300 is for switching on and off the supply lines of various circuit parts via an I²C bus signal. Furthermore, it can be used to supply current for switching diodes in radio and television tuners. It contains 5 output stages, which are capable of supplying up to 85 mA in the ON state or sinking up to −100 μA in the OFF state.

Current limiting and short-circuit protection are included. The output stages are driven by a shift register/latch combination which is loaded via data from the I²C bus. A power-on reset of the latches ensures the OFF state of the output stages (OUT 2 to OUT 5) without data reception from the I²C bus. A subaddressing system allows the connection of up to three circuits on the same I²C bus lines; one of the outputs (OUT 1, pin 7) can also be used

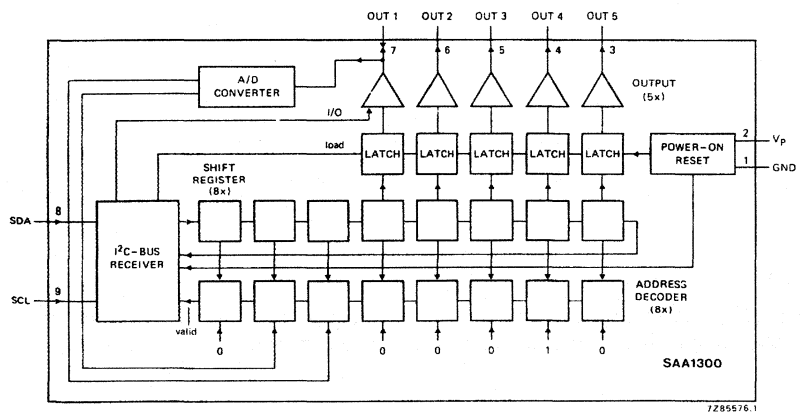


Fig.1 Block diagram.

PACKAGE OUTLINE

9-lead SIL; plastic (SOT142); SOT142-1; 1996 September 05.

PINNING

PIN NO.	SYMBOL	FUNCTION	
1	GND	ground	
2	V_P	positive supply	
3	OUT 5	outputs	
4	OUT 4		
5	OUT 3		
6	OUT 2		
7	OUT 1	output and subaddressing input	
8	SDA	serial data line	I²C bus
9	SCL	serial clock line	

I²C BUS INFORMATION

Address, first byte

0 1 0 0 0 A B 0 where,

A	B	FUNCTION	CONDITION
0	0	general address	OUT 1 = output
0	1	OUT 1 = input	address accepted if $V_{OUT\,1} = V_{OUT\,L}$ (LOW)
1	0	OUT 1 = input	address accepted if $V_{OUT\,1} = V_{OUT\,H}$ (HIGH)
1	1	OUT 1 = input	address accepted if $V_{OUT\,1} = V_{OUT\,M}$ (MEDIUM)

Data, second byte

OUT 5, OUT 4, OUT 3, OUT 2, OUT 1, X, X, X

The I/O output stage (OUT 1) is switched as an input stage after a power-on reset. It depends on the contents of the first data transmission whether the output stage is switched as an output or remains as an input.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max. 13,2	V
Input voltage range at SDA, SCL	V_I	−0,5 to + 6,0	V
Input voltage range at OUT 1	V_I	−0,5 to + 12,5	V
Output voltage range at OUT 1 to OUT 5	V_O	−0,5 to + 12,5	V
Input current at SDA, SCL	I_I	max. 20	mA
Input current at OUT 1	I_I	max. 20	mA
Total power dissipation	P_{tot}	max. 825	mW
Storage temperature range	T_{stg}	−40 to + 125	°C
Operating ambient temperature ranges	T_{amb}	−20 to + 80	°C

CHARACTERISTICS

V_P = 8 V; T_{amb} = 24 °C; unless otherwise specified

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply (pin 2)					
Supply voltage range	V_P	4	8	12	V
Supply current					
5 outputs LOW	I_{PL}	5	10	15	mA
5 outputs HIGH	I_{PH}	30	50	70	mA
Power on reset level output stage in "OFF" condition	V_{PR}	–	3,5	3,8	V
Maximum power dissipation[1]	P_{max}	–	650	–	mW
Inputs SDA, SCL (pins 8 and 9)					
Input voltage HIGH	V_{IH}	3,0	–	5,5	V
Input voltage LOW	V_{IL}	0	–	1,5	V
Input current HIGH	$-I_{IH}$	–	–	10	µA
Input current LOW	I_{IH}	–	–	0,4	µA
Acknowledge sink current	I_{ACK}	2,5	–	–	mA
Maximum input frequency	$f_{i\,max}$	100	–	–	kHz
Outputs OUT 1 to OUT 5 (pins 3 to 7)					
Maximum output current; source: "ON"	I_{Oso}	+85	–	+150	mA
Maximum output current; source: "ON"					
T_{amb} = 80 °C	I_{Oso}	60	–	–	mA
Output voltage HIGH					
at I_{Oso} = 85 mA	V_{OH}	V_P–2	–	–	V
Output current; sink "OFF"	I_{Osi}	–100	–300	–	µA
Output voltage LOW					
at I_{Osi} = –100 µA	V_{OL}	–	–	100	mV
Output voltage MEDIUM					
at I_O = 10 mA	V_{OM}	V_P–0,5	–	–	V
OUT 1 used as subaddressing input					
Input voltage HIGH (code 1 0)	$V_{OUT\,1H}$	0,72 V_P	–	V_P	V
Input voltage MEDIUM (code 1 1)	$V_{OUT\,1M}$	0,39 V_P	–	0,61 V_P	V
Input voltage LOW (code 0 1)	$V_{OUT\,1L}$	0	–	0,28 V_P	V

Note

1. Outputs must not be driven simultaneously at maximum source current.

I²C-bus SIM card interface TDA8003TS

FEATURES

- Subscriber Identification Module (SIM) card interface in accordance with GSM11.11, GSM11.12 (Global System for Mobile communication) and ISO 7816 requirements
- V_{CC} regulation (3 or 5 V ±8%) with controlled rise and fall times
- Card take-off protection
- One protected and buffered pseudo-bidirectional I/O line (I/O referenced to V_{CC} and SIMI/O referenced to V_{DDI})
- Clock generation (up to 10 MHz) with synchronous start and frequency doubling
- Clock stop LOW, clock stop HIGH or 1.25 MHz (from internal oscillator) for cards Power-down mode
- Automatic activation and deactivation sequences of an independent sequencer
- Automatic processing of pin RST with count of the 45000 CLK cycles for begin of the Answer To Reset (ATR)
- Warm reset command
- Supply voltage supervisor for Power-on reset, spikes killing and emergency deactivation in case of supply drop-out
- DC-to-DC converter (doubler, tripler or follower) allowing operation in a 3 or 5 V environment ($2.5 \leq V_{DD} \leq 6$ V)
- Enhanced Electrostatic discharge (ESD) protections on card side (6 kV minimum)
- Power-down mode with several active features and current reduction
- Off mode with 2 µA current
- Control from a microcontroller via a 400 kHz slave I²C-bus (4 possible addresses: 48H, 4AH, 4CH and 4EH)
- Four parallel devices possible due to 2 sub-address wires
- Interface signals supplied by an independent voltage ($1.5 \leq V_{DDI} \leq 6$ V).

APPLICATIONS

- GSM mobile phones
- SAM interfaces in banking terminals
- Portable card readers, etc.

GENERAL DESCRIPTION

The TDA8003TS is a low cost one chip SIM interface, in accordance with GSM11.11, GSM11.12 and EMV96 (Europay, Mastercard, Visa) with card current limitation. Controlled by I²C-bus, it is optimized in terms of board space, external components count and connection count (see Chapter "Application information").

Due to its integrated DC-to-DC converter, it ensures fully cross-compatibility between 3 or 5 V cards and 3 or 5 V environments. The very low-power consumption in Power-down mode and Off mode saves battery power.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8003TS/C1	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage on pins V_{DDS} and V_{DDP}		2.5	–	6	V
I_{DD}	supply current on pins V_{DDS} and V_{DDP}	Off mode; V_{DD} = 3.3 V	–	–	2	µA
		Power-down mode; V_{DD} = 3.3 V; V_{CC} = 5 V; I_{CC} = 100 µA; SIMCLK connected to PGND or V_{DDI}; CLK is stopped	–	–	500	µA
		active mode; V_{DD} = 3.3 V; V_{CC} = 3 V; I_{CC} = 6 mA; f_{CLK} = 3.25 MHz	–	–	18	mA
		active mode; V_{DD} = 3.3 V; V_{CC} = 5 V; I_{CC} = 10 mA; f_{CLK} = 3.25 MHz	–	–	50	mA
		active mode; V_{DD} = 5 V; V_{CC} = 3 V; I_{CC} = 6 mA; f_{CLK} = 3.25 MHz	–	–	10	mA
		active mode; V_{DD} = 5 V; V_{CC} = 5 V; I_{CC} = 10 mA; f_{CLK} = 3.25 MHz	–	–	30	mA
V_{DDI}	interface signal supply voltage		1.5	–	6	V
V_{CC}	card supply voltage	5 V card; active mode; 0 < I_{CC} < 15 mA; 40 nAs dynamic load on 200 nF capacitor	4.6	5	5.4	V
		3 V card; active mode; 0 < I_{CC} < 10 mA; 24 nAs dynamic load on 200 nF capacitor	2.75	3	3.25	V
		5 V card; bit PDOWN = 1; I_{CC} < 5 mA	4.6	–	5.4	V
		3 V card; bit PDOWN = 1; I_{CC} < 5 mA	2.75	–	3.25	V
SR	slew rate on V_{CC} (rise and fall)	$C_{L(max)}$ = 200 nF	0.05	–	0.25	V/µs
t_{de}	deactivation time		–	–	120	µs
t_{act}	activation time		–	–	150	µs
$f_{i(SIMCLK)}$	clock input frequency		0	–	20	MHz
T_{amb}	operating ambient temperature		–40	–	+85	°C

BLOCK DIAGRAM

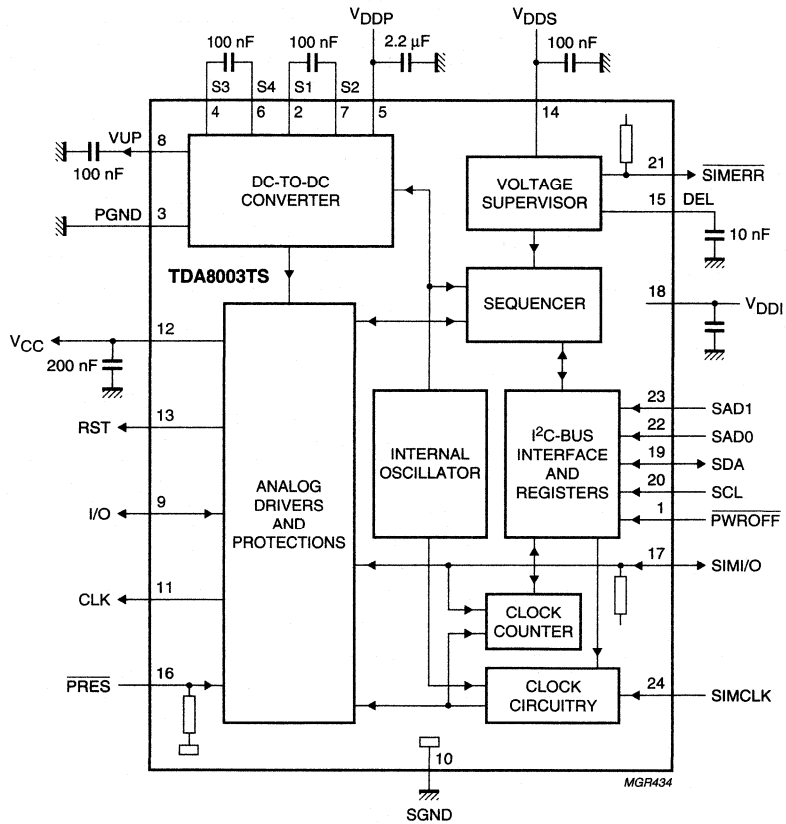


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
$\overline{PWROFF}$	1	control input for entering the Off mode (active LOW)
S1	2	capacitor connection for the DC-to-DC converter (between S1 and S2)
PGND	3	power ground
S3	4	capacitor connection for the DC-to-DC converter (between S3 and S4)
V_{DDP}	5	power supply voltage
S4	6	capacitor connection for the DC-to-DC converter (between S3 and S4)
S2	7	capacitor connection for the DC-to-DC converter (between S1 and S2)
VUP	8	DC-to-DC converter output (must be decoupled with 100 nF to ground)
I/O	9	input/output to and from the card reader (C7I); see Fig.7
SGND	10	signal ground
CLK	11	clock output to the card reader (C3I)
V_{CC}	12	supply voltage to the card reader (C1I)
RST	13	reset output to the card reader (C2I)
V_{DDS}	14	signal supply voltage
DEL	15	external capacitor connection for the delay on voltage supervisor
$\overline{PRES}$	16	card presence indication input (active LOW); note 1
SIMI/O	17	input/output to and from the microcontroller (internal 20 kΩ pull-up resistor connected to V_{DDI})
V_{DDI}	18	supply voltage for the interface signals with the system
SDA	19	I²C-bus serial data input/output
SCL	20	I²C-bus serial clock input
$\overline{SIMERR}$	21	interrupt output (active LOW; internal 100 kΩ pull-up resistor connected to V_{DDI})
SAD0	22	I²C-bus slave address selection input
SAD1	23	I²C-bus slave address selection input
SIMCLK	24	external clock input

Note

1. Card presence input with negative current source. To be used with the card reader switch connected to V_{DDS} or V_{DDP}. The switch is normally closed when the card is not present. If the switch connection is open-circuit or pin 16 is not connected, then the interface will always detect a present card (see Fig.7).

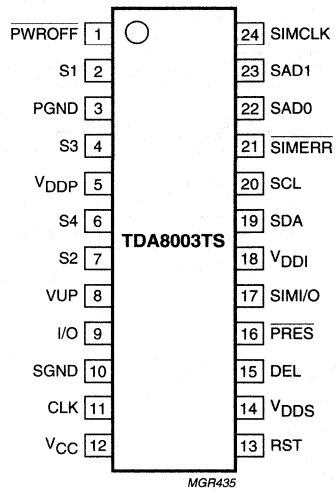


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Figure 1 shows the block diagram of the TDA8003TS. The functional blocks will be described in the following sections. It is assumed that the reader of this specification is aware of GSM11.11 and ISO 7816 terminology.

I²C-bus control

The I²C-bus interface is used:

- To configure the clock to the card in active mode ($\frac{1}{2}f_{SIMCLK}$ and $\frac{1}{4}f_{SIMCLK}$)
- To configure the clock to the card in power reduction mode (stop LOW, stop HIGH or ±1.25 MHz derived from the internal oscillator)
- For selecting operation with a 3 or 5 V card
- For starting or stopping sessions (cold reset)
- For initiating a warm reset
- For entering or leaving the Power-down mode
- For asking the status (card present or not, hardware problem occurred, unresponsive card after activation, supply drop-out detected by the voltage supervisor, card powered or not)
- To configure SIMI/O and I/O in high-impedance (for use of several TDA8003TS in parallel).

The structure of the I²C-bus data frames is as follows:

- Commands to the TDA8003TS:
  - START/ADDRESS/WRITE
  - COMMAND BYTE
  - STOP.

  The fixed address is 01001XY. X and Y are defined by the logic levels on pins SAD1 and SAD0 as shown in Table 1 (connect to ground for logic 0; connect to V_{DDI} for logic 1). The command bits are described in Table 2. The commands are executed on the rising edge of the 9th SCL pulse.
- Status from the TDA8003TS (see Table 4). The fixed address is 01001XY. X and Y are defined by the logic levels on pins SAD1 and SAD0 as shown in Table 1.

Table 1 Address selections

ADDRESS	SAD1	SAD0
48H	0	0
4AH	0	1
4CH	1	0
4EH	1	1

Table 2 Description of the command bits; note 1

SYMBOL	BIT	DESCRIPTION
START/STOP	0	Logic 1 initiates an activation sequence and a cold reset procedure. Logic 0 initiates a deactivation sequence.
WARM	1	Logic 1 initiates a warm reset procedure. It will be automatically reset by hardware when the card starts answering, or when the 2 times 45000 CLK pulses have expired without answer from the card.
3 V/5 VN	2	Logic 1 sets the card supply voltage V_{CC} to 3 V. Logic 0 sets V_{CC} to 5 V.
PDOWN	3	Logic 1 applies on CLK the frequency defined by bits CLKPD1 and CLKPD2, and enters a reduced consumption mode. Logic 0 sets the circuit back to normal mode.
CLKPD1	4	Bits 4 and 5 determine the clock to the card at power-down as shown in Table 3.
CLKPD2	5	
DT/DFN	6	Logic 1 sets f_{CLK} to $\frac{1}{2}f_{SIMCLK}$ (in active mode). Logic 0 sets f_{CLK} to $\frac{1}{4}f_{SIMCLK}$.
I/OEN	7	Logic 1 will transfer I/O to SIMI/O. Logic 0 sets I/O and SIMI/O to high-impedance.

Note

1. All bits are cleared at reset.

Table 3 Clock to the card at power-down

BIT 4	BIT 5	FUNCTION
0	0	clock stop LOW
0	1	clock stop HIGH
1	0	clock is $\frac{1}{2}f_{osc}$
1	1	no change

Table 4 Description of the status bits; note 1

SYMBOL	BIT	DESCRIPTION
PRES	0	Logic 1 when the card is present. Logic 0 when the card is not present.
PRESL	1	Logic 1 when the card has been extracted or inserted. Logic 0 when the status is read-out.
–	2	Bit 2 is not used and is fixed to logic 0.
SUPL	3	Logic 1 when the voltage supervisor has signalled a fault. Logic 0 when the status is read-out.
PROT	4	Logic 1 when an overload has occurred during a session. Logic 0 when the status is read-out.
MUTE	5	Logic 1 when a card has not answered after 2 times 45000 CLK cycles. Logic 0 when the status is read-out.
EARLY	6	Logic 1 when a card has answered between 200 and 352 CLK cycles. Logic 0 when the status is read-out.
ACTIVE	7	Logic 1 when the card is power-on. Logic 0 when the card is power-off.

Note

1. In case of card extraction, supply drop-out or overload detection within a session, the card will be automatically deactivated, $\overline{\text{SIMERR}}$ pulled LOW, bit START = 0 and the corresponding status bit = 1. The status bit will be logic 0 and $\overline{\text{SIMERR}}$ will be released when the microcontroller reads out the status register, on the 7th SCL pulse. After a supply drop-out, $\overline{\text{SIMERR}}$ will be released at the end of the alarm pulse and bit SUPL = 1.

Power supply

The circuit operates within a supply voltage range of 2.5 to 6 V. The supply pins are V_{DDS} and SGND. Pins V_{DDP} and PGND only supply the DC-to-DC converter for the analog drivers to the card and must be decoupled externally because of the large current spikes that the card and the DC-to-DC converter can create. An integrated spike killer ensures the card contacts to remain inactive during power-up or power-down. An internal voltage reference is generated which is used for the DC-to-DC converter, the voltage supervisor and the V_{CC} generator.

All interface signals with the microcontroller ($\overline{PWROFF}$, SIMCLK, SAD1, SAD0, $\overline{SIMERR}$, SCL, SDA and SIMI/O) are referenced to a separate supply pin V_{DDI}, which may be different from V_{DD} ($1.5 \leq V_{DDI} \leq 6$ V).

The pull-up resistors on bus lines SDA and SCL may be referenced to a voltage higher than V_{DDI}. This allows the use of peripherals which do not operate at V_{DDI}.

The voltage supervisor (see Fig.3) senses V_{DDS}. It generates an alarm pulse, whose length t_W is defined by an external capacitor connected to pin DEL, when V_{DD} is too low to ensure proper operation (1 ms per 1 nF typical).

During this alarm pulse, $\overline{SIMERR}$ is LOW and the I²C-bus is unresponsive. $\overline{SIMERR}$ goes back to HIGH, and the I²C-bus becomes operational at the end of this alarm pulse. Bit SUPL is set as long as the status has not been read.

It is also used in order to either block any spurious signals on card contacts during microcontroller reset, or to force an automatic deactivation of the contacts in the event of supply drop-out.

Outside a card session, $\overline{SIMERR}$ is LOW as long as the voltage supervisor is active. If a supply drop-out occurs during a session, $\overline{SIMERR}$ falls to LOW, bit START is cleared and an automatic deactivation is initiated.

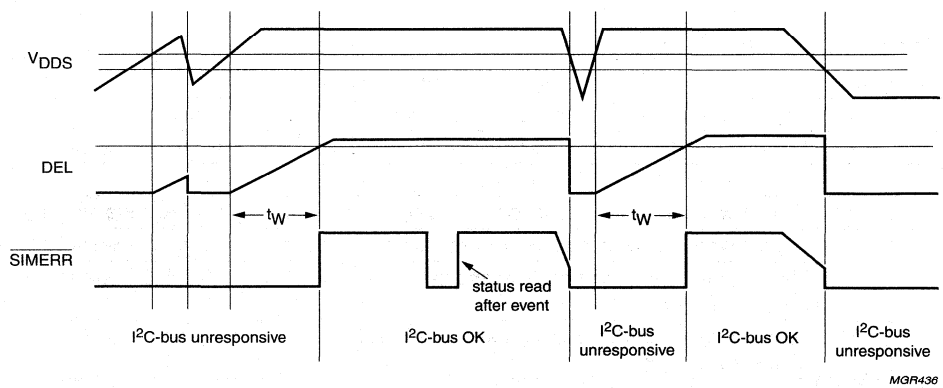


Fig.3 Voltage supervisor.

DC-to-DC converter

The whole circuit is powered by V_{DDS}, except for the V_{CC} generator, the other card contact buffers and the interface signals.

The DC-to-DC converter acts as a doubler or a tripler, depending on the supply voltage V_{DD} and the card supply voltage V_{CC}. There are basically four possible situations:

- V_{DD} = 3 V and V_{CC} = 3 V. The DC-to-DC converter acts as a doubler with a regulation of V_{VUP} at approximately 4.5 V
- V_{DD} = 3 V and V_{CC} = 5 V. The DC-to-DC converter acts as a tripler with a regulation of V_{VUP} at approximately 6.5 V
- V_{DD} = 5 V and V_{CC} = 3 V. The DC-to-DC converter is disabled and V_{DD} is applied to pin VUP
- V_{DD} = 5 V and V_{CC} = 5 V. The DC-to-DC converter acts as a doubler with a regulation of V_{VUP} at approximately 6.5 V.

The recognition of the supply voltage is done by the TDA8003TS at approximately 3.75 V.

When a card session is requested by the microcontroller, the sequencer will first start the DC-to-DC converter, which is a switched capacitors type, clocked by an internal oscillator at a frequency f_{osc} of approximately 2.5 MHz. The output voltage V_{VUP} is regulated at approximately 4.5 or 6.5 V and subsequently fed to the V_{CC} generator. V_{CC} and PGND are used as a reference for all other card contacts.

POWER-DOWN MODE

The Power-down mode is used for current consumption reduction when the card is in Sleep mode.

For entering Power-down mode, the microcontroller must first select CLK in this mode (stop LOW, stop HIGH or 1.25 MHz from the internal oscillator) with bits CLKPD1 and CLKPD2. Subsequently, the microcontroller sends the command PDOWN, CLK is switched to the value predefined by bits CLKPD1 and CLKPD2, and SIMCLK may be stopped (HIGH or LOW).

If the selected CLK is stopped, the biasing currents in the buffers to the card will be reduced. The voltage supervisor and all control functions also remain active. The maximum current taken by the card in this mode when CLK is stopped is assumed to be less than 5 mA.

Before leaving the Power-down mode, the clock signal must first be applied to SIMCLK, and then bit PDOWN must be set to logic 0.

OFF MODE

The Off mode is entered when the $\overline{\text{PWROFF}}$ signal is LOW. In this mode, no function is valid. This mode avoids switching off the power supply of the device, and gives a current consumption less than 2 μA. Before entering the Off mode, the card must be deactivated.

The Off mode is resumed when the $\overline{\text{PWROFF}}$ signal returns to HIGH. This re-initializes the voltage supervisor, and has the same effect as a reset of the device. As long as the device is not ready to operate, the $\overline{\text{SIMERR}}$ signal will remain LOW.

Sequencer and clock counter

The sequencer handles the ensuring activation and deactivation sequences in accordance with GSM11.11 and ISO 7816, even in case of emergency (card take-off, short-circuit and supply drop-out). The sequencer is clocked with the internal oscillator frequency f_{osc}.

The activation is initiated with the START command (only if the card is present, and if the voltage supervisor does not detect a fault on the supply). During activation, V_{CC} goes HIGH and subsequently I/O is enabled and CLK is started with RST = LOW. The clock counter counts the CLK pulses till a start bit is detected on I/O.

After 45000 CLK pulses, if no start bit on I/O has been detected, the sequencer toggles RST to HIGH, and counts again 45000 CLK pulses. If, again, no start bit has been detected, $\overline{\text{SIMERR}}$ will be pulled LOW and the information of bit MUTE is set in the status register.

If a start bit has been detected during the two 45000 CLK pulses slots, the clock counter is stopped, RST is kept at the same level and the session can go on between the card and the system.

The clock counter does not take care of any start bit during the 200 first CLK pulses of both slots; if a start bit is detected between 200 and 352 CLK pulses of both slots, then $\overline{\text{SIMERR}}$ will be pulled LOW and the information of bit EARLY is set in the status register.

The deactivation is initiated either by the microcontroller (STOP command), or automatically by the TDA8003TS in case of card take-off, short-circuit or supply voltage drop-out detected by the voltage supervisor. During deactivation, RST will go LOW, CLK is stopped, I/O is disabled and V_{CC} goes LOW.

Clock circuitry

The clock to the card is either derived from pin SIMCLK (2 to 20 MHz) or from the internal oscillator.

During a card session, f_{CLK} may be chosen to be $\frac{1}{2}f_{SIMCLK}$ or $\frac{1}{4}f_{SIMCLK}$ depending on bit DT/DFN.

For the card Sleep mode, CLK may be chosen stop LOW, stop HIGH or $\frac{1}{2}f_{osc}$ (1.25 MHz) with bits CLKPD1 and CLKPD2. This predefined value will be applied to CLK when bit PDOWN is set to logic 1.

The first CLK pulse has the correct width, and all frequency changes are synchronous, ensuring that no pulse is smaller than 45% of the shortest period.

The duty cycle is within 45 and 55% in stable state, the rise and fall times are less than 8% of the period and precaution has been taken so that there is no overshoot or undershoot.

ACTIVATION SEQUENCE

Figure 4 shows the activation sequence. When the card is inactive, V_{CC}, CLK, RST and I/O are LOW, with low-impedance with respect to ground. The DC-to-DC converter is stopped. SIMI/O is pulled HIGH at V_{DDI} via the 20 kΩ pull-up resistor. When all conditions are met (supply voltage, card present, no hardware problems), the microcontroller may initiate an activation sequence by setting bit START to logic 1 (t_0) via the I²C-bus:

1. The DC-to-DC converter is started (t_1).
2. V_{CC} starts rising from 0 to 3 or to 5 V according to 3 V/5 VN control bit with a controlled rise time of 0.17 V/µs typically (t_2).
3. I/O buffer is enabled in reception mode (t_3).
4. CLK is sent to the card reader with RST = LOW, and the count of 45000 CLK pulses is started ($t_4 = t_{act}$).
5. If a start bit is detected on I/O, the clock counter is stopped with RST = LOW. If not, RST = HIGH, and a new count of 45000 CLK pulses is started (t_5).

If a start bit is detected on I/O and the clock counter is stopped with RST = HIGH, the card session may continue. If not, bit MUTE is set in the status register and $\overline{\text{SIMERR}}$ is pulled LOW. The microcontroller may initiate a deactivation sequence by setting bit START to logic 0.

If a start bit is detected during the 200 first CLK pulses of each count slot, then it will not be taken into account. If a start bit is detected during 200 and 352 CLK pulses of each slot, then bit EARLY is set in the status register and $\overline{\text{SIMERR}}$ is pulled LOW. The microcontroller may initiate a deactivation sequence by setting bit START to logic 0.

The sequencer is clocked by $\frac{1}{64}f_{osc}$ which leads to a time interval T of 25 µs typically. Thus $t_1 = 0$ to $\frac{1}{64}T$; $t_2 = t_1 + \frac{3}{2}T$; $t_3 = t_1 + \frac{7}{2}T$; $t_4 = t_1 + 4T$ and t_5 depends on the SIMCLK frequency.

DEACTIVATION SEQUENCE

Figure 5 shows the deactivation sequence. When the session is completed, the microcontroller sets bit START to logic 0. The circuit will execute an automatic deactivation sequence:

1. Card reset, RST falls to LOW (t_{10}).
2. CLK is stopped (t_{11}).
3. I/O falls to LOW (t_{12}).
4. V_{CC} falls to 0 V with typically 0.17 V/µs slew rate (t_{13}). The deactivation is completed when V_{CC} reaches 0.4 V (t_{de}).
5. The DC-to-DC converter is stopped and CLK, RST, V_{CC} and I/O become low-impedance with respect to PGND (t_{14}).

$t_{10} < \frac{1}{64}T$; $t_{11} = t_{10} + \frac{1}{2}T$; $t_{12} = t_{10} + T$; $t_{13} = t_{12} + 5$ µs and $t_{14} = t_{10} + 4T$.

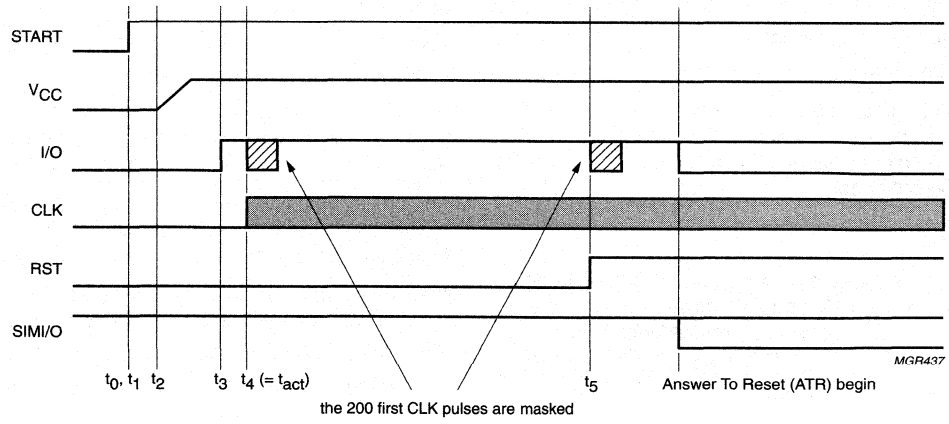


Fig.4 Activation sequence.

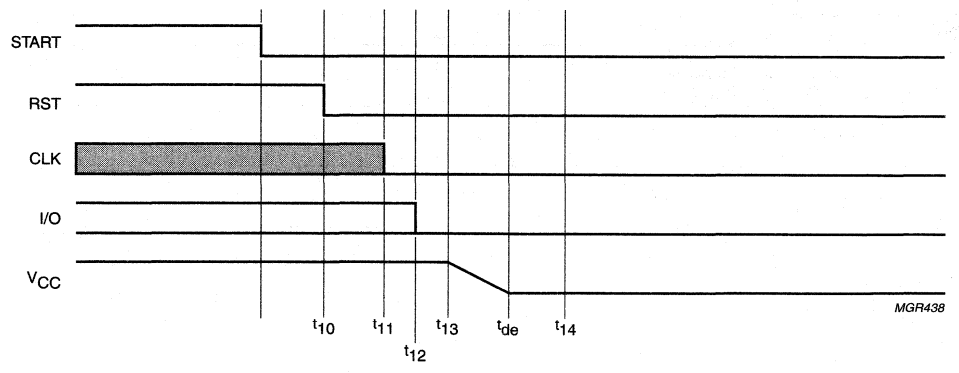


Fig.5 Deactivation sequence.

Protections

The following main hardware fault conditions are monitored by the circuit:

- Short-circuits between V_{CC} and other contacts
- Card take-off during transaction
- Supply drop-out.

When one of these problems is detected during a card session, the security logic block pulls $\overline{SIMERR}$ to LOW, in order to warn the microcontroller and initiates an automatic deactivation of the contacts (see Fig.6).

I/O circuitry

The Idle state is realized by both I/O and SIMI/O being pulled HIGH (via a 10 kΩ pull-up resistor from I/O to V_{CC} and via a 20 kΩ pull-up resistor from SIMI/O to V_{DDI}.

I/O is referenced to V_{CC} and SIMI/O to V_{DDI}, thus allowing operation with $V_{CC} \neq V_{DD} \neq V_{DDI}$.

When configuration bit I/OEN is logic 0, then I/O and SIMI/O are independent, which allows parallelization of several TDA8003TS with only one I/O line on the microcontroller side (up to 4 different I²C-bus addresses).

When bit I/OEN is logic 1, then the data transmission between I/O and SIMI/O is enabled.

The first side on which a falling edge occurs becomes the master. An anti-latch circuit disables the detection of falling edges on the other side, which becomes a slave.

After a delay time t_d (<500 ns) on the falling edge, the N transistor on the slave side is turned on, thus transmitting the logic 0 present on the master side.

When the master goes back to logic 1, the P transistor on the slave side is turned on during t_d, and then both sides return to their Idle states.

The maximum frequency on these lines is 1 MHz.

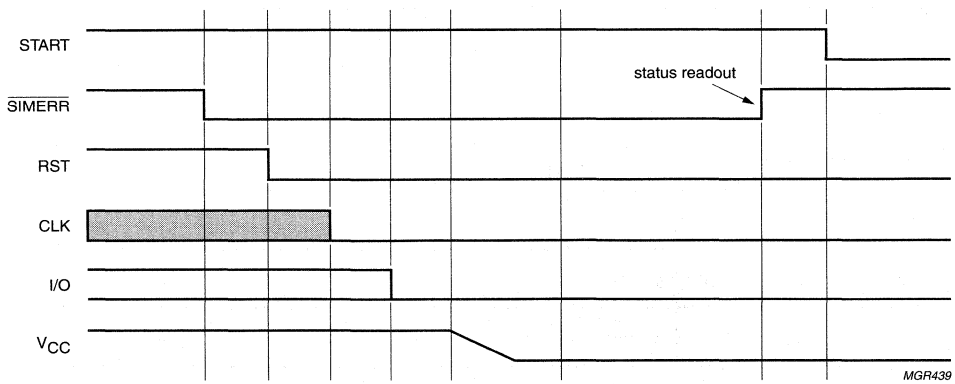


Fig.6 Emergency deactivation.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDP}	power supply voltage		−0.5	+6.5	V
V_{DDS}	signal supply voltage		−0.5	+6.5	V
V_{DDI}	interface signal supply voltage		−0.5	+6.5	V
$V_{i(n)}$	input voltage				
	on pins 1, 17, 21 and 24		−0.5	+6.5	V
	on pins 15, 16, 22 and 23		−0.5	V_{DDS} + 0.5	V
	on pins 19 and 20		−0.5	+6.5	V
	on pins 9, 11 and 13		−0.5	V_{CC} + 0.5	V
	on pin 12		−0.5	+6.5	V
	on pin 8		−0.5	+7.5	V
	on pins 2, 4, 6 and 7		−0.5	V_{VUP} + 0.5	V
$I_{i(n)}$	DC input current				
	on pins 1, 17, 19, 20, 21, 22, 23 and 24		−5	+5	mA
	on pin 15		−5	+10	mA
$I_{i/o(n)}$	DC input/output current				
	on pins 2, 4, 6, 7 and 8		−40	+40	mA
	on pin 16		−5	+5	mA
P_{tot}	continuous total power dissipation	T_{amb} = −40 to +85 °C	−	230	mW
T_j	operating junction temperature		−	125	°C
T_{stg}	IC storage temperature		−55	+150	°C
$V_{esd(n)}$	electrostatic discharge voltage				
	on pins 9, 11, 12, 13 and 16		−6	+6	kV
	on any other pin		−2	+2	kV

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handle Metal Oxide Semiconductor (MOS) devices.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	102	K/W

CHARACTERISTICS

V_{DD} = 3.3 V; V_{DDI} = 1.5 V; f_{SIMCLK} = 13 MHz; f_{CLK} = 3.25 MHz; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage on pins V_{DDS} and V_{DDP}		2.5	–	6.0	V
I_{DD}	supply current on pins V_{DDS} and V_{DDP}	Off mode	–	–	2	µA
		inactive mode	–	–	50	µA
		Power-down mode; V_{CC} = 5 V; I_{CC} = 100 µA; SIMCLK connected to SGND or V_{DDI}; CLK is stopped	–	–	500	µA
		active mode; V_{CC} = 3 V; I_{CC} = 6 mA	–	–	18	mA
		active mode; V_{CC} = 5 V; I_{CC} = 10 mA	–	–	50	mA
		active mode; V_{DD} = 5 V; V_{CC} = 3 V; I_{CC} = 6 mA	–	–	10	mA
		active mode; V_{DD} = 5 V; V_{CC} = 5 V; I_{CC} = 10 mA	–	–	30	mA
V_{DDI}	interface signal supply voltage		1.5	–	6	V
I_{DDI}	interface signals supply current	SIMCLK connected to PGND or V_{DDI}	–	–	2	µA
		f_{SIMCLK} = 13 MHz; V_{DDI} = 1.5 V	–	–	120	µA
$V_{th(VDD)}$	threshold voltage on V_{DD}	falling edge	2	–	2.3	V
V_{hys}	hysteresis voltage on $V_{th(VDD)}$		40	–	200	mV
$V_{th(DEL)}$	threshold voltage on pin DEL		–	1.38	–	V
V_{DEL}	voltage on pin DEL		–	–	V_{DD}	V
$I_{ch(DEL)}$	charge current on pin DEL		–0.5	–1	–2.5	µA
$I_{dch(DEL)}$	discharge current on pin DEL	V_{DEL} = V_{DD}	0.5	–	–	mA
t_W	alarm pulse width	C_{DEL} = 10 nF	15	–	25	ms
Pin SIMCLK						
$f_{i(SIMCLK)}$	clock input frequency		0	–	20	MHz
t_f	fall time		–	–	1	µs
t_r	rise time		–	–	1	µs
V_{IL}	LOW-level input voltage		0	–	$0.3V_{DDI}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DDI}$	–	V_{DDI} + 0.3	V
I_L	leakage current		–	–	±3	µA
DC-to-DC converter						
$½f_{osc}$	oscillator frequency		1	–	1.5	MHz
V_{VUP}	voltage on pin VUP	5 V card	–	6.0	–	V
		3 V card	–	4.5	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pin SDA (open-drain)						
V_{IL}	LOW-level input voltage		−0.3	–	$+0.3V_{DDI}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DDI}$	–	6	V
I_{LH}	HIGH-level leakage current		–	–	1	μA
I_{IL}	LOW-level input current	depends on the pull-up resistor	–	–	–	μA
V_{OL}	LOW-level output voltage	I_{OL} = 3 mA	–	–	0.3	V
Pin SCL (open-drain)						
V_{IL}	LOW-level input voltage		−0.3	–	$+0.3V_{DDI}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DDI}$	–	6	V
I_{LI}	input leakage current		–	–	1	μA
Pin $\overline{\text{SIMERR}}$ (100 kΩ pull-up resistor to V_{DDI})						
V_{OL}	LOW-level output voltage	I_{OL} < 1 mA	–	–	$0.3V_{DDI}$	V
V_{OH}	HIGH-level output voltage	I_{OH} < −1 μA	$0.7V_{DDI}$	–	–	V
Pins SAD0, SAD1 and $\overline{\text{PWROFF}}$						
V_{IL}	LOW-level input voltage		0	–	$0.3V_{DDI}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DDI}$	–	V_{DDI} + 0.3	V
I_{LI}	input leakage current		–	–	±1	μA
Pin RST						
V_O	output voltage	inactive mode; I_O = 1 mA	−0.3	–	+0.4	V
I_O	output current	inactive mode; pin RST grounded	–	–	−1	mA
V_{OL}	LOW-level output voltage	I_{OL} = 200 μA	−0.2	–	+0.3	V
V_{OH}	HIGH-level output voltage	I_{OH} < −200 μA	V_{CC} − 0.5	–	V_{CC} + 0.2	V
t_f	fall time	C_L = 30 pF	–	–	0.5	μs
t_r	rise time	C_L = 30 pF	–	–	0.5	μs
Pin CLK						
V_O	output voltage	inactive mode; I_O = 1 mA	−0.3	–	+0.4	V
I_O	output current	inactive mode; pin CLK grounded	–	–	−1	mA
V_{OL}	LOW-level output voltage	I_{OL} = 200 μA	−0.2	–	+0.3	V
V_{OH}	HIGH-level output voltage	I_{OH} = −200 μA	V_{CC} − 0.5	–	V_{CC} + 0.2	V
t_f	fall time	C_L = 30 pF	–	–	8	ns
t_r	rise time	C_L = 30 pF	–	–	8	ns
f_{clk}	clock frequency	1 MHz power-down configuration	1	–	1.5	MHz
		regular activity	0	–	10	MHz
δ	duty factor	C_L = 30 pF	45	–	55	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pin V_{CC}						
V_O	output voltage	inactive mode; I_O = 1 mA	–	–	0.4	V
		active mode; 5 V card; no load	4.85	5.10	5.40	V
		active mode; 3 V card; no load	2.8	3.05	3.22	V
		active mode; with 200 nF capacitor; including static load (up to 20 mA) and dynamic current pulses; I_{max} = 200 mA, f_{max} = 5 MHz; duration <400 ns				
		5 V card; 40 nAs pulses	4.60	–	5.40	V
		3 V card; 24 nAs pulses	2.75	–	3.22	V
I_O	output current	inactive mode; pin V_{CC} grounded	–	–	–1	mA
		V_{CC} = 5 or 3 V; V_{DD} = 2.5 V	–	–	15	mA
		V_{CC} = 5 or 3 V; V_{DD} = 5.5 V	–	–	40	mA
SR	slew rate on V_{CC} (rise and fall)	$C_{L(max)}$ = 300 nF	0.05	0.17	0.25	V/µs
Pin I/O						
V_O	output voltage	inactive mode; I_O = 1 mA	–	–	0.4	V
I_O	output current	inactive mode; pin I/O grounded	–	–	–1	mA
V_{OL}	LOW-level output voltage	I_{OL} = 1 mA	–0.2	–	+0.3	V
V_{OH}	HIGH-level output voltage	+25 < I_{OH} < –25 µA	$0.8V_{CC}$	–	V_{CC} + 0.2	V
V_{IL}	LOW-level input voltage		–0.3	–	+0.8	V
V_{IH}	HIGH-level input voltage		1.5	–	V_{CC} + 0.3	V
I_{LIH}	HIGH-level input leakage current		–	–	10	µA
I_{IL}	LOW-level input current		–	–	–600	µA
$t_{t(DI)}$	data input transition time	C_L = 30 pF	–	–	1	µs
$t_{t(DO)}$	data output transition time	C_L = 30 pF	–	–	0.5	µs
t_d	delay time on falling edge		–	–	500	ns
$R_{pu(int)}$	internal pull-up resistance between pins I/O and V_{CC}		8	–	13	kΩ
Pin SIMI/O						
V_{OL}	LOW-level output voltage	I_{OL} = 1 mA	–0.2	–	+0.3	V
V_{OH}	HIGH-level output voltage	with internal 20 kΩ pull-up resistor to V_{DDI}; I_O = 10 µA	V_{DDI} – 0.3	–	V_{DDI} + 0.2	V
V_{IL}	LOW-level input voltage		–0.3	–	$+0.3V_{DDI}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DDI}$	–	V_{DDI} + 0.3	V
I_{LIH}	HIGH-level input leakage current		–	–	10	µA
I_{IL}	LOW-level input current	with internal 20 kΩ pull-up resistor to V_{DDI}; V_I = 0 V	–	–	$\frac{-V_{DDI}}{10k\Omega}$	µA
$t_{t(DI)}$	data input transition time	C_L = 30 pF	–	–	1	µs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{t(DO)}$	data output transition time	C_L = 30 pF	–	–	0.5	µs
t_d	delay time on falling edge		–	–	500	ns
$R_{pu(int)}$	internal pull-up resistance between pins SIMI/O and V_{DDI}		16	–	26	kΩ
Pin $\overline{PRES}$						
V_{IL}	LOW-level input voltage		–0.3	–	$+0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	–	V_{DD} + 0.3	V
I_{IL}	LOW-level input current		–	–	5	µA
I_{IH}	HIGH-level input current		–	–	–5	µA
Timing						
t_{act}	activation time		–	–	150	µs
t_{de}	deactivation time		–	–	120	µs

APPLICATION INFORMATION

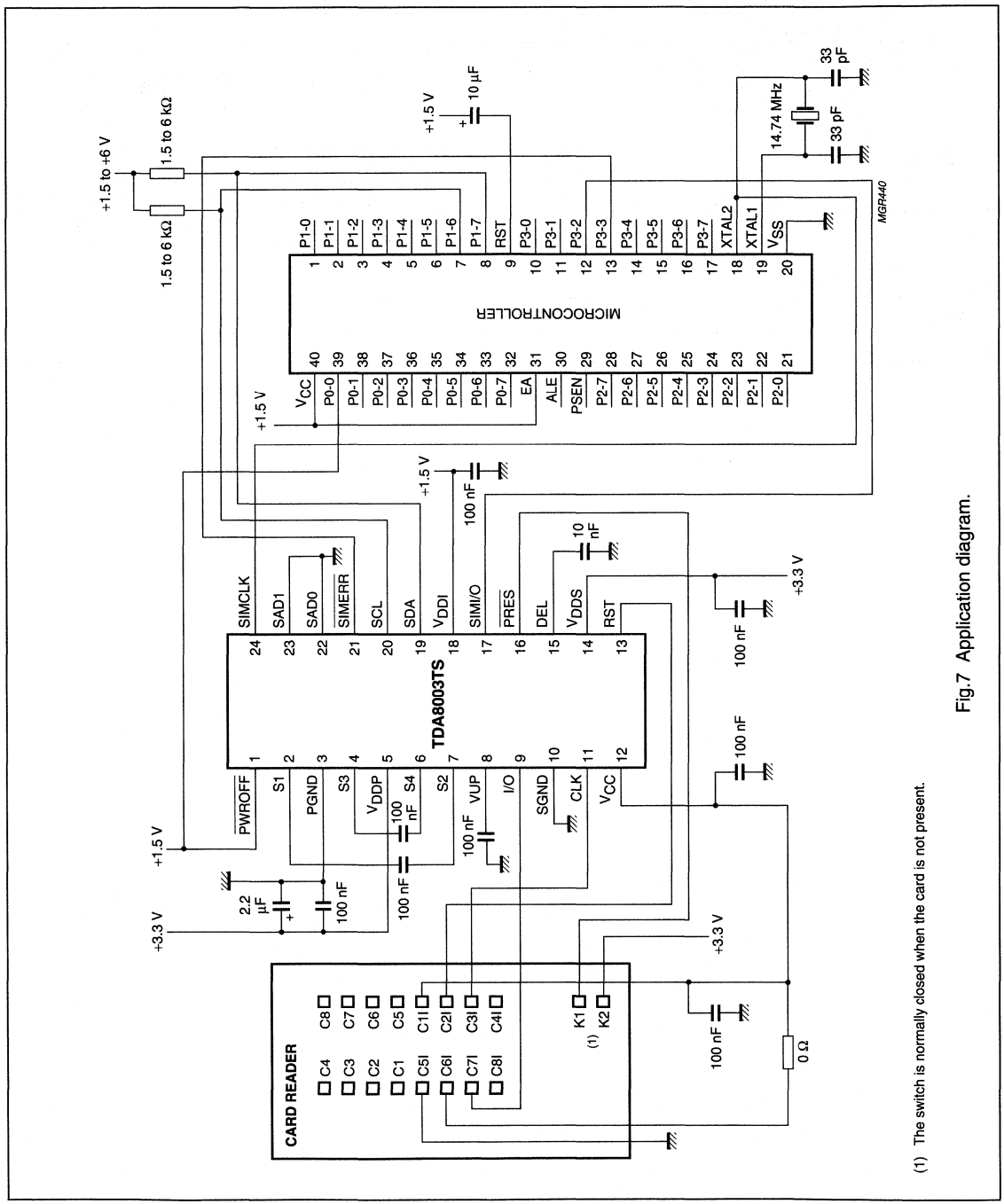


Fig.7 Application diagram.

(1) The switch is normally closed when the card is not present.

I²C-bus interface for colour decoders TDA8442

GENERAL DESCRIPTION

The TDA8442 provides control of four analogue functions and has one high-current and two switching outputs. Control of the IC is performed via the two-line, bidirectional I²C-bus.

Features

- Four analogue control outputs
- One high-current output port (npn open emitter)
- Two switching output ports (npn collector with internal pull-up resistor)
- I²C-bus slave receiver
- Power-down reset.

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38); SOT38-1; 1996 July 23.

QUICK REFERENCE DATA

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX	UNIT
Supply voltage (pin 9)		V_P	10.8	12.0	13.2	V
Supply current	no outputs loaded	I_P	8	13	18	mA
Total power dissipation	no outputs loaded	P_{tot}	–	–	1	W
Operating ambient temperature range		T_{amb}	–20	–	+70	°C

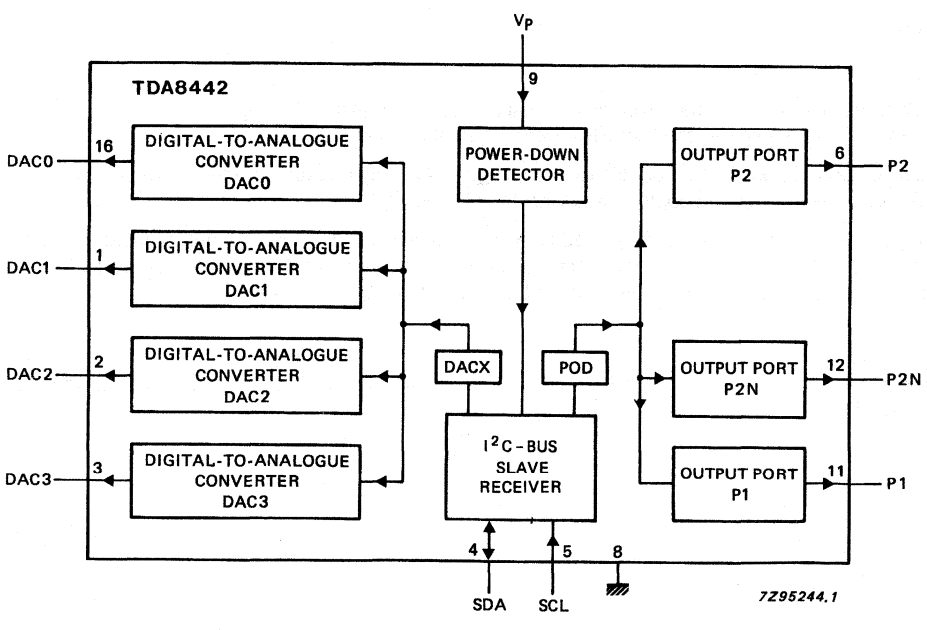


Fig.1 Block diagram.

PINNING

PIN	SYMBOL	DESCRIPTION
1	DAC1	analogue output 1
2	DAC2	analogue output 2
3	DAC3	analogue output 3
4	SDA	serial data line; I²C-bus
5	SCL	serial clock line; I²C-bus
6	P2	Port 2 npn collector output with internal pull-up resistor
7	n.c.	not connected
8	GND	supply return (ground)
9	V_P	positive supply voltage
10	n.c.	not connected
11	P1	Port 1 open npn emitter output
12	P2N	inverted P2 output
13	n.c.	not connected
14	n.c.	not connected
15	n.c.	not connected
16	DAC0	analogue output 0

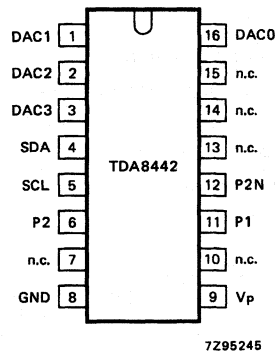


Fig.2 Pinning diagram

FUNCTIONAL DESCRIPTION

Control

Analogue control is facilitated by four 6-bit digital-to-analogue converters (DAC0 to DAC3).
The values of the output voltages from the DACs are set via the I²C-bus.

The high-current output port (P1) is suitable for switching between internal and external RGB signals.
It is an open npn emitter output capable of sourcing 14 mA (min.).

The two output ports (P2 and P2N) can be used for NTSC/PAL switching. These are npn collector outputs with internal pull-up resistors of 10 kΩ (typ.). Both outputs are capable of sinking up to 2 mA with a voltage drop of less than 400 mV. If one output is switched on (LOW), the other output is switched off, and vice versa.

Reset

The power-down-reset mode occurs whenever the positive supply voltage falls below 8.5 V (typ.) and resets all registers to a defined state.

OPERATION

Write

The TDA8442 is controlled via the I²C-bus (specifications for the I²C-bus will be supplied on request). Programming of the TDA8442 is performed using the format shown in Fig.3.

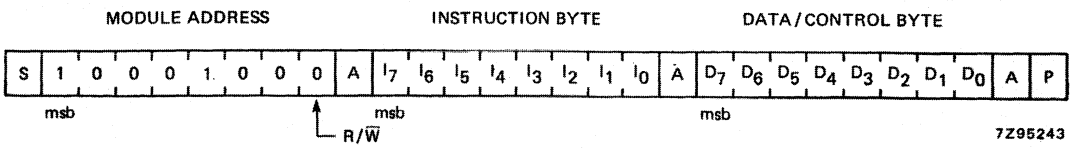


Fig.3 TDA8442 programming format.

Acknowledge (A) is generated by the TDA8442 only when a valid address is received and the device is not in the power-down-reset mode (V_P > 8.5 V (typ.)).

Control

Control is implemented by the instruction bytes POD (port output data) and DACX (digital-to-analogue converter control) together with the corresponding data/control bytes (see Fig.4).

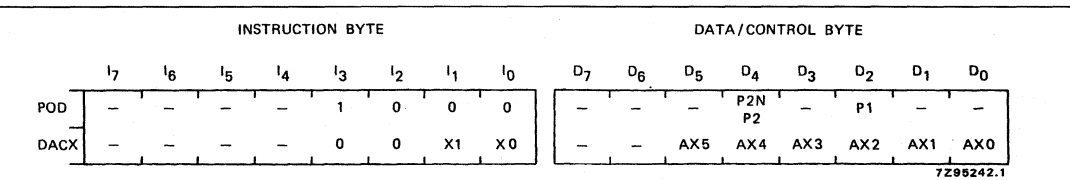


Fig.4 Control porgramming.

POD bit P1

If a logic 1 is programmed, the P1 output is switched on. If a logic 0 is programmed or after a power-down-reset, the P1 output is switched off (high-impedance state).

POD bit P2/P2N

If a logic 1 is programmed, the P2 output is switched off and the P2N output is switched on (LOW). If a logic 0 is programmed or after a power-down-reset, the P2 output is switched on (LOW) and the P2N output is switched off.

DAX bits AX5 to AX0

The digital-to-analogue converter selected corresponds to the decimal equivalent of the two bits X1 and X0. The output voltage of the selected DAC is programmed using bits AX5 to AX0, the lowest value being with all data AX5 to AX0 at logic 0 or when power-down-reset has been activated.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Supply voltage range (pin 9)	V_P	−0.3	+13.2	V
Input/output voltage ranges				
pin 4	V_{SDA}	−0.3	+13.2	V
pin 5	V_{SCL}	−0.3	+13.2	V
pin 6	V_{P2}	−0.3	V_P; note 1	V
pin 11	V_{P1}	−0.3	V_P; note 1	V
pin 12	V_{P2N}	−0.3	V_P; note 1	V
pin 1 to 3 and pin 16	V_{DAX}	−0.3	V_P; note 1	V
Total power dissipation	P_{tot}	–	1	W
Operating ambient temperature range	T_{amb}	−20	+70	°C
Storage temperature range	T_{stg}	−55	+150	°C

Note

1. Pin voltage may exceed V_P if the current in that pin is limited to 10 mA.

CHARACTERISTICS

V_P = 12 V; T_{amb} = +25 °C; unless otherwise specified

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supplies						
Supply voltage (pin 9)		V_P	10.8	12.0	13.2	V
Supply current (pin 9)	no outputs loaded	I_P	8	13	18	mA
I²C-bus inputs						
SDA (pin 4); SCL (pin 5)						
Input voltage HIGH	note 1	V_{IH}	3.0	–	V_P − 1	V
Input voltage LOW		V_{IL}	−0.3	–	1.5	V
Input current HIGH	note 1	I_{IH}	–	–	10	μA
Input current LOW	note 1	I_{IL}	–	–	10	μA
I²C-bus output						
SDA (pin 4)	open collector					
Output voltage LOW	I_{OL} = 3.0 mA	V_{OL}	–	–	0.4	V
Maximum output sink current		I_{OL}	3	5	–	mA

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Ports P2 and P2N						
(pins 6 and 12)	npn collector output with pull-up resistor to V_P					
Internal pull-up resistor to V_P		R_O	5	10	15	kΩ
Output voltage switched on (LOW)	I_{OL} = 2 mA	V_{OL}	–	–	0.4	V
Maximum output sink current		I_{OL}	2	5	–	mA
Leakage current output switched off		$-I_{leak}$	–	–	25	µA
Port P1 (pin 11)	open npn emitter output					
Output current switched on	V_O = 0 to 5 V	I_O	14	–	–	mA
Leakage current switched off	V_O = 0 to V_P	$\pm I_{leak}$	–	–	100	µA
Digital-to-analogue outputs	note 2					
DAC0 (pin 16)						
Maximum output voltage	unloaded; note 3	$V_{O\ max}$	3.0	–	4.25	V
Minimum output voltage	unloaded; note 3	$V_{O\ min}$	0.15	–	1.0	V
Positive value of smalles step	I_O = 2 mA (1 lsb); note 3	$V_{O\ lsb}$	16	–	72	mV
Deviation from linearity	I_O = 2 mA	ΔV	–	–	45	mV
Output impedance	I_O = –2 to +2 mA	Z_O	–	–	30	Ω
Maximum output source current		$-I_{OH}$	2	–	6	mA
Maximum output sink current		I_{OL}	2	8	–	mA
DAC1 (pin 1)						
Maximum output voltage	unloaded; note 3	$V_{O\ max}$	4.0	–	5.0	V
Minimum output voltage	unloaded; note 3	$V_{O\ min}$	1.0	–	1.7	V
Positive value of smallest step	I_O = 2 mA (1 lsb); note 3	$V_{O\ lsb}$	18	–	86	mV
Deviation from linearity	I_O = 2 mA	ΔV	–	–	50	mV
Output impedance	I_O = –2 to +2 mA	Z_O	–	–	30	Ω
Maximum output source current		$-I_{OH}$	2	–	6	mA
Maximum output sink current		I_{OL}	2	8	–	mA

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
DAC2 (pin 2)						
Maximum output voltage	unloaded; note 3	$V_{O\,max}$	4.0	–	5.0	V
Minimum output voltage	unloaded; note 3	$V_{O\,min}$	1.0	–	1.7	V
Positive value of smallest step	I_O = 2 mA (1 lsb); note 3	$V_{O\,lsb}$	18	–	86	mV
Deviation from linearity	I_O = 2 mA	ΔV	–	–	50	mV
Output impedance	I_O = −2 to +2 mA	Z_O	–	–	30	Ω
Maximum output source current		$-I_{OH}$	2	–	6	mA
Maximum output sink current		I_{OL}	2	8	–	mA
DAC3 (pin 3)						
Maximum output voltage	unloaded; note 3	$V_{O\,max}$	10.0	–	11.2	V
Minimum output voltage	unloaded; note 3	$V_{O\,min}$	0.1	–	1.0	V
Positive value of smallest step	I_O = 2 mA (1 lsb); note 3	$V_{O\,lsb}$	70	–	250	mV
Deviation from linearity	I_O = 2 mA	ΔV	–	–	150	mV
Output impedance	I_O = −2 to +2 mA	Z_O	–	–	30	Ω
Maximum output source current		$-I_{OH}$	2	–	6	mA
Maximum output sink current		I_{OL}	2	8	–	mA
Power-down reset						
Maximum value of V_P at which power-down reset is active		V_{PD}	6	–	10	V
Rise time of V_P during power-on	V_P rising from 0 V to V_{PD}	t_r	5	–	–	µs

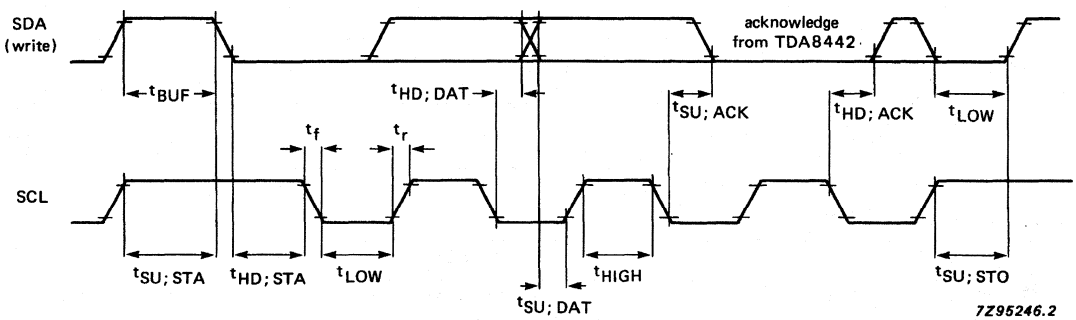
Notes to the Characteristics

1. If V_P < 1 V, the input current is limited to 10 µA at input voltages up to 13.2 V.
2. Pure capacitive load should be avoided because of possible oscillations.
3. Values are proportional to V_P.

I²C-BUS TIMING

Bus loading conditions: 4kΩ pull-up resistor to +5 V; 200 pF capacitor to GND.
All values are referred to V_{IH} = 3 V and V_{IL} = 1.5 V.

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Bus free before start	t_{BUF}	4.0	–	–	µs
Start condition set-up time	$t_{SU;\,STA}$	4.0	–	–	µs
Start condition hold time	$t_{HD;\,STA}$	4.0	–	–	µs
LOW period SCL, SDA	t_{LOW}	4.0	–	–	µs
HIGH period SCL	t_{HIGH}	4.0	–	–	µs
Rise time SCL, SDA	t_r	–	–	1.0	µs
Fall time SCL, SDA	t_f	–	–	0.30	µs
Data set-up time (write)	$t_{SU;\,DAT}$	1	–	–	µs
Data hold time (write)	$t_{HD;\,DAT}$	1	–	–	µs
Acknowledge (from TDA8442) set-up time	$t_{SU;\,ACK}$	–	–	3.5	µs
Acknowledge (from TDA8442) hold time	$t_{HD;\,ACK}$	0	–	–	µs
Stop condition set-up time	$t_{SU;\,STO}$	4.0	–	–	µs



Reference levels are 10 and 90%.

Fig.5 I²C-bus timing; TDA8442.

Octuple 6-bit DACs with I²C-bus

TDA8444; TDA8444T; TDA8444AT

FEATURES

- Eight DACs with 6-bit resolution
- Adjustable common output swing
- Push-pull outputs
- Outputs short-circuit protected
- Three programmable slave address bits
- Large supply voltage range
- Low temperature coefficient.

GENERAL DESCRIPTION

The interface circuit is a bipolar IC in a DIP16, SO16, or SO20 package made in an I2L-compatible 18 V process.

The TDA8444 contains eight programmable 6-bit DAC outputs, an I²C-bus slave receiver with three (two for SO16) programmable address bits and one input (V_{MAX}) to set the maximum output voltage. Each DAC can be programmed separately by a 6-bit word to 64 values, but V_{MAX} determines the maximum output voltage for all DACs. The resolution will be approximately $^1/_{64}V_{MAX}$.

At power-on all DACs are set to their lowest value.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		4.5	12	13.2	V
I_{CC}	supply current	V_{CC} = 12 V	–	14	–	mA
P	power dissipation		–	170	–	mW
V_{VMAX}	input effective voltage		1	–	V_{CC} – 2.0	V
$V_{o(DACn)}$	DAC output voltage	$V_{MAX} = V_{CC}$	0.1	–	V_{CC} – 0.5	V
$V_{o(DACn)(max)}$	maximum DAC output voltage	$1 < V_{MAX} < V_{CC} - 2.0$	–	V_{MAX} + 0.3	–	V
$I_{source(min)}$	minimum DAC source current	data = 1FH	2	–	–	mA
$I_{sink(min)}$	minimum DAC sink current	data = 1FH	2	–	–	mA

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8444	DIP16	plastic dual in-line package; 16 leads (300 mil); long body	SOT38-1
TDA8444T	SO16	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1
TDA8444AT	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1

BLOCK DIAGRAM

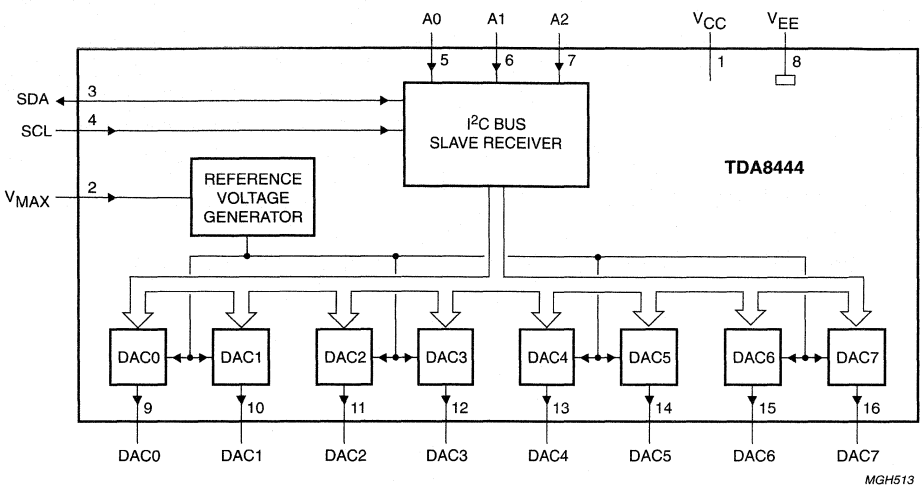


Fig.1 Block diagram.

PINNING

SYMBOL	PIN			DESCRIPTION
	TDA8444 (DIP16)	TDA8444T (SO16)	TDA8444AT (SO20)	
V_{CC}	1	1	1	supply voltage
V_{MAX}	2	2	2	control input for DAC maximum output voltage
SDA	3	3	3	I²C-bus serial data input/output
SCL	4	4	4	I²C-bus serial clock
A0	5	6	7	programmable address bit 0 for I²C-bus slave receiver
A1	6	7	8	programmable address bit 1 for I²C-bus slave receiver
A2	7	–	9	programmable address bit 2 for I²C-bus slave receiver
V_{EE}	8	8	10	ground
DAC0	9	9	11	analog voltage output 0
DAC1	10	10	13	analog voltage output 1
DAC2	11	11	14	analog voltage output 2
DAC3	12	12	15	analog voltage output 3
DAC4	13	13	16	analog voltage output 4
DAC5	14	14	17	analog voltage output 5
DAC6	15	15	18	analog voltage output 6
DAC7	16	16	20	analog voltage output 7
n.c.	–	5	5, 6, 12, 19	not connected

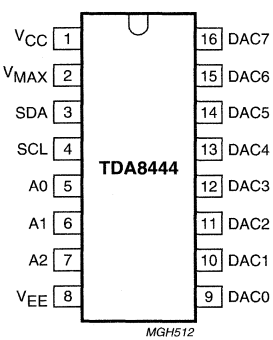


Fig.2 Pin configuration (TDA8444; DIP16).

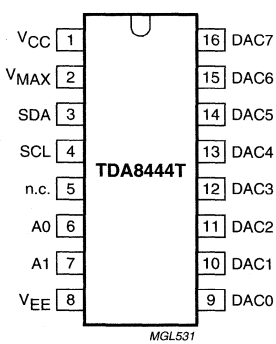


Fig.3 Pin configuration (TDA8444T; SO16).

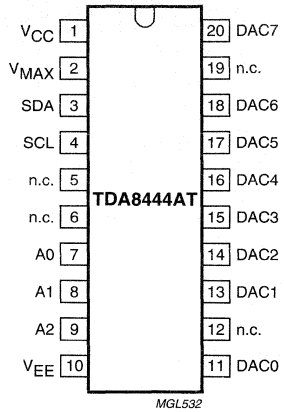


Fig.4 Pin configuration (TDA8444AT; SO20).

FUNCTIONAL DESCRIPTION

I²C-bus interface

The I²C-bus interface is a receive-only slave, which accepts data according the format shown in Table 1.

Table 1 I²C-bus format (see note 1)

S	0	1	0	0	A2	A1	A0	0	A	I3	I2	I1	I0	SD	SC	SB	SA	A	X	X	D5	D4	D3	D2	D1	D0	A	P

Note

1. S = START condition; A2 to A0 = programmable address bits; A = Acknowledge; I3 to I0 = Instruction bits; SD to SA = subaddress bits; X = don't care; D5 to D0 = data bits; P = STOP condition.

Valid addresses are:

TDA8444 and TDA8444AT: 40H, 42H, 44H, 46H, 48H, 4AH, 4CH and 4EH

TDA8444T: 48H, 4AH, 4CH and 4EH (A2 is always logic 1).

All other addresses cannot be acknowledged by the circuit. The actual slave address depends on the programmable address bits A2, A1 and A0. This way up to eight circuits can be used on one I²C-bus.

Valid instructions are: 00H to 0FH; F0H to FFH.

The circuit will not react to other combinations of the 4 instruction bits I3 to I0 than 0 or F, but will still generate an acknowledge. The difference between instruction 0 and F is only important when more than one data byte is sent within one transmission. Instruction 0 causes the data bytes to be written into the DAC-latches with consecutive subaddresses starting with the subaddress given in the instruction byte (auto-increment of subaddress), while instruction F will cause a consecutive writing of the data bytes into the same DAC-latch whose subaddress was given in the instruction byte. In case of only one data byte the DAC-latch with the subaddress equal to the subaddress in the instruction byte will receive the data.

Valid subaddresses are: 0H to 7H.

The subaddresses correspond to DAC0 to DAC7. The Auto-Increment (AI) function of instruction 0, however, works on all possible subaddresses 0 to F in such a way that next to subaddress F, subaddress 0 will follow, and so on.

The data will be latched into the DAC-latch on the positive-going edge of the acknowledge related clock pulse.

The specification of the SCL and SDA I/O meets the I²C-bus specification. For protection against positive voltage pulses on pins 3 and 4, zener diodes are connected between these pins and V_{EE}. This means that normal bus line voltage should not exceed 5.5 V.

The address inputs A0, A1 and A2 can be easily programmed by either a connection to V_{EE} (An = 0) or V_{CC} (An = 1). If the inputs are left floating the result will be An = 1.

V_{MAX}

The V_{MAX} input gives a means of compressing the DAC output voltage swing. The maximum DAC output voltage will be equal to $V_{MAX} + V_{DAC(min)}$, while the 6-bit resolution is maintained. This enables a higher voltage resolution for smaller output swings.

DACs

The DACs consist of a 6-bit data-latch, current switches and an opamp. The current sources connected to the switches have values with weights 2^0 to 2^5. The sum of the switched on currents is converted by the opamp into a voltage between approximately 0.5 and 10.5 V if $V_{MAX} = V_{CC} = 12$ V. The DAC outputs are short-circuit protected against V_{CC} and V_{EE}. Capacitive load on the DAC outputs should not exceed 2 nF in order to prevent possible oscillations at certain levels. The temperature coefficient for each of the outputs remains in all possible conditions well below 0.1 LSB per Kelvin.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	−0.5	+18	V
I_{CC}	supply current	−10	+40	mA
$P_{(max)}$	maximum power dissipation	−	500	mW
$V_{i(n)}$	input voltage	−0.5	+5.9	V
	pins SDA and SCL	−0.5	+5.9	V
	pins V_{MAX}, A0 to A2 and DAC0 to DAC7	−0.5	V_{CC} + 0.5	V
I_n	current in all pins except V_{CC} and V_{EE}	−	±10	mA
T_{stg}	storage temperature	−65	+150	°C
T_{amb}	operating ambient temperature	−20	+70	°C

QUALITY SPECIFICATION

In accordance with *"SNW-FQ-611-E"*.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air		
	TDA8444		75	K/W
	TDA8444T	note 1	100	K/W
	TDA8444AT	note 1	85	K/W

Note

1. When mounted on a Printed-Circuit Board (PCB).

CHARACTERISTICS

V_{CC} = 12 V; T_{amb} = 25 °C; unless otherwise specified.

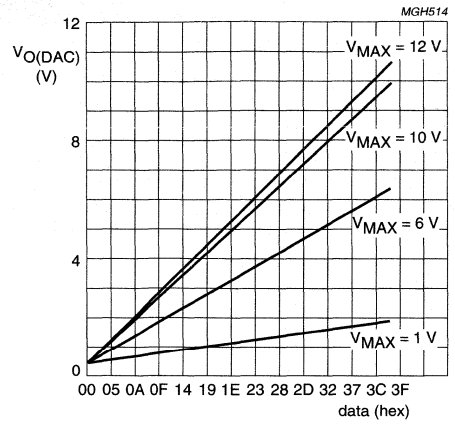
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CC}	supply voltage		4.5	12	13.2	V
I_{CC}	supply current	$V_{MAX} = V_{CC}$ = 12 V; data = 00H	12	14	19	mA
P	power dissipation		–	170	250	mW
V_{rst}	power reset voltage		1	–	4	V
Pin V_{MAX}						
$V_{i(VMAX)}$	input effective voltage		1	–	V_{CC} – 2.0	V
I_i	input current	$V_{MAX} = V_{CC}$	–	–	10	μA
		V_{MAX} = 1 V	–	–	10	μA
Pins SDA and SCL						
V_I	input voltage		0	–	5.5	V
V_{IL}	LOW-level input voltage		–	–	1.0	V
V_{IH}	HIGH-level input voltage		3.0	–	–	V
I_{IL}	LOW-level input current	$V_{SDA} = V_{SCL}$ = –0.3 V	–	–	–10	μA
I_{IH}	HIGH-level input current	$V_{SDA} = V_{SCL}$ = 6 V	–	–	±10	μA
PIN SDA						
V_{OL}	LOW-level output voltage	I_L = 3 mA	–	–	0.4	V
$I_{o(sink)}$	output sink current		3	8	–	mA
Address bits (A0 to A2)						
V_I	input voltage		0	–	V_{CC}	V
V_{IL}	LOW-level input voltage		–	–	1.0	V
V_{IH}	HIGH-level input voltage		2.2	–	–	V
I_{IL}	LOW-level input current	$V_{An} = V_{EE}$	–10	–15	–	μA
I_{IH}	HIGH-level input current	$V_{An} = V_{CC}$	–	–	1	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DACs (DAC0 to DAC7)						
V_o	DAC output voltage	$V_{MAX} = V_{CC}$	0.1	–	$V_{CC} - 0.5$	V
$V_{o(min)}$	minimum output voltage	data = 00H; $I_L = -2$ mA	0.1	0.28	0.5	V
$V_{o(max)}$	maximum output voltage	data = 3FH; $I_L = -2$ mA				
		$V_{MAX} = V_{CC}$	10.0	10.5	11.5	V
		$1 < V_{MAX} < 10$ V	–	note 1	–	V
$I_{o(sink)}$	output sink current	$V_{DAC} = V_{CC}$; data = 1FH	2	8	15	mA
$I_{o(source)}$	output source current	$V_{DAC} = V_{EE}$; data = 1FH	−2	–	−6	mA
Z_o	output impedance	$-2 \leq I_L \leq +2$ mA; data = 1FH	–	4	50	Ω
DNL	differential non-linearity	$V_{MAX} = V_{CC}$; $I_L = -2$ mA	–	–	±0.5	LSB
INL	integral non-linearity	$V_{MAX} = V_{CC}$; $I_L = -2$ mA	–	–	±0.5	LSB
ΔG_{FS}	DC gain match at full-scale	data = 3FH; $I_L = -2$ mA	–	–	5	%
$\Delta G/\Delta$data	DC gain versus other DAC data change	data = 3FH; $I_L = -2$ mA	–	<±0.5	–	LSB
TC	temperature coefficient	data = 3FH; $I_L = -2$ mA	–	<±0.1	–	LSB/K

Note

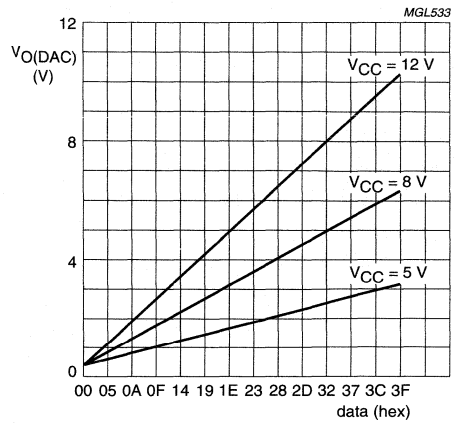
1. The output voltage is typically: $\frac{V_{swing}}{(V_{CC} - 2.0)} \times V_{MAX} + V_{o(00H)}$ with $V_{swing} = V_{o(3FH)} - V_{o(00H)}$ for $V_{MAX} = V_{CC}$.

TEST AND APPLICATION INFORMATION



V_{CC} = 12 V.

Fig.5 DAC output voltage as a function of programmed value.



$V_{MAX} = V_{CC}$.

Fig.6 DAC output voltage as a function of programmed value.

4 × 4 video switch matrix TDA8540

FEATURES

- I²C-bus or non-I²C-bus mode (controlled by DC voltages)
- S-VHS or CVBS processing
- 3-state switches for all channels
- Selectable gain for the video channels
- sub-address facility
- Slave receiver in the I²C mode
- Auxiliary logic outputs for audio switching
- System expansion possible up to 7 devices (28 sources)
- Static short-circuit proof outputs
- ESD protection.

APPLICATIONS

- Colour Television (CTV) receivers
- Peritelevision sets
- Satellite receivers.

GENERAL DESCRIPTION

The TDA8540 has been designed for switching between composite video signals, therefore the minimum of four input lines are provided as requested for switching between two S-VHS sources. Each of the four outputs can be set to a high impedance state, to enable parallel connection of several devices.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		7.2	–	8.8	V
I_{CC}	supply current		–	20	30	mA
I_{SO}	isolation 'OFF' state	at f = 5 MHz	60	80	–	dB
B	3 dB bandwidth		12	–	–	MHz
α_{ct}	crosstalk attenuation between channels		60	70	–	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8540	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1
TDA8540T	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1

BLOCK DIAGRAM

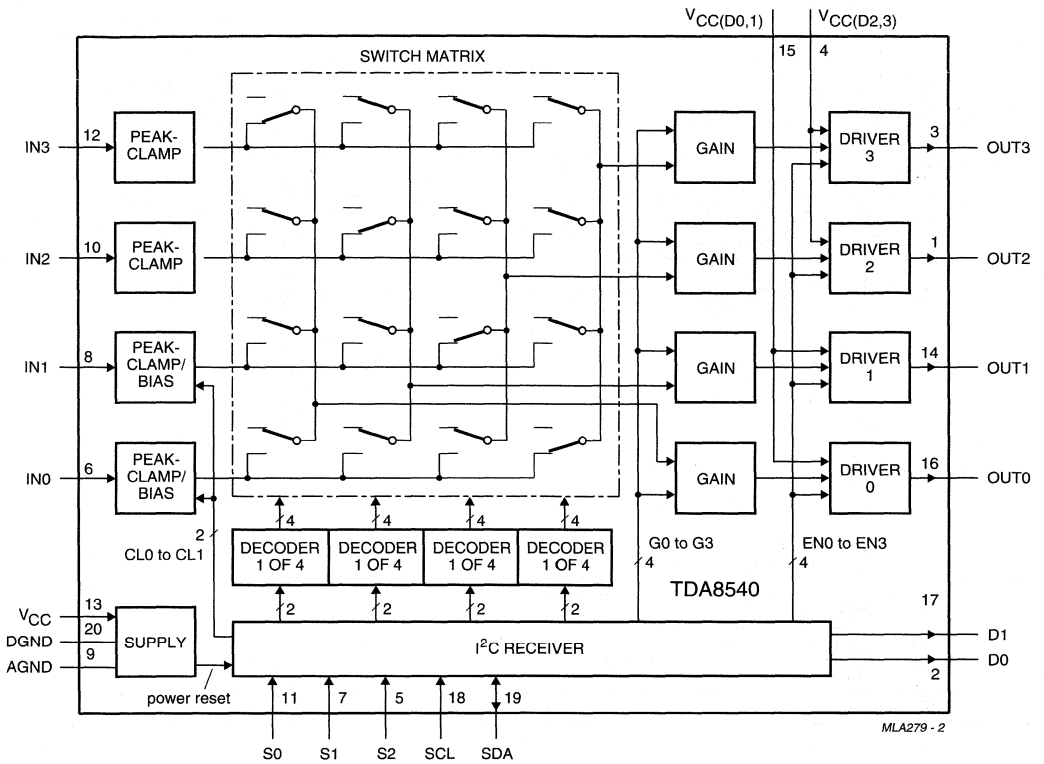


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
OUT2	1	video output 2
D0	2	control output 0
OUT3	3	video output 3
$V_{CC(D2,3)}$	4	driver supply voltage; for drivers 2 and 3
S2	5	sub-address input 2
IN0	6	video input 0 (CVBS or chrominance signal)
S1	7	sub-address input 1
IN1	8	video input 1 (CVBS or chrominance signal)
AGND	9	analog ground
IN2	10	video input 2 (CVBS or luminance signal)
S0	11	sub-address input 0
IN3	12	video input 3 (CVBS or luminance signal)
V_{CC}	13	general supply voltage
OUT1	14	video output 1
$V_{CC(D0,1)}$	15	driver supply voltage; for drivers 0 and 1
OUT0	16	video output 0
D1	17	control output 1
SCL	18	serial clock input
SDA	19	serial data input/output
DGND	20	digital ground

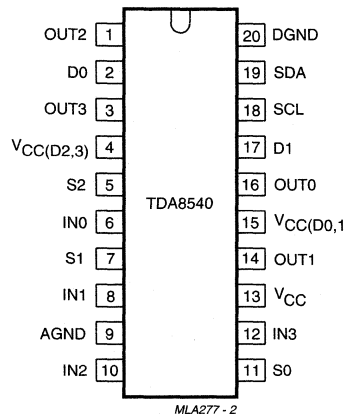


Fig.2 Pinning configuration.

FUNCTIONAL DESCRIPTION

The TDA8540 is controlled via a bidirectional I²C-bus. 3 bits of the I²C address can be selected via the address pin, thus providing a facility for parallel connection of 7 devices.

Control options via the I²C-bus:

- The input signals can be clamped at their negative peak (top sync).
- The gain factor of the outputs can be selected between 1× or 2×.
- Each of the four outputs can individually be connected to one of the four inputs.
- Each output can individually be set in a high impedance state.
- Two binary output data lines can be controlled for switching accompanying sound signals.

The SDA and SCL pins (pins 19 and 18) can be connected to the I²C-bus or to DC switching voltage sources. Address inputs S0 to S2 (pins 11, 7 and 5) are used to select sub-addresses or switching to the non-I²C mode. Inputs S0 to S2 can be connected to the supply voltage (HIGH) or the ground (LOW). In this way no peripheral components are required for selection.

Table 1 I²C-bus sub-addressing

S2	S1	S0	SUB-ADDRESS		
			A2	A1	A0
L	L	L	0	0	0
L	L	H	0	0	1
L	H	L	0	1	0
L	H	H	0	1	1
H	L	L	1	0	0
H	L	H	1	0	1
H	H	L	1	1	0
H	H	H	non I²C addressable		

I²C-bus control

After power-up the outputs are initialized in the high impedance state, and D0 and D1 are at a LOW level.

Detailed description of the I²C-bus specification, with applications, is given in brochure *"The I²C-bus and how to use it"*. This brochure may be ordered using the code 9398 393 40011.

The TDA8540 is a **slave receiver** and the protocol is given in Table 2.

Table 2 The TDA8540 protocol

SEQUENCE									
S[1]	SLV[2]	A[3]	SUB	A[3]	DATA	A[3]	DATA	A[3]	P[4]

Notes

1. S = START condition.
2. Data transmission to the TDA8540 starts with the slave address (SLV).
3. A = acknowledge bit, generated by TDA8540.
4. P = STOP condition.

Table 3 Data transmission to the TDA8540 begins with SLV

A6 MSB	A5	A4	A3	A2	A1	A0	R/$\overline{W}$ LSB
1	0	0	1	A2[1]	A1[1]	A0[1]	0[2]

Notes

1. A2 to A0: pin programmable slave address bits.
2. R/$\overline{W}$ = 0; write only.

After the SLV, a second byte, SUB, is required for selecting the functions, as shown in Table 4.

Table 4 The second byte: SUB

7 MSB	6	5	4	3	2	1	0 LSB
0	0	0	0	0	0	RS1	RS0

Options for SUB:

If SUB = 00H: access to switch control (SW1)

If SUB = 01H: access to gain/clamp/data control (GCO)

If SUB = 02H: access to output enable control (OEN).

Remarks:

If more than one data byte is sent, the SUB byte will be automatically incremented.

If more than 3 data bytes are sent, the internal counter will roll over and the device will then rewrite the first register.

Data Bytes

SWI (SUB = 00H): selects which input is connected to the different outputs, as shown in Table 5.

Table 5 SWI (SUB = 00H) selection of inputs connected to outputs

7 MSB	6	5	4	3	2	1	0 LSB
S31	S30	S21	S20	S11	S10	S01	S00

Table 6 Selection of inputs

OUTPUT	Sj1 AND Sj0[1]			
	00	01	10	11
OUTj	IN0	IN1	IN2	IN3

Note

1. For j = 0 to 3.
   Example: if S21 = 0 and S20 = 1, then OUT2 is connected to IN1.

GCO (SUB = 01H):

- Selects the gain of each output.
- Selects the clamp action or mean value on inputs 0 and 1.
- Determines the value of the auxiliary outputs D1 and D0.

Table 7 GCO byte

7 MSB	6	5	4	3	2	1	0 LSB
G3[1]	G2[1]	G1[1]	G0[1]	CL1[2]	CL0[2]	D1[3]	D0[3]

Notes

1. For j = 0 to 3: if Gj = 0 (1), then output j has a gain of 2 (1).
2. If CL0 (CL1) = 0, then input signal on IN0 (IN1) is clamped.
3. For j = 0 or 1: if Dj = 0 (1), then logical output j is LOW (HIGH).

OEN (SUB = 02H): selects, for each output, if the output is active or high impedance, see Table 8.

Table 8 OEN (SUB = 02H) determines which output is active or high impedance

7 MSB	6	5	4	3	2	1	0 LSB
X(1)	X(1)	X(1)	X(1)	EN3(2)	EN2(2)	EN1(2)	EN0(2)

Notes

1. X = don't care.
2. For j = 0 to 3: if ENj = 0 (1), then OUT j is high impedance (active).

After a power-on reset:

- The outputs are set to a high impedance state; the outputs are connected to IN0; the gains are set at two and inputs IN0 and IN1 are clamped.
- Programming of the device is necessary because the outputs are in high impedance state.

Non-I²C-bus control

If the S0, S1 and S2 pins are all connected to V_{CC} the device will enter the non-I²C-bus mode.

After a power-on reset:

- Gain is set at two for all outputs.
- All inputs are clamped.
- All outputs are active.
- The matrix position is given by the SDA and SCL voltage level.

Table 9 Non-I²C-bus control

OUTPUT	SCL AND SDA			
	00	01	10	11
OUT3	IN3	IN2	IN1	IN0
OUT2	IN2	IN3	IN0	IN1
OUT1	IN1	IN0	IN3	IN2
OUT0	IN0	IN1	IN2	IN3

SCL and SDA act as normal input pins:

SCL interchanges (OUT3 and OUT2) with (OUT1 and OUT0).

SDA interchanges OUT3 with OUT2 and OUT1 with OUT0.

Remark: For use with chrominance signals, the clamp action must be overruled by external bias.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage (pin 13)		−0.3	+9.1	V
P_{tot}	total power dissipation		−	750	mW
$V_{CC(D0,1)}$, $V_{CC(D2,3)}$	driver supply voltage		−0.3	+13.8	V
IN0 to IN3	video input voltage		−0.3	+7.2	V
OUT0 to OUT3	video output voltage		−0.3	+7.2	V
D0, D1	control output voltage		−0.3	+7.2	V
SDA, SDL	I^2C input/output voltage		−0.3	+8.8	V
S0 to S2	sub-address input voltage		−0.3	+8.8	V
T_{stg}	IC storage temperature		−55	+125	°C
T_j	junction temperature		−	+150	°C
V_{es}	electrostatic handling	HBM; note 1	−1500	+1500	V
		MM; note 2	−200	+200	V

Notes

1. Human Body Model (HBM): in accordance with UZW-BO/FQ-A302.
2. Machine Model (MM): in accordance with UZW-BO/FQ-B302 (stress reference pins: AGND and DGND short-circuited and V_{CC}).

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	SOT146-1	60 (typ.)	K/W
	SOT163-1	85 (typ.)	K/W

OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
General						
V_{CC}	supply voltage (pin 13)		7.2	−	8.8	V
T_{amb}	operating ambient temperature		0	−	70	°C
Video inputs (pins 6, 8, 10 and 12)						
C_I	external capacitor		−	100	−	nF
$V_{I(p\text{-}p)}$	C signal amplitude (peak-to-peak value)	note 1	−	−	1	V
$V_{I(p\text{-}p)}$	CVBS or Y-signal amplitude (peak-to-peak value)	note 2	−	−	1.5	V
Video drivers (pins 4 and 15)						
R_D	external collector resistor	note 3	−	25	−	Ω
C_D	external decoupling capacitor	note 4	−	22	−	µF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Sub-address S0, S1 and S2 (pins 5, 7 and 11)						
V_{IH}	HIGH level input voltage		4	–	V_{CC}	V
V_{IL}	LOW level input voltage		0	–	1	V

Notes

1. Only for pins 6 and 8 when clamp action is not selected for these pins.
2. On all the video input pins, when non-I²C-bus control mode is selected or when clamp action is selected on pins 6 and 8 (by I²C-bus control).
3. Connected between V_{CC} and pin 4 or pin 15.
4. Connected between AGND and pin 4 or pin 15.

CHARACTERISTICS

V_{CC} = 8 V; T_{amb} = 25 °C; gain condition, clamp condition and OFF state are controlled by the I²C-bus; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
I_{CC}	supply current	without load	–	20	30	mA
		OFF state	–	12	–	mA
Video inputs: IN0 to IN3 when the clamp is active (see Figs 3 and 4)						
I_{LI}	input leakage current	V_I = 3 V	–	0.4	1	μA
V_{clamp}	input clamping voltage	I_I = 5 μA	–	2.2	–	V
I_{clamp}	input clamping current	V_I = 0 V	1.2	–	–	mA
Video inputs: IN0 and IN2 when the clamp is not active (see Fig.3)						
V_{bias}	DC input bias level	I_I = 0	–	2.9	–	V
R_I	input resistance		–	10	–	kΩ
Video outputs: OUT0 to OUT3 (see Fig.5)						
Z_O	output impedance	OFF state	100	–	–	kΩ
R_O	output resistance		–	5	–	Ω
ISO	isolation	OFF state; f = 5 MHz	60	–	–	dB
V_O	output top sync level; (Y or CVBS)		0.4	0.7	1	V
V_{bias}	output mean value for chrominance signals	G = 2; load = 150 Ω	1.5	1.9	2.2	V
		G = 1; without load	1	1.3	1.6	V
G_v	voltage gain	G = 1; f = 1 MHz	−1	0	+1	dB
		G = 2; f = 1 MHz	5	6	7	dB
G_{diff}	differential gain	note 1	–	0.5	3	%
φ_{diff}	differential phase	note 1	–	0.6	–	deg
NL	non linearity	note 2	–	0.5	2	%
α_{ct}	crosstalk attenuation between channels	note 3	60	70	–	dB
SVRR	supply voltage rejection	note 4	36	55	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ΔG	maximum gain variation	100 kHz < f < 5 MHz	–	0.5	–	dB
		100 kHz < f < 8.5 MHz	–	1	–	dB
		100 kHz < f < 12 MHz	–	3	–	dB
α_{ct}	crosstalk attenuation of I²C-bus signals		60	–	–	dB
Auxiliary outputs D0 and D1 (open collector)						
I_{OH}	HIGH level output current	V_{OH} = 5.5 V	–	–	10	μA
V_{OL}	LOW level output voltage	I_{OL} = 4 mA	–	–	0.4	V
I²C-bus inputs SCL and SDA						
I_{IH}	HIGH level input current	V_{IH} = 3.0 V	–	–	10	μA
I_{IL}	LOW level input current	V_{IL} = 1.5 V	−10	–	–	μA
C_i	input capacitance		–	–	10	pF
I²C-bus output SDA						
V_{OL}	LOW level output voltage	I_{OL} = 3 mA	–	–	0.4	V
Sub-address S0, S1 and S2						
I_{IH}	HIGH level input current	$V_{IH} = V_{CC}$	–	–	10	μA
I_{IL}	LOW level input current	V_{IL} = 0 V	–	–	10	μA

Notes

1. Gain set at 2; R_L = 150 Ω; test signal D2 from CCIR 330.
2. Gain set at 2; R_L = 150 Ω; test signal D1 from CCIR 17.
3. Measured from any selected input to output; f = 5 MHz; R_L = 150 Ω; gain set at 2; V_I = 1.5 V (peak-to-peak value). This measurement requires an optimized board.
4. Supply voltage ripple rejection: $20 \log \frac{V_{ripple\ (supply)}}{V_{ripple\ (on\ output)}}$;
   measured at f = 1 kHz with $V_{ripple\ (supply\ max)}$ = 100 mV (peak-to-peak value).
   The supply voltage rejection ratio is >36 dB at f_{max} = 100 kHz.

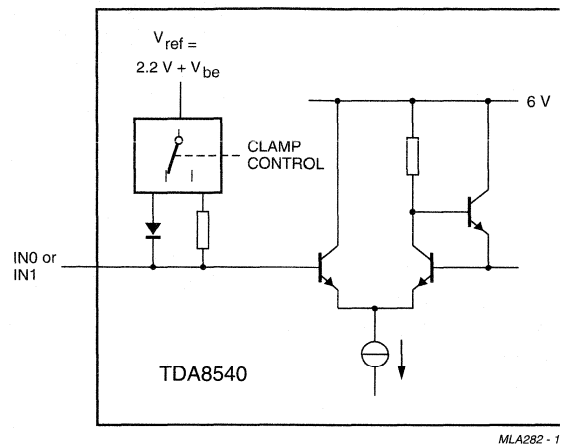


Fig.3 IN0 and IN1 inputs.

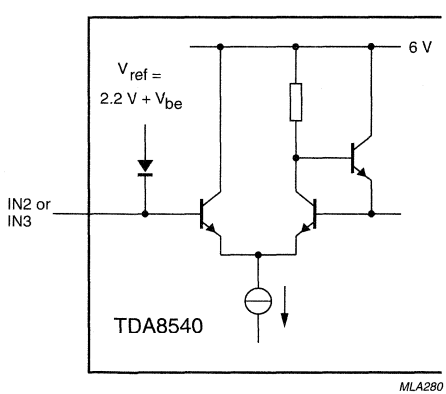


Fig.4 IN2 and IN3 inputs.

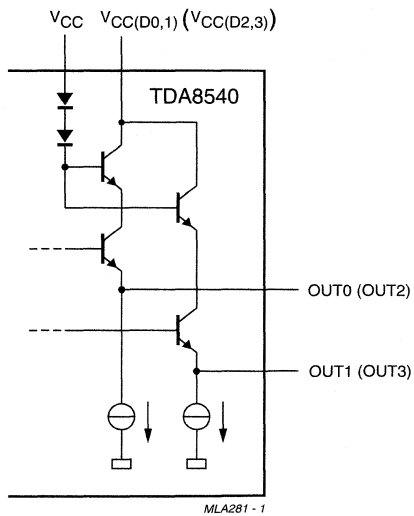
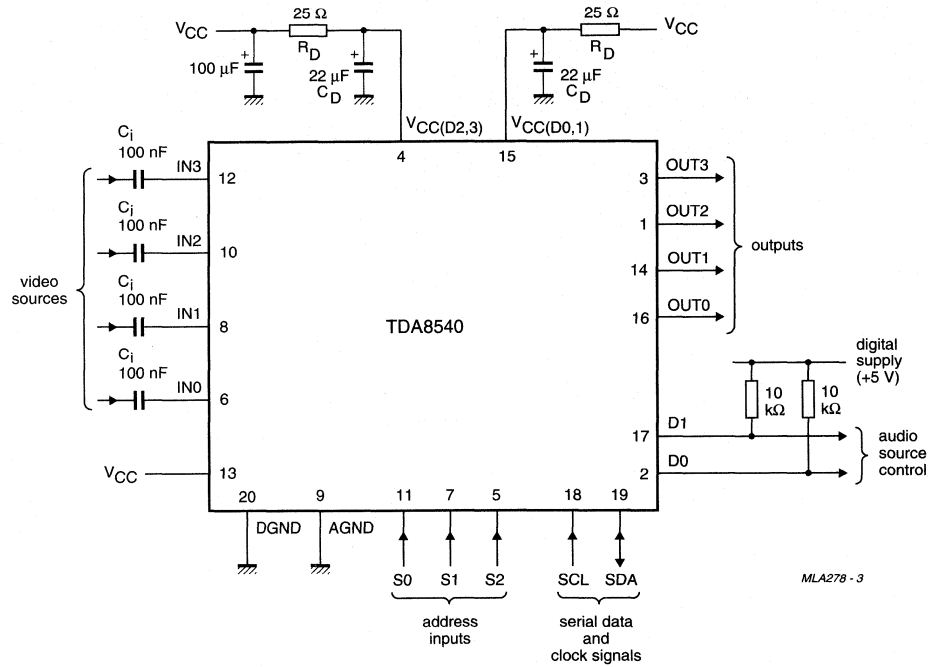


Fig.5 Driver output stage.

APPLICATION INFORMATION



V_{CC} = analog supply (+8 V).

Fig.6 Application diagram.

Triple high speed Analog-to-Digital Converter (ADC)

TDA8752

FEATURES

- Triple 8-bit ADC
- Sampling rate up to 100 MHz
- IC controllable via a serial interface, which can be either I²C-bus or 3-wire, selected via a TTL input pin
- IC analog voltage input from 0.4 to 1.2 V (p-p) to produce full-scale ADC input of 1 V (p-p)
- 3 clamps for programming a clamping code between −63.5 and +64 in steps of ½LSB
- 3 controllable amplifiers: gain controlled via the serial interface to produce a full scale resolution of ½LSB peak-to-peak
- Amplifier bandwidth of 250 MHz
- Low gain variation with temperature
- PLL, controllable via the serial interface to generate the ADC clock, which can be locked to a line frequency from 15 to 280 kHz
- Integrated PLL divider
- Programmable phase clock adjustment cells
- Internal voltage regulators
- TTL compatible digital inputs and outputs
- Chip enable high-impedance ADC output
- Power-down mode
- Possibility to use up to four ICs in the same system, using the I²C-bus interface, or more, using the 3-wire serial interface
- 1 W power dissipation.

APPLICATIONS

- R, G and B high speed digitizing
- LCD panels drive
- LCD projection systems
- VGA and higher resolutions
- Using two ICs in parallel, higher display resolution can be obtained; 200 MHz pixel frequency.

GENERAL DESCRIPTION

The TDA8752 is a triple 8-bit ADC with controllable amplifiers and clamps for the digitizing of large bandwidth RGB signals.

The clamp level, the gain and all of the other settings are controlled via a serial interface (either I²C-bus or 3-wire serial bus, selected via a logic input).

The IC also includes a PLL that can be locked on the horizontal line frequency and generates the ADC clock. The PLL jitter is minimized for high resolution PC graphics applications. An external clock can also be input to the ADC.

It is possible to set the TDA8752 serial bus address between four fixed values, in the event that several TDA8752 ICs are used in a system, using the I²C-bus interface (for example, two ICs used in an odd/even configuration).

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			SAMPLING FREQUENCY (MHz)
	NAME	DESCRIPTION	VERSION	
TDA8752H/6	QFP100	plastic quad flat package; 100 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT317-2	60
TDA8752H/8				100

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage	for R, G and B channels	4.75	5.0	5.25	V
V_{DDD}	logic supply voltage	for I^2C-bus and 3-wire	4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output stages supply voltage	for R, G and B channels	4.75	5.0	5.25	V
$V_{CCA(PLL)}$	analog PLL supply voltage		4.75	5.0	5.25	V
$V_{CCO(PLL)}$	output PLL supply voltage		4.75	5.0	5.25	V
I_{CCA}	analog supply current		–	120	–	mA
I_{DDD}	logic supply current	for I^2C-bus and 3-wire	–	1.0	–	mA
I_{CCD}	digital supply current		–	40	–	mA
I_{CCO}	output stages supply current	f_{CLK} = 100 MHz; ramp input	–	6	–	mA
$I_{CCA(PLL)}$	analog PLL supply current		–	28	–	mA
$I_{CCO(PLL)}$	output PLL supply current		–	5	–	mA
f_{CLK}	maximum clock frequency	TDA8752/6	60	–	–	MHz
		TDA8752/8	100	–	–	MHz
$f_{ref(PLL)}$	PLL reference clock frequency		15	–	280	kHz
f_{VCO}	VCO output clock frequency		12	–	100	MHz
INL	DC integral non linearity	from analog input to digital output; full-scale; ramp input; f_{CLK} = 100 MHz	–	±0.5	±1.5	LSB
DNL	DC differential non linearity	from analog input to digital output; full-scale; ramp input; f_{CLK} = 100 MHz	–	±0.5	±1.0	LSB
$\Delta G_{amp}/T$	amplifier gain stability as a function of temperature	V_{ref} = 2.5 V with 100 ppm/°C maximum	–	–	200	ppm/°C
B	amplifier bandwidth	–3 dB; T_{amb} = 25 °C	250	–	–	MHz
t_{set}	settling time of the ADC block plus AGC	input signal settling time < 1 ns; T_{amb} = 25 °C	–	–	6	ns
DR_{PLL}	PLL divider ratio		100	–	4095	
P_{tot}	total power consumption	f_{CLK} = 100 MHz; ramp input	–	1.0	–	W
$j_{PLL(rms)}$	maximum PLL phase jitter (RMS value)	f_{ref} = 66.67 kHz; f_{CLK} = 100 MHz	–	0.3	–	ns

BLOCK DIAGRAM

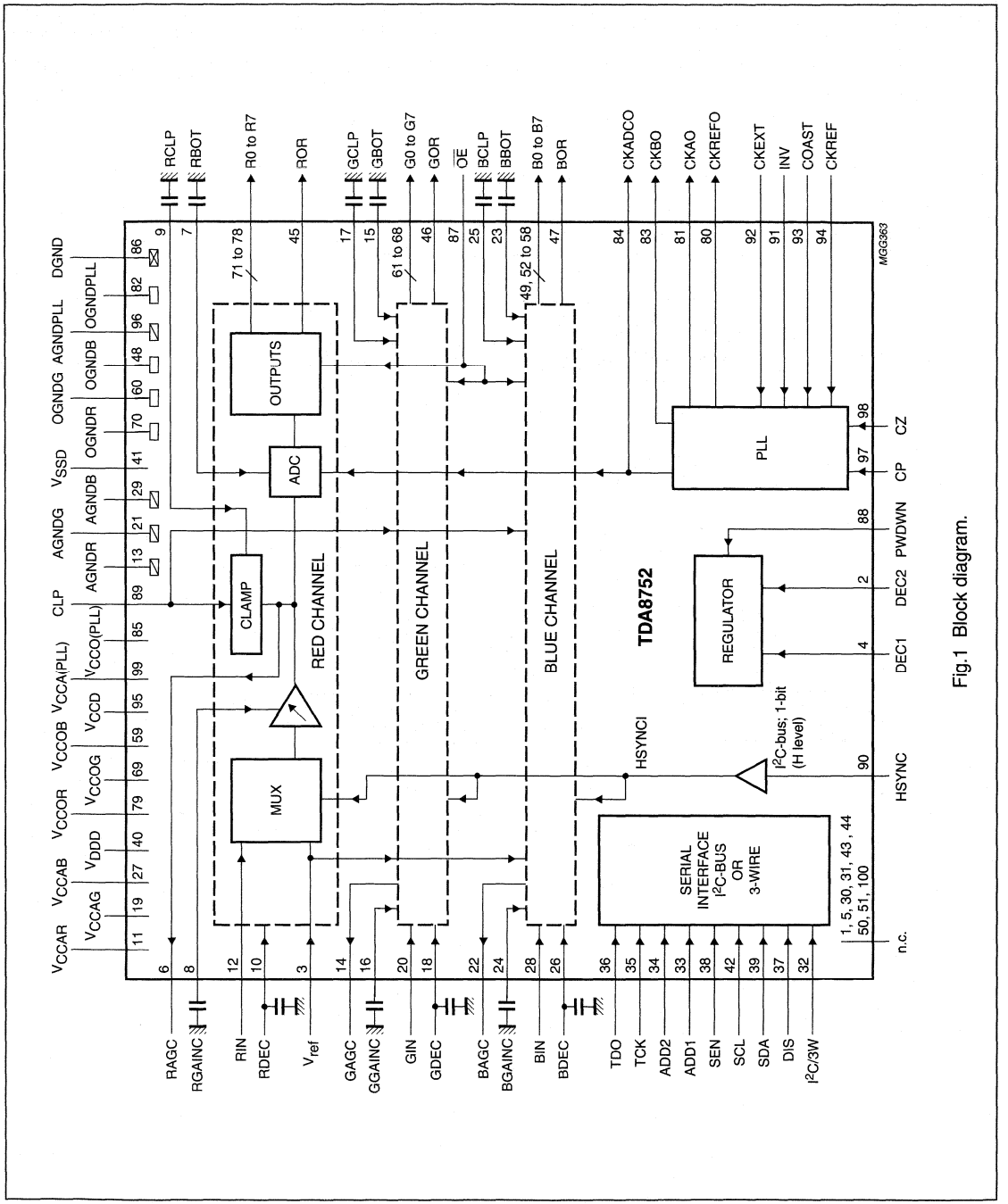


Fig.1 Block diagram.

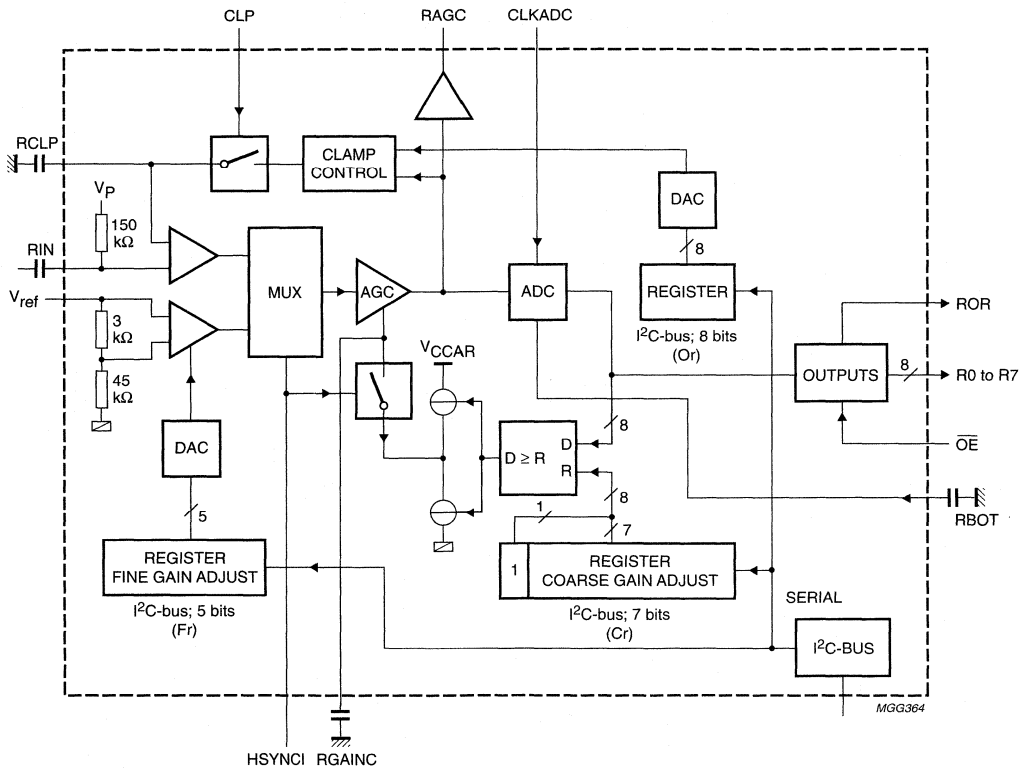


Fig.2 Red channel diagram.

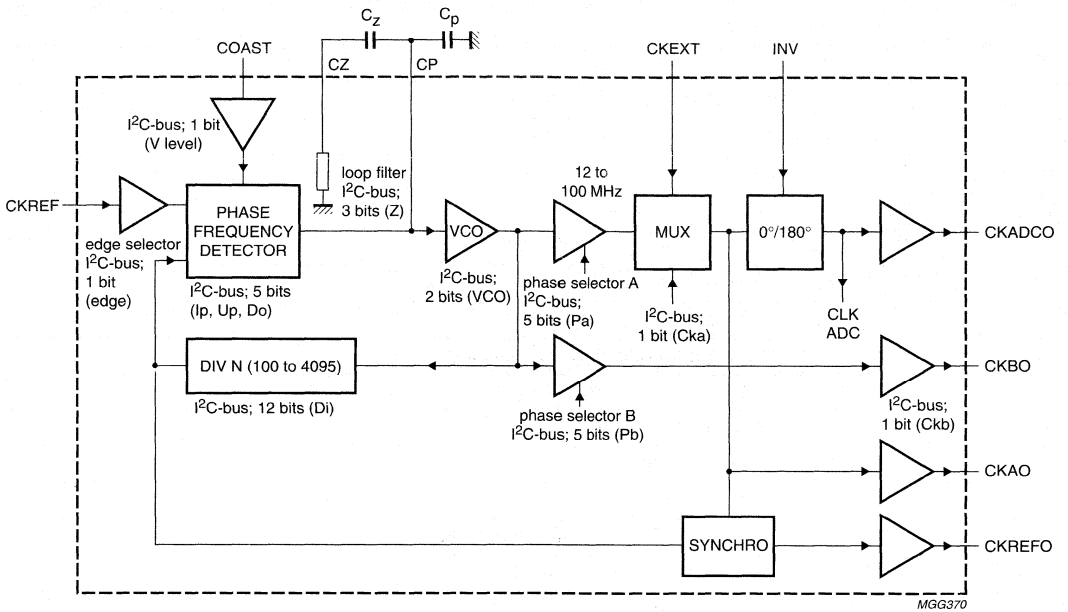


Fig.3 PLL diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
DEC2	2	main regulator decoupling input
V_{ref}	3	gain stabilizer voltage reference input
DEC1	4	main regulator decoupling input
n.c.	5	not connected
RAGC	6	red channel AGC output
RBOT	7	red channel ladder decoupling input (BOT)
RGAINC	8	red channel gain capacitor input
RCLP	9	red channel gain clamp capacitor input
RDEC	10	red channel gain regulator decoupling input
V_{CCAR}	11	red channel gain analog power supply
RIN	12	red channel gain analog input
AGNDR	13	red channel gain analog ground
GAGC	14	green channel AGC output
GBOT	15	green channel ladder decoupling input (BOT)
GGAINC	16	green channel gain capacitor input
GCLP	17	green channel gain clamp capacitor input
GDEC	18	green channel gain regulator decoupling input
V_{CCAG}	19	green channel gain analog power supply
GIN	20	green channel gain analog input
AGNDG	21	green channel gain analog ground
BAGC	22	blue channel AGC output
BBOT	23	blue channel ladder decoupling input (BOT)
BGAINC	24	blue channel gain capacitor input
BCLP	25	blue channel gain clamp capacitor input
BDEC	26	blue channel gain regulator decoupling input
V_{CCAB}	27	blue channel gain analog power supply
BIN	28	blue channel gain analog input
AGNDB	29	blue channel gain analog ground
n.c.	30	not connected
n.c.	31	not connected
I^2C/3W	32	selection input between I^2C-bus (active HIGH) and 3-wire serial bus (active LOW)
ADD1	33	I^2C-bus address control input 1
ADD2	34	I^2C-bus address control input 2
TCK	35	scan test mode (active HIGH)

SYMBOL	PIN	DESCRIPTION
TDO	36	scan test output
DIS	37	I^2C and 3W disable control input (disable at HIGH level)
SEN	38	select enable for 3-wire serial bus input (see Fig.10)
SDA	39	I^2C/3W serial data input
V_{DDD}	40	logic I^2C/3W digital power supply
V_{SSD}	41	logic I^2C/3W digital ground
SCL	42	I^2C/3W serial clock input
n.c.	43	not connected
n.c.	44	not connected
ROR	45	red channel ADC output bit out of range
GOR	46	green channel ADC output bit out of range
BOR	47	blue channel ADC output bit out of range
OGNDB	48	blue channel ADC output ground
B0	49	blue channel ADC output bit 0 (LSB)
n.c.	50	not connected
n.c.	51	not connected
B1	52	blue channel ADC output bit 1
B2	53	blue channel ADC output bit 2
B3	54	blue channel ADC output bit 3
B4	55	blue channel ADC output bit 4
B5	56	blue channel ADC output bit 5
B6	57	blue channel ADC output bit 6
B7	58	blue channel ADC output bit 7 (MSB)
V_{CCOB}	59	blue channel ADC output power supply
OGNDG	60	green channel ADC output ground
G0	61	green channel ADC output bit 0 (LSB)
G1	62	green channel ADC output bit 1
G2	63	green channel ADC output bit 2
G3	64	green channel ADC output bit 3
G4	65	green channel ADC output bit 4
G5	66	green channel ADC output bit 5
G6	67	green channel ADC output bit 6
G7	68	green channel ADC output bit 7 (MSB)
V_{CCOG}	69	green channel ADC output power supply
OGNDR	70	red channel ADC output ground
R0	71	red channel ADC output bit 0 (LSB)

SYMBOL	PIN	DESCRIPTION
R1	72	red channel ADC output bit 1
R2	73	red channel ADC output bit 2
R3	74	red channel ADC output bit 3
R4	75	red channel ADC output bit 4
R5	76	red channel ADC output bit 5
R6	77	red channel ADC output bit 6
R7	78	red channel ADC output bit 7 (MSB)
V_{CCOR}	79	red channel ADC output power supply
CKREFO	80	reference output clock resynchronized horizontal pulse
CKAO	81	PLL clock output 3 (in phase with reference output clock)
OGNDPLL	82	PLL digital ground
CKBO	83	PLL clock output 2
CKADCO	84	PLL clock output 1 (in phase with internal ADC clock)
$V_{CCO(PLL)}$	85	PLL output power supply
DGND	86	digital ground
$\overline{OE}$	87	output enable not (when $\overline{OE}$ is HIGH, the outputs are in high-impedance)
PWDWN	88	power-down control input (IC is in power-down mode when this pin is HIGH)
CLP	89	clamp pulse input (clamp active HIGH)
HSYNC	90	horizontal synchronization input pulse
INV	91	PLL clock output inverter command input (invert when HIGH)
CKEXT	92	external clock input
COAST	93	PLL coast command input
CKREF	94	PLL reference clock input
V_{CCD}	95	digital power supply
AGNDPLL	96	PLL analog ground
CP	97	PLL filter input
CZ	98	PLL filter input
V_{CCAPLL}	99	PLL analog power supply
n.c.	100	not connected

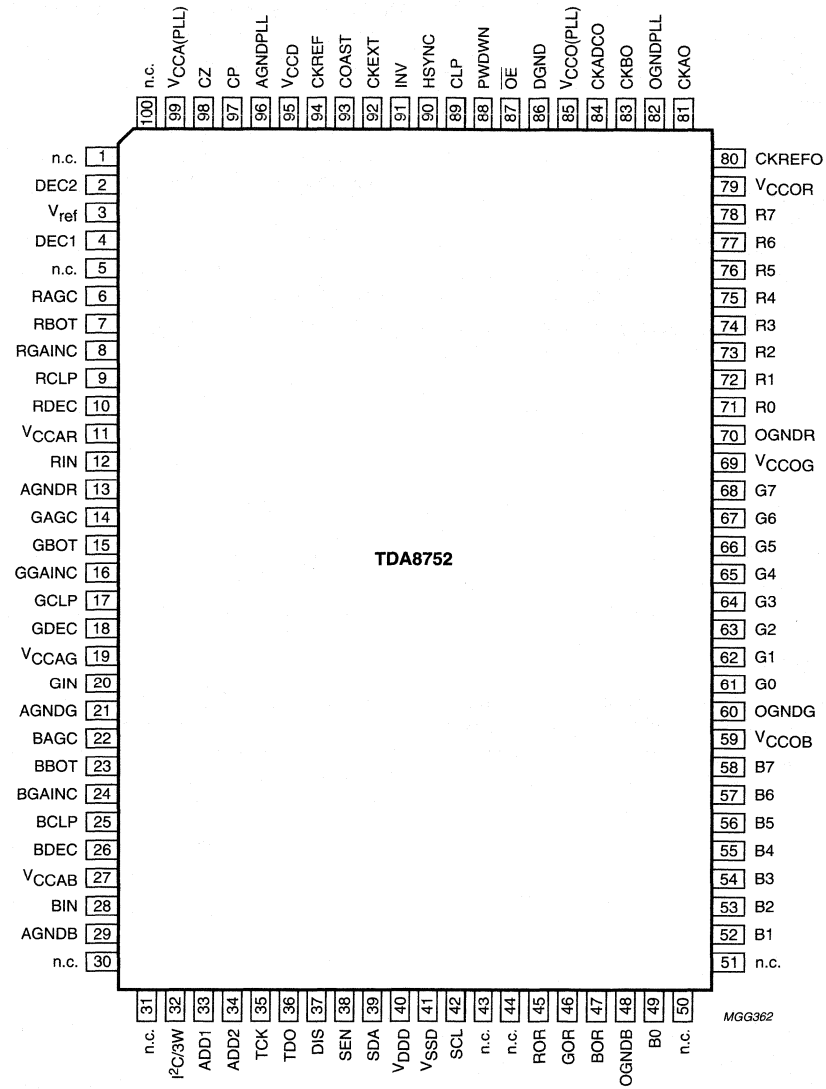


Fig.4 Pin configuration.

FUNCTIONAL DESCRIPTION

This triple high-speed 8-bit ADC is designed to convert RGB signals, from a PC or work station, into data used by a LCD driver (pixel clock up to 200 MHz, using 2 ICs).

IC analog video inputs

The video inputs are internally DC polarized. These inputs are AC coupled externally.

Clamps

Three independent parallel clamping circuits are used to clamp the video input signals on the black level and to control the brightness level. The clamping code is programmable between code −63.5 and +64 in steps of ½LSB. The programming of the clamp value is achieved via an 8-bit DAC. Each clamp must be able to correct an offset from ±0.1 V to ±10 mV within 300 ns, and correct the total offset in 10 lines.

The clamps are controlled by an external TTL positive going pulse (pin CLP). The drop of the video signal is <1 LSB.

Normally, the circuit operates with a 0 code clamp, corresponding to the 0 ADC code. This clamp code can be changed from −63.5 to +64 as represented in Fig.7, in steps of ½LSB. The digitized video signal is always between code 0 and code 255 of the ADC.

Variable gain amplifier

Three independent variable gain amplifiers are used to provide, to each channel, a full-scale input range signal to the 8-bit ADC. The gain adjustment range is designed so that, for an input range varying from 0.4 to 1.2 V (p-p), the output signal corresponds to the ADC full-scale input of 1 V (p-p).

To ensure that the gain does not vary over the whole operating temperature range, an external reference of +2.5 V DC, (V_{ref} with a 100 ppm/°C maximum variation) supplied externally, is used to calibrate the gain at the beginning of each video line before the clamp pulse using the following principle.

A differential of 0.156 V (p-p) ($1/16 V_{ref}$) reference signal is generated internally from the reference voltage (V_{ref}). During the synchronization part of the video line, the multiplexer, controlled by the TTL synchronization signal (HSYNCI, coming from HSYNC; see Fig.1) with a width equal to one of the video synchronization signals (e.g. signal coming from a synchronization separator), is switched between the two amplifiers.

The output of the multiplexer is either the normal video signal or the 0.156 V reference signal (during HSYNC).

The corresponding ADC outputs are then compared to a pre-set value loaded in a register. Depending on the result of the comparison, the gain of the variable gain amplifiers is adjusted (coarse gain control; see Figs 2 and 8). The three 7-bit registers receive data via a serial interface to enable the gain to be programmed.

The pre-set value loaded in the 7-bit register is chosen between approximately 67 codes to ensure the full-scale input range (see Fig.8). A contrast control can be achieved using these registers. In this case care should be taken to stay within the allowed code range (32 to 99).

A fine correction using three 5-bit DACs, also controlled via the serial interface, is used to finely tune the gain of the three channels (fine gain control; see Figs 2 and 9) and to compensate the channel-to-channel gain mismatch.

With a full scale ADC input, the resolution of the fine register corresponds to ½LSB peak-to-peak variation.

To use these gain controls correctly, it is recommended to fix the coarse gain (to have a full-scale ADC input signal) to within 4LSB and then adjust it with the fine gain. The gain is adjusted during HSYNC. During this time the output signal is not related to the amplified input signal. The outputs, when the coarse gain system is stable, is related to the programmed coarse code (see Fig.8).

ADCs

The ADCs are 8-bit with a maximum clock frequency of 100 Msps. The ADCs input range is 1 V (p-p) full-scale. One out of range bit exists per channel (ROR, GOR and BOR). It will be at logic 1 when the signal is out of range of the full scale of the ADCs.

Pipeline delay in the ADCs is 1 clock cycle from sampling to data output.

The ADCs reference ladders regulators are integrated.

ADC outputs

ADC outputs are straight binary. An output enable pin ($\overline{OE}$; active LOW) enables the output status between active and high-impedance ($\overline{OE}$ = HIGH) to be switched; it is recommended to load the outputs with a 10 pF capacitive load. The timing must be checked very carefully if the capacitive load is more than 10 pF.

Phase-locked loop

The ADCs are clocked either by an internal PLL locked to the CKREF clock, (all of the PLL is on-chip except the loop filter capacitance) or an external clock, CKEXT. Selection is performed via the serial interface bus.

The reference clock (CKREF) range is between 15 and 280 kHz. Consequently, the VCO minimum frequency is 12 MHz and the maximum frequency 100 MHz for the TDA8752/8 and 60 MHz for the TDA8752/6. The gain of the VCO part can be controlled via the serial interface, depending on the frequency range to which the PLL is locked.

To increase the bandwidth of the PLL, the charge pump current, controlled by the serial interface, must also be increased. The relationship between the frequency and the current is given by the following equation:

$$f_n = \frac{1}{2\pi}\sqrt{\frac{K_O I_P}{(C_z + C_P)N}}$$

Where:

f_n = the natural PLL frequency

K_O = the VCO gain

N = the division number

C_z and C_P = capacitors of the PLL filter.

The other PLL equation is as follows:

$$f_z = \frac{1}{2\pi \times R \times C_z} \text{ and } \left(\xi = \frac{1}{2} \times \frac{f_n}{f_z}\right)$$

Where:

f_z = loop filter zero frequency

R = the chosen resistance for the filter

ξ = the damping factor.

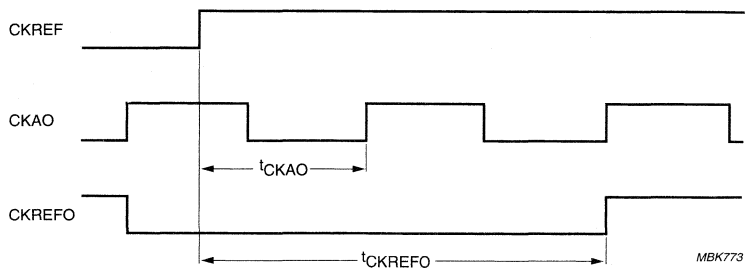
Different resistances for the filter can be programmed via the serial interface. To have better performances, the PLL parameters should be chosen so that:

$f_n/f_{ref} \cong 0.05$

$\xi \cong 1.5$.

It is possible to control (independently) the phase of the ADC clock and the phase of an additional clock output (which could be used to drive a second TDA8752). For this, two serial interface-controlled digital phase-shift controllers are included (controlled by 5-bit registers, phase shift controller steps are 11.25° each on the whole PLL frequency range).

CKREF is resynchronized, by the synchro block, on the CKAO clock. The output is CKREFO (LOW during 8 clock periods). CKAO is the clock at the output of the phase selector A. This clock can be used as the clocks for CKBO and CKADCO. The timing is given in Fig.5.



$t_{CKAO} = t_{CLK(buffer)} + t_{phase\ selector}$ ($t_{CLK(buffer)}$ = 10 ns and $t_{phase\ selector} = \frac{t_{phase\ selector}}{2\pi} \times T_{CLK(pixel)}$).

t_{CKREFO} = either t_{CKAO} if phase A ≥01000 or $t_{CKAO} + T_{CLK(pixel)}$ if phase A <01000.

Fig.5 Timing.

The COAST pin is used to disconnect the PLL phase frequency detector during the frame flyback or the unavailability of the CKREF signal. This signal can normally be derived from the VSYNC signal.

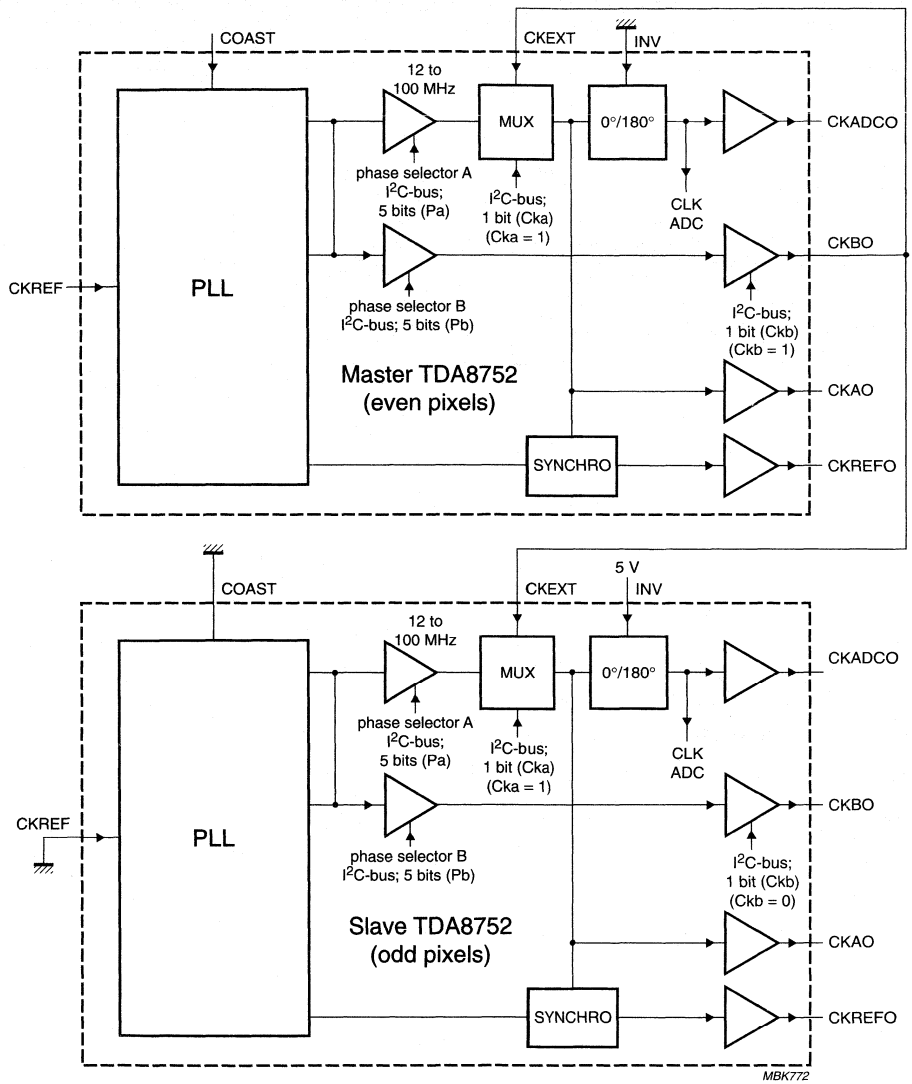
The clock output is able to drive an external 10 pF load (for the on-chip ADCs).

The PLL can be used in three different methods:

1. The IC can be used as stand-alone with a sampling frequency of up to 100 MHz for the TDA8752/8 and up to 60 MHz for the TDA8752/6.
2. When an RGB signal is at a pixel frequency exceeding 100 to 200 MHz, it is possible to follow one of the two possibilities given below;
   a) Using one TDA8752; the sampling rate can be reduced by a factor of two, by sampling the even pixels in the even frame and the odd pixels in the odd frame. The INV pin is used to toggle between frames.
   b) Using two TDA8752s the PLL of the master TDA8752 is used to drive both ADC clocks. The PLL of the slave TDA8752 is disconnected and the CKBO of the master TDA8752 is connected to pin CKEXT of both TDA8752.

   The master TDA8752 is used to sample the even pixels and the slave TDA8752 for odd pixels, using a 180° phase shift between the clocks (CKADCO pins). The master chip has its INV pin LOW while the slave chip has its INV pin HIGH, which guarantees the 180° shift ADC clock drive. It is then necessary to adjust phase B of the master chip. Special care should be taken with the quality of the input signal (input setting time).

   If CKREFO output signal at the master chip is needed, it is possible to use one of the two phase A values in order to avoid set-up and hold problems in the SYNCHRO function; e.g. PHASEA = 100000 and PHASEA = 111111.



Slave at 180° phase shift with respect to pin CKADCO of the master TDA8752.

Fig.6 Dual TDA8752 solution for pixel clock rate with a single phase adjustment (100 to 200 MHz).

I²C-bus and 3-wire serial bus interface

The I²C-bus and 3-wire serial buses control the status of the different control DACs and registers. Control pin DIS enables or disables the full serial interface function (disable at HIGH level). Four ICs can be used in the same system and programmed by the same bus. Therefore, two pins (ADD1 and ADD2) are available to set each address respectively, for use with the I²C-bus interface. All programming is described in Chapter "I²C-bus and 3-wire interfaces".

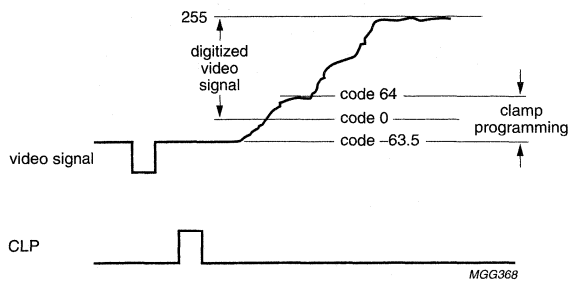


Fig.7 Clamp definition.

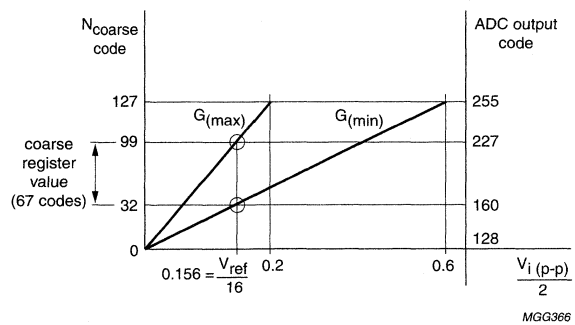


Fig.8 Coarse gain control.

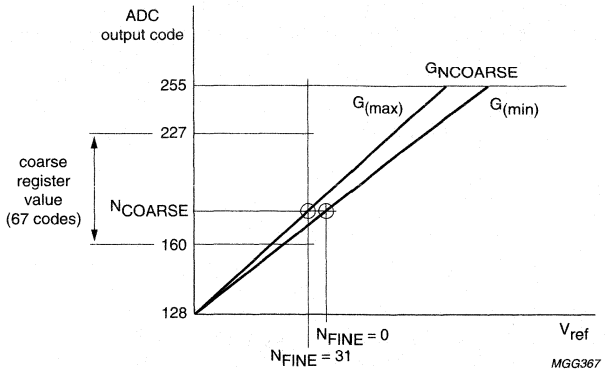


Fig.9 Fine gain correction for a coarse gain $G_{NCOARSE}$.

I²C-BUS AND 3-WIRE INTERFACES

Register definitions

The configuration of the different registers is as follows:

Table 1 I²C-bus and 3-wire registers

FUNCTION NAME	SUB-ADDRESS								BIT DEFINITION								DEFAULT VALUE
	A7	A6	A5	A4	A3	A2	A1	A0	MSB							LSB	
SUBADDR	–	–	–	–	–	–	–	–	X	X	X	Mode	Sa3	Sa2	Sa1	Sa0	xxx1 0000
OFFSETR	X	X	X	X	0	0	0	0	Or7	Or6	Or5	Or4	Or3	Or2	Or1	Or0	0111 1111
COARSER	X	X	X	X	0	0	0	1	X	Cr6	Cr5	Cr4	Cr3	Cr2	Cr1	Cr0	x010 0000
FINER	X	X	X	X	0	0	1	0	X	X	X	Fr4	Fr3	Fr2	Fr1	Fr0	xxx0 0000
OFFSETG	X	X	X	X	0	0	1	1	Og7	Og6	Og5	Og4	Og3	Og2	Og1	Og0	0111 1111
COARSEG	X	X	X	X	0	1	0	0	X	Cg6	Cg5	Cg4	Cg3	Cg2	Cg1	Cg0	x010 0000
FINEG	X	X	X	X	0	1	0	1	X	X	X	Fg4	Fg3	Fg2	Fg1	Fg0	xxx0 0000
OFFSETB	X	X	X	X	0	1	1	0	Ob7	Ob6	Ob5	Ob4	Ob3	Ob2	Ob1	Ob0	0111 1111
COARSEB	X	X	X	X	0	1	1	1	X	Cb6	Cb5	Cb4	Cb3	Cb2	Cb1	Cb0	x010 0000
FINEB	X	X	X	X	1	0	0	0	X	X	X	Fb4	Fb3	Fb2	Fb1	Fb0	xxx0 0000
CONTROL	X	X	X	X	1	0	0	1	V level	H level	edge	Up	Do	Ip2	Ip1	Ip0	0000 0100
VCO	X	X	X	X	1	0	1	0	Z2	Z1	Z0	Vco1	Vco0	Di11	Di10	Di9	0110 0001
DIVIDER (LSB)	X	X	X	X	1	0	1	1	Di8	Di7	Di6	Di5	Di4	Di3	Di2	Di1	1001 0000
PHASEA	X	X	X	X	1	1	0	0	X	Di0	Cka	Pa4	Pa3	Pa2	Pa1	Pa0	x000 0000
PHASEB	X	X	X	X	1	1	0	1	X	X	Ckb	Pb4	Pb3	Pb2	Pb1	Pb0	xx00 0000

All the registers are defined by a sub-address of 8 bits; bit A4 refers to the mode which is used with the I²C-bus interface; bits Sa3 to Sa0 are the subaddresses of each register.

The bit mode, used only with the I²C-bus, enables two modes to be programmed:

- If Mode = 0, each register is programmed independently by giving its sub-address and its content
- If Mode = 1, all the registers are programmed one after the other by giving this initial condition (xxx1 1111) as the sub-address state; thus, the registers are charged following the predefined sequence of 16 bytes (from sub-address 0000 to 1101).

OFFSET REGISTER

This register controls the clamp level for the RGB channels. The relationship between the programming code and the level of the clamp code is given in Table 2.

Table 2 Coding

PROGRAMMED CODE	CLAMP CODE	ADC OUTPUT
0	−63.5	underflow
1	−63	
2	−62.5	
↓	↓	
127	0	0
↓	↓	↓
254	63.5	63 or 64
255	64	64

The default programmed value is:

- Programmed code = 127
- Clamp code = 0
- ADC output = 0.

COARSE AND FINE REGISTERS

These two registers enable the gain control, the AGC gain with the coarse register and the reference voltage with the fine register. The coarse register programming equation is as follows:

$$GAIN = \frac{N_{COARSE} + 1}{V_{ref}\left(1 - \frac{N_{FINE}}{32 \times 16}\right)} \times \frac{1}{16} =$$

$$\frac{N_{COARSE} + 1}{V_{ref}(512 - N_{FINE})} \times 32$$

Where: V_{ref} = 2.5 V.

The gain correspondence is given in Table 3. The gain is linear with reference to the programming code (N_{FINE} = 0).

Table 3 Gain correspondence (COARSE)

N_{COARSE}	GAIN	V_i TO BE FULL-SCALE
32	0.825	1.212
99	2.5	0.4

The default programmed value is as follows:

- N_{COARSE} = 32
- Gain = 0.825
- V_i to be full-scale = 1.212.

To modulate this gain, the fine register is programmed using the above equation. With a full-scale ADC input, the fine register resolution is a ½LSB peak-to-peak (see Table 4 for N_{COARSE} = 32).

Table 4 Gain correspondence (FINE)

N_{FINE}	GAIN	V_i TO BE FULL-SCALE
0	0.825	1.212
31	0.878	1.139

The default programmed value is: N_{FINE} = 0.

CONTROL REGISTER

COAST and HSYNC signals can be inverted by setting the I²C-bus control bits V level and H level respectively. When V level and H level are set to zero respectively, COAST and HSYNC are active HIGH.

The bit 'edge' defines the rising or falling edge of CKREF to synchronise the PLL. It will be on the rising edge if the bit is at logic 0 and on the falling edge if the bit is at logic 1.

The bits Up and Do are used for the test, to force the charge pump current. These bits have to be logic 0 during normal use.

The bits Ip0, Ip1 and Ip2 control the charge pump current, to increase the bandwidth of the PLL, as shown in Table 5.

Table 5 Charge-pump current control

Ip2	Ip1	Ip0	CURRENT (μA)
0	0	0	6.25
0	0	1	12.5
0	1	0	25
0	1	1	50
1	0	0	100
1	0	1	200
1	1	0	400
1	1	1	700

The default programmed value is as follows:

- Charge pump current = 100 μA
- Test bits: no test mode; bits Up and Do at logic 0
- Rising edge of CKREF: bit edge at logic 0
- COAST and HSYNC inputs are active HIGH: V level and H level at logic 0.

VCO REGISTER

The bits Z2, Z1 and Z0 enable the internal resistance for the VCO filter to be selected.

Table 6 VCO register bits

Z2	Z1	Z0	RESISTANCE (kΩ)
0	0	0	high impedance
0	0	1	128
0	1	0	32
0	1	1	16
1	0	0	8
1	0	1	4
1	1	0	2
1	1	1	1

Table 7 VCO gain control

V_{CO1}	V_{CO0}	VCO gain (MHz/V)	PIXEL CLOCK FREQUENCY RANGE (MHz)
1	0	60	10 to 17
0	1	30	17 to 35
1	0	60	35 to 60
1	1	100	60 to 100

The bits V_{CO1} and V_{CO0} control the VCO gain.

The default programmed value is as follows:

- Internal resistance = 16 kΩ
- VCO gain = 15 MHz/V.

DIVIDER REGISTER

This register controls the PLL frequency. The bits are the LSB bits.

The default programmed value is 0011 0010 0000 = 800.

The MSB bits (Di11, Di10, Di9) and the LSB bit (Di0) have to be programmed before the bits Di8 to Di1 to have the required divider ratio. The bit Di0 is used for the parity divider number = Di0 = 0 = even number Di0 = 1 = odd number. It should be noted that if the I²C-bus programming is done in mode = 1 and the bit Di0 has to be toggled, then the registers have to be loaded twice to have the update divider ratio.

POWER-DOWN MODE

- When the supply is completely switched off, the registers are set to their default values; in that event they have to be reprogrammed if the required settings are different (e.g. through an EEPROM)
- When the device is in power-down mode, the previously programmed register values remain unaffected.

PHASEA AND PHASEB REGISTERS

The bit Cka is logic 0 when the used clock is the PLL clock, and logic 1 when the used clock is the external clock.

The bit Ckb is logic 0 when the second clock is not used.

The bits Pa4 to Pa0 and Pb4 to Pb0 are used to program the phase shift for the clock, CKADCO, CKAO and CKBO (see Table 8).

Table 8 Phase registers bits

Pa4, Pb4	Pa3, Pb3	Pa2, Pb2	Pa1, Pb1	Pa0, Pb0	PHASE SHIFT (°)
0	0	0	0	0	0
0	0	0	0	1	11.25
↓	↓	↓	↓	↓	↓
↓	↓	↓	↓	↓	↓
1	1	1	1	0	337.5
1	1	1	1	1	348.75

The default programmed value is as follows:

- No external clock: CKA at logic 0
- No use of the second clock: CKB at logic 0
- Phase shift for CKAO and CKADCO = 0°
- Phase shift for CKBO = 0°.

I²C-bus protocol

Table 9 I²C-bus address

A7	A6	A5	A4	A3	A2	A1	A0
1	0	0	1	1	ADD2	ADD1	0

The I²C-bus address of the circuit is 10011 xx0.

Bits A2 and A1 are fixed by the potential on pins ADD1 and ADD2. Thus, four TDA8752s can be used on the same system, using the addresses for ADD1 and ADD2 with the I²C-bus. The A0 bit must always be equal to logic 0 because it is not possible to read the data in the register. The timing and protocol for the I²C-bus are standard. Two sequences are available, see Tables 10 and 11.

Table 10 Address sequence for mode 0

S	IC ADDRESS	ACK	SUBADDRESS REGISTER1	ACK	DATA REGISTER1 (see Table 1)	ACK	SUBADDRESS REGISTER2	ACK	....	P

Where: S = START condition, ACK = acknowledge and P = STOP condition.

Table 11 Address sequence for mode 1

S	IC ADDRESS	ACK	SUBADDRESS xxx1 1111	ACK	DATA REGISTER1 (see Table 1)	ACK	DATA REGISTER2	ACK	....	P

Where: S = START condition, ACK = acknowledge and P = STOP condition.

3-wire protocol

For the 3-wire serial bus the first byte refers to the register address which is programmed. The second byte refers to the data to be sent to the chosen register (see Table 1). The acquisition is achieved via SEN.

Using the 3-wire interface, an indefinite number of ICs can operate on the same system. Pin SEN is used to validate the circuits.

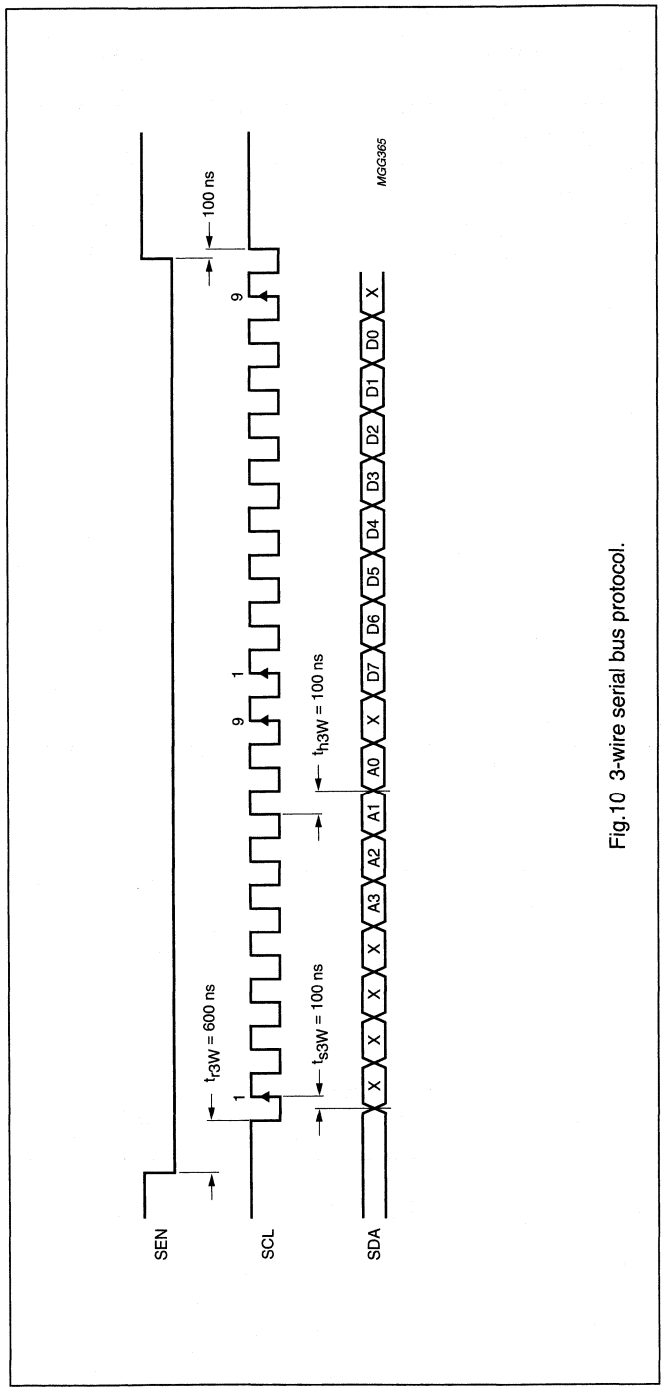


Fig.10 3-wire serial bus protocol.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage		−0.3	+7.0	V
V_{CCD}	digital supply voltage		−0.3	+7.0	V
V_{DDD}	logic input voltage		−0.3	+7.0	V
V_{CCO}	output stages supply voltage		−0.3	+7.0	V
ΔV_{CC}	supply voltage differences				
	$V_{CCA} - V_{CCD}$		−1.0	+1.0	V
	$V_{CCO} - V_{CCD}$, $V_{CCO} - V_{DDD}$		−1.0	+1.0	V
	$V_{CCA} - V_{DDD}$, $V_{CCD} - V_{DDD}$		−1.0	+1.0	V
	$V_{CCA} - V_{CCO}$		−1.0	+1.0	V
$V_{i(RGB)}$	RGB input voltage range	referenced to AGND	−0.3	+7.0	V
I_o	output current		−	10	mA
T_{stg}	storage temperature		−55	+150	°C
T_{amb}	operating ambient temperature		0	70	°C
T_j	junction temperature		−	150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	52	K/W

CHARACTERISTICS

V_{CCA} = V11 (or V19, V27 or V99) referenced to AGND (V13, V21, V29 or V96 = 4.75 to 5.25 V; V_{CCD} = V95 referenced to DGND (V86) = 4.75 to 5.25 V; V_{DDD} = V40 referenced to V_{SSD} (V41) = 4.75 to 5.25 V; V_{CCO} = V59 (or V69, V79 or V85) referenced to OGND (V48, V60, V70 or V82) = 4.75 to 5.25 V; AGND, DGND, OGND and V_{SSD} short circuited together. T_{amb} = 0 to 70 °C; typical values measured at $V_{CCA} = V_{DDD} = V_{CCD} = V_{CCO}$ = 5 V and T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{DDD}	logic supply voltage		4.75	5.0	5.25	V
V_{CCO}	output stages supply voltage		4.75	5.0	5.25	V
I_{CCA}	analog supply current		–	120	–	mA
I_{DDD}	logic supply current for I^2C-bus and 3-wire		–	1.0	–	mA
I_{CCD}	digital supply current		–	40	–	mA
I_{CCO}	output stages supply current	ramp input; f_{CLK} = 100 MHz	–	6	–	mA
$I_{CCO(PLL)}$	output PLL supply current		–	5	–	mA
$I_{CCA(PLL)}$	analog PLL supply current		–	28	–	mA
ΔV_{CC}	supply voltage differences					
	$V_{CCA} - V_{CCD}$		–0.25	–	+0.25	V
	$V_{CCO} - V_{CCD}$, $V_{CCO} - V_{DDD}$		–0.25	–	+0.25	V
	$V_{CCA} - V_{DDD}$, $V_{CCD} - V_{DDD}$		–0.25	–	+0.25	V
	$V_{CCA} - V_{CCO}$		–0.25	–	+0.25	V
P_{tot}	total power consumption	ramp input; f_{CLK} = 100 MHz	–	1.0	–	W
P_{pd}	power consumption in power-down mode		–	87	–	mW
R, G and B amplifiers						
B	bandwidth	–3 dB; T_{amb} = 25 °C	250	–	–	MHz
t_{set}	settling time of the block ADC plus AGC	full-scale (black-to-white) transition; input signal settling time < 1 ns; 1 to 99%; T_{amb} = 25 °C	–	4.5	6	ns
$G_{NCOARSE}$	coarse gain range	V_{ref} = 2.5 V; minimum coarse gain register; code = 32; (see Fig.8)	–	–1.67	–	dB
		maximum coarse gain register; code = 99; (see Fig.8)	–	8	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
G_{FINE}	fine gain correction range	fine register input code = 0; (see Fig.9)	–	0	–	dB
		fine register input code = 31; (see Fig.9)	–	−0.5	–	dB
$\Delta G_{amp}/T$	amplifier gain stability as a function of temperature	V_{ref} = 2.5 V with 100 ppm/°C maximum variation	–	–	200	ppm/°C
I_{GC}	gain current		–	±20	–	µA
t_{stab}	amplifier gain adjustment speed	HSYNC active; capacitors on pins 8, 16 and 24 = 22 nF	–	25	–	mdB/µs
$V_{i(p-p)}$	input voltage range (peak-to-peak value)	corresponding to full-scale output	0.4	–	1.2	V
$t_{r(Vi)}$	input voltage rise time	f_i = 100 MHz; square wave	–	–	2.5	ns
$t_{f(Vi)}$	input voltage fall time	f_i = 100 MHz; square wave	–	–	2.5	ns
$G_{E(rms)}$	channel-to-channel gain matching (RMS value)	maximum coarse gain; T_{amb} = 25 °C	–	1	–	%
		minimum coarse gain; T_{amb} = 25 °C	–	2	–	%
Clamps						
P_{CLP}	precision	black level noise on RGB channels = 10 mV (max.) (RMS value); T_{amb} = 25 °C	−1	–	+1	LSB
t_{COR1}	clamp correction time to within ±10 mV	±100 mV black level input variation; clamp capacitor = 4.7 nF	–	–	300	ns
t_{COR2}	clamp correction time to less than 1 LSB	±100 mV black level input variation; clamp capacitor = 4.7 nF	–	–	10	lines
$t_{W(CLP)}$	clamp pulse width		500	–	2000	ns
CLP_E	channel-to-channel clamp matching		−1	–	+1	LSB
A_{off}	code clamp reference	clamp register input code = 0	–	−63.5	–	LSB
		clamp register input code = 255	–	64	–	LSB
Phase-locked loop						
$j_{PLL(rms)}$	long term PLL jitter (RMS value)	f_{CLK} = 60 MHz; see Table 13	–	450	–	ps
		f_{CLK} = 100 MHz; see Table 13	–	360	–	ps
DR	divider ratio		100	–	4095	
f_{ref}	reference clock frequency range		15	–	280	kHz
f_{PLL}	output clock frequency range		12	–	100	MHz
$t_{COASTmax}$	maximum coast mode time		–	–	40	lines

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{recap}	PLL recapture time	when coast mode is aborted	–	3	–	lines
t_{cap}	PLL capture time	in start-up conditions	–	–	5	ms
Φ_{step}	phase shift step	T_{amb} = 25 °C	–	11.25	–	deg
ADCs						
f_s	maximum sampling frequency	TDA8752/6	60	–	–	MHz
		TDA8752/8	100	–	–	MHz
INL	DC integral non linearity	from IC analog input to digital output; ramp input; f_{CLK} = 100 MHz	–	±0.5	±1.5	LSB
DNL	DC differential non linearity	from IC analog input to digital output; ramp input; f_{CLK} = 100 MHz	–	±0.5	±1.0	LSB
ENOB	effective number of bits	from IC analog input to digital output; 10 kHz sine wave input; ramp input; f_{CLK} = 100 MHz; note 1	–	7.4	–	bits
Signal-to-noise ratio						
S/N	signal-to-noise ratio	maximum gain; f_{CLK} = 100 MHz	–	45	–	dB
		minimum gain; f_{CLK} = 100 MHz	–	44	–	dB
Spurious free dynamic range						
SFDR	spurious free dynamic range	maximum gain; f_{CLK} = 100 MHz	–	60	–	dB
		minimum gain; f_{CLK} = 100 MHz	–	60	–	dB
Clock timing output (CKADCO, CKBO and CKAO)						
η_{ext}	ADC clock duty cycle	100 MHz output	45	50	55	%
$f_{CLK(max)}$	maximum clock frequency		100	–	–	MHz
Clock timing input (CKEXT)						
$f_{CLK(max)}$	maximum clock frequency		100	–	–	MHz
t_{CPH}	clock pulse width HIGH		3.6	–	–	ns
t_{CPL}	clock pulse width LOW		4.5	–	–	ns
$t_{d(CLKO)}$	delay from CKEXT to CKADCO	INV set to LOW	13.6	14.7	15.2	ns
		INV set to HIGH	–	$\frac{t_{CLK}}{2}$	–	ns
Δt_{sample}	time difference between samples	operating in the same supply and temperature condition	–	0.1	0.3	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Data timing (see Fig.11); **f_{CLK} = 100 MHz; C_L = 10 pF**; note 2						
$t_{d(s)}$	sampling delay time	referenced to CKADCO	–	–	–	ns
$t_{d(o)}$	output delay time		–	–3.3	–2.6	ns
$t_{h(o)}$	output hold time		4.6	5.5	–	ns
3-state output delay time; (see Fig.12)						
t_{dZH}	output enable HIGH		–	12	–	ns
t_{dZL}	output enable LOW		–	10	–	ns
t_{dHZ}	output disable HIGH		–	50	–	ns
t_{dLZ}	output disable LOW		–	65	–	ns
PLL clock output						
V_{OL}	LOW-level output voltage	I_o = 1 mA	–	0.3	0.8	V
V_{OH}	HIGH-level output voltage	I_o = – 1 mA	2.4	3.5	–	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	–	2	–	mA
I_{OH}	HIGH-level output current	V_{OH} = 2.7 V	–	–0.4	–	mA
ADC data outputs						
V_{OL}	LOW-level output voltage	I_o = 1 mA	–	0	0.8	V
V_{OH}	HIGH-level output voltage	I_o = – 1 mA	2.4	V_{CCD}	–	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	–	2	–	mA
I_{OH}	HIGH-level output current	V_{OH} = 2.7 V	–	–0.5	–	mA
TTL digital inputs (CKREF, COAST, CKEXT, INV, HSYNC and CLP)						
V_{IL}	LOW level input voltage		–	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	–	V
I_{IL}	LOW level input current	V_{IL} = 0.4 V	400	–	–	µA
I_{IH}	HIGH level input current	V_{IH} = 2.7 V	–	–	100	µA
Z_i	input impedance		–	4	–	kΩ
C_i	input capacitance		–	4.5	–	pF
3-wire serial bus						
t_{reset}	reset time of the chip before 3-wire communication		–	600	–	ns
t_{su}	data set-up time		–	100	–	ns
t_h	data hold time		–	100	–	ns
I²C-bus; see note 3						
f_{SCL}	clock frequency		0	–	100	kHz
t_{BUF}	time the bus must be free before new transmission can start		4.7	–	–	µs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{HD;STA}$	start condition hold time		4.0	–	–	µs
$t_{SU;STA}$	start condition set-up time	repeated start	4.7	–	–	µs
t_{CKL}	LOW level clock period		4.7	–	–	µs
t_{CKH}	HIGH level clock period		4.0	–	–	µs
$t_{SU;DAT}$	data set-up time		250	–	–	ns
$t_{HD;DAT}$	data hold time		0	–	–	ns
t_r	SDA and SCL rise time	for f_{SCL} = 100 kHz	–	–	1.0	µs
t_f	SDA and SCL fall time	for f_{SCL} = 100 kHz	–	–	300	ns
$t_{SU;STOP}$	stop condition set-up time		4.0	–	–	µs
$C_{L(bus)}$	capacitive load for each bus line		–	–	400	pF

Notes to the characteristics

1. Effective bits are obtained via a Fast Fourier Transform (FFT) treatment taking 8000 acquisition points per equivalent fundamental period. The calculation takes into account all harmonics and noise up to half clock frequency (NYQUIST frequency). Conversion-to-noise ratio: S/N = EB × 6.02 + 1.76 dB.
2. Output data acquisition is available after the maximum delay time $t_{d(o)}$, which is the time during which the data is available. All the timings are given for a 10 pF capacitive load. A higher load can be used but the timing must then be rechecked.
3. The I²C-bus timings are given for a frequency of 100 kbit/s (100 kHz). This bus can be used at a frequency of 400 kbit/s (400 kHz).

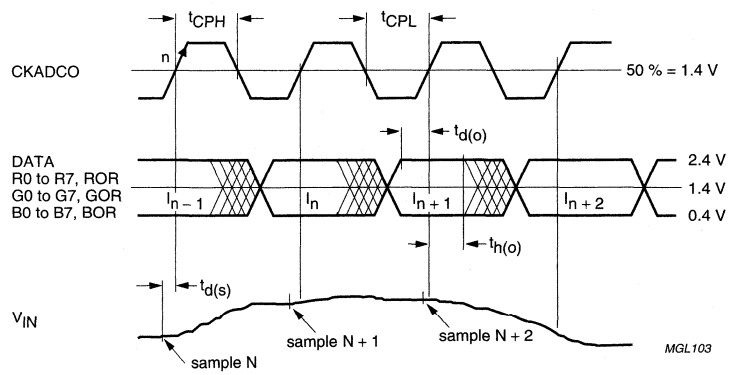
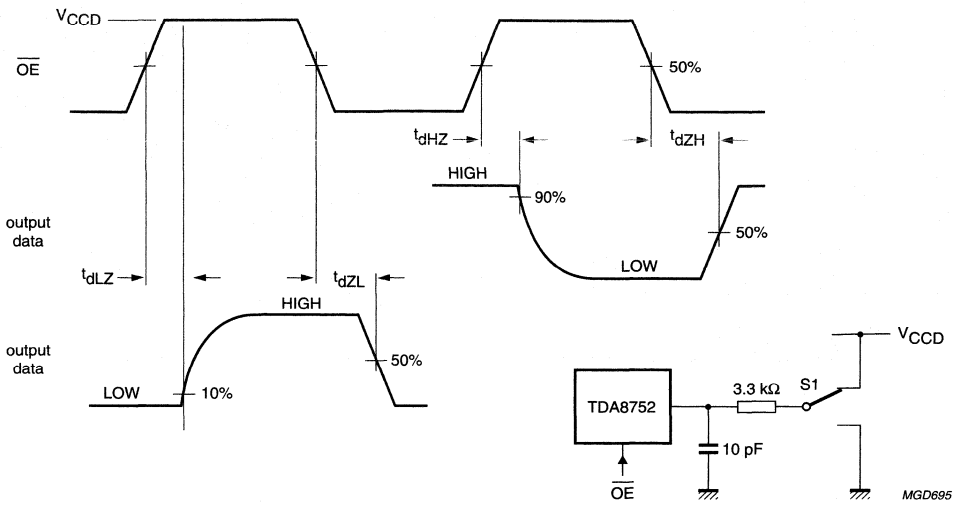


Fig.11 Timing diagram.



$t_{\overline{OE}}$ = 100 kHz.

Fig.12 Timing diagram and test conditions of 3-state output delay time.

Table 12 Test conditions for Fig.12

TEST	SWITCH S1
t_{dLZ}	V_{CCD}
t_{dZl}	V_{CCD}
t_{dHZ}	GND
t_{dZH}	GND

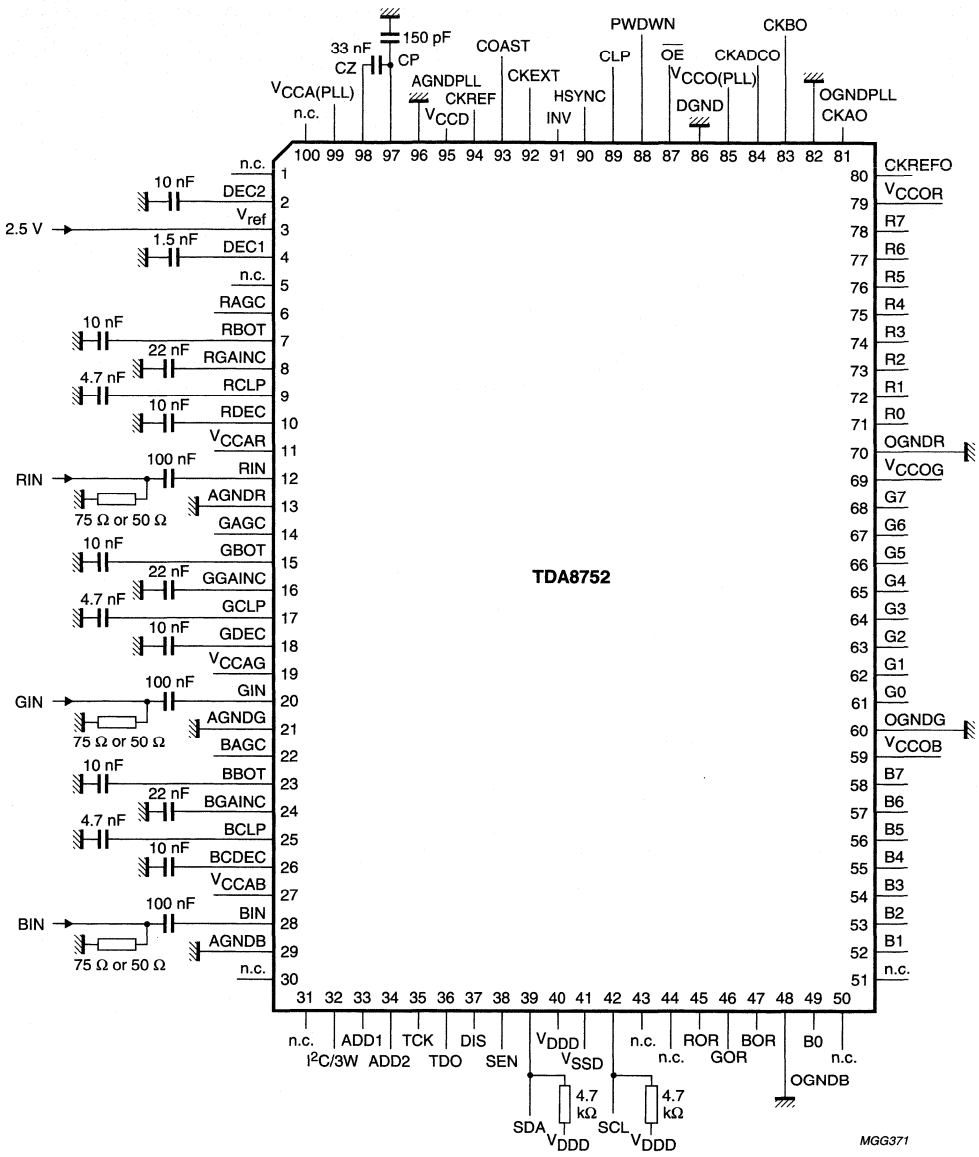
APPLICATION INFORMATION

Table 13 Examples of PLL settings and performances; note 1

VIDEO STANDARDS	f_{ref} (kHz)	f_{CLK} (MHz)	N	KO (MHz/V)	CZ (nF)	CP (nF)	I_P (μA)	Z (kΩ)	LONG TIME JITTER[2]		PLL PHASE DRIFT[3] (ns)
									ps (RMS)	ns (p-p)	
CGA: 640 × 200	15.75	14.3	912	15	150	1	200	4	–	–	1.2
VGA: 640 × 480	31.5	25.2	800	30	150	1	400	2	610	3.6	0.7
VESA: 800 × 600	48.08	50	1040	60	150	1	700	1	480	2.9	0.55
VESA: 1024 × 768	60.02	78.8	1312	100	150	1	700	1	380	2.3	0.3
SUN: 1152 × 900	66.67	100	1500	100	150	1	700	1	360	2.2	0.3

Notes

1. Values measured at $V_{CCA} = V_{DDD} = V_{CCD} = V_{CCO} = 5$ V and $T_{amb} = 25$°C.
2. PLL long-term time jitter is measured at the end of the video line, where it is at its maximum.
3. Measured between 0 and 70 °C.



All supply pins have to be decoupled, with two capacitors:
one for high frequencies (approximately 1 nF) and one for the low frequencies (approximately 100 nF or higher).

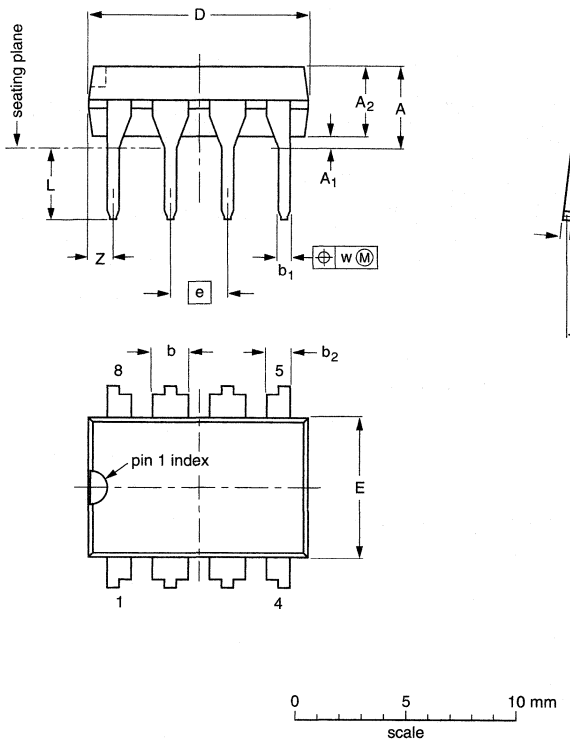
Fig.13 Application diagram.

PACKAGE INFORMATION

INDEX

DIP

DIP8: plastic dual in-line package; 8 leads (300 mil) SOT97-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

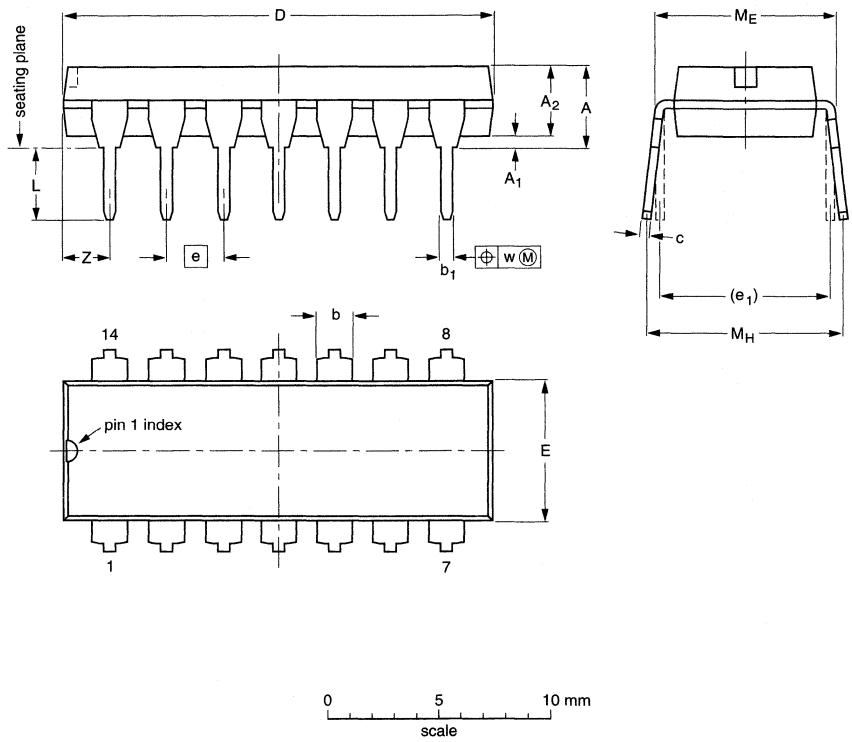
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D(1)	E(1)	e	e_1	L	M_E	M_H	w	Z(1) max.
mm	4.2	0.51	3.2	1.73 1.14	0.53 0.38	1.07 0.89	0.36 0.23	9.8 9.2	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	1.15
inches	0.17	0.020	0.13	0.068 0.045	0.021 0.015	0.042 0.035	0.014 0.009	0.39 0.36	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.045

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT97-1	050G01	MO-001AN				~~92-11-17~~ 95-02-04

DIP14: plastic dual in-line package; 14 leads (300 mil) **SOT27-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

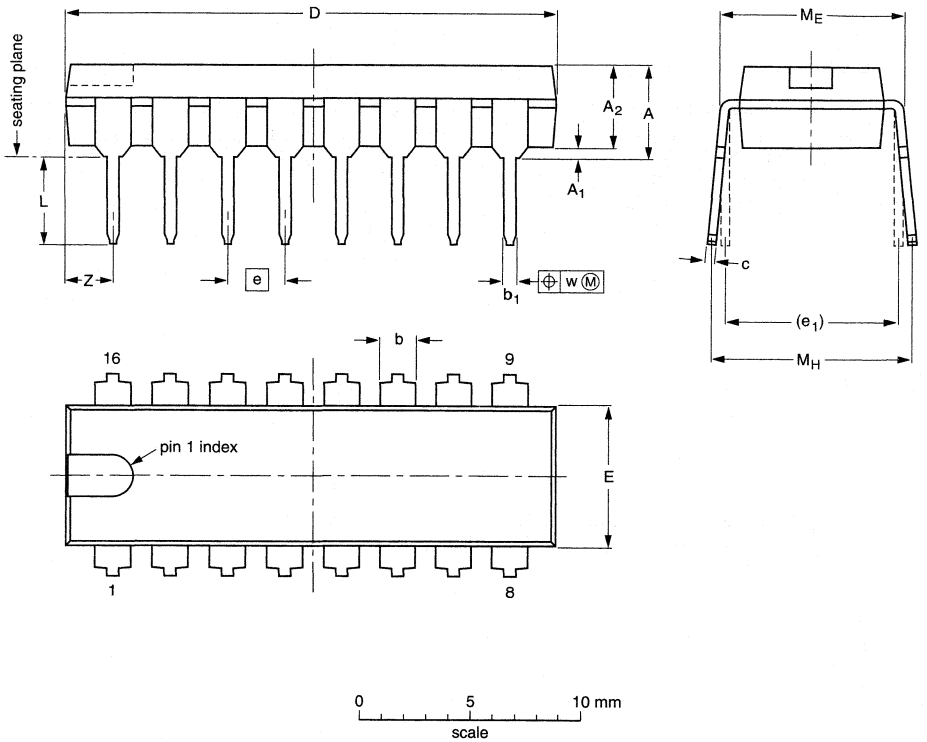
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.020	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT27-1	050G04	MO-001AA				~~92-11-17~~ 95-03-11

DIP16: plastic dual in-line package; 16 leads (300 mil); long body SOT38-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

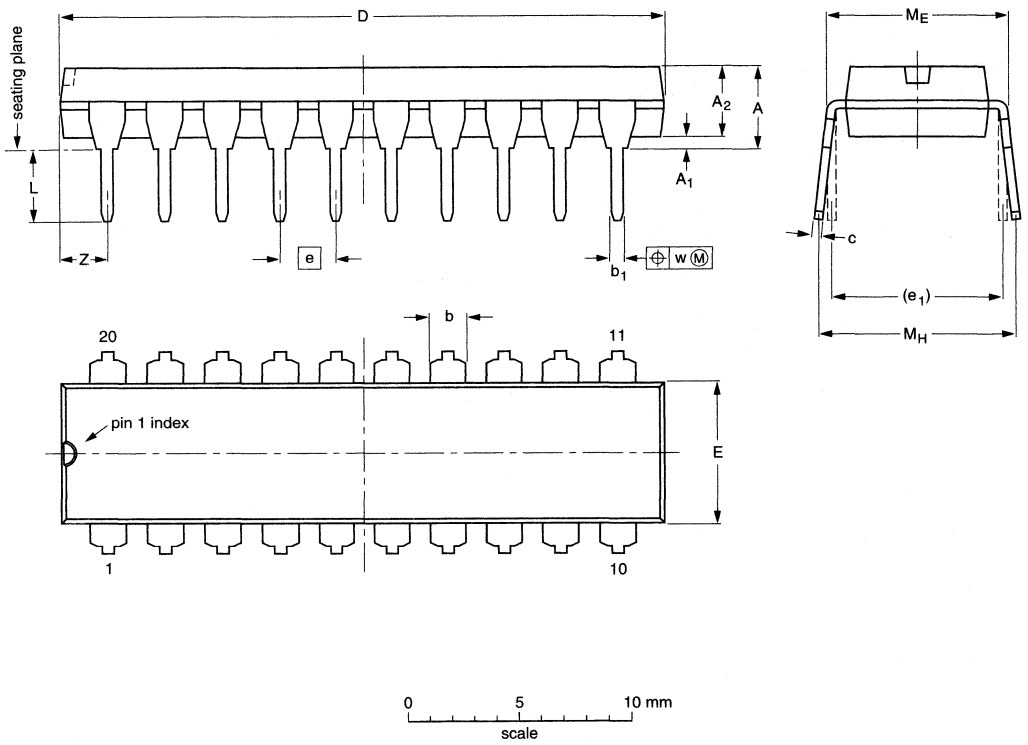
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.7	1.40 1.14	0.53 0.38	0.32 0.23	21.8 21.4	6.48 6.20	2.54	7.62	3.9 3.4	8.25 7.80	9.5 8.3	0.254	2.2
inches	0.19	0.020	0.15	0.055 0.045	0.021 0.015	0.013 0.009	0.86 0.84	0.26 0.24	0.10	0.30	0.15 0.13	0.32 0.31	0.37 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-1	050G09	MO-001AE				~~92-10-02~~ 95-01-19

DIP20: plastic dual in-line package; 20 leads (300 mil) **SOT146-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

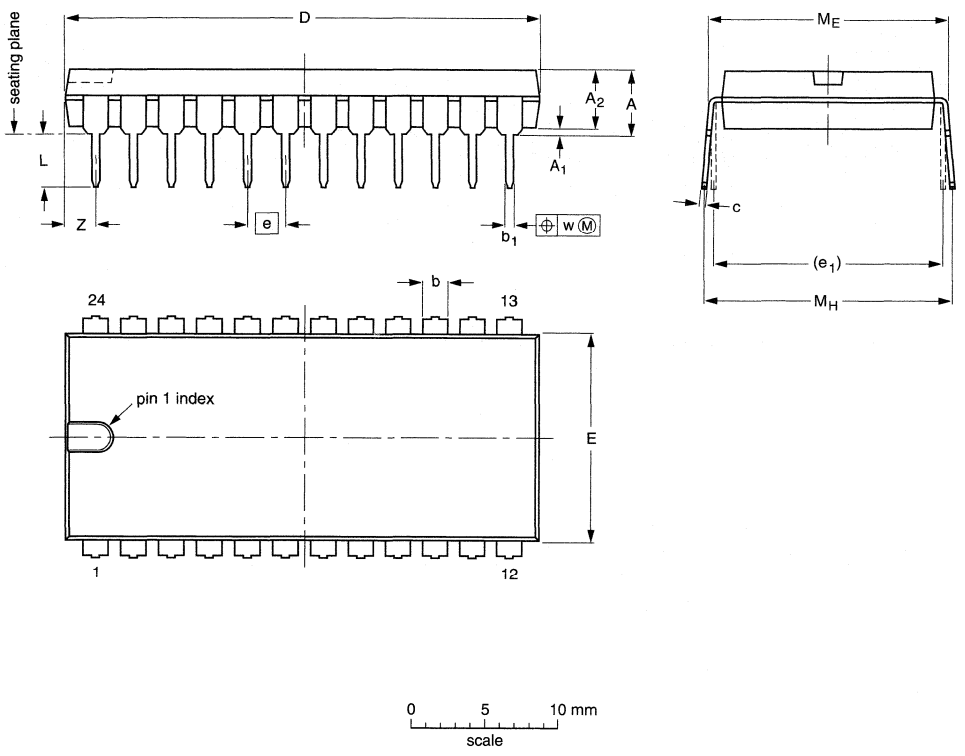
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			~~92-11-17~~ 95-05-24

DIP24: plastic dual in-line package; 24 leads (600 mil)

SOT101-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

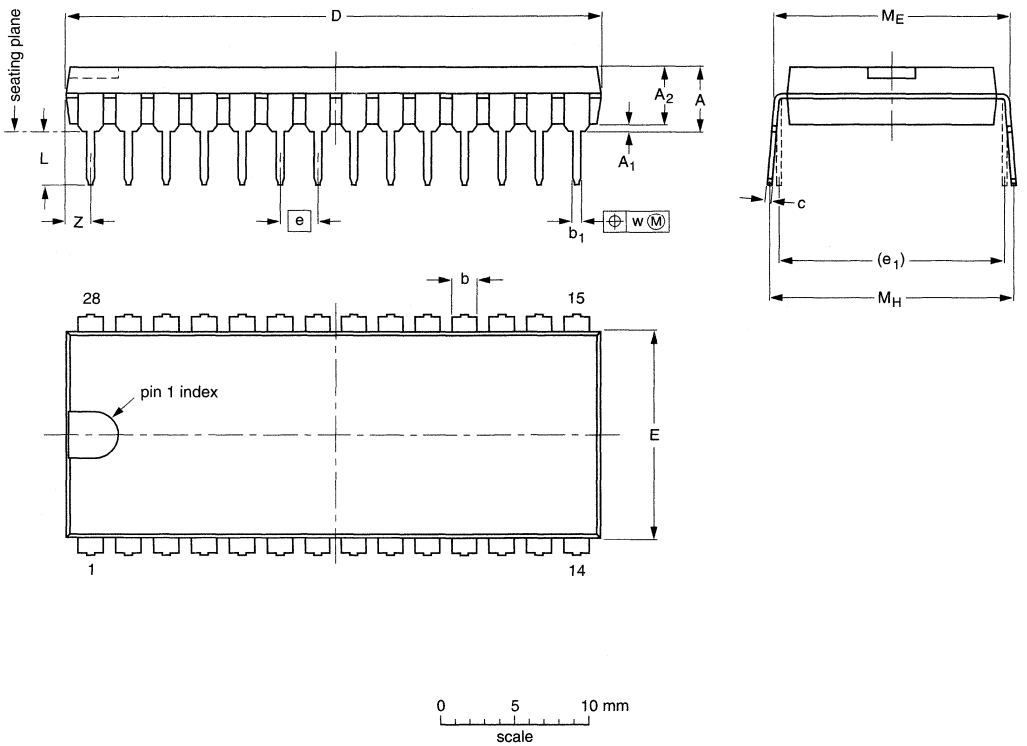
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.1	0.51	4.0	1.7 1.3	0.53 0.38	0.32 0.23	32.0 31.4	14.1 13.7	2.54	15.24	3.9 3.4	15.80 15.24	17.15 15.90	0.25	2.2
inches	0.20	0.020	0.16	0.066 0.051	0.021 0.015	0.013 0.009	1.26 1.24	0.56 0.54	0.10	0.60	0.15 0.13	0.62 0.60	0.68 0.63	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT101-1	051G02	MO-015AD				~~92-11-17~~ 95-01-23

DIP28: plastic dual in-line package; 28 leads (600 mil) SOT117-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

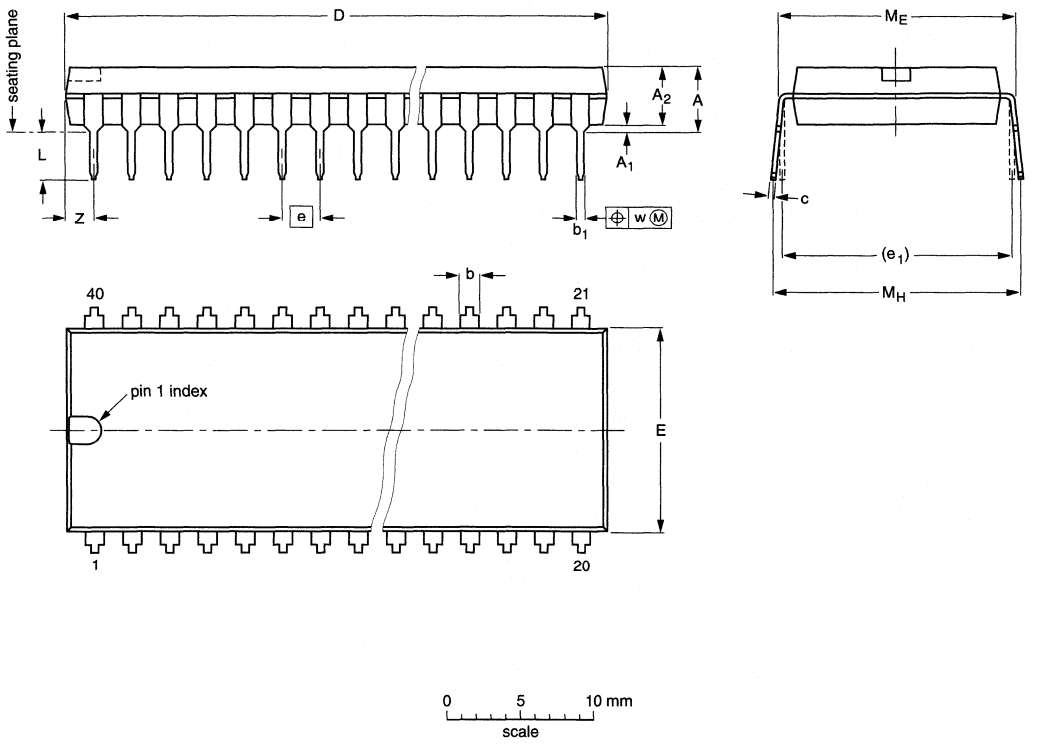
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.1	0.51	4.0	1.7 1.3	0.53 0.38	0.32 0.23	36.0 35.0	14.1 13.7	2.54	15.24	3.9 3.4	15.80 15.24	17.15 15.90	0.25	1.7
inches	0.20	0.020	0.16	0.066 0.051	0.020 0.014	0.013 0.009	1.41 1.34	0.56 0.54	0.10	0.60	0.15 0.13	0.62 0.60	0.68 0.63	0.01	0.067

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT117-1	051G05	MO-015AH				~~92-11-17~~ 95-01-14

DIP40: plastic dual in-line package; 40 leads (600 mil) **SOT129-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	$D^{(1)}$	$E^{(1)}$	e	e_1	L	M_E	M_H	w	$Z^{(1)}$ max.
mm	4.7	0.51	4.0	1.70 1.14	0.53 0.38	0.36 0.23	52.50 51.50	14.1 13.7	2.54	15.24	3.60 3.05	15.80 15.24	17.42 15.90	0.254	2.25
inches	0.19	0.020	0.16	0.067 0.045	0.021 0.015	0.014 0.009	2.067 2.028	0.56 0.54	0.10	0.60	0.14 0.12	0.62 0.60	0.69 0.63	0.01	0.089

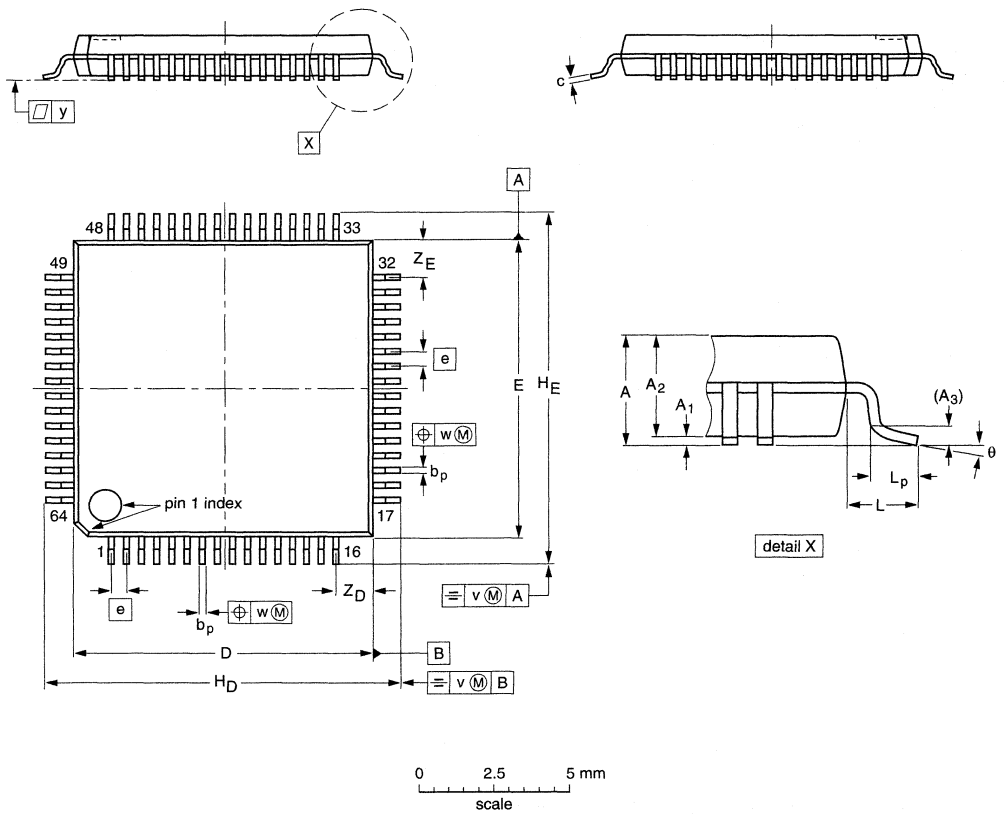
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT129-1	051G08	MO-015AJ				~~92-11-17~~ 95-01-14

LQFP

LQFP64: plastic low profile quad flat package; 64 leads; body 10 x 10 x 1.4 mm SOT314-2



DIMENSIONS (mm are the original dimensions)

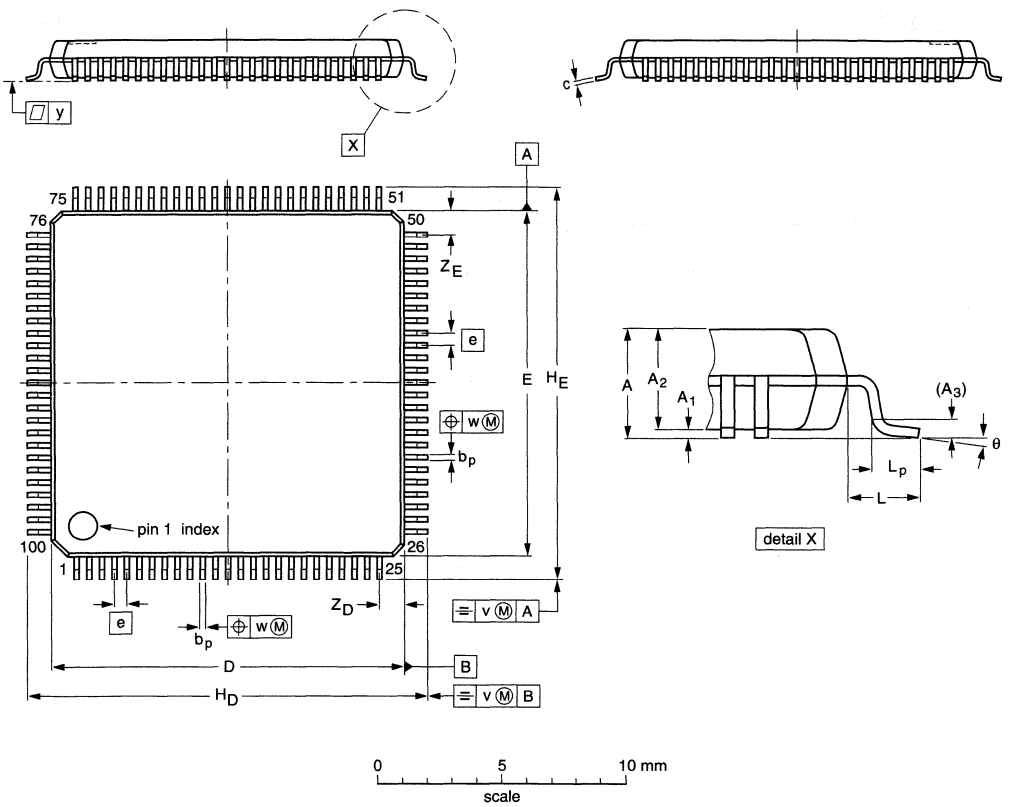
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	10.1 9.9	10.1 9.9	0.5	12.15 11.85	12.15 11.85	1.0	0.75 0.45	0.2	0.12	0.1	1.45 1.05	1.45 1.05	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT314-2						~~95-12-19~~ 97-08-01

LQFP100: plastic low profile quad flat package; 100 leads; body 14 x 14 x 1.4 mm **SOT407-1**



DIMENSIONS (mm are the original dimensions)

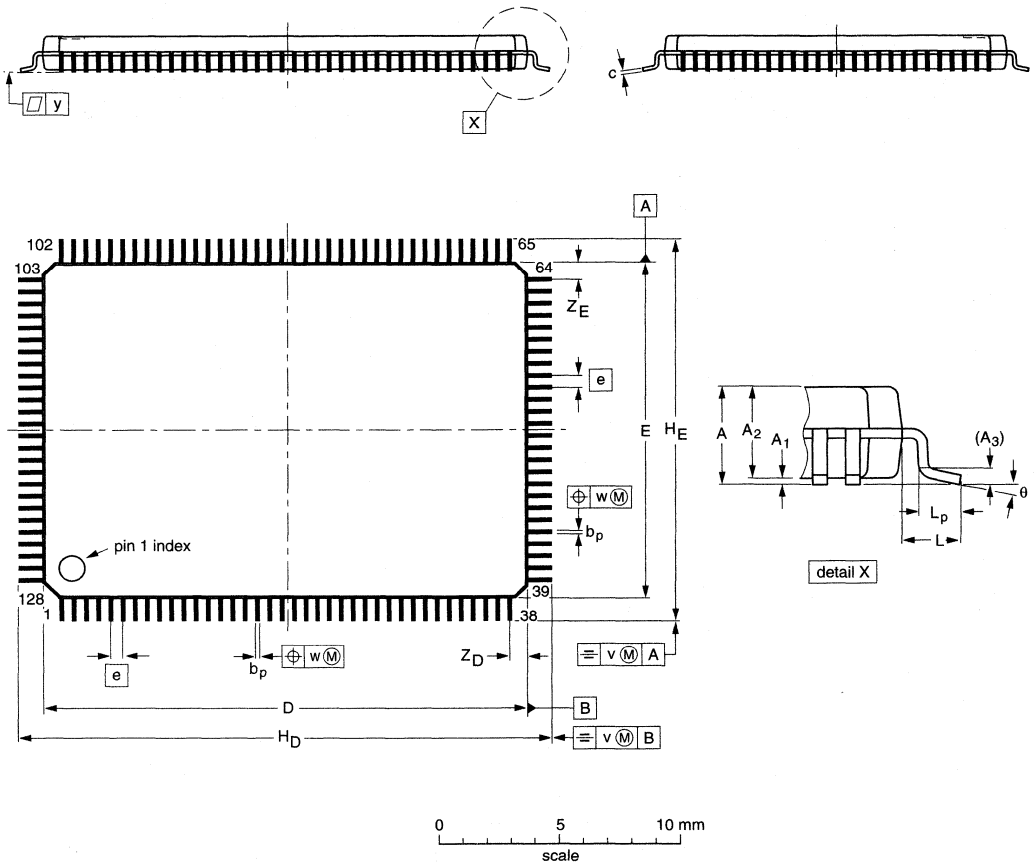
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.5 1.3	0.25	0.28 0.16	0.18 0.12	14.1 13.9	14.1 13.9	0.5	16.25 15.75	16.25 15.75	1.0	0.75 0.45	0.2	0.12	0.1	1.15 0.85	1.15 0.85	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT407-1						~~95-12-19~~ 97-08-04

LQFP128: plastic low profile quad flat package; 128 leads; body 14 x 20 x 1.4 mm **SOT425-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	20.1 19.9	14.1 13.9	0.5	22.15 21.85	16.15 15.85	1.0	0.75 0.45	0.2	0.12	0.1	0.81 0.59	0.81 0.59	7° 0°

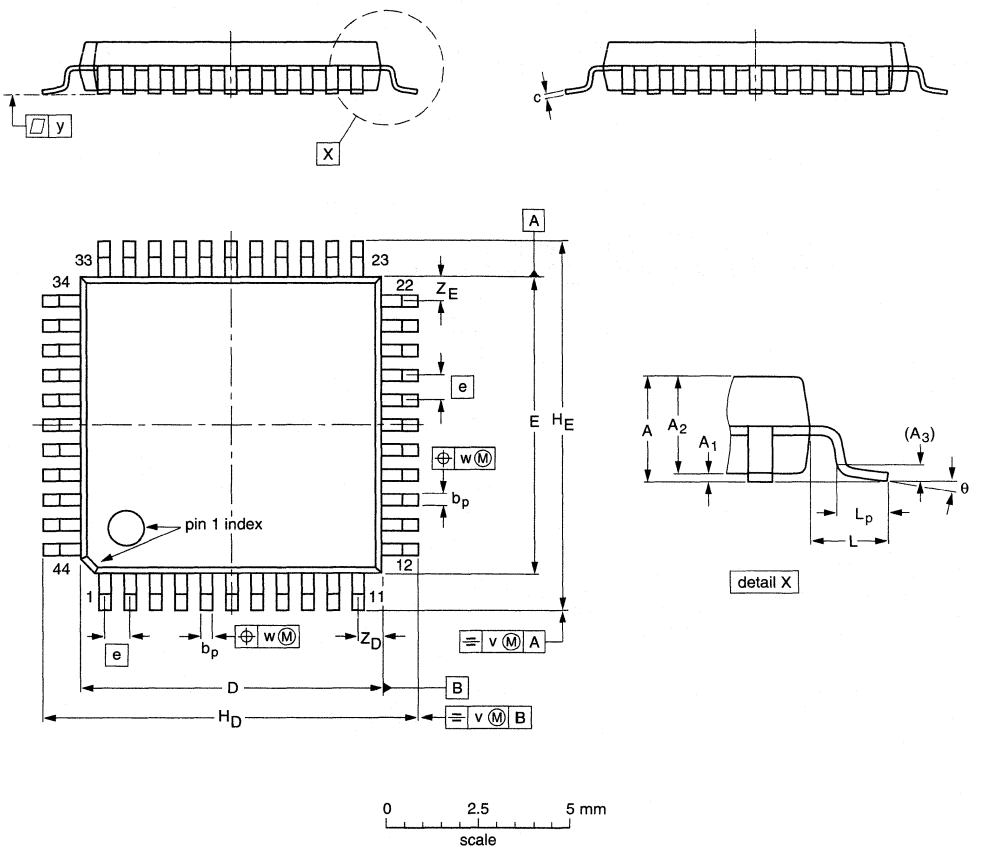
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT425-1						~~96-04-02~~ 97-08-04

QFP

QFP44: plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 x 10 x 1.75 mm SOT307-2



DIMENSIONS (mm are the original dimensions)

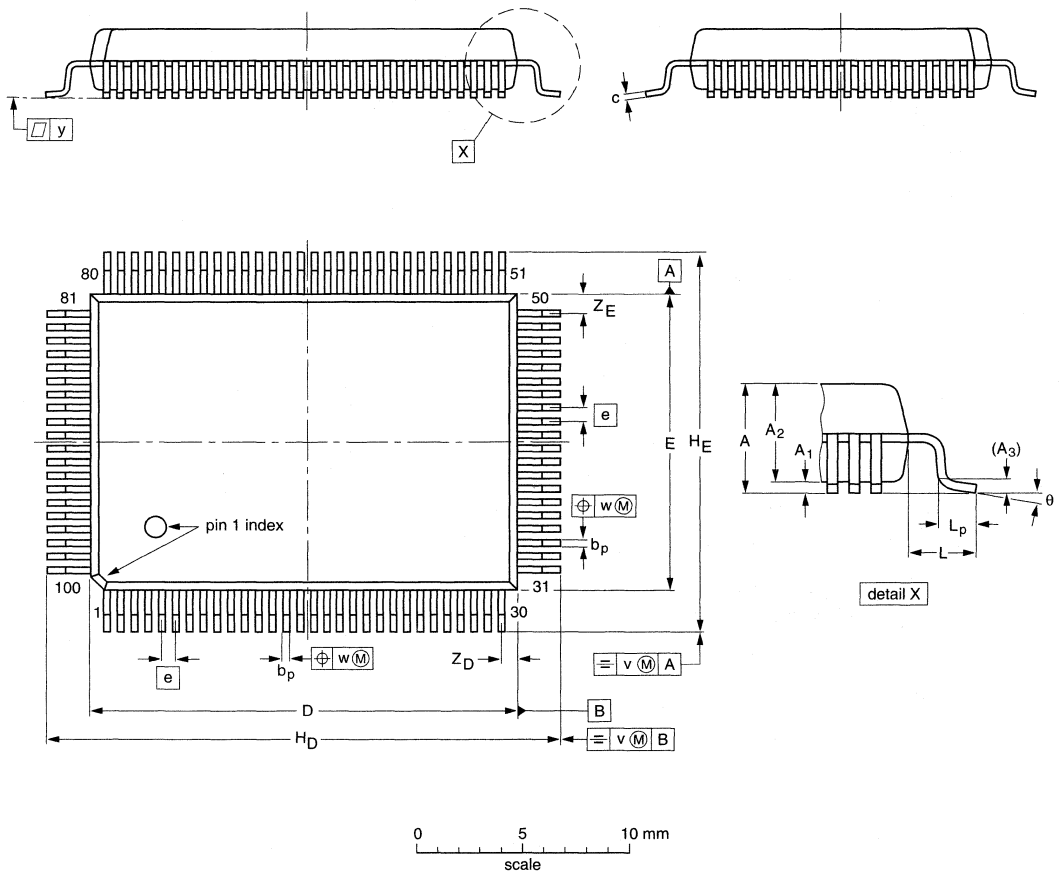
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	2.10	0.25 0.05	1.85 1.65	0.25	0.40 0.20	0.25 0.14	10.1 9.9	10.1 9.9	0.8	12.9 12.3	12.9 12.3	1.3	0.95 0.55	0.15	0.15	0.1	1.2 0.8	1.2 0.8	10^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT307-2						~~95-02-04~~ 97-08-01

QFP100: plastic quad flat package; 100 leads (lead length 1.95 mm); body 14 x 20 x 2.8 mm **SOT317-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	3.20	0.25 0.05	2.90 2.65	0.25	0.40 0.25	0.25 0.14	20.1 19.9	14.1 13.9	0.65	24.2 23.6	18.2 17.6	1.95	1.0 0.6	0.2	0.15	0.1	0.8 0.4	1.0 0.6	7° 0°

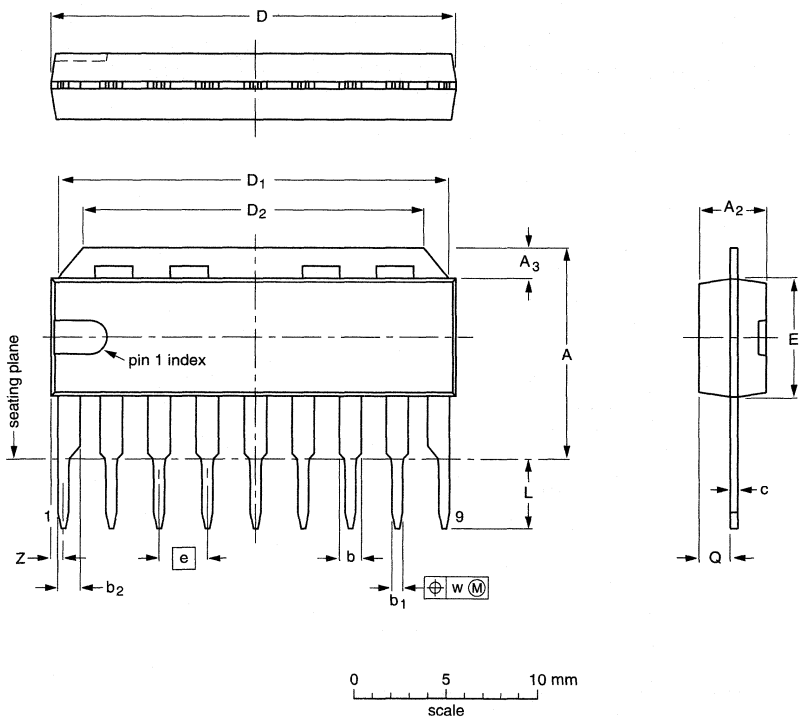
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT317-2						~~95-02-04~~ 97-08-01

SIL

SIL9MP: plastic single in-line medium power package; 9 leads SOT142-1



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_2 max.	A_3	b	b_1	b_2	c	$D^{(1)}$	D_1	D_2	$E^{(1)}$	e	L	Q	w	$Z^{(1)}$ max.
mm	12 11	3.7	1.8 1.4	1.40 1.14	0.67 0.50	1.40 1.14	0.48 0.38	21.8 21.4	21.4 20.7	18.6 18.2	6.48 6.20	2.54	3.9 3.4	1.75 1.55	0.25	1.0

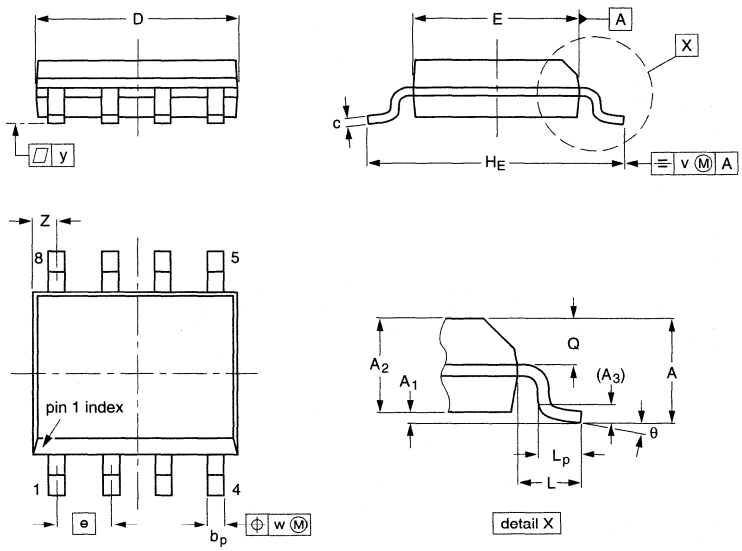
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT142-1						~~95-02-09~~ 97-12-16

SO

SO8: plastic small outline package; 8 leads; body width 3.9 mm SOT96-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

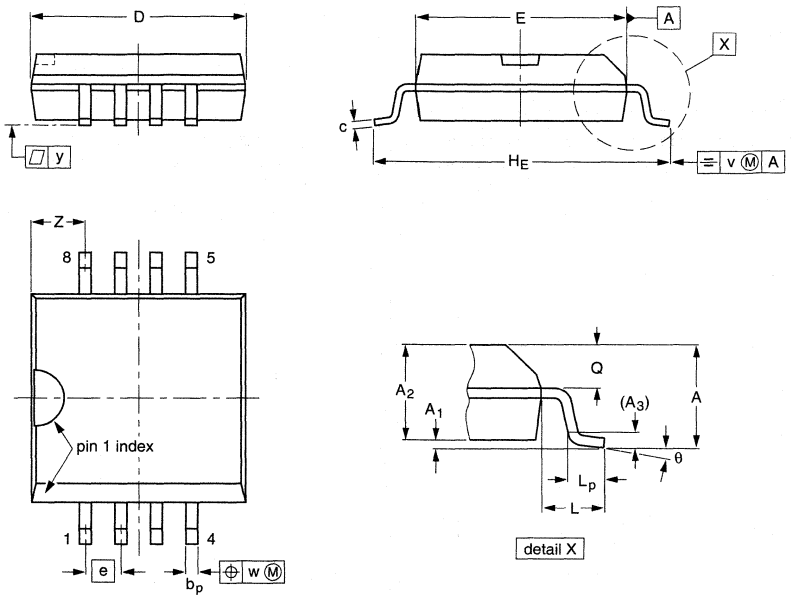
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

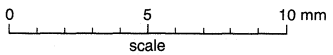
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03S	MS-012AA				~~95-02-04~~ 97-05-22

SO8: plastic small outline package; 8 leads; body width 7.5 mm SOT176-1





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

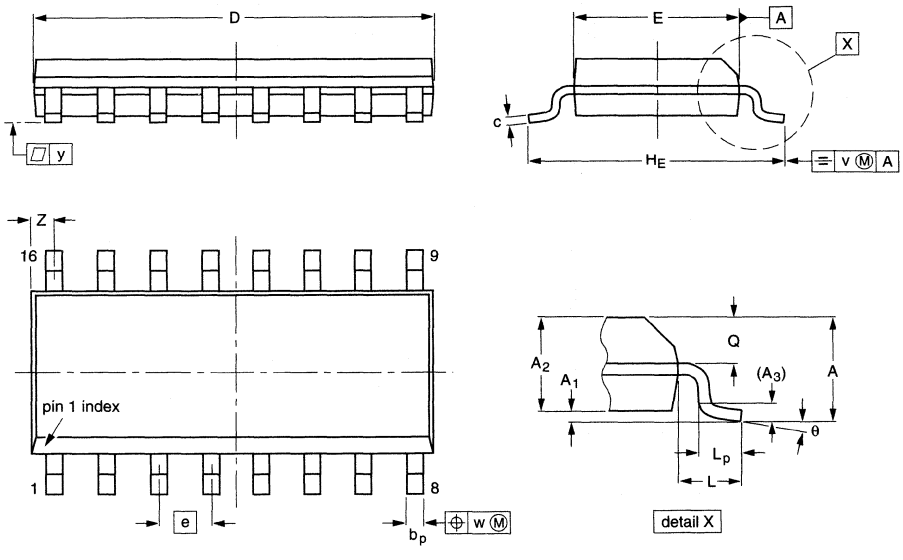
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	7.65 7.45	7.6 7.4	1.27	10.65 10.00	1.45	1.1 0.45	1.1 1.0	0.25	0.25	0.1	2.0 1.8	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.30 0.29	0.30 0.29	0.050	0.419 0.394	0.057	0.043 0.018	0.043 0.039	0.01	0.01	0.004	0.079 0.071	

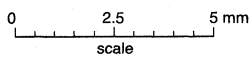
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT176-1						~~95-02-25~~ 97-05-22

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

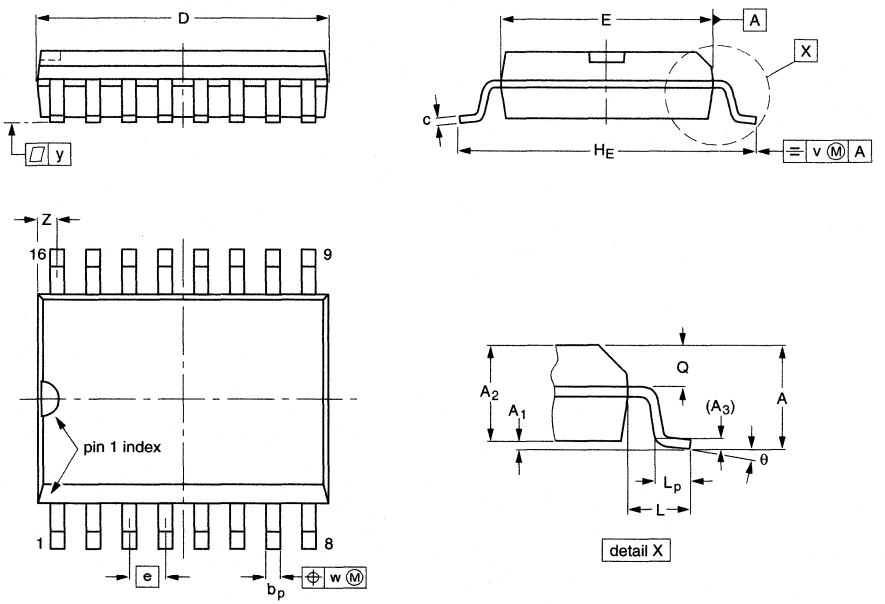
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				~~95-01-23~~ 97-05-22

SO16: plastic small outline package; 16 leads; body width 7.5 mm **SOT162-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

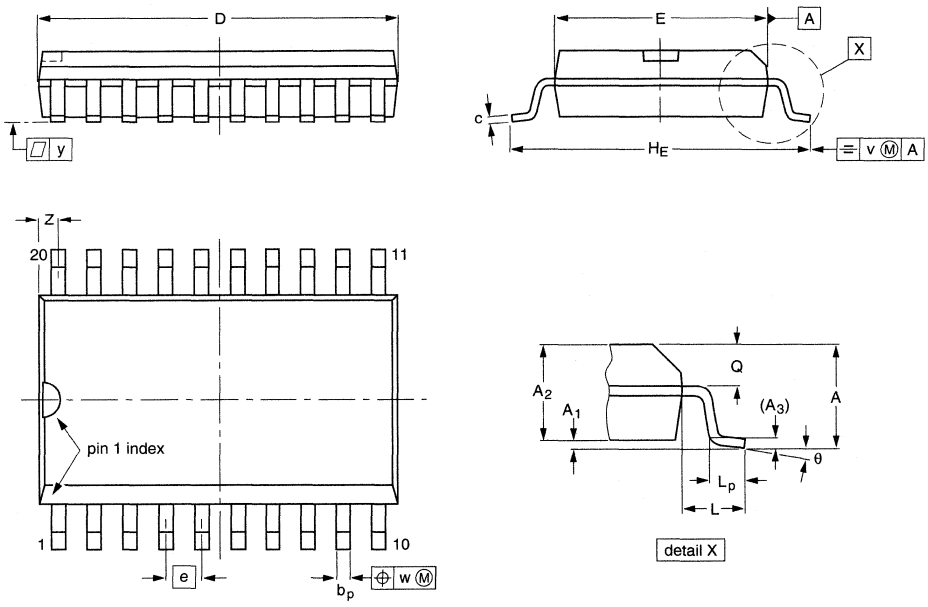
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	10.5 10.1	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.41 0.40	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT162-1	075E03	MS-013AA				~~95-01-24~~ 97-05-22

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

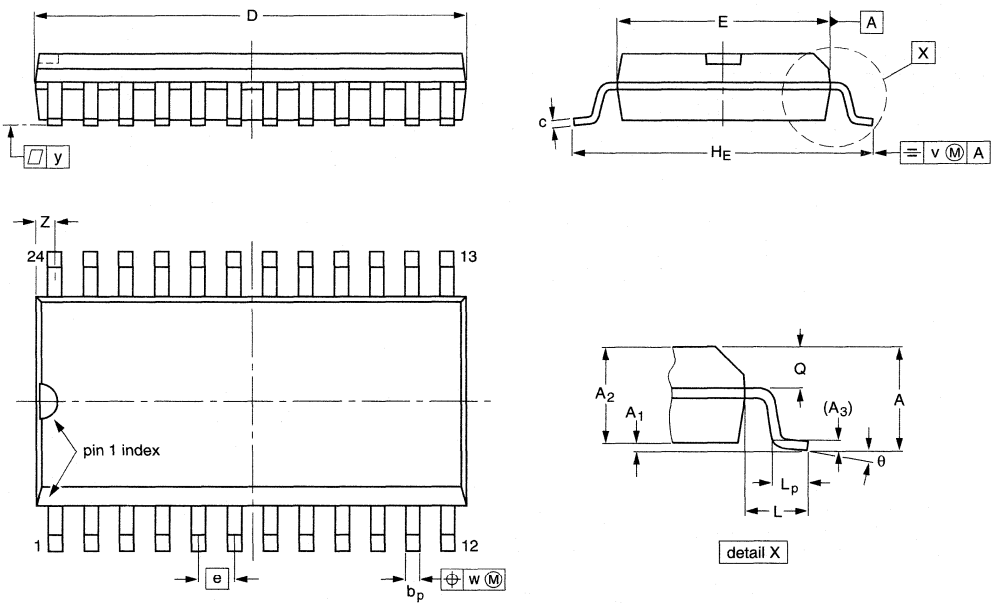
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				~~95-01-24~~ 97-05-22

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

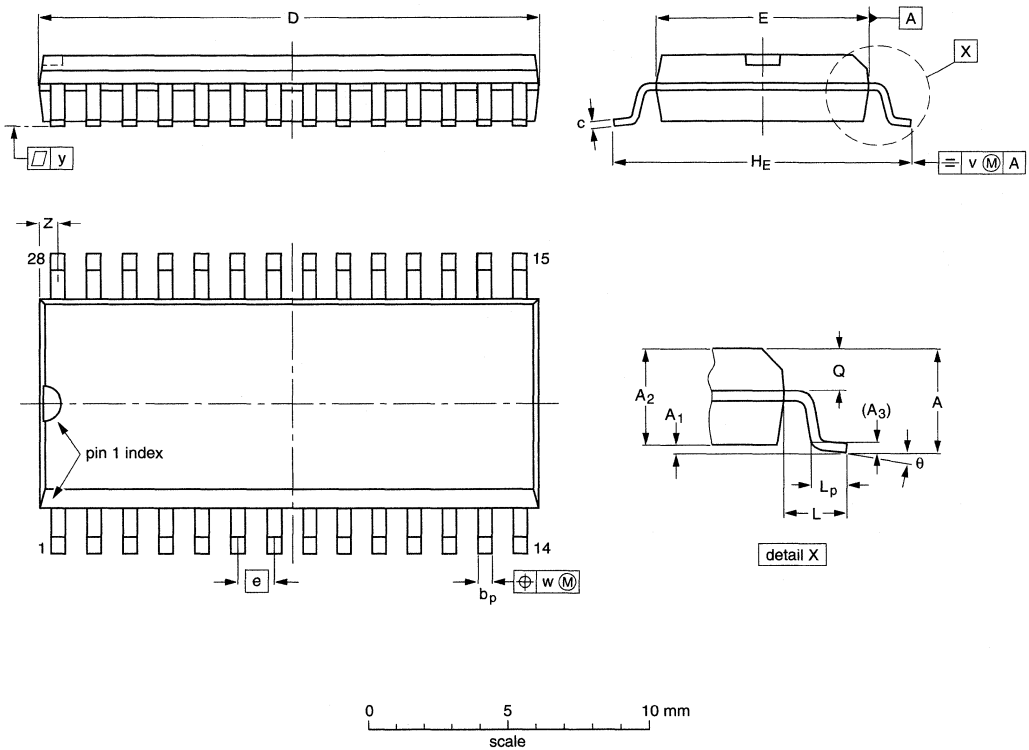
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013AD				~~95-01-24~~ 97-05-22

SO28: plastic small outline package; 28 leads; body width 7.5 mm SOT136-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	18.1 17.7	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.71 0.69	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

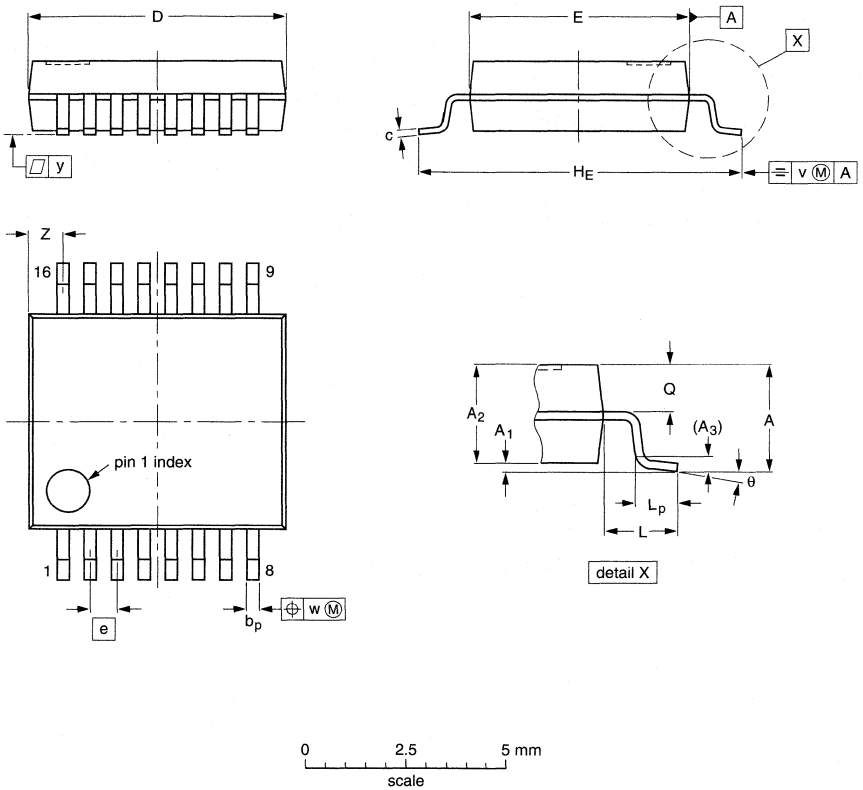
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT136-1	075E06	MS-013AE				~~95-01-24~~ 97-05-22

SSOP

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm SOT338-1



DIMENSIONS (mm are the original dimensions)

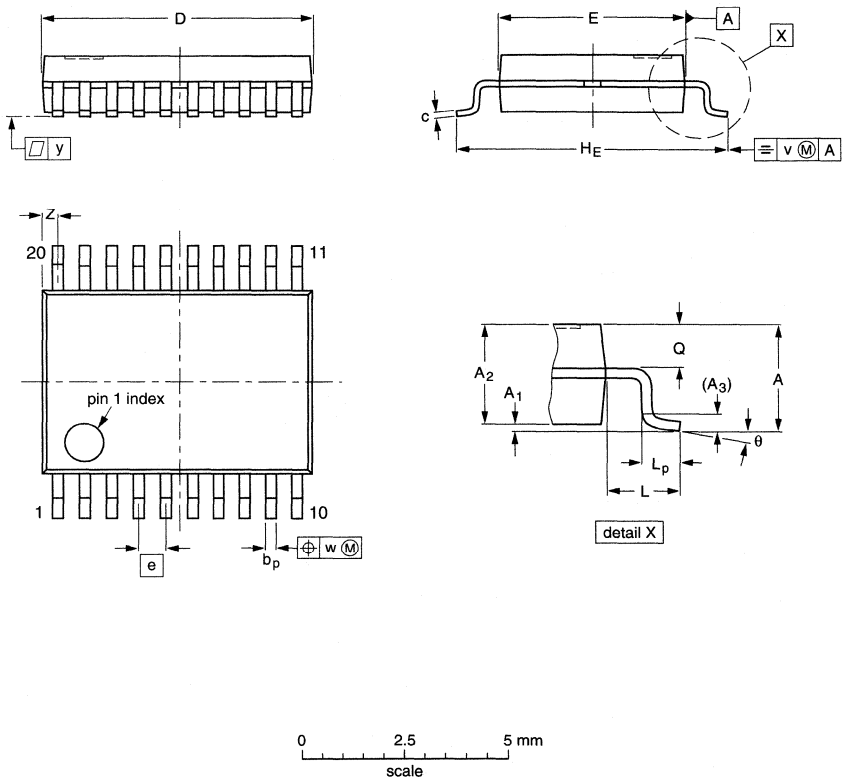
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT338-1		MO-150AC				~~94-01-14~~ 95-02-04

SSOP20: plastic shrink small outline package; 20 leads; body width 4.4 mm **SOT266-1**



DIMENSIONS (mm are the original dimensions)

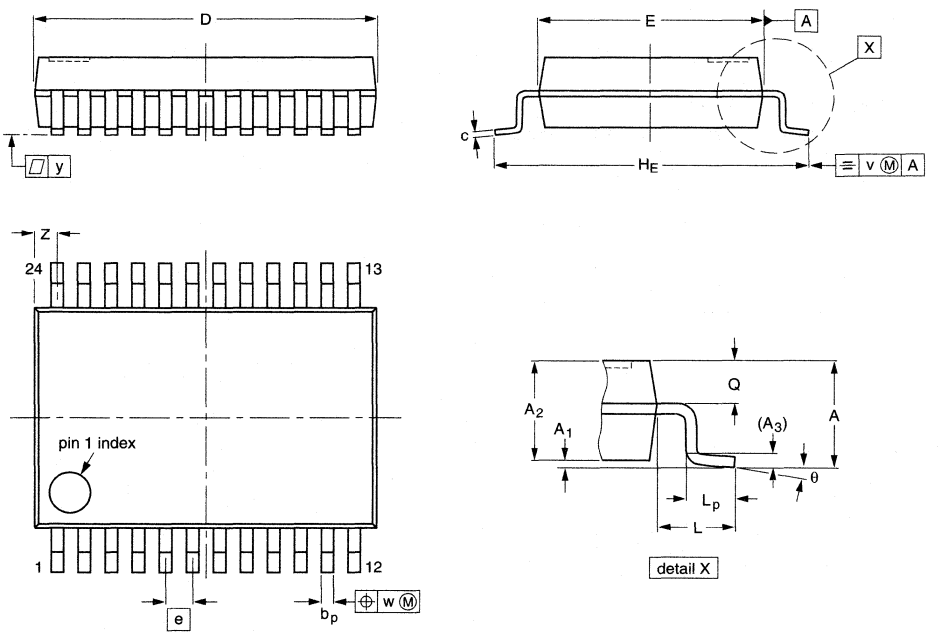
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.5	0.15 0	1.4 1.2	0.25	0.32 0.20	0.20 0.13	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.45	0.65 0.45	0.2	0.13	0.1	0.48 0.18	10^o 0^o

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES					EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ				
SOT266-1							~~90-04-05~~ 95-02-25

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm **SOT340-1**



DIMENSIONS (mm are the original dimensions)

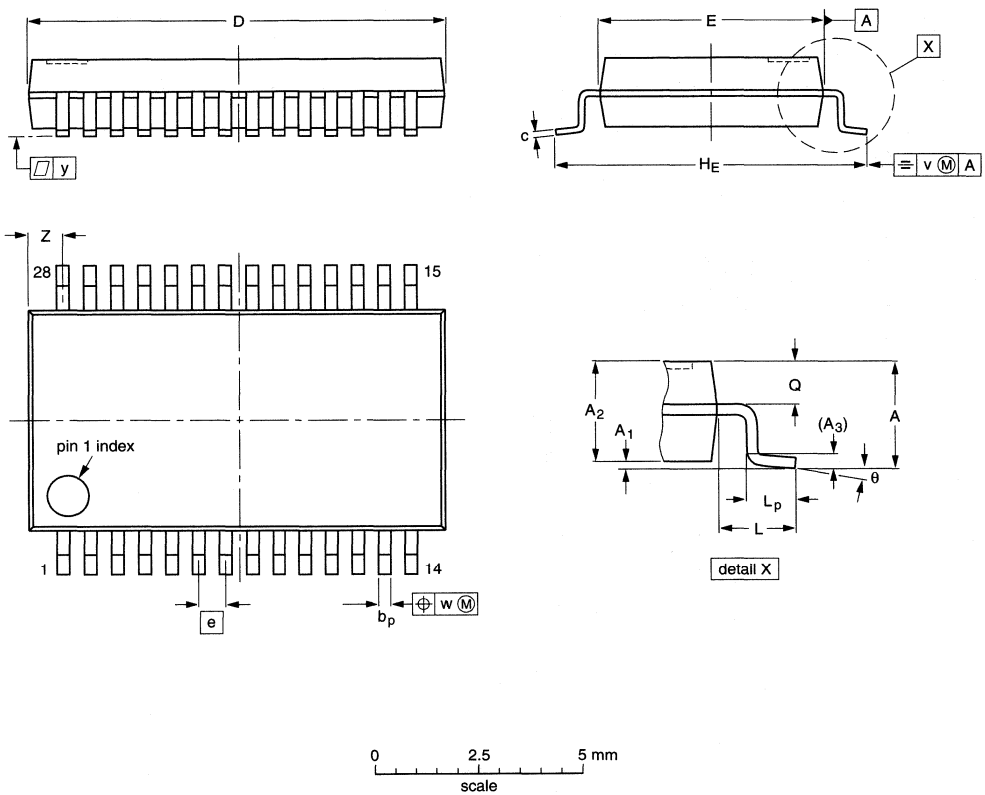
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT340-1		MO-150AG				~~93-09-08~~ 95-02-04

SSOP28: plastic shrink small outline package; 28 leads; body width 5.3 mm **SOT341-1**



DIMENSIONS (mm are the original dimensions)

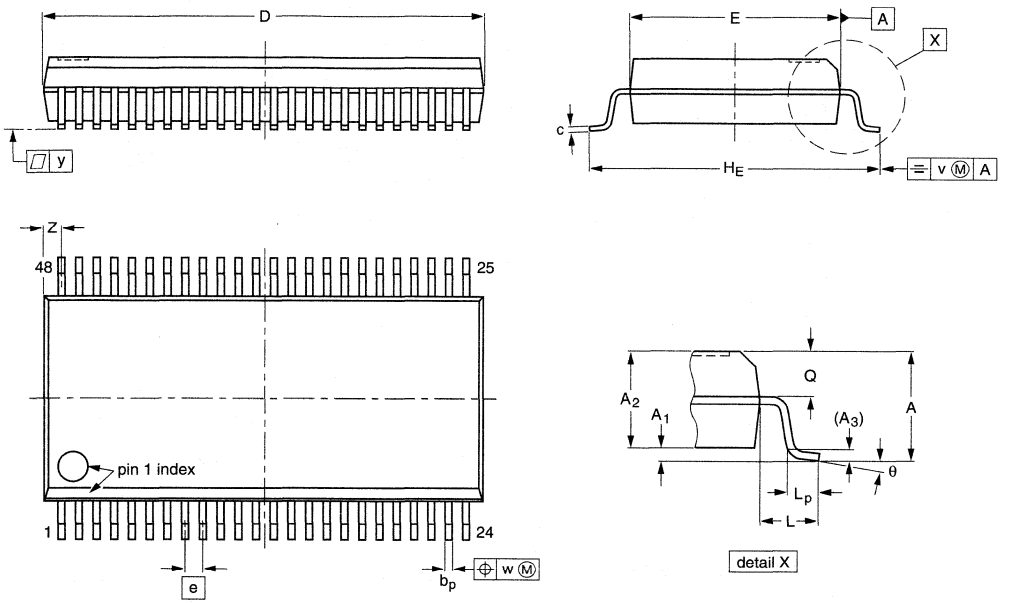
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	10.4 10.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.1 0.7	8° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT341-1		MO-150AH				~~93-09-08~~ 95-02-04

SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm **SOT370-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	16.00 15.75	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

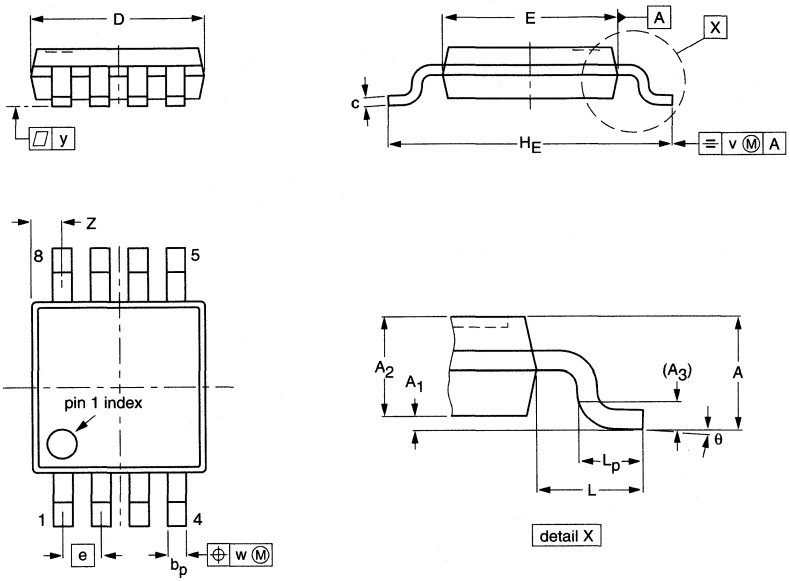
Note

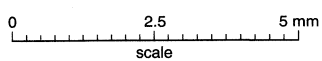
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT370-1		MO-118AA				~~93-11-02~~ 95-02-04

TSSOP

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm SOT505-1





DIMENSIONS (mm are the original dimensions)

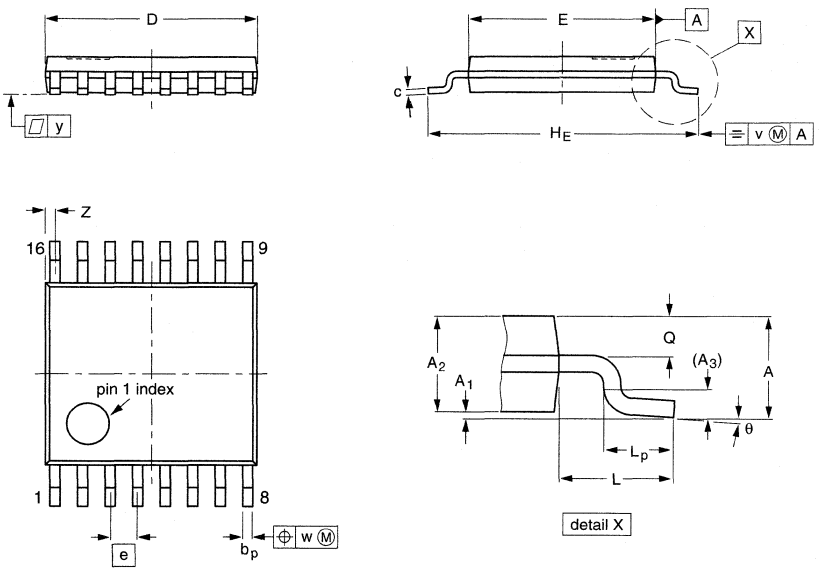
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.45 0.25	0.28 0.15	3.10 2.90	3.10 2.90	0.65	5.10 4.70	0.94	0.70 0.40	0.1	0.1	0.1	0.70 0.35	6° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT505-1						99-04-09

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(2)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

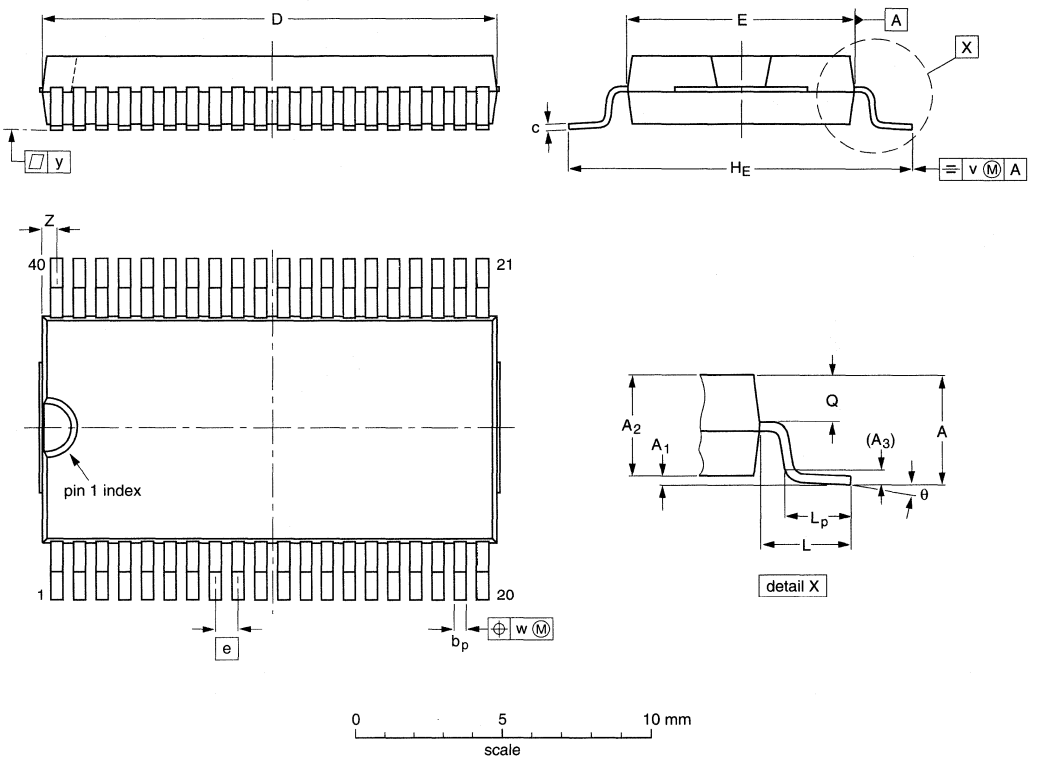
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT403-1		MO-153				~~94-07-12~~ 95-04-04

VSO

VSO40: plastic very small outline package; 40 leads SOT158-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

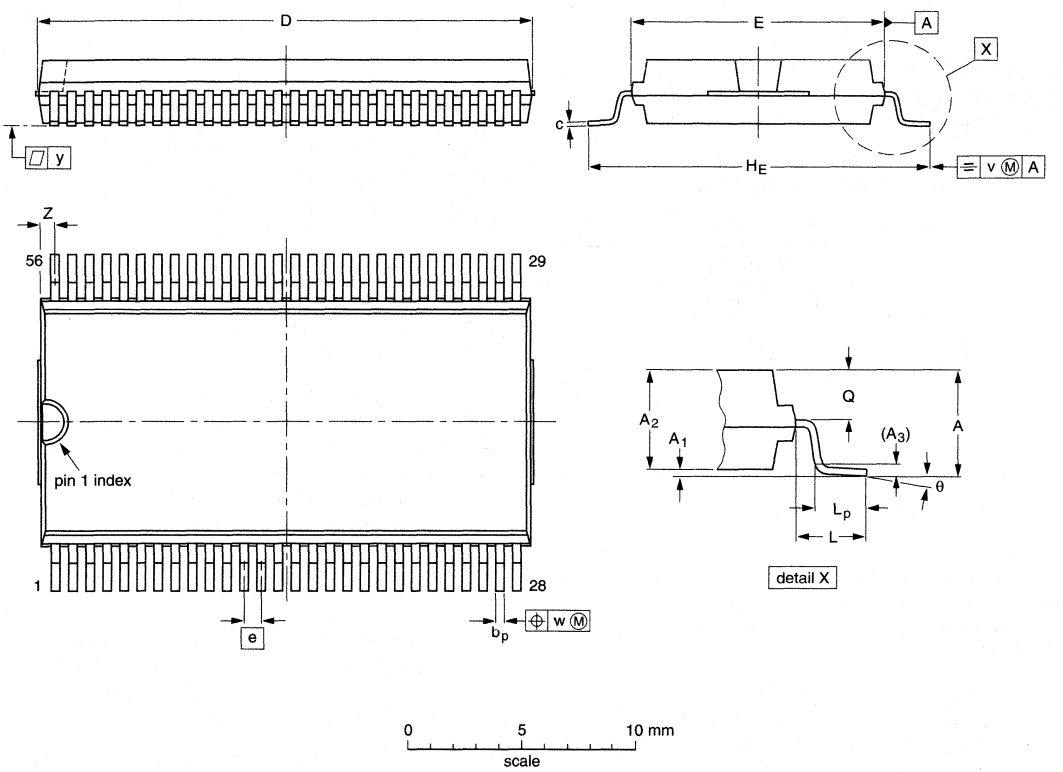
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.70	0.3 0.1	2.45 2.25	0.25	0.42 0.30	0.22 0.14	15.6 15.2	7.6 7.5	0.762	12.3 11.8	2.25	1.7 1.5	1.15 1.05	0.2	0.1	0.1	0.6 0.3	7° 0°
inches	0.11	0.012 0.004	0.096 0.089	0.010	0.017 0.012	0.0087 0.0055	0.61 0.60	0.30 0.29	0.03	0.48 0.46	0.089	0.067 0.059	0.045 0.041	0.008	0.004	0.004	0.024 0.012	

Notes

1. Plastic or metal protrusions of 0.4 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT158-1						~~92-11-17~~ 95-01-24

VSO56: plastic very small outline package; 56 leads **SOT190-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	3.3	0.3 0.1	3.0 2.8	0.25	0.42 0.30	0.22 0.14	21.65 21.35	11.1 11.0	0.75	15.8 15.2	2.25	1.6 1.4	1.45 1.30	0.2	0.1	0.1	0.90 0.55	7° 0°
inches	0.13	0.012 0.004	0.12 0.11	0.01	0.017 0.012	0.0087 0.0055	0.85 0.84	0.44 0.43	0.0295	0.62 0.60	0.089	0.063 0.055	0.057 0.051	0.008	0.004	0.004	0.035 0.022	

Note

1. Plastic or metal protrusions of 0.3 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT190-1						~~96-04-02~~ 97-08-11

INTRODUCTION

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9397 750 0011).

THROUGH-HOLE MOUNTED PACKAGES

Table 14 Types of through-hole mounted packages

TYPE	DESCRIPTION
DIP	plastic dual in-line package
SDIP	plastic shrink dual in-line package
HDIP	plastic heat-dissipating dual in-line package
DBS	plastic dual in-line bent from a single in-line package
SIL	plastic single in-line package

Soldering by dipping or wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

SURFACE MOUNTED PACKAGES

Table 15 Types of surface mounted packages

TYPE	DESCRIPTION
SO	plastic small outline package
SSOP	plastic shrink small outline package
TSSOP	plastic thin shrink small outline package
VSO	plastic very small outline package
QFP	plastic quad flat package
LQFP	plastic low profile quad flat package
SQFP	plastic shrink quad flat package
TQFP	plastic thin quad flat package
PLCC	plastic leaded chip carrier

Reflow soldering

Reflow soldering techniques are suitable for all SMD packages, ease of soldering varies with the type of package as indicated in Table 16.

The choice of heating method may be influenced by larger plastic packages (QFP or PLCC with 44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information on moisture prevention, refer to the Drypack chapter in our *"Quality Reference Handbook"* (order code 9397 750 00192).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Table 16 Suitability of surface mounted packages for various soldering methods: rating from 'a' to 'd': **'a' indicates most suitable** (soldering is not difficult); **'d' indicates least suitable** (soldering is achievable with difficulty).

PACKAGE TYPE	REFLOW METHOD					DOUBLE WAVE METHOD
	INFRARED	HOT BELT	HOT GAS	VAPOUR PHASE	RESISTANCE	
SO	a	a	a	a	d	a
SSOP	a	a	a	c	d	c
TSSOP	b	b	b	c	d	d
VSO	b	b	a	b	a	b
QFP	b	b	a	c	a	c
LQFP	b	b	a	c	d	d
SQFP	b	b	a	c	d	d
TQFP	b	b	a	c	d	d
PLCC	c	b	b	d	d	b

Wave soldering

Wave soldering is **not** recommended for SSOP, TSSOP, QFP, LQFP, SQFP or TQFP packages, this is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- For SSOP, TSSOP and VSO packages, the longitudinal axis of the package footprint must be parallel to the solder flow **and** must incorporate solder thieves at the downstream end.
- For QFP, LQFP and TQFP packages, the footprint must be at an angle of 45° to the board direction **and** must incorporate solder thieves downstream and at the side corners.

Even with these conditions, consider wave soldering only for the following package types:

- SO
- VSO
- PLCC
- SSOP **only with body width 4.4 mm**, e.g. SSOP16 (SOT369-1) or SSOP20 (SOT266-1).
- QFP **except** QFP52 (SOT379-1), QFP100 (SOT317-1, SOT317-2, SOT382-1) and QFP160 (SOT322-1); these are **not** suitable for wave soldering.
- LQFP **except** LQFP32 (SOT401-1), LQFP48 (SOT313-1, SOT313-2), LQFP64 (SOT314-2), LQFP80 (SOT315-1); these are **not** suitable for wave soldering.
- TQFP **except** TQFP64 (SOT357-1), TQFP80 (SOT375-1) and TQFP100 (SOT386-1); these are **not** suitable for wave soldering.

SQFP are **not** suitable for wave soldering.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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DATA HANDBOOK SYSTEM

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Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 20 0733, Fax. +375 172 20 0773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 68 9211, Fax. +359 2 68 9102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381, Fax. +1 800 943 0087

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Sydhavnsgade 23, 1780 COPENHAGEN V,
Tel. +45 33 29 3333, Fax. +45 33 29 3905

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 9 615 800, Fax. +358 9 6158 0920

France: 51 Rue Carnot, BP317, 92156 SURESNES Cedex,
Tel. +33 1 4099 6161, Fax. +33 1 4099 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 2353 60, Fax. +49 40 2353 6300

Hungary: see Austria

India: Philips INDIA Ltd, Band Box Building, 2nd floor,
254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025,
Tel. +91 22 493 8541, Fax. +91 22 493 0966

Indonesia: PT Philips Development Corporation, Semiconductors Division,
Gedung Philips, Jl. Buncit Raya Kav.99-100, JAKARTA 12510,
Tel. +62 21 794 0040 ext. 2501, Fax. +62 21 794 0080

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Via Casati, 23 - 20052 MONZA (MI), Tel.
+39 039 203 6838, Fax +39 039 203 6800

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108-8507,
Tel. +81 3 3740 5130, Fax. +81 3 3740 5057

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
Tel. +9-5 800 234 7381, Fax +9-5 800 943 0087

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Pakistan: see Singapore

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI, Metro MANILA,
Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Al.Jerozolimskie 195 B, 02-222 WARSAW,
Tel. +48 22 5710 000, Fax. +48 22 5710 001

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
Tel. +7 095 755 6918, Fax. +7 095 755 6919

Singapore: Lorong 1, Toa Payoh, SINGAPORE 319762,
Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

Slovenia: see Italy

South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,
2092 JOHANNESBURG, P.O. Box 58088 Newville 2114,
Tel. +27 11 471 5401, Fax. +27 11 471 5398

South America: Al. Vicente Pinzon, 173, 6th floor, 04547-130 SÃO PAULO, SP,
Brazil, Tel. +55 11 821 2333, Fax. +55 11 821 2382

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 93 301 6312, Fax. +34 93 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,
Tel. +46 8 5985 2000, Fax. +46 8 5985 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. +41 1 488 2741 Fax. +41 1 488 3263

Taiwan: Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1, TAIPEI,
Taiwan Tel. +886 2 2134 2886, Fax. +886 2 2134 2874

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,
Tel. +66 2 745 4090, Fax. +66 2 398 0793

Turkey: Yukari Dudullu, Org. San. Blg., 2.Cad. Nr. 28 81260 Umraniye,
ISTANBUL, Tel. +90 216 522 1500, Fax. +90 216 522 1813

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 208 730 5000, Fax. +44 208 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. +1 800 234 7381, Fax. +1 800 943 0087

Uruguay: see South America

Vietnam: see Singapore

Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,
Tel. +381 11 62 5344, Fax.+381 11 63 5777

For all other countries apply to: Philips Semiconductors, International Marketing & Sales Communications,
Building BE-p, P.O. Box 218, 5600 MD EINDHOVEN, The Netherlands, Fax. +31 40 27 24825

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